DATA SHEET

BITSTREAM CONVERSION

UDA1341TS
Economy audio CODEC for MiniDisc (MD) home stereo and portable applications

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Economy audio CODEC for MiniDisc (MD) home stereo and portable applications

UDA1341TS

CONTENTS

1 FEATURES

BITSTREAM CONVERSION

1.1 General

- Low power consumption
- 3.0 V power supply
- $256f_s$, $384f_s$ or $512f_s$ system clock frequencies (f_{sys})
- Small package size (SSOP28)
- Partially pin compatible with UDA1340M and UDA1344TS
- Fully integrated analog front end including digital AGC
- ADC plus integrated high-pass filter to cancel DC offset
- ADC supports 2 V (RMS value) input signals
- Overload detector for easy record level control
- Separate power control for ADC and DAC
- No analog post filter required for DAC
- Easy application
- Functions controllable via L3-interface.

1.2 Multiple format data interface

- I^2S-bus, MSB-justified and LSB-justified format compatible
- Three combinational data formats with MSB data output and LSB 16, 18 or 20 bits data input
- $1f_s$ input and output format data rate.

1.3 DAC digital sound processing

- Digital dB-linear volume control (low microcontroller load)
- Digital tone control, bass boost and treble
- Digital de-emphasis for 32, 44.1 or 48 kHz audio sample frequencies (f_s)
- Soft mute.

1.4 Advanced audio configuration

- DAC and ADC polarity control
- Two channel stereo single-ended input configuration
- Microphone input with on-board PGA
- Optional differential input configuration for enhanced ADC sound quality
- Stereo line output (under microcontroller volume control)
- Digital peak level detection
- High linearity, dynamic range and low distortion.

2 GENERAL DESCRIPTION

The UDA1341TS is a single-chip stereo Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) with signal processing features employing bitstream conversion techniques. Its fully integrated analog front end, including Programmable Gain Amplifier (PGA) and a digital Automatic Gain Control (AGC). Digital Sound Processing (DSP) featuring makes the device an excellent choice for primary home stereo MiniDisc applications, but by virtue of its low power and low voltage characteristics it is also suitable for portable applications such as MD/CD boomboxes, notebook PCs and digital video cameras.

The UDA1341TS is similar to the UDA1340M and the UDA1344TS but adds features such as digital mixing of two input signals and one channel with a PGA and a digital AGC.

The UDA1341TS supports the I^2S-bus data format with word lengths of up to 20 bits, the MSB-justified data format with word lengths of up to 20 bits, the LSB-justified serial data format with word lengths of 16, 18 and 20 bits and three combinations of MSB data output combined with LSB 16, 18 and 20 bits data input. The UDA1341TS has DSP features in playback mode like de-emphasis, volume, bass boost, treble and soft mute, which can be controlled via the L3-interface with a microcontroller.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1341TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{DDA(ADC)}$	ADC analog supply voltage		2.4	3.0	3.6	V
$V_{DDA(DAC)}$	DAC analog supply voltage		2.4	3.0	3.6	V
V_{DDD}	digital supply voltage		2.4	3.0	3.6	V
$I_{DDA(ADC)}$	ADC analog supply current	operation mode	–	12.5	–	mA
		ADC power-down	–	6.0	–	mA
$I_{DDA(DAC)}$	DAC analog supply current	operation mode	–	7.0	–	mA
		DAC power-down	–	50	–	μA
I_{DDD}	digital supply current	operation mode	–	7.0	–	mA
T_{amb}	operating ambient temperature		–20	–	+85	°C
Analog-to-digital converter						
$V_{i(rms)}$	input voltage (RMS value)	notes 1 and 2	–	1.0	–	V
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	stand-alone mode				
		0 dB	–	–85	–80	dB
		–60 dB; A-weighted	–	–37	–33	dB
		double differential mode				
		0 dB	–	–90	–85	dB
		–60 dB; A-weighted	–	–40	–36	dB
S/N	signal-to-noise ratio	V_i = 0 V; A-weighted				
		stand-alone mode	–	97	–	dB
		double differential mode	–	100	–	dB
α_{cs}	channel separation		–	100	–	dB
Programmable gain amplifier						
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	1 kHz; f_s = 44.1 kHz				
		0 dB	–	–85	–	dB
		–60 dB; A-weighted	–	–37	–	dB
S/N	signal-to-noise ratio	V_i = 0 V; A-weighted	–	95	–	dB
Digital-to-analog converter						
$V_{o(rms)}$	output voltage (RMS value)	supply voltage = 3 V; note 3	–	900	–	mV
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	0 dB	–	–91	–86	dB
		–60 dB; A-weighted	–	–40	–	dB
S/N	signal-to-noise ratio	code = 0; A-weighted	–	100	–	dB
α_{cs}	channel separation		–	100	–	dB

Notes

1. The ADC inputs can be used in a 2 V (RMS value) input signal configuration when a resistor of 12 kΩ is used in series with the inputs and 1 or 2 V (RMS value) input signal operation can be selected via the Input Gain Switch (IGS).
2. The ADC input signal scales inversely proportional with the power supply voltage.
3. The DAC output voltage scales linear with the DAC analog supply voltage.

5 BLOCK DIAGRAM

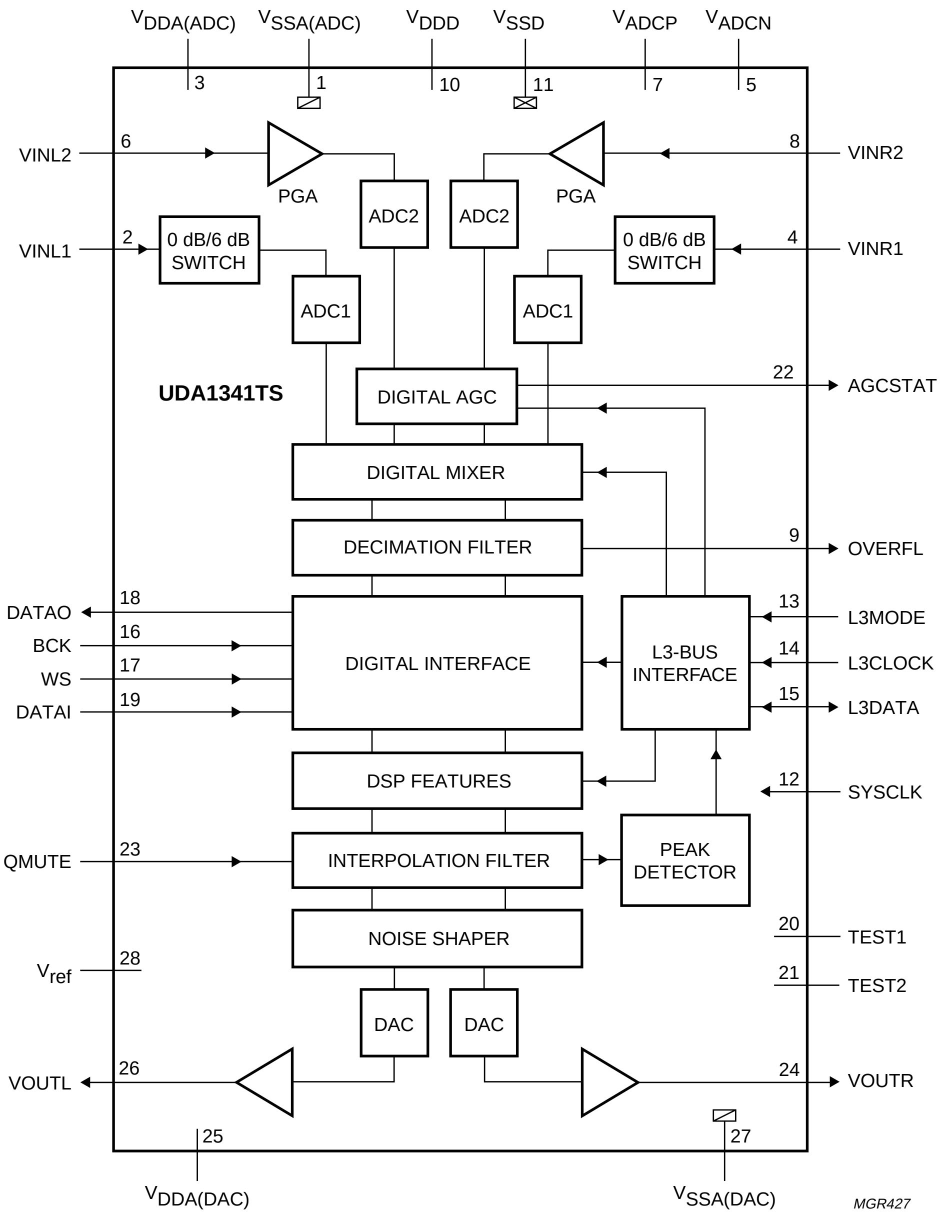


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
$V_{SSA(ADC)}$	1	ADC analog ground
VINL1	2	ADC1 input left
$V_{DDA(ADC)}$	3	ADC analog supply voltage
VINR1	4	ADC1 input right
V_{ADCN}	5	ADC negative reference voltage
VINL2	6	ADC2 input left
V_{ADCP}	7	ADC positive reference voltage
VINR2	8	ADC2 input right
OVERFL	9	decimation filter overflow output
V_{DDD}	10	digital supply voltage
V_{SSD}	11	digital ground
SYSCLK	12	system clock $256f_s$, $384f_s$ or $512f_s$
L3MODE	13	L3-bus mode input
L3CLOCK	14	L3-bus clock input
L3DATA	15	L3-bus data input and output
BCK	16	bit clock input
WS	17	word select input
DATAO	18	data output
DATAI	19	data input
TEST1	20	test control 1 (pull-down)
TEST2	21	test control 2 (pull-down)
AGCSTAT	22	AGC status
QMUTE	23	quick mute input
VOUTR	24	DAC output right
$V_{DDA(DAC)}$	25	DAC analog supply voltage
VOUTL	26	DAC output left
$V_{SSA(DAC)}$	27	DAC analog ground
V_{ref}	28	ADC and DAC reference voltage

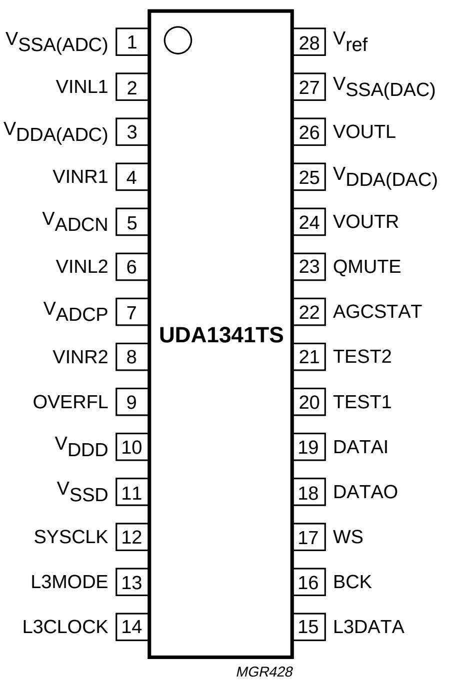


Fig.2 Pin configuration.

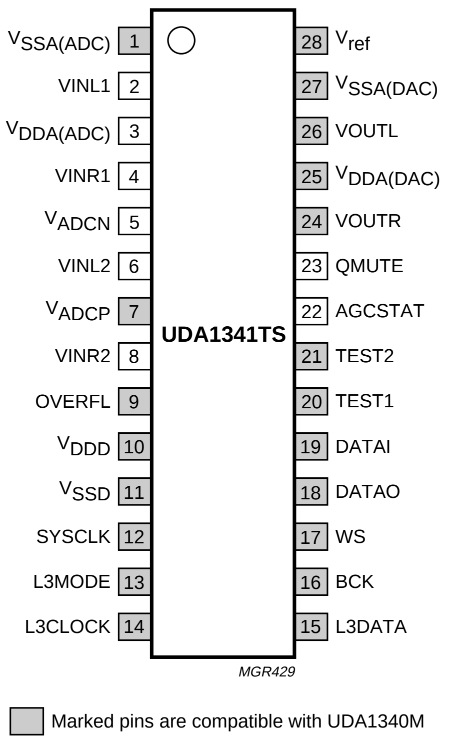


Fig.3 Compatible pins with UDA1340M.

7 FUNCTIONAL DESCRIPTION

7.1 System clock

The UDA1341TS accommodates slave mode only, this means that in all applications the system devices must provide the system clock. The system frequency is selectable. The options are $256f_s$, $384f_s$ or $512f_s$. The system clock must be locked in frequency to the digital interface signals.

7.2 Pin compatibility

The UDA1341TS is partially pin compatible with the UDA1340M and UDA1344TS, making an upgrade of a printed-circuit board from UDA1340M to UDA1341TS easier. The pins that are compatible with the UDA1340M are marked in Fig.3.

7.3 Analog front end

The analog front end of the UDA1341TS consists of two stereo ADCs with a Programmable Gain Amplifier (PGA) in channel 2. The PGA is intended to pre-amplify a microphone signal applied to the input channel 2.

Input channel 1 has a selectable 0 or 6 dB gain stage, to be controlled via the L3-interface. In this way, input signals of 1 V (RMS value) or 2 V (RMS value) e.g. from a CD source can be supported using an external resistor of 12 kΩ in series with the input channel 1. The application modes are given in Table 1.

Table 1 Application modes using input gain stage

RESISTOR (12 kΩ)	INPUT GAIN SWITCH	MAXIMUM INPUT VOLTAGE
Present	0 dB	2 V (RMS value) input signal; note 1
Present	6 dB	1 V (RMS value) input signal
Absent	0 dB	1 V (RMS value) input signal
Absent	6 dB	0.5 V (RMS value) input signal

Note

1. If there is no need for 2 V (RMS value) input signal support, the external resistor should not be used.

7.4 Programmable Gain Amplifier (PGA)

The PGA can be set via the L3-interface at the gain settings: –3, 0, 3, 9, 15, 21 or 27 dB.

7.5 Analog-to-Digital Converter (ADC)

The stereo ADC of the UDA1341TS consists of two 3rd-order Sigma-Delta modulators. They have a modified Ritchie-coder architecture in a differential switched capacitor implementation. The over-sampling ratio is 128.

7.6 Digital Automatic Gain Control (AGC)

Input channel 2 has a digital AGC to compress the dynamic range when a microphone signal is applied to input channel 2. The digital AGC can be switched on and off via the L3-interface. In the on state the AGC compresses the dynamic range of the input signal of input channel 2. Via the L3-interface the user can set the parameters of the AGC: attack time, decay time and output level. When the AGC is set off via the L3-interface, the gain of input channel 2 can be set manually. In this case the gain of the PGA and digital AGC are combined. The range of the gain of the input channel 2 is from –3 to +60.5 dB in steps of 0.5 dB.

7.7 AGC status detection

The AGCSTAT signal from the digital AGC is HIGH when the gain level of the AGC is below 8 dB. This signal can be used to give the PGA a new gain setting via the L3-interface and to power e.g. a LED.

7.8 Digital mixer

The two stereo ADCs (including the AGC) can be used in four modes:

- ADC1 only mode (for line input); input channel 2 is off
- ADC2 only mode, including PGA and digital AGC (for microphone input); input channel 1 is off
- ADC1 + ADC2 mixer mode, including PGA and AGC
- ADC1 and ADC2 double differential mode (improved ADC performance).

Important: In order to prevent crosstalk between the line inputs no signal should be applied to the microphone input in the double differential mode.

In all modes (except the double differential mode) a reference voltage is always present at the input of the ADC. However, in the double differential mode there is no reference voltage present at the microphone input.

In the mixer mode, the output signals of both ADCs in channel 1 and channel 2 (after the digital AGC) can be mixed with coefficients that can be set via the L3-interface. The range of the mixer coefficients is from 0 to –∞ dB in 1.5 dB steps.

7.9 Decimation filter (ADC)

The decimation from $128f_s$ is performed in two stages.

The first stage realizes 3rd order $\frac{\sin x}{x}$ characteristic, decimating by 16. The second stage consists of 3 half-band filters, each decimating by a factor of 2.

Table 2 Decimation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Passband ripple	0 to $0.45f_s$	±0.05
Stop band	$>0.55f_s$	–60
Dynamic range	0 to $0.45f_s$	108
Overall gain	input channel 1; 0 dB input	–1.16

7.10 Overload detection (ADC)

This name is convenient but a little inaccurate. In practice the output is used to indicate whenever that output data, in either the left or right channel, is bigger than –1 dB (actual figure is –1.16 dB) of the maximum possible digital swing. If this condition is detected the OVERFL output is forced HIGH for at least $512f_s$ cycles (11.6 ms at f_s = 44.1 kHz). This time-out is reset for each infringement.

7.11 Mute (ADC)

On recovery from power-down or switching on of the system clock, the serial data output DATAO is held LOW until valid data is available from the decimation filter.

7.12 Interpolation filter (DAC)

The digital filter interpolates from $1f_s$ to $128f_s$ by means of a cascade of a recursive filter and a Finite Impulse Response (FIR) filter.

Table 3 Interpolation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Passband ripple	0 to $0.45f_s$	±0.03
Stop band	$>0.55f_s$	–50
Dynamic range	0 to $0.45f_s$	108

7.13 Peak detector

In the playback path a peak level detector is build in. The position of the peak detection can be set via the L3-interface to either before or after the sound features.

The peak level detector is implemented as a peak-hold detector, which means that the highest sound level is hold until the peak level is read out via the L3-interface. After read-out the peak level registers are reset.

7.14 Quick mute

A hard mute can be activated via the static pin QMUTE. When QMUTE is set HIGH, the output signal is instantly muted to zero. Setting QMUTE to LOW, the mute is instantly in-activated.

7.15 Noise shaper (DAC)

The 3rd-order noise shaper operates at $128f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique allows for high signal-to-noise ratios. The noise shaper output is converted into an analog signal using a filter stream digital-to-analog converter.

7.16 Filter Stream Digital-to-Analog Converter (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

7.17 Multiple format input/output interface

The UDA1341TS supports the following data formats:

- I^2S-bus with word length up to 20 bits
- MSB-justified serial format with word length up to 20 bits
- LSB-justified serial format with word length of 16, 18 or 20 bits
- MSB data output with LSB 16, 18 or 20 bits input.

Left and right data-channel words are time multiplexed. The formats are illustrated in Fig.4.

The UDA1341TS allows for double speed data monitoring purposes. In this case the sound features bass boost, treble and de-emphasis cannot be used. However, volume control and soft-mute can still be controlled. The double speed monitoring option can be set via the L3-interface.

The bit clock frequency must be 64 times word select frequency or less, so $f_{BCK} \leq 64 \times f_{WS}$.

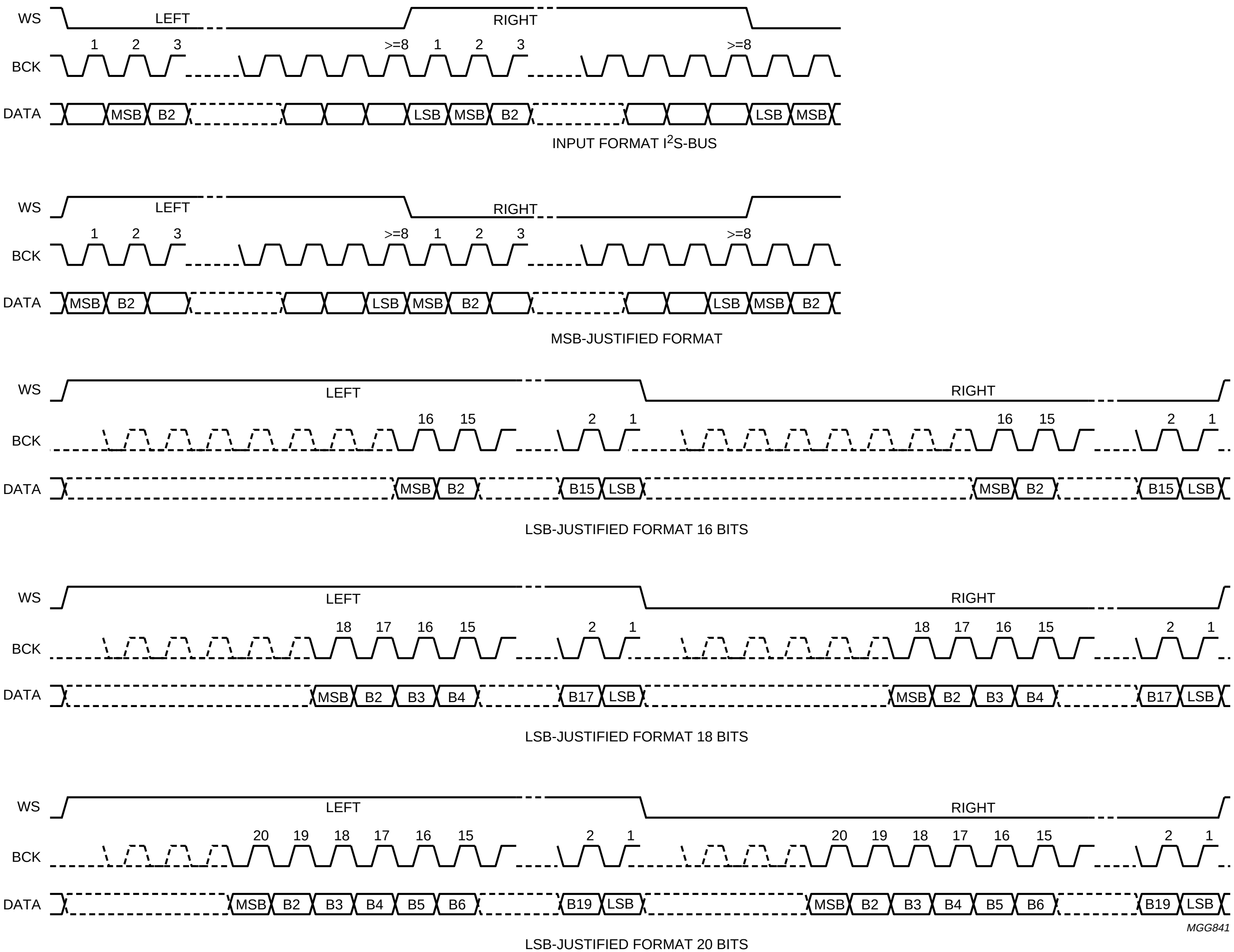


Fig.4 Serial interface formats.

7.18 L3-interface

The UDA1341TS has a microcontroller input mode. In the microcontroller mode, all the digital sound processing features and the system controlling features can be controlled by the microcontroller.

The controllable features are:

- Reset
- System clock frequency
- Power control
- DAC gain switch
- ADC input gain switch
- ADC/DAC polarity control
- Double speed playback
- De-emphasis
- Volume
- Mode switch
- Bass boost
- Treble
- Mute
- MIC sensitivity control
- AGC control
- Input amplifier gain control
- Digital mixer control
- Peak detection position.

Via the L3-interface the peak level value of the signal in the DAC path can be read out from the UDA1341TS to the microcontroller.

The exchange of data and control information between the microcontroller and the UDA1341TS is accomplished through a serial hardware L3-interface comprising the following pins:

- L3DATA: microcontroller interface data line
- L3MODE: microcontroller interface mode line
- L3CLOCK: microcontroller interface clock line.

Information transfer through the microcontroller bus is organized in accordance with the so called ‘L3’ format, in which two different modes of operation can be distinguished: address mode and data transfer mode.

The address mode is required to select a device communicating via the L3-bus and to define the destination registers for the data transfer mode.

Data transfer can be in both directions: input to the UDA1341TS to program its sound processing and system controlling features and output from the UDA1341TS to provide the peak level value.

7.19 Address mode

The address mode is used to select a device for subsequent data transfer and to define the destination registers. The address mode is characterized by L3MODE being LOW and a burst of 8 pulses on L3CLOCK, accompanied by 8 data bits. The fundamental timing is shown in Fig.5.

Data bits 7 to 2 represent a 6-bit device address, with bit 7 being the MSB and bit 2 the LSB. The address of the UDA1341TS is 000101.

Data bits 0 to 1 indicate the type of the subsequent data transfer as shown in Table 4.

In the event that the UDA1341TS receives a different address, it will deselect its microcontroller interface logic.

7.20 Data transfer mode

The selection activated in the address mode remains active during subsequent data transfers, until the UDA1341TS receives a new address command.

The fundamental timing of data transfers is essentially the same as the timing in the address mode and is given in Fig.6.

Note that ‘L3DATA write’ denotes data transfer from the microcontroller to the UDA1341TS and ‘L3DATA peak read’ denotes data transfer in the opposite direction.
The maximum input clock and data rate is $64f_s$.
All transfers are byte-wise, i.e. they are based on groups of 8 bits. Data will be stored in the UDA1341TS after the eighth bit of a byte has been received.

A multibyte transfer is illustrated in Fig.7.

Table 4 Selection of data transfer

BIT 1	BIT 0	MODE	TRANSFER
0	0	DATA0	direct addressing registers: volume, bass boost, treble, peak detection position, de-emphasis, mute and mode
			extended addressing registers: digital mixer control, AGC control, MIC sensitivity control, input gain, AGC time constant and AGC output level
0	1	DATA1	peak level value read-out (information from UDA1341TS to microcontroller)
1	0	STATUS	reset, system clock frequency, data input format, DC-filter, input gain switch, output gain switch, polarity control, double speed and power control
1	1	not used	

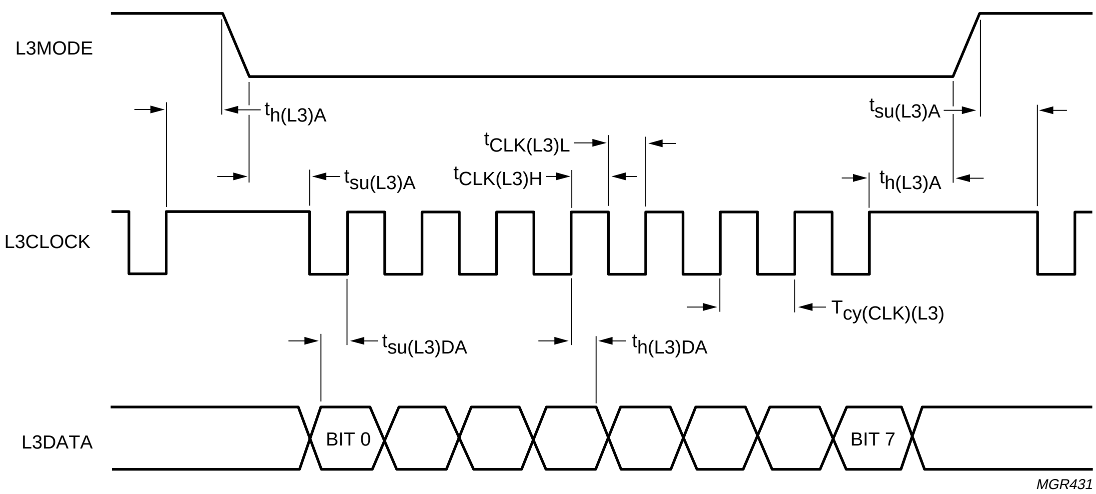


Fig.5 Timing address mode.

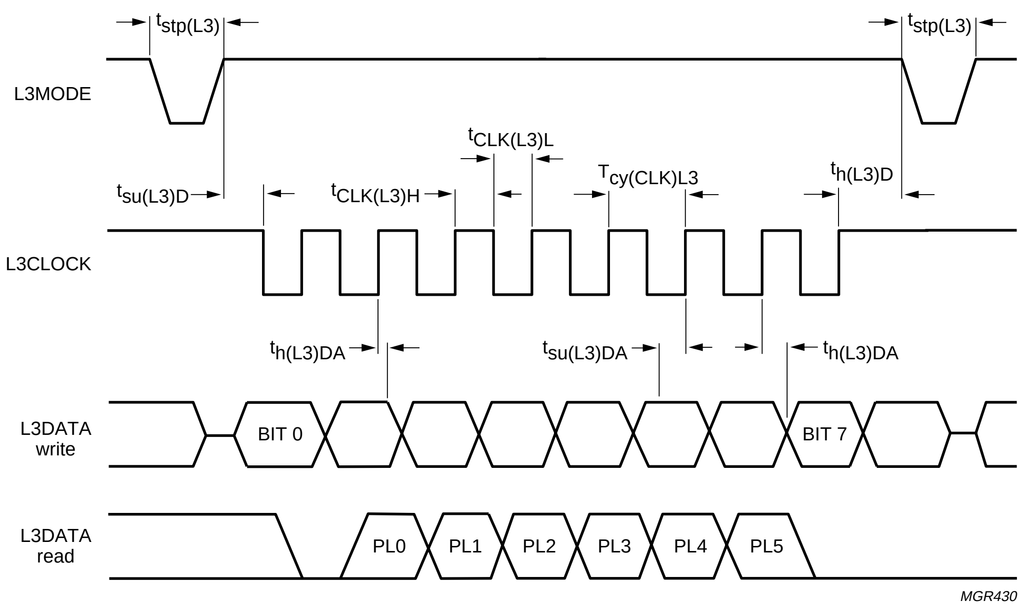


Fig.6 Timing for data transfer mode.

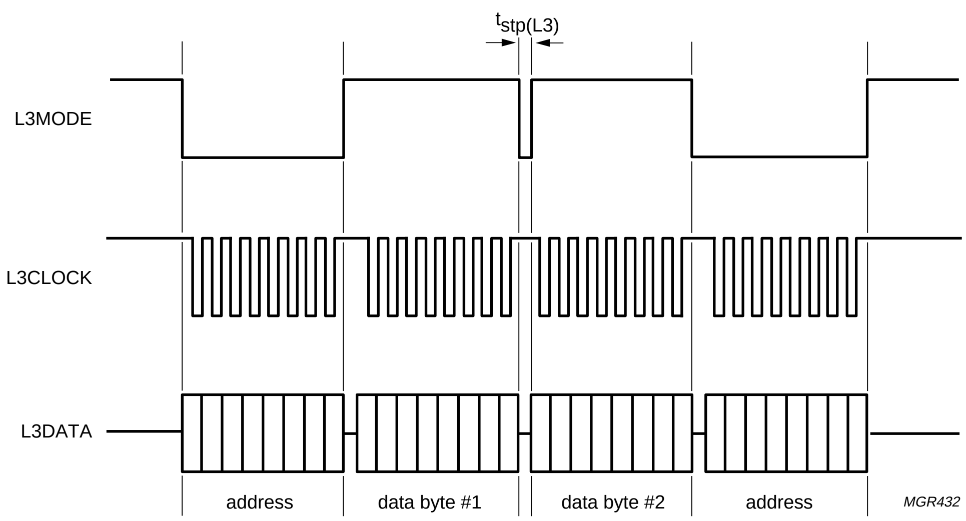


Fig.7 Multibyte transfer.

7.21 Programming the sound processing and other features

The sound processing and other feature values are stored in independent registers.

The first selection of the registers is achieved by the choice of data type that is transferred. This is performed in the address mode using bit 0 and bit 1 (see Table 4).
The second selection is performed by the 2 or 3 MSBs of the data byte (bits 7 and 6 or bits 7, 6 and 5).
The other bits in the data byte (bits 5 to 0 or bits 4 to 0) represent the value that is placed in the selected registers.

For the UDA1341TS the following modes can be selected:

- STATUS

  In this mode the features reset, system clock frequency, data input format, DC-filter, input gain switch, output gain switch, polarity control, double speed and power control can be controlled.

- DATA0

  There are two addressing modes: direct addressing mode and extended addressing mode.

  Direct addressing mode is using the 2 MSB bits of the data byte. Via this addressing mode the features volume, bass boost, treble, peak position, de-emphasis, mute, and mode can be controlled directly.

  Extended addressing mode is provided for controlling the features digital mixer, AGC control, MIC sensitivity, input gain, AGC time constants, and AGC output level. An extended address can be set via the EA registers (3 bits). The data in the extended registers can be set by writing data to the ED registers (5 bits).

- DATA1

  In this mode the detected peak level value can be read out.

Table 5 Default settings

SYMBOL	FEATURE	SETTING OR VALUE
Status		
OGS	Output gain switch	0 dB
IGS	Input gain switch	0 dB
PAD	Polarity of ADC	non-inverting
PDA	Polarity of DAC	non-inverting
DS	Double speed	single speed
PC	Power control ADC and DAC	on
Direct control		
VC	Volume control	0 dB
BB	Bass boost	0 dB
TR	Treble	0 dB
PP	Peak detection position	after the tone features
DE	De-emphasis	no de-emphasis
MT	Mute	no mute
M	Mode switch	flat
Extended programming		
MA	Mixer gain channel 1	–6 dB
MB	Mixer gain channel 2	–6 dB
MS	MIC sensitivity	0 dB
MM	Mixer mode switch	double differential
AG	AGC control	disable AGC
AT	AGC attack and decay time	11 ms and100 ns
AL	AGC output level	–9 dB FS

7.21.1 STATUS CONTROL

Table 6 Data transfer of type 'STATUS'

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	RST	SC1	SC0	IF2	IF1	IF0	DC	RST = reset
								SC = system clock frequency (2 bits)
								IF = data input format (3 bits)
								DC = DC-filter
1	OGS	IGS	PAD	PDA	DS	PC1	PC0	OGS = output gain (6 dB) switch
								IGS = input gain (6 dB) switch
								PAD = polarity of ADC
								PDA = polarity of DAC
								DS = double speed
								PC = power control (2 bits)

7.21.1.1 Reset

A 1-bit value to initialize the L3-registers with the default settings except system clock frequency.

Table 7 Reset settings

RST	FUNCTION
0	no reset
1	reset

7.21.1.2 System clock frequency

A 2-bit value to select the used external clock frequency.

Table 8 System clock settings

SC1	SC0	FUNCTION
0	0	$512f_s$
0	1	$384f_s$
1	0	$256f_s$
1	1	not used

7.21.1.3 DC-filter

A 1-bit value to enable the digital DC-filter.

Table 9 DC-filtering settings

DC	FUNCTION
0	no DC-filtering
1	DC-filtering

7.21.1.4 Data input format

A 3-bit value to select the data input format.

Table 10 Data input format settings

IF2	IF1	IF0	FUNCTION
0	0	0	I^2S-bus
0	0	1	LSB-justified 16 bits
0	1	0	LSB-justified 18 bits
0	1	1	LSB-justified 20 bits
1	0	0	MSB-justified
1	0	1	LSB-justified 16 bits input and MSB-justified output
1	1	0	LSB-justified 18 bits input and MSB-justified output
1	1	1	LSB-justified 20 bits input and MSB-justified output

7.21.1.5 Output gain switch

A 1-bit value to control the DAC output gain switch. The default setting is given in Table 5.

Table 11 Gain switch of DAC settings

OGS	GAIN OF DAC
0	0 dB
1	6 dB

7.21.1.6 Input gain switch

A 1-bit value to control the ADC input gain switch. The default setting is given in Table 5.

Table 12 Gain switch of ADC settings

IGS	GAIN OF ADC
0	0 dB
1	6 dB

7.21.1.7 Polarity of ADC

A 1-bit value to control the ADC polarity. The default setting is given in Table 5.

Table 13 Polarity control of ADC settings

PAD	POLARITY OF ADC
0	non-inverting
1	inverting

7.21.1.8 Polarity of DAC

A 1-bit value to control the DAC polarity. The default setting is given in Table 5.

Table 14 Polarity control of DAC settings

PDA	POLARITY OF DAC
0	non-inverting
1	inverting

7.21.1.9 Double speed

A 1-bit value to enable the double speed playback. The default setting is given in Table 5.

Table 15 Double speed settings

DS	FUNCTION
0	single speed playback
1	double speed playback

7.21.1.10 Power control

A 2-bit value to disable the ADC and/or DAC to reduce power consumption. The default setting is given in Table 5.

Table 16 Power control settings

PC1	PC0	FUNCTION	
		ADC	DAC
0	0	off	off
0	1	off	on
1	0	on	off
1	1	on	on

7.21.2 DATA0 DIRECT CONTROL

Table 17 Data transfer of type 'DATA0'

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	0	VC5	VC4	VC3	VC2	VC1	VC0	VC = volume control (6 bits)
0	1	BB3	BB2	BB1	BB0	TR1	TR0	BB = bass boost (4 bits)
								TR = treble (2 bits)
1	0	PP	DE1	DE0	MT	M1	M0	PP = peak detection position
								DE = de-emphasis (2 bits)
								MT = mute
								M = mode switch (2 bits)
1	1	0	0	0	EA2	EA1	EA0	EA = extended address (3 bits)
1	1	1	ED4	ED3	ED2	ED1	ED0	ED = extended data (5 bits)

7.21.2.1 Volume control

A 6-bit value to program the left and right channel volume attenuation. The range is from 0 to –∞ dB in steps of 1 dB. The default setting is given in Table 5.

Table 18 Volume settings

VC5	VC4	VC3	VC2	VC1	VC0	VOLUME (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	–1
0	0	0	0	1	1	–2
:	:	:	:	:	:	:
1	1	1	0	1	1	–58
1	1	1	1	0	0	–59
1	1	1	1	0	1	–60
1	1	1	1	1	0	–∞
1	1	1	1	1	1	–∞

7.21.2.2 Bass boost

A 4-bit value to program the bass boost settings. The used set depends on the mode bits. The default setting is given in Table 5.

Table 19 Bass boost settings

BB3	BB2	BB1	BB0	BASS BOOST		
				FLAT (dB)	MIN. (dB)	MAX. (dB)
0	0	0	0	0	0	0
0	0	0	1	0	2	2
0	0	1	0	0	4	4
0	0	1	1	0	6	6
0	1	0	0	0	8	8
0	1	0	1	0	10	10
0	1	1	0	0	12	12
0	1	1	1	0	14	14
1	0	0	0	0	16	16
1	0	0	1	0	18	18
1	0	1	0	0	18	20
1	0	1	1	0	18	22
1	1	0	0	0	18	24
1	1	0	1	0	18	24
1	1	1	0	0	18	24

7.21.2.3 Treble

A 2-bit value to program the treble setting. The used set depends on the mode bits. The default setting is given in Table 5.

Table 20 Treble settings

TR1	TR0	TREBLE		
		FLAT (dB)	MIN. (dB)	MAX. (dB)
0	0	0	0	0
0	1	0	2	2
1	0	0	4	4
1	1	0	6	6

7.21.2.4 Peak detection position

A 1-bit value to control the position of the peak level detector in the signal processing path. The default setting is given in Table 5.

Table 21 Peak detection position settings

PP	FUNCTION
0	before tone features
1	after tone features

7.21.2.5 De-emphasis

A 2-bit value to enable the digital de-emphasis filter. The default setting is given in Table 5.

Table 22 De-emphasis settings

DE1	DE0	FUNCTION
0	0	no de-emphasis
0	1	de-emphasis: 32 kHz
1	0	de-emphasis: 44.1 kHz
1	1	de-emphasis: 48 kHz

7.21.2.6 Mute

A 1-bit value to enable the digital mute. The default setting is given in Table 5.

Table 23 Mute settings

MT	FUNCTION
0	no mute
1	mute

7.21.2.7 Mode

A 2-bit value to program the mode of the sound processing filters of bass boost and treble. The default setting is given in Table 5.

Table 24 Mode filter switch settings

M1	M0	FUNCTION
0	0	flat
0	1	minimum
1	0	minimum
1	1	maximum

7.21.3 DATA0 EXTENDED PROGRAMMING REGISTERS

Table 25 Extended control registers

EA2	EA1	EA0	ED4	ED3	ED2	ED1	ED0	REGISTER SELECTED
0	0	0	MA4	MA3	MA2	MA1	MA0	MA = mixer gain channel 1 (5 bits)
0	0	1	MB4	MB3	MB2	MB1	MB0	MB = mixer gain channel 2 (5 bits)
0	1	0	MS2	MS1	MS0	MM1	MM0	MS = MIC sensitivity (3 bits)
								MM = mixer mode (2 bits)
1	0	0	AG	0	0	IG1	IG0	AG = AGC control
								IG = input amplifier gain channel 2 (2 bits)
1	0	1	IG6	IG5	IG4	IG3	IG2	IG = input amplifier gain channel 2 (5 bits)
1	1	0	AT2	AT1	AT0	AL1	AL0	AT = AGC time constant (3 bits)
								AL = AGC output level (2 bits)

Programming via extended addressing is done by first sending a DATA0 data byte EA (3 bits) which specifies the addresses of the extended register followed by a DATA0 data byte which specifies the contents of the extended data register (5 bits). The EA extended addresses and names of the extended data registers are given in Table 25.

7.21.3.1 Mixer gain control

Two 5-bit values to program the channel 1 (MA) and channel 2 (MB) coefficients in the mixer mode. The range is from 0 to –∞ dB in steps of 1.5 dB. The default settings are given in Table 5.

Table 26 Mixer gain control channel 1 and channel 2 settings

MA4 MB4	MA3 MB3	MA2 MB2	MA1 MB1	MA0 MB0	MIXER GAIN (dB)
0	0	0	0	0	0
0	0	0	0	1	–1.5
0	0	0	1	0	–3.0
:	:	:	:	:	:
1	1	1	0	1	–43.5
1	1	1	1	0	–45.0
1	1	1	1	1	–∞

7.21.3.2 MIC sensitivity

A 3-bit value to program eight gain settings of the microphone amplifier. These settings are valid only when AGC control is enabled and not in the double differential mode. The default setting is given in Table 5.

Table 27 MIC sensitivity settings

MS2	MS1	MS0	MIC AMPLIFIER GAIN (dB)
0	0	0	–3
0	0	1	0
0	1	0	+3
0	1	1	+9
1	0	0	+15
1	0	1	+21
1	1	0	+27
1	1	1	not used

7.21.3.3 Mixer mode

A 2-bit value to program the mode of the digital mixer. There are four modes: double differential, input channel 1 select, input channel 2 select and digital mixer mode. The default setting is given in Table 5.

Table 28 Mixer mode switch settings

MM1	MM0	FUNCTION
0	0	double differential mode
0	1	input channel 1 select (input channel 2 off)
1	0	input channel 2 select (input channel 1 off)
1	1	digital mixer mode (input 1 × MA + input 2 × MB)

7.21.3.4 AGC control

A 1-bit value to enable the AGC input. The default setting is given in Table 5.

Table 29 AGC control settings

AG	FUNCTION
0	disable AGC: manual gain setting through IG (7 bits)
1	enable AGC: gain control with manual MIC sensitivity setting

7.21.3.5 AGC output level

A 2-bit value to program the AGC output level. The default setting is given in Table 5.

Table 30 AGC output level settings

AL1	AL0	OUTPUT LEVEL (dB FS)
0	0	–9.0
0	1	–11.5
1	0	–15.0
1	1	–17.5

7.21.3.6 Input channel 2 amplifier gain

A 7-bit value to program the input channel 2 amplifier gain. The range is from –3 to +60.5 dB in steps of 0.5 dB. These settings are only valid when AGC control is disabled and not valid in the double differential mode.

Table 31 Input channel 2 amplifier gain settings

IG6	IG5	IG4	IG3	IG2	IG1	IG0	INPUT CHANNEL 2 AMPLIFIER GAIN (dB)
0	0	0	0	0	0	0	–3.0
0	0	0	0	0	0	1	–2.5
0	0	0	0	0	1	0	–2.0
0	0	0	0	0	1	1	–1.5
0	0	0	0	1	0	0	–1.0
0	0	0	0	1	0	1	–0.5
0	0	0	0	1	1	0	0.0
:	:	:	:	:	:	:	:
1	1	1	1	1	0	1	59.5
1	1	1	1	1	1	0	60.0
1	1	1	1	1	1	1	60.5

7.21.3.7 AGC time constant

A 3-bit value to program the attack and the decay parameters of the digital AGC. The default setting is given in Table 5.

Table 32 AGC time constant settings

AT2	AT1	AT0	ATTACK TIME (ms)	DECAY TIME (ns)
0	0	0	11	100
0	0	1	16	100
0	1	0	11	200
0	1	1	16	200
1	0	0	21	200
1	0	1	11	400
1	1	0	16	400
1	1	1	21	400

7.21.4 DATA1 CONTROL

Table 33 Data transfer of type 'DATA1'

BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	READ-OUT DATA
PL5	PL4	PL3	PL2	PL1	PL0	peak level value (6 bits)

7.21.4.1 Peak level value

A 6-bit value to indicate the peak level value of the playback data. The largest value of the left and right channel data in the playback signal path is held since the last read-out of the microcontroller.

Table 34 Peak level read-out data

PL5	PL4	PL3	PL2	PL1	PL0	PEAK VALUE(1) (dB)
0	0	0	0	0	0	$-\infty$
0	0	0	0	0	1	n.a.
0	0	0	0	1	0	n.a.
0	0	0	0	1	1	–90.31
0	0	0	1	0	0	n.a.
0	0	0	1	0	1	n.a.
0	0	0	1	1	0	n.a.
0	0	0	1	1	1	–84.29
:	:	:	:	:	:	:
0	1	0	0	1	1	note 2
0	1	0	1	0	0	note 3
:	:	:	:	:	:	:
1	1	1	1	0	1	–2.87
1	1	1	1	1	0	–1.48
1	1	1	1	1	1	0.00

Notes

1. Peak value (dB) = (Peak level – 63.5) $\times$ 5 $\times$ log 2.
2. For peak data >010011, the error in the peak value is $< \frac{11 \times \log 2}{4}$
3. For peak data <010100, the error is larger due to limited bit length.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); $V_{DDD} = V_{DDA} = 3$ V; all voltages measured with respect to ground; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	–	5.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	operating ambient temperature		–20	+85	°C
V_{es}	electrostatic handling	note 2	–2000	+2000	V
		note 3	–250	+250	V

Notes

1. All V_{DD} and V_{SS} connections must be made to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 µH series inductor.

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	90	K/W

10 DC CHARACTERISTICS

$V_{DDD} = V_{DDA} = 3$ V; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; all voltages measured with respect to ground (pins 1, 11 and 27); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{DDA(ADC)}$	ADC analog supply voltage	note 1	2.4	3.0	3.6	V
$V_{DDA(DAC)}$	DAC analog supply voltage	note 1	2.4	3.0	3.6	V
V_{DDD}	digital supply voltage	note 1	2.4	3.0	3.6	V
$I_{DDA(ADC)}$	ADC analog supply current	operation mode	–	12.5	–	mA
		ADC power-down	–	6.0	–	mA
$I_{DDA(DAC)}$	DAC analog supply current	operation mode	–	7.0	–	mA
		DAC power-down	–	50	–	µA
I_{DDD}	digital supply current	operation mode	–	7.0	–	mA
		DAC power-down	–	4.0	–	mA
		ADC power-down	–	3.0	–	mA
Digital input pins						
V_{IH}	HIGH-level input voltage		$0.8V_{DDD}$	–	$V_{DDD} + 0.5$	V
V_{IL}	LOW-level input voltage		–0.5	–	$0.2V_{DDD}$	V
$\|I_{LI}\|$	input leakage current		–	–	10	µA
C_i	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital output pins						
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–	–	0.4	V
Analog-to-digital converter						
V_{ADCP}	positive reference voltage		–	V_{DDA}	–	V
V_{ADCN}	negative reference voltage		0.0	0.0	0.0	V
$R_{o(ref)}$	V_{ref} reference output resistance	pin 28	–	24	–	kΩ
R_i	input resistance	measured at 1 kHz				
		stand-alone mode	–	12.5	–	kΩ
		double differential mode	–	6.25	–	kΩ
C_i	input capacitance		–	20	–	pF
Programmable gain amplifier (input channel 2)						
R_i	input resistance	microphone mode	–	12.5	–	kΩ
		double differential mode	–	>1	–	MΩ
Digital-to-analog converter						
R_o	output resistance		–	0.13	3.0	Ω
$I_{o(max)}$	maximum output current	(THD + N)/S < 0.1%	–	0.22	–	mA
R_L	load resistance		3	–	–	kΩ
C_L	load capacitance	note 2	–	–	50	pF
Reference voltage						
V_{ref}	reference voltage	with respect to V_{SSA}	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V

Notes

1. All power supply pins (V_{DD} and V_{SS}) must be connected to the same external power supply unit.
2. When higher capacitive loads (above 50 pF) must be driven then a resistor of 100 Ω must be connected in series with the DAC output in order to prevent oscillations in the output operational amplifier.

11 AC CHARACTERISTICS (ANALOG)

$V_{DDD} = V_{DDA} = 3$ V; $f_i = 1$ kHz; $f_s = 44.1$ kHz; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; all voltages measured with respect to ground (pins 1, 11 and 27); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converter						
$V_{i(rms)}$	input voltage (RMS value)	notes 1 and 2	–	1.0	–	V
ΔV_i	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	stand-alone mode				
		0 dB	–	–85	–80	dB
		–60 dB; A-weighted	–	–37	–33	dB
		double differential mode				
		0 dB	–	–90	–85	dB
		–60 dB; A-weighted	–	–40	–36	dB
S/N	signal-to-noise ratio	$V_i = 0$ V; A-weighted				
		stand-alone mode	–	97	–	dB
		double differential mode	–	100	–	dB
α_{cs}	channel separation		–	100	–	dB
PSRR	power supply rejection ratio	$f_{ripple} = 1$ kHz; $V_{ripple(p-p)} = 30$ mV	–	30	–	dB
Manual gain mode (AGC disabled)						
G_{min}	minimum gain		–	–3	–	dB
G_{max}	maximum gain		–	60.5	–	dB
G_{step}	digital gain step		–	0.5	–	dB
Programmable gain amplifier						
$V_{i(rms)}$	input voltage (RMS value)	at full-scale				
		–3 dB setting	–	1414	–	mV
		0 dB setting	–	1000	–	mV
		3 dB setting	–	708	–	mV
		9 dB setting	–	355	–	mV
		15 dB setting	–	178	–	mV
		21 dB setting	–	89	–	mV
		27 dB setting	–	44	–	mV
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB				
		–3 dB setting	–	–75	–	dB
		0 dB setting	–	–85	–	dB
		3 dB setting	–	–85	–	dB
		9 dB setting	–	–85	–	dB
		15 dB setting	–	–80	–	dB
		21 dB setting	–	–75	–	dB
		27 dB setting	–	–75	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at –60 dB; A-weighted				
		–3 dB setting	–	tbf	–	dB
		0 dB setting	–	–37	–	dB
		3 dB setting	–	tbf	–	dB
		9 dB setting	–	tbf	–	dB
		15 dB setting	–	tbf	–	dB
		27 dB setting	–	tbf	–	dB
Digital-to-analog converter						
$V_{o(rms)}$	output voltage (RMS value)	note 3	–	900	–	mV
ΔV_o	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	0 dB	–	–91	–86	dB
		–60 dB; A-weighted	–	–40	–	dB
S/N	signal-to-noise ratio	code = 0; A-weighted	–	100	–	dB
α_{cs}	channel separation		–	100	–	dB
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; $V_{ripple(p-p)}$ = 100 mV	–	50	–	dB

Notes

1. The ADC inputs can be used in a 2 V (RMS value) input signal configuration when a resistor of 12 kΩ is used in series with the inputs and 1 or 2 V (RMS value) input signal operation can be selected via the Input Gain Switch (IGS).
2. The ADC input signal scales inversely proportional with the power supply voltage.
3. The DAC output voltage scales linear with the DAC analog supply voltage.

12 AC CHARACTERISTICS (DIGITAL)

$V_{DDD} = V_{DDA} = 2.7$ to 3.6 V; $T_{amb} = -20$ to +85 °C; all voltages measured with respect to ground (pins 1, 11 and 27); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock timing (see Fig.8)						
T_{sys}	clock cycle time	$f_{sys} = 256f_s$	78	88	131	ns
		$f_{sys} = 384f_s$	52	59	87	ns
		$f_{sys} = 512f_s$	39	44	66	ns
t_{CWL}	LOW-level pulse width	$f_{sys} < 19.2$ MHz	$0.30T_{sys}$	–	$0.70T_{sys}$	ns
		$f_{sys} \geq 19.2$ MHz	$0.40T_{sys}$	–	$0.60T_{sys}$	ns
t_{CWH}	HIGH-level pulse width	$f_{sys} < 19.2$ MHz	$0.30T_{sys}$	–	$0.70T_{sys}$	ns
		$f_{sys} \geq 19.2$ MHz	$0.40T_{sys}$	–	$0.60T_{sys}$	ns
Serial input/output data timing (see Fig.9)						
T_{cy}	bit clock cycle time		300	–	–	ns
$t_{BCK(H)}$	bit clock HIGH time		100	–	–	ns
$t_{BCK(L)}$	bit clock LOW time		100	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{s;DATI}$	data input set-up time		20	–	–	ns
$t_{h;DATI}$	data input hold time		0	–	–	ns
$t_{d;DATO(BCK)}$	data output delay time (from BCK falling edge)		–	–	80	ns
$t_{d;DATO(WS)}$	data output delay time (from WS edge)	MSB-justified format	–	–	80	ns
$t_{h;DATO}$	data output hold time		0	–	–	ns
$t_{s;WS}$	word select set-up time		20	–	–	ns
$t_{h;WS}$	word select hold time		10	–	–	ns
Microcontroller L3-interface timing (see Figs 5 and 6)						
$T_{cy(CLK)(L3)}$	L3CLOCK		500	–	–	ns
$t_{CLK(L3)H}$	L3CLOCK HIGH time		250	–	–	ns
$t_{CLK(L3)L}$	L3CLOCK LOW time		250	–	–	ns
$t_{su(L3)A}$	L3MODE set-up time	addressing mode	190	–	–	ns
$t_{h(L3)A}$	L3MODE hold time	addressing mode	190	–	–	ns
$t_{su(L3)D}$	L3MODE set-up time	data transfer mode	190	–	–	ns
$t_{h(L3)D}$	L3MODE hold time	data transfer mode	190	–	–	ns
$t_{su(L3)DA}$	L3DATA set-up time	data transfer and addressing mode	190	–	–	ns
$t_{h(L3)DA}$	L3DATA hold time	data transfer and addressing mode	30	–	–	ns
$t_{stp(L3)}$	L3MODE halt time		190	–	–	ns

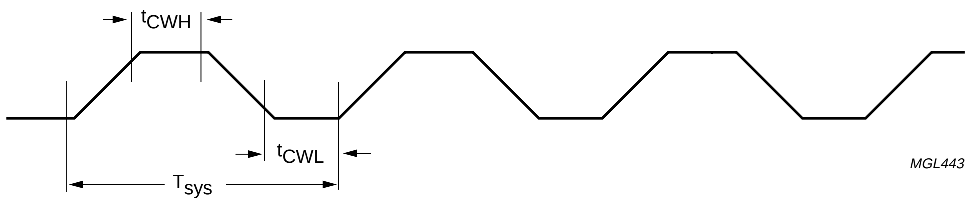


Fig.8 System clock timing.

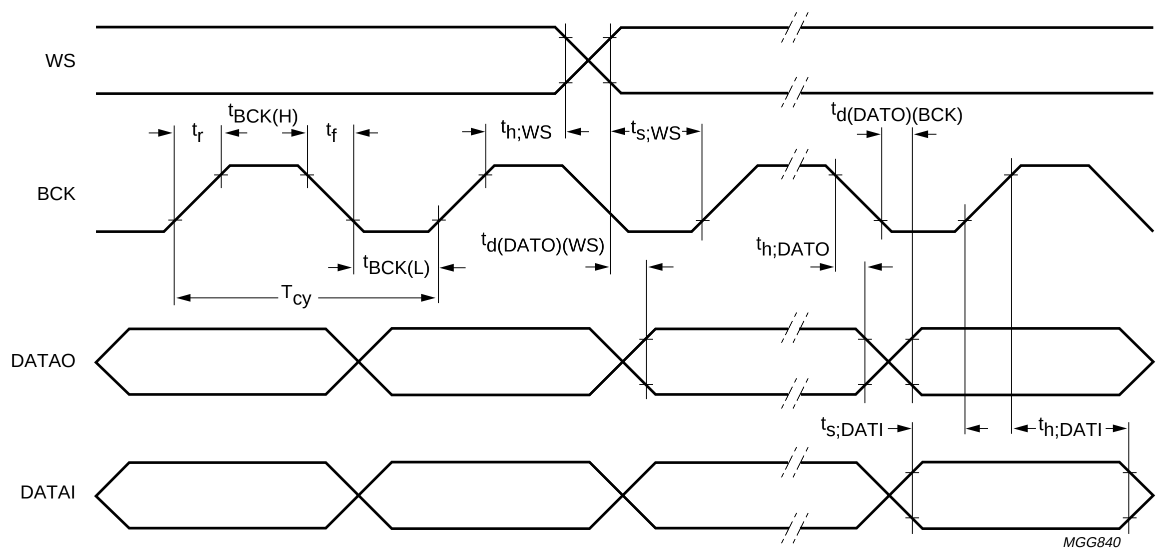


Fig.9 Serial interface timing.

13 APPLICATION INFORMATION

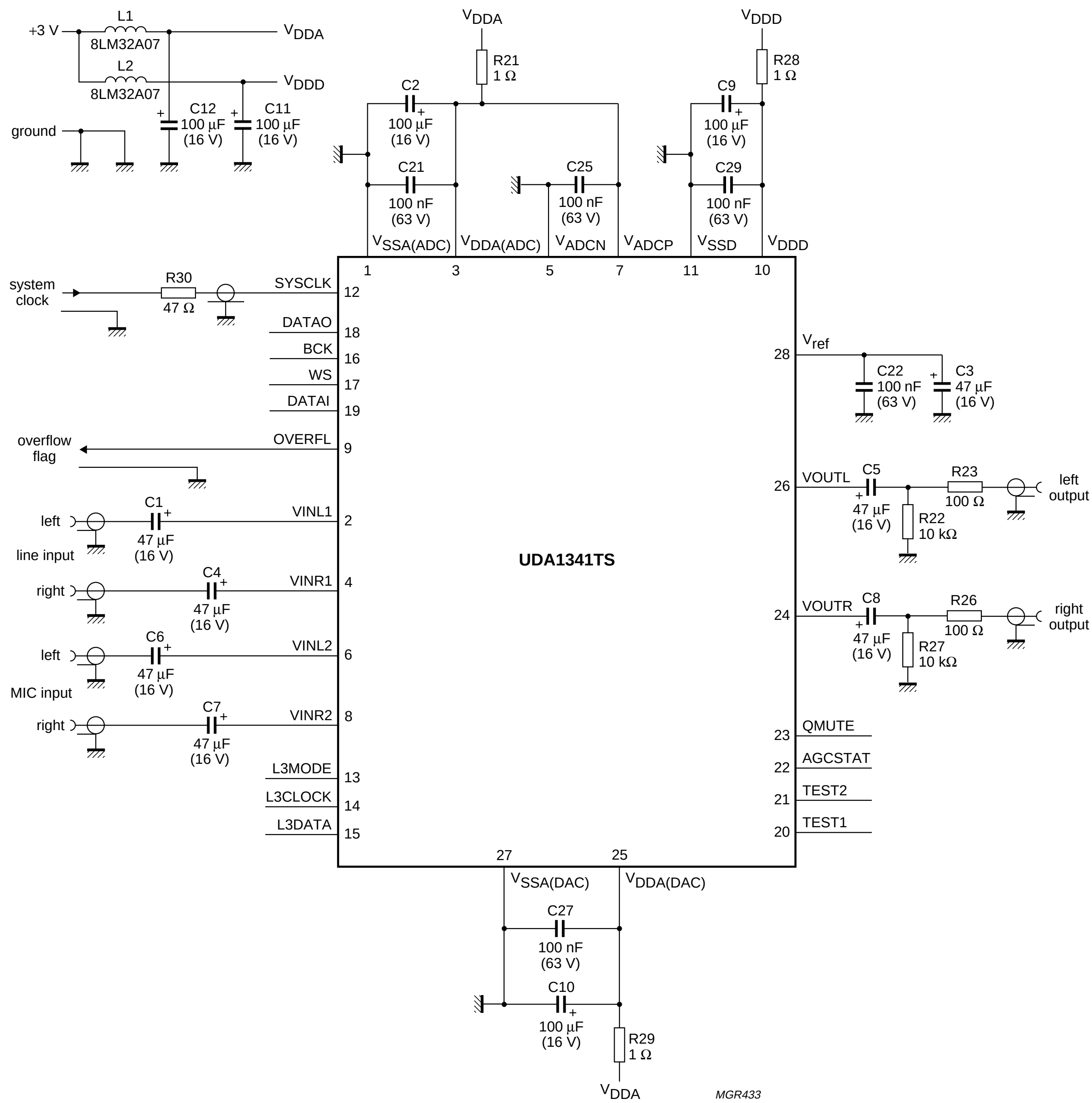
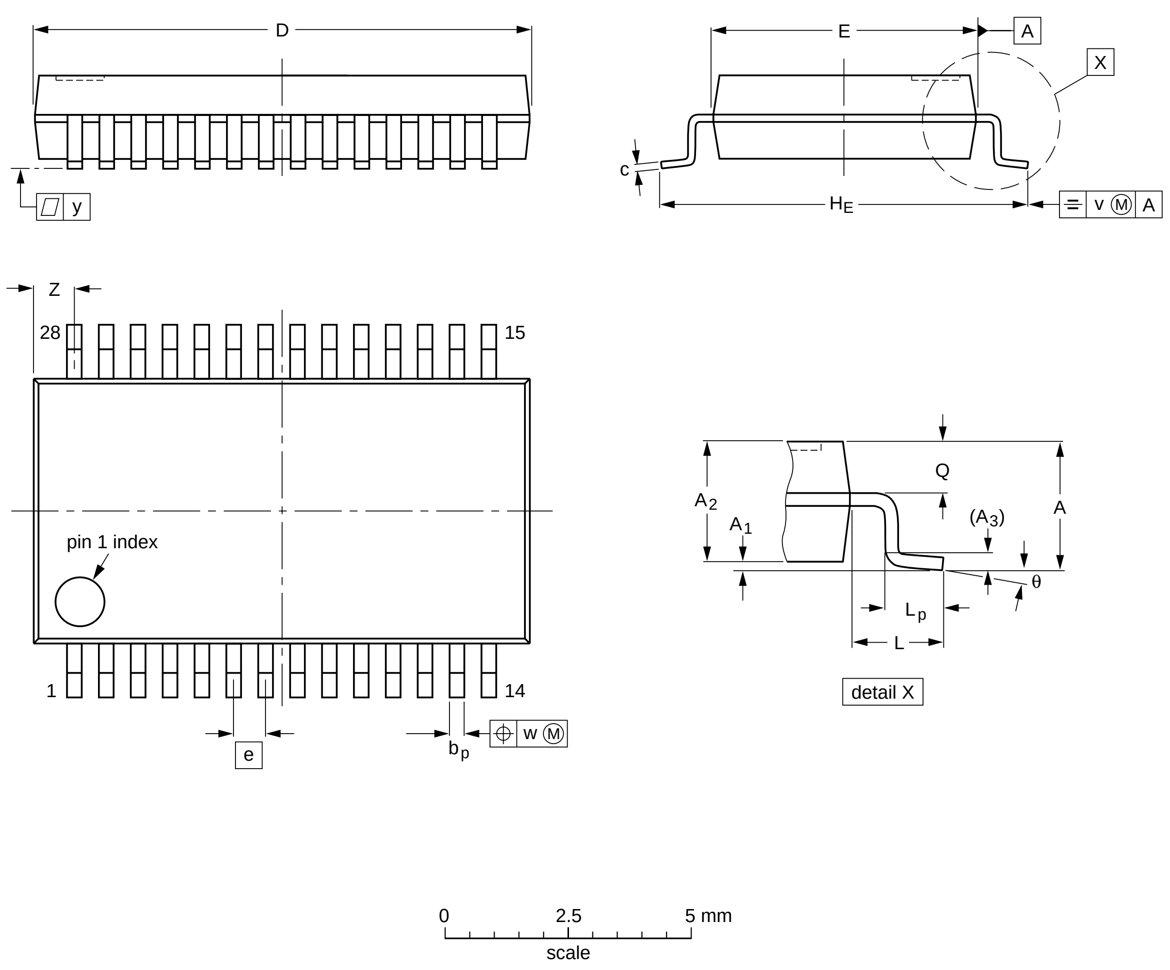


Fig.10 Application diagram.

14 PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

15 SOLDERING

15.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

15.2 Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

15.3 Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

17 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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