

Sample &

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TS5A3359

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Support &

Community

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TS5A3359 1-Ω SP3T Bidirectional Analog Switch 5-V/3.3-V Single-Channel 3:1 Multiplexer and Demultiplexer

Technical

Documents

1 Features

- Isolation in Power-Down Mode, V_{CC} = 0
- Specified Break-Before-Make Switching
- Low ON-State Resistance (1 Ω)
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection (5 pC V_{CC} = 1.8 V)
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals

3 Description

Tools &

Software

The TS5A3359 device is a bidirectional, single channel, single-pole triple-throw (SP3T) analog switch that is designed to operate from 1.65 V to 5.5 V. This device provides a signal switching solution while maintaining excellent signal integrity, which makes the TS5A3359 suitable for a wide range of applications in various markets including personal electronics, test and measurement equipment, and portable instrumentation. The device maintains the signal integrity by its low ON-state resistance, excellent ON-state resistance matching, and total harmonic distortion (THD) performance. To prevent signal distortion during the transferring of a signal from one channel to another, the TS5A3359 device also has a specified break-before-make feature. The device consumes very low power and provides isolation when $V_{CC} = 0$.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
T05402504	US8 (8)	2.30 mm × 2.00 mm
TS5A33591	DSBGA (8)	0.00 mm × 0.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic





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4 Revision History

CI	hanges from Revision D (May 2015) to Revision E Pa	age
•	Added T _J Junction Temperature to the <i>Absolute Maximum Ratings</i>	4
•	Changed Input leakage current UNIT value From: µA To: nA in <i>Electrical Characteristics for 5-V Supply</i>	5
CI	hanges from Revision C (June 2008) to Revision D Pa	age

•	Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation	
	section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and	
	Mechanical, Packaging, and Orderable Information section	1
•	Changed YZP pinout numbering.	3



5 Pin Configuration and Functions





Pin Functions

PIN		PIN I/O		DESCRIPTION		
NAME	DCU	YZP	1/0	DESCRIPTION		
NO0	1	A1	I/O	Normally open		
NO1	2	B1	I/O	Normally open		
NO2	3	C1	I/O	nally open		
GND	4	D1	_	und		
IN2	5	D2	I	ital control to connect COM to NO		
IN1	6	C2	I	Digital control to connect COM to NO		
СОМ	7	B2	I/O	nmon		
VCC	8	A2	—	Power supply		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽³⁾		-0.5	6.5	V
V _{NO} V _{COM}	Analog voltage ^{(3) (4) (5)}		-0.5	V _{CC} + 0.5	V
I _K	Analog port diode current V _{NO} , V _{COM} < 0		-50		mA
I _{NO}	On-state switch current	V_{NO} , $V_{COM} = 0$ to V_{CC}	-200	200	mA
ICOM	On-state switch current		-400	400	
VI	Digital input voltage ⁽³⁾ ⁽⁴⁾		-0.5	6.5	V
I _{IK}	Digital input clamp current	V ₁ < 0	-50		mA
I _{CC}	Continuous current through V _{CC}			100	mA
I _{GND}	Continuous current through GND	-100	100	mA	
T _{stg}	Storage temperature			150	°C
TJ	Junction temperature			150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(3) All voltages are with respect to ground, unless otherwise specified.

(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(5) This value is limited to 5.5-V maximum.

6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all $\ensuremath{\text{pins}^{(2)}}$	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}		1.65	5.5	V
V _{NO} V _{COM}	Analog voltage	0	V_{CC}	V
VI	Digital input voltage	0	V _{CC}	V

6.4 Thermal Information

		TS5A		
	THERMAL METRIC ⁽¹⁾	DCU (US8)	YZP (DSBGA)	UNIT
		8 PINS	8 PINS	
R_{\thetaJA}	Junction-to-ambient thermal resistance	204.2	105.8	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	76.2	1.6	°C/W
$R_{ extsf{ heta}JB}$	Junction-to-board thermal resistance	82.9	10.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.6	3.1	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	82.5	10.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics for 5-V Supply

 V_{CC} = 4.5 V to 5.5 V, T_A = -40°C to 85°C (unless otherwise noted)⁽¹⁾

PARAM	IETER	TEST COI	NDITIONS	TA	V _{cc}	MIN	TYP	MAX	UNIT	
ANALOG SWIT	СН									
Analog signal range	V _{COM} , V _{NO}					0		V _{CC}	V	
Peak ON resistance	r _{peak}	$0 \le (V_{NO}) \le V_{CC},$	Switch ON, See Figure 18	25°C	4.5 V		0.8	1.1	Ω	
resistance	F	$I_{COM} = -100 \text{ mA},$	See Figure 18	Full				1.5		
ON-state	r _{on}	$V_{NO} = 2.5 V,$	Switch ON,	25°C	4.5 V		0.7	0.9	Ω	
resistance	011	$I_{COM} = -100 \text{ mA},$	See Figure 18	Full				1.1		
ON-state				25°C			0.1	0.1		
resistance match between channels	Δr_{on}	$V_{NO} = 2.5 V,$ $I_{COM} = -100 mA,$	Switch ON, See Figure 18	Full	4.5 V			0.1	Ω	
ON-state resistance flatness		$0 \le (V_{NO}) \le V_{CC},$ $I_{COM} = -100 \text{ mA},$	Switch ON, See Figure 18	25°C			0.15			
	r _{on(flat)}	V _{NO} = 1 V, 1.5 V, 2.5	Switch ON,	25°C	4.5 V		0.1	0.25	Ω	
						See Figure 18				
		$V_{NO} = 1 \text{ V or } 4.5 \text{ V},$	Switch OFF,	25°C	5.5 V	-20	5	20	nA	
NO	I _{NO(OFF)}	$V_{COM} = 1 V \text{ to } 4.5 V,$	See Figure 19	Full		-150		150		
OFF leakage current		$I_{\text{NO(PWROFF)}} \begin{array}{l} V_{\text{NO}} = 0 \text{ to } 5.5 \text{ V}, \\ V_{\text{COM}} = 5.5 \text{ V to } 0, \end{array}$	Switch OFF,	25°C	0.14	-1	0.8	1		
				See Figure 19	Full	ull 0 V	-25		25	μA
NO	I	$V_{NO} = 1 V \text{ or } 4.5 V,$	Switch ON,	25°C		-30	5	30		
ON leakage current	I _{NO(ON)}	$V_{COM} = Open,$	See Figure 19	Full	5.5 V	-220		220	nA	
	V_{COM} = 1 V or 4.5 V, See	$V_{NO} = 4.5 \text{ V or } 1 \text{ V},$	Switch OFF,	25°C		-25	8	25	^	
COM			Full	5.5 V	-250		250	nA		
OFF leakage current		$V_{COM} = 0$ to 5.5 V,	Switch OFF,	25°C	0.)/	-8	0.1	8	۵	
	ICOM(PWROFF)	$V_{NO} = 5.5 V \text{ to } 0,$	See Figure 19	Full	0 V	-50		50	μA	
СОМ	1	V _{NO} = Open,	Switch ON,	25°C		-30	5	30		
ON leakage current	$V_{\text{NO}} = \text{Open},$ $V_{\text{COM}} = 1 \text{ V or } 4$	$V_{COM} = 1 \text{ V or } 4.5 \text{ V},$	See Figure 19	Full	5.5 V	-220		220	nA	
DIGITAL CONT	ROL INPUTS (IN1, IN2) ⁽²⁾								
Input logic high	V _{IH}			Full		2.4		5.5	V	
Input logic low	V _{IL}			Full		0		0.8	V	
Input leakage				25°C		-2		2		
current	I _{IH} , I _{IL}	$V_{I} = 5.5 V \text{ or } 0$		Full	5.5 V	-20		20	nA	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

Electrical Characteristics for 5-V Supply (continued)

PARAMETER		TEST CONDITIONS			V _{CC}	MIN	TYP	MAX	UNIT
DYNAMIC									
Turne en time e		$V_{COM} = V_{CC}$	C ₁ = 35 pF,	25°C	5 V	1	2.5	21	
Turnon time	t _{ON}	$R_L = 50 \Omega$,	See Figure 22	Full	4.5 V to 5.5 V	1		23.5	ns
Turn off times		$V_{COM} = V_{CC},$	C _L = 35 pF,	25°C	5 V	1	6	10.5	20
Turnoff time	off time t _{OFF}	$R_L = 50 \Omega$,	See Figure 22	Full	4.5 V to 5.5 V	1		12	ns
Break-before-	t	$V_{NO} = V_{CC},$	C _L = 35 pF,	25°C	5 V	0.5	8.5	18	ns
make time	t _{BBM}	$R_L = 50 \Omega$,	See Figure 23	Full	4.5 V to 5.5 V	0.5		23	115
Charge injection	Q _C	$V_{GEN} = 0,$ $R_{GEN} = 0,$	C _L = 1 nF, See Figure 27	25°C	5 V		20		рС
NO OFF capacitance	$C_{\text{NO(OFF)}}$	$V_{NO} = V_{CC}$ or GND, Switch OFF,	See Figure 21	25°C	5 V		18		pF
COM OFF capacitance	$C_{\text{COM}(\text{OFF})}$	$V_{COM} = V_{CC}$ or GND, Switch OFF,	See Figure 21	25°C	2.5 V		54		pF
NO ON capacitance	C _{NO(ON)}	$V_{NO} = V_{CC}$ or GND, Switch ON,	See Figure 21	25°C	5 V		78		pF
COM ON capacitance	C _{COM(ON)}	$V_{COM} = V_{CC}$ or GND, Switch ON,	See Figure 21	25°C	5 V		78		pF
Digital input capacitance	CI	$V_I = V_{CC}$ or GND,	See Figure 21	25°C	5 V		2.5		pF
Bandwidth	BW	$R_L = 50 $ Ω, Switch ON,	See Figure 24	25°C	5 V		75		MHz
OFF isolation	O _{ISO}		Switch OFF, See Figure 25	25°C	5 V		-64		dB
Crosstalk	X _{TALK}	$ \begin{array}{l} R_{L} = 50 \ \Omega, \\ f = 1 \ MHz \ , \end{array} $	Switch ON, See Figure 26	25°C	5 V		-64		dB
Total harmonic distortion	THD	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 20 Hz to 20 kHz, See Figure 28	25°C	5 V		0.005%		
SUPPLY		· · · · · · · · · · · · · · · · · · ·			· · · · · · · · · · · · · · · · · · ·				
Positive supply	1			25°C	E E V		16	50	~ ^
current	I _{CC}	$V_I = V_{CC}$ or GND,	Switch ON or OFF	Full	5.5 V			1200	nA

6.6 Electrical Characteristics for 3.3-V Supply

 V_{CC} = 3 V to 3.6 V, T_{A} = –40°C to 85°C (unless otherwise noted) $^{(1)}$

PARAN	IETER	TEST CO	ONDITIONS	T _A	V _{cc}	MIN	TYP	MAX	UNIT
ANALOG SWIT	СН								
Analog signal range	V _{COM} , V _{NO}					0		V _{CC}	V
Peak ON	r	$0 \le (V_{NO}) \le V_{CC},$	Switch ON,	25°C	3 V		1.3	1.6	Ω
resistance	r _{peak}	$I_{COM} = -100 \text{ mA},$	See Figure 18	Full	0 1			2	32
ON-state	r _{on}	$V_{NO} = 2 V$,	Switch ON,	25°C	3 V		1.2	1.6	Ω
resistance	011	$I_{COM} = -100 \text{ mA},$	See Figure 18	Full				1.8	
ON-state resistance		V _{NO} = 2 V, 0.8 V,	Switch ON,	25°C			0.1	0.15	
match between channels	∆r _{on}	$I_{\rm COM} = -100 \text{ mA},$	See Figure 18	Full	Full 3 V			0.15	Ω
ON-state		$\begin{array}{l} 0 \leq (V_{\rm NO}) \leq V_{\rm CC}, \\ I_{\rm COM} = -100 \ {\rm mA}, \end{array}$	Switch ON, See Figure 18	25°C	21/		0.2		
resistance flatness	r _{on(flat)}	V _{NO} = 2 V, 0.8 V,	Switch ON,	25°C	3 V		0.2	0.35	Ω
		$I_{COM} = -100 \text{ mA},$	See Figure 18	Full				0.35	
	I _{NO(OFF)}	$V_{NO} = 1 V \text{ or } 3 V,$	Switch OFF,	25°C	3.6 V	-15	3	15	nA
NO OFF leakage		$V_{COM} = 1 V \text{ to } 3 V,$	See Figure 19	Full	0.0 1	-30		30	10.0
current	I _{NO(PWROFF)}	$V_{NO} = 0$ to 3.6 V,	Switch OFF,	25°C	0 V	-1	0.2	1	μA
		$V_{COM} = 3.6 V \text{ to } 0,$	See Figure 19	Full	-	-10		10	F.
NO ON leakage	I _{NO(ON)}	$V_{NO} = 1 V \text{ or } 3 V,$	Switch ON,	25°C	3.6 V	-15	3	15	nA
current	'NO(ON)	V _{COM} = Open,	See Figure 19	Full	0.0 1	-40		40	
		$V_{NO} = 0 V \text{ to } 3.6 V,$		25°C		-15	3	15	
COM OFF leakage	I _{COM(OFF)}	$V_{COM} = 1 V \text{ or}$ $V_{NO} = 3.6 V \text{ to } 0,$ $V_{COM} = 3 V,$	Switch OFF, See Figure 19	Full	3.6 V	-75		75	nA
current	1	$V_{COM} = 0$ to 3.6 V,	Switch OFF,	25°C	0 V	-1 0.2	1	μA	
	I _{COM} (PWROFF)	$V_{NO} = 3.6 V \text{ to } 0,$	See Figure 19	Full	0 0	-20		20	μΑ
COM		V _{NO} = Open,	Switch ON,	25°C	0.0.1/	-15	4	15	
ON leakage current	I _{COM(ON)}	$V_{COM} = 1 V \text{ or } 3 V,$	See Figure 19	Full	3.6 V	-40		40	nA
DIGITAL CONT	ROL INPUTS (IN1, IN2) ⁽²⁾				1			
Input logic high	V _{IH}			Full		2		5.5	V
Input logic low	V _{IL}			Full		0		0.8	V
Input leakage		V _I = 5.5 V or 0		25°C	3.6 V	-2		2	nA
current	I _{IH} , I _{IL}	vi = 3.3 v 0i 0		Full	3.0 V	-20		20	11A

(1)

The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004). (2)

Electrical Characteristics for 3.3-V Supply (continued)

V_{CC} = 3 V to 3.6 V, T_A = -40°C to 85°C (unless otherwise	noted) ⁽¹⁾
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PARAM	IETER	TEST CO	NDITIONS	TA	V _{CC}	MIN	TYP	MAX	UNIT
DYNAMIC									
T		$V_{COM} = V_{CC}$	$C_{1} = 35 pF_{2}$	25°C	3.3 V	1	16	30.5	
Turnon time	t _{ON}	$R_L = 50 \Omega$,	See Figure 22	Full	3 V to 3.6 V	1		34	ns
T	$V_{COM} = V_{CC},$	$V_{COM} = V_{CC}$	$C_1 = 35 \text{pF},$	25°C	3.3 V	1	6	11.5	
Turnoff time	t _{OFF}	$R_L = 50 \Omega$,	See Figure 22	Full	3 V to 3.6 V	1		12.5	ns
Break-before-		$V_{NO} = V_{CC},$	C _L = 35 pF,	25°C	3.3 V	0.5	13	26	
make time	t _{BBM}	$R_L = 50 \Omega$,	See Figure 23	Full	3 V to 3.6 V	0.5		30	ns
Charge injection	Q _C	$V_{GEN} = 0,$ $R_{GEN} = 0,$	C _L = 1 nF, See Figure 27	25°C	3.3 V		12		рС
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_{CC}$ or GND, Switch OFF,	See Figure 21	25°C	3.3 V		18		pF
COM OFF capacitance	$C_{\text{COM}(\text{OFF})}$	$V_{COM} = V_{CC}$ or GND, Switch OFF,	See Figure 21	25°C	3.3 V		55		pF
NO ON capacitance	C _{NO(ON)}	$V_{NO} = V_{CC}$ or GND, Switch ON,	See Figure 21	25°C	3.3 V		78		pF
COM ON capacitance	C _{COM(ON)}	$V_{COM} = V_{CC}$ or GND, Switch ON,	See Figure 21	25°C	3.3 V		78		pF
Digital input capacitance	Cl	$V_I = V_{CC}$ or GND,	See Figure 21	25°C	3.3 V		2.5		pF
Bandwidth	BW	$R_L = 50 \Omega$, Switch ON,	See Figure 24	25°C	3.3 V		73		MHz
OFF isolation	O _{ISO}	$ \begin{array}{l} R_{L} = 50 \ \Omega, \\ f = 1 \ MHz, \end{array} $	Switch OFF, See Figure 25	25°C	3.3 V		-64		dB
Crosstalk	X _{TALK}	$\begin{array}{l} R_{L} = 50 \ \Omega, \\ f = 1 \ MHz, \end{array}$	Switch ON, See Figure 26	25°C	3.3 V		-64		dB
Total harmonic distortion	THD	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 20 Hz to 20 kHz, See Figure 28	25°C	3.3 V		0.01%		
SUPPLY					·				
Positive supply	1	$V_{I} = V_{CC}$ or GND,	Switch ON or OFF	25°C	3.6 V		2	20	n^
current	I _{CC}	$v_{\rm I} = v_{\rm CC}$ of GND,	Switch ON OF OFF	Full	3.0 V			350	nA

6.7 Electrical Characteristics for 2.5-V Supply

 V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted) $^{(1)}$

PARAM	IETER	TEST CON	IDITIONS	T _A	V _{cc}	MIN	TYP	MAX	UNIT
ANALOG SWIT	СН								
Analog signal range	V _{COM} , V _{NO}					0		V _{CC}	V
Peak ON	r .	$0 \le (V_{NO}) \le V_{CC},$	Switch ON,	25°C	2.3 V		1.8	2.5	Ω
resistance	r _{peak}	$I_{COM} = -8 \text{ mA},$	See Figure 18	Full	2.5 V			2.7	32
ON-state	r _{on}	V _{NO} = 1.8 V,	Switch ON,	25°C	2.3 V		1.5	2	Ω
resistance	on	$I_{COM} = -8 \text{ mA},$	See Figure 18	Full	2.0 1			2.4	
ON-state resistance		V _{NO} = 1.8 V,	Switch ON,	25°C				0.2	
match between channels	Δr_{on}	$V_{\rm NO} = 1.6 \text{ V},$ $I_{\rm COM} = -8 \text{ mA},$	See Figure 18	Full	2.3 V			0.2	Ω
ON-state resistance flatness		$\begin{array}{l} 0 \leq (V_{NO}) \leq V_{CC}, \\ I_{COM} = -8 \ mA, \end{array}$	Switch ON, See Figure 18	25°C	0.0.1/		0.6		0
	r _{on(flat)}	V _{NO} = 0.8 V, 1.8 V	Switch ON,	25°C	2.3 V		0.6	1	Ω
		$I_{COM} = -8 \text{ mA},$	See Figure 18	Full				1	
NO OFF leakage		$V_{NO} = 0.5 V \text{ or } 2.3 V,$	Switch OFF,	25°C	2.7 V	-15	3	15	nA
	NO(OFF)	$V_{COM} = 0.5 V \text{ to } 2.3 V,$	See Figure 19	Full		-30		30	
current	I _{NO(PWROFF)}	$V_{NO} = 0$ to 2.7 V,	Switch OFF,	25°C	0 V	-1	0.1	1	μA
		$V_{COM} = 2.7 V \text{ to } 0,$	See Figure 19	Full		-10		10	
NO ON leakage	I _{NO(ON)}	$V_{NO} = 0.5 V \text{ or } 2.3 V,$	Switch ON,	25°C	2.7 V	-15	3	15	nA
current	'NO(ON)	V _{COM} = Open,	See Figure 19	Full	2.7 1	-35		35	
	1	$V_{NO} = 0.3 V \text{ to } 2.3 V,$	Switch OFF,	25°C	2.7 V	-15	3	15	- 0
COM OFF leakage	I _{COM(OFF)}	$V_{COM} = 0.5 V \text{ or } 2.3 V,$	See Figure 19	Full	2.1 V	-60		60	nA
current		$V_{COM} = 0$ to 2.7 V,	Switch OFF,	25°C	0 V	-1	0.1	1	μA
	ICOM(PWROFF)	$V_{NO} = 2.7 V \text{ to } 0,$	See Figure 19	Full	0 0	-10		10	μΛ
COM		V _{NO} = Open,	Switch ON,	25°C	271/	-15	3.5	15	54
ON leakage current	I _{COM(ON)}	$V_{COM} = 0.5 \text{ V or } 2.2 \text{ V},$	See Figure 19	Full	2.7 V	-40		40	nA
DIGITAL CONT	ROL INPUTS (IN1, IN2) ⁽²⁾							
Input logic high	V _{IH}			Full		1.8		5.5	V
Input logic low	V _{IL}			Full		0		0.6	V
Input leakage	I _{IH} , I _{IL}	V ₁ = 5.5 V or 0		25°C	2.7 V	1		1	nΔ
current	ıH, IL	vi – 0.0 v 0i 0		Full	2.1 V	10		10	nA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

Electrical Characteristics for 2.5-V Supply (continued)

V_{CC} = 2.3 V to 2.7 V, T_A = -40°C to 85°C (unless otherwise note	d) ⁽¹⁾
---	-------------------

PARAM	IETER	TEST CONDITIONS			V _{cc}	MIN	TYP	MAX	UNIT
DYNAMIC									
Turn on time		$V_{COM} = V_{CC},$	C _L = 35 pF,	25°C	2.5 V	2	4.5	43	~~
Turnon time	t _{ON}	$R_L = 50 \Omega$,	See Figure 22	Full	2.3 V to 2.7 V	2		47.5	ns
Turnoff time	+	$V_{COM} = V_{CC},$	C _L = 35 pF,	25°C	2.5 V	2	8.5	11	ns
rumon ume	t _{OFF}	$R_L = 50 \Omega$,	See Figure 22	Full	2.3 V to 2.7 V	2		12.5	115
Break-before-	taav	$V_{NO} = V_{CC},$	C _L = 35 pF,	25°C	2.5 V	0.5	18.5	38.5	ns
make time	t _{BBM}	$R_L = 50 \Omega$,	See Figure 23	Full	2.3 V to 2.7 V	0.5		43	115
Charge injection	Q _C	$V_{GEN} = 0,$ $R_{GEN} = 0,$	C _L = 1 nF, See <mark>Figure 27</mark>	25°C	2.5 V		8		рС
NO OFF capacitance	$C_{\text{NO(OFF)}}$	$V_{NO} = V_{CC}$ or GND, Switch OFF,	See Figure 21	25°C	2.5 V		18.5		pF
COM OFF capacitance	$C_{\text{COM}(\text{OFF})}$	$V_{COM} = V_{CC}$ or GND, Switch OFF,	See Figure 21	25°C	2.5 V		55		pF
NO ON capacitance	C _{NO(ON)}	$V_{NO} = V_{CC}$ or GND, Switch ON,	See Figure 21	25°C	2.5 V		78		pF
COM ON capacitance	C _{COM(ON)}	$V_{COM} = V_{CC}$ or GND, Switch ON,	See Figure 21	25°C	2.5 V		78		pF
Digital input capacitance	Cl	$V_{I} = V_{CC}$ or GND,	See Figure 21	25°C	2.5 V		3		pF
Bandwidth	BW	$R_L = 50 \Omega$, Switch ON,	See Figure 24	25°C	2.5 V		73		MHz
OFF isolation	O _{ISO}	$\begin{array}{l} R_{L} = 50 \ \Omega, \\ f = 1 \ MHz, \end{array}$	Switch OFF, See Figure 25	25°C	2.5 V		-64		dB
Crosstalk	X _{TALK}	$\begin{array}{l} R_{L} = 50 \ \Omega, \\ f = 1 \ MHz, \end{array}$	Switch ON, See Figure 26	25°C	2.5 V		-64		dB
Total harmonic distortion	THD	$R_L = 600 \Omega,$ $C_L = 50 pF,$	f = 20 Hz to 20 kHz, See Figure 28	25°C	2.5 V		0.03%		
SUPPLY									
Positive supply	Icc	$V_{I} = V_{CC}$ or GND,	Switch ON or OFF	25°C	2.7 V		1	10	nA
current	ICC		GWIGH ON ULOFF	Full	2.1 V			250	ПA



6.8 Electrical Characteristics for 1.8-V Supply

 V_{CC} = 1.65 V to 1.95 V, T_A = -40°C to 85°C (unless otherwise noted)⁽¹⁾

PARAM	ETER	TEST CON	DITIONS	TA	V _{cc}	MIN	TYP	MAX	UNIT
ANALOG SWIT	ГСН								
Analog signal range	V_{COM}, V_{NO}					0		V _{CC}	V
Peak ON resistance	r _{peak}	$0 \le (V_{NO}) \le V_{CC},$ $I_{COM} = -2 \text{ mA},$	Switch ON, See Figure 18	25°C Full	1.65 V		5	30	Ω
ON-state resistance	r _{on}	$V_{NO} = 1.5 V,$ $I_{COM} = -2 mA,$	Switch ON, See Figure 18	25°C Full	1.65 V		2	2.5 3.5	Ω
ON-state				25°C			0.15	0.4	
resistance match between channels	Δr _{on}	$V_{NO} = 1.5 V,$ $I_{COM} = -2 mA,$	Switch ON, See Figure 18	Full	1.65 V			0.4	Ω
ON-state resistance flatness		$0 \le (V_{NO}) \le V_{CC},$ $I_{COM} = -2 \text{ mA},$	Switch ON, See Figure 18	25°C	1.65 V		5		Ω
	r _{on(flat)}	$V_{NO} = 0.6 V, 1.5 V$ $I_{COM} = -2 mA,$	Switch ON, See Figure 18	25°C Full			4.5 5		
NO	I _{NO(OFF)}	V _{NO} =0.3 V or 1.65 V, V _{COM} = 0.3 V to 1.65 V,	Switch OFF, See Figure 19	25°C Full	1.95 V	-15 -30	3	15 30	nA
OFF leakage current	I _{NO(PWROFF)}	$V_{NO} = 0$ to 1.95 V,	Switch OFF,	25°C	0 V	-1	0.1	1	μA
NO		$V_{COM} = 1.95 V \text{ to } 0,$ $V_{NO} = 0.3 V \text{ or } 1.65 V,$	See Figure 19 Switch ON,	Full 25°C		-15 -15	3	15 15	nA
ON leakage current	I _{NO(ON)}	$V_{COM} = Open,$	See Figure 19	Full	1.95 V	-30		30	
СОМ	I _{COM(OFF)}	$V_{NO} = 0.3 V \text{ to } 1.65 V,$ $V_{COM} = 0.3 V \text{ or } 1.65 V,$	Switch OFF, See Figure 19	25°C Full	1.95 V	-15 -50	3	15 50	nA
OFF leakage current	I _{COM(PWROF} F)	V _{COM} = 0 to 1.95 V, V _{NO} = 1.95 V to 0,	Switch OFF, See Figure 19	25°C Full	0 V	-1 -10	0.1	1 10	μA
COM		V _{NO} = Open,	Switch ON,	25°C	1.95 V	-15	3	15	۳A
ON leakage current	I _{COM(ON)}	$V_{COM} = 0.3 \text{ V or } 1.65 \text{ V},$	See Figure 19	Full	1.90 V	-30		30	nA
DIGITAL CONT	ROL INPUTS	(IN1, IN2) ⁽²⁾							
Input logic high	V _{IH}			Full		1.5		5.5	V
Input logic low	V _{IL}			Full		0		0.6	V
Input leakage current	I _{IH} , I _{IL}	$V_{I} = 5.5 V \text{ or } 0$		25°C Full	1.95 V	-2 -20		2 20	nA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

 (2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, SCBA004.

Electrical Characteristics for 1.8-V Supply (continued)

 V_{CC} = 1.65 V to 1.95 V, T_A = -40°C to 85°C (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			V _{cc}	MIN	TYP	MAX	UNIT
DYNAMIC				I	<u>I</u> I				
Turne en time e		$V_{COM} = V_{CC},$	$C_1 = 35 pF_1$	25°C	1.8 V	3	38.5	85	
Turnon time	t _{ON}	$R_L = 50 \Omega$,	See Figure 22	Full	1.65 V to 1.95 V	3		90	ns
Turnoff time		$V_{COM} = V_{CC},$	C _L = 35 pF,	25°C	1.8 V	2	8.5	16	20
rumon time	t _{OFF}	$R_L = 50 \Omega$,	See Figure 22	Full	1.65 V to 1.95 V	2		18	ns
Break-before-	t	$V_{NO} = V_{CC},$	C _L = 35 pF,	25°C	1.8 V	1	33	75	ns
make time	t _{BBM}	$R_L = 50 \Omega$,	See Figure 23	Full	1.65 V to 1.95 V	1		80	115
Charge injection	Q _C	$V_{GEN} = 0,$ $R_{GEN} = 0,$	C _L = 1 nF, See Figure 27	25°C	1.8 V		5		рС
NO OFF capacitance	$C_{\text{NO(OFF)}}$	$V_{NO} = V_{CC}$ or GND, Switch OFF,	See Figure 21	25°C	1.8 V		18.5		pF
COM OFF capacitance	$C_{\text{COM(OFF)}}$	$V_{COM} = V_{CC}$ or GND, Switch OFF,	See Figure 21	25°C	1.8 V		55		pF
NO ON capacitance	C _{NO(ON)}	$V_{NO} = V_{CC}$ or GND, Switch ON,	See Figure 21	25°C	1.8 V		78		pF
COM ON capacitance	C _{COM(ON)}	$V_{COM} = V_{CC}$ or GND, Switch ON,	See Figure 21	25°C	1.8 V		78		pF
Digital input capacitance	CI	$V_{I} = V_{CC}$ or GND,	See Figure 21	25°C	1.8 V		3		pF
Bandwidth	BW	$R_{L} = 50 \Omega$, Switch ON,	See Figure 24	25°C	1.8 V		73		MHz
OFF isolation	O _{ISO}		Switch OFF, See Figure 25	25°C	1.8 V		-64		dB
Crosstalk	X _{TALK}	$ \begin{array}{l} R_{L} = 50 \ \Omega, \\ f = 1 \ MHz, \end{array} $	Switch ON, See Figure 26	25°C	1.8 V		-64		dB
Total harmonic distortion	THD		f = 20 Hz to 20 kHz, See Figure 28	25°C	1.8 V		0.08%		
SUPPLY					· · · · · · · · · · · · · · · · · · ·				
Positive supply current	I _{CC}	$V_{I} = V_{CC}$ or GND,	Switch ON or OFF	25°C Full	1.95 V		1	200	nA



6.9 Typical Characteristics





Typical Characteristics (continued)





Typical Characteristics (continued)



7 Parameter Measurement Information











Figure 20. ON-State Leakage Current (I_{COM(ON)}, I_{NO(ON)})



Parameter Measurement Information (continued)







- A. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, ZO = 50 Ω , t_r < 5 ns, t_f < 5 ns.
- B. C_L includes probe and jig capacitance.

Figure 22. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

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A. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, ZO = 50 Ω , t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.





Figure 24. Bandwidth (BW)







Channel ON: NO0 to COM

Network Analyzer Setup

(632-mV P-P at 50-Ω load)

Source Power = 0 dBM

DC Bias = 350 mV

 $V_I = V_{CC}$ or GND

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Figure 26. Crosstalk (X_{TALK})



- A. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, ZO = 50 Ω , t_r < 5 ns, t_f < 5 ns.
- B. C_L includes probe and jig capacitance.

Figure 27. Charge Injection (Q_c)



A. C_L includes probe and jig capacitance.



NSTRUMENTS

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Table 1. Parameter Description

SYMBOL	DESCRIPTION
V _{COM}	Voltage at COM
V _{NO}	Voltage at NO
r _{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
r _{peak}	Peak ON-state resistance over a specified voltage range
Δr _{on}	Difference of r _{on} between channels in a specific device
r _{on(flat)}	Difference between the maximum and minimum value of ron in a channel over the specified range of conditions
I _{NO(OFF)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
I _{NO(PWROFF)}	Leakage current measured at the NO port during the power-down condition, $V_{CC} = 0$.
I _{NO(ON)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
I _{COM(ON)}	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
I _{COM(OFF)}	Leakage current measured at the COM port during the power-down condition, $V_{CC} = 0$
I _{COM(PWROFF)}	Leakage current measured at the COM port during the power-down condition, $V_{CC} = 0$.
V _{IH}	Minimum input voltage for logic high for the control input (IN)
V _{IL}	Maximum input voltage for logic low for the control input (IN)
VI	Voltage at the control input (IN)
I _{IH} , I _{IL}	Leakage current measured at the control input (IN)
t _{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t _{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
t _{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q _C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_c = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
C _{NO(OFF)}	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
C _{NO(ON)}	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
C _{COM(ON)}	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C _{COM(OFF)}	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
CI	Capacitance of control input (IN)
O _{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X _{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is -3 dB less than the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I _{CC}	Static power-supply current with the control (IN) pin at V _{CC} or GND

PARAMETER	CHARACTERISTIC
Configuration	Triple 3:1 Multiplexer/ Demultiplexer (1 × SP3T)
Number of channels	1
ON-state resistance (ron)	1.1 Ω
ON-state resistance match (Δr_{on})	0.1 Ω
ON-state resistance flatness (r _{on(flat)})	0.15 Ω
Turnon/turnoff time (t _{ON} /t _{OFF})	40 ns/35 ns
Break-before-make time (t _{BBM})	1 ns
Charge injection (Q _C)	40 pC
Bandwidth (BW)	100 MHz
OFF isolation (O _{ISO})	-65 dB at 10 MHz
Crosstalk (X _{TALK})	-66 dB at 10 MHz
Total harmonic distortion (THD)	0.01%
Leakage current (I _{COM(OFF)} /I _{NO(OFF)})	±20 μΑ
Power supply current (I _{CC})	0.1 µA
Package options	8-pin DCU or YZP

Table 2. Summary of Characteristics⁽¹⁾

(1) $V_{CC} = 5 V, T_A = 25^{\circ}C$

8 Detailed Description

8.1 Overview

The TS5A3359 is a bidirectional, single-channel, single-pole triple-throw (SP3T) analog switch that is designed to operate from 1.65 V to 5.5 V. This device provides a signal switching solution while maintaining excellent signal integrity, which makes the TS5A3359 suitable for a wide range of applications in various markets including personal electronics, portable instrumentation, and test and measurement equipment. The device maintains the signal integrity by its low ON-state resistance, excellent ON-state resistance matching, and total harmonic distortion (THD) performance. To prevent signal distortion during the transferring of a signal from one channel to another, the TS5A3359 device also has a specified break-before-make feature. The device consumes very low power and provides isolation when $V_{CC} = 0$.

8.2 Functional Block Diagram



8.3 Feature Description

Isolation in Power-Down Mode, $V_{CC} = 0$

When power is not supplied to the VCC pin, $V_{CC} = 0$, the signal paths NO and COM are high impedance. This is specificed in the electrical characterisitics table under the COM and NO OFF leakage current when $V_{CC} = 0$. Because the device is high impedance when it is not powered, you may connect other signals to the signal chain without interference of the TS5A3359.

8.4 Device Functional Modes

IN2	IN1	COM TO NO, NO TO COM
L	L	OFF
L	Н	COM = NO0
Н	L	COM = NO1
н	Н	COM = NO2

Table 3. Function Table



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A3359 switch is bidirectional, so the NO and COM pins can be used as either inputs or outputs. This switch is typically used when there is only one signal path that needs to be able to communicate to 3 different signal paths.

9.2 Typical Application



Figure 29. Typical Application Schematic

9.2.1 Design Requirements

The TS5A3359 device can be properly operated without any external components. However, TI recommends connecting unused pins to ground through a $50-\Omega$ resistor to prevent signal reflections back into the device. TI also recommends pulling up the digital control pins (IN1 and IN2) to VCC or pulling down to GND to avoid undesired switch positions that could result from the floating pin.

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A3359 input and output signal swing through NO and COM are dependent on the supply voltage V_{CC} . For example, if the desired signal level to pass through the switch is 5 V, V_{CC} must be greater than or equal to 5 V. $V_{CC} = 3.3$ V would not be valid for passing a 5-V signal since the Analog signal voltage cannot exceed the supply.

9.2.2 Detailed Design Procedure

The TS5A3359 device can be properly operated without any external components. However, TI recommends connecting unused pins to ground through a $50-\Omega$ resistor to prevent signal reflections back into the device. TI also recommends pulling up the digital control pins (IN1 and IN2) to VCC or pulling down to GND to avoid undesired switch positions that could result from the floating pin.

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Typical Application (continued)

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A3359 input/output signal swing through NO and COM are dependent of the supply voltage V_{CC} .

9.2.3 Application Curve





10 Power Supply Recommendations

TI recommends proper power-supply sequencing for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC on first, followed by NO or COM.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A $0.1-\mu$ F capacitor, connected from VCC to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

TI recommends following common printed-circuit board layout guidelines to ensure reliability of the device.

- Bypass capacitors should be used on power supplies.
- · Short trace lengths should be used to avoid excessive loading.

11.2 Layout Example







12 Device and Documentation Support

12.1 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E[™] Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



PACKAGING INFORMATION

Orderable Device	Status	Package Type	•	Pins	•	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
TS5A3359DCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SNBI	Level-1-260C-UNLIM	-40 to 85	(AL ~ JALR) JZ	Samples
TS5A3359DCURG4	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AL ~ JALR) JZ	Samples
TS5A3359DCUT	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU CU SNBI	Level-1-260C-UNLIM	-40 to 85	(AL ~ JALR) JZ	Samples
TS5A3359DCUTG4	ACTIVE	VSSOP	DCU	8	250	TBD	Call TI	Call TI	-40 to 85	(AL ~ JALR) JZ	Samples
TS5A3359YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(J9 ~ J97)	Samples
TS5A3359YZPRB	OBSOLETE	DSBGA	YZP	8		TBD	Call TI	Call TI		J97	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



PACKAGE OPTION ADDENDUM

25-Jan-2016

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3359DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A3359DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A3359YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

25-Jan-2016



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3359DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A3359DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A3359YZPR	DSBGA	YZP	8	3000	210.0	185.0	35.0

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

D. Falls within JEDEC MO-187 variation CA.





- NOTES: A. All linear dimensions are in millimeters. В. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- A. All linear dimensions are in millimeters. Dimension B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.



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