# WLED DRIVER FOR NOTEBOOK DISPLAY

**Check for Samples: TPS61181A**

## FEATURES

- **4.5 V to 24 V Input Voltage**
- **38V Maximum Output Voltage**
- **Integrated 1.5 A/40 V MOSFET**
- **1.0-MHz Switching Frequency**
- **Adaptive Boost Output to WLED Voltages**
- **Small External Components**
- **Integrated Loop Compensation**
- **Six Current Sinks of 30 mA**
- **Up to 10 WLED in Series**
- **1% Typical Current Matching and Accuracy**
- **Up to 1000:1 PWM Brightness Dimming**
- **Minimized Output Ripple Under PWM Dimming**
- **Driver for Input/Output Isolation PFET**
- **True Shutdown**
- **Over Voltage Protection**
- **WLED Open/Short Protection**
- **Built-in Soft Start**
- **16L 3 mm×3 mm QFN**

## APPLICATIONS

- **Notebook LCD Display Backlight**
- **UMPC LCD Display Backlight**
- **Backlight for Media Form Factor LCD display**

## DESCRIPTION

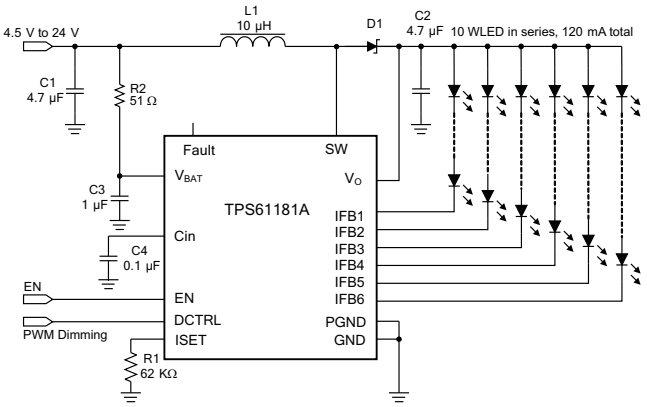
The TPS61181A IC provides highly integrated solutions for media size LCD backlighting. These devices have a built-in high efficiency boost regulator with integrated 1.5A/40V power MOSFET. The six current sink regulators provide high precision current regulation and matching. In total, the device can support up to 60 WLEDs. In addition, the boost output automatically adjusts its voltage to the WLED forward voltage to improve efficiency.

The devices support pulse width modulation (PWM) brightness dimming. During dimming, the WLED current is turned on/off at the duty cycle and frequency determined by the PWM signal input to the DCRTL pin. One potential issue of PWM dimming is audible noise from the output ceramic capacitors. The TPS61181A is designed to minimize this output AC ripple across a wide dimming duty cycle and frequency range and therefore, reduce this audible noise.

The TPS61181A provides a driver output for an external PFET connected between the input and inductor. During short circuit or over-current conditions, the IC turns off the external PFET and disconnects the battery from the WLEDs. The PFET is also turned off during IC shutdown (thereby giving "true" shutdown) to prevent any leakage current from the battery. The device also integrates over-voltage protection, soft-start and thermal shutdown.

The TPS61181A has a built-in linear regulator for the IC supply. The devices are in a 3×3 mm QFN package.

### TPS61181A TYPICAL APPLICATION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION(1)

| PACKAGE | PACKAGE MARKING |
|---|---|
| TPS61181ARTE | QWF |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

| | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Voltage Range (2) | $V_{BAT}$ and Fault | –0.3 | 24 | V |
| | $C_{in}$ and ISET | –0.3 | 3.6 | |
| | SW and $V_O$ | –0.3 | 40 | |
| | IFB1 to IFB6, EN and DCTRL | –0.3 | 20 | |
| ESD Rating(3) | Humen Body Mode – (HBM) | | 3 | kV |
| | Machine Mode – (MM) | | 200 | V |
| | Charge Device Mode – (CDM) | | 1 | kV |
| Continuous power dissipation | | See Thermal Information Table | | |
| Operating junction temperature range | | –40 | 150 | °C |
| Storage temperature range | | –65 | 150 | |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | TPS61181A | UNITS |
|---|---|---|---|
| | | QFN (16) PIN | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 43.1 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 38.3 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 14.6 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.4 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 14.4 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 3.6 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{bat}$ | Battery input voltage range | 4.5 | | 24 | V |
| $V_O$ | Output voltage range | Vin | | 38 | V |
| L | Inductor | 4.7 | | 10 | µH |
| $C_O$ | Output capacitor | 2.2 | | 10 | µF |
| $F_{PWM}$ | PWM dimming frequency at $D_{PWM}$ ≥ 1% | 0.1 | | 1 | kHz |
| | PWM dimming frequency at $D_{PWM}$ ≥ 5% | 1 | | 5 | |
| $T_A$ | Operating ambient temperature | –40 | | 85 | °C |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

## ELECTRICAL CHARACTERISTICS

$V_{BAT}$ = 10.8 V, 0.1 µF at Cin, EN = Logic High, IFB current = 20 mA, IFB voltage = 500 mV, $T_A$ = –40°C to 85°C, typical values are at $T_A$ = 25°C (unless otherwise noted)

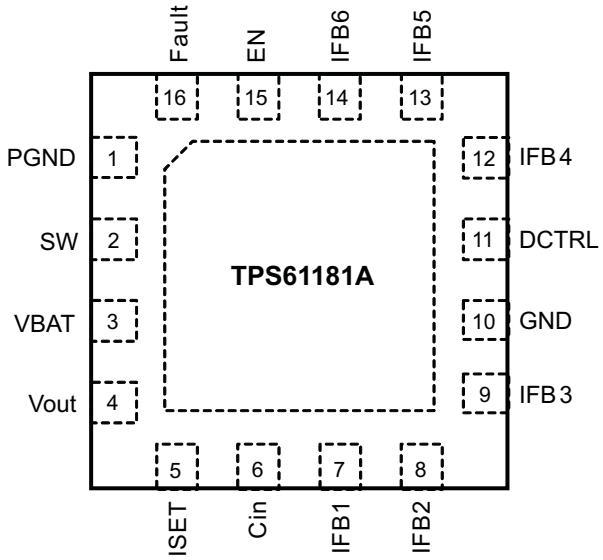
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $V_{BAT}$ | Battery input voltage range | | 4.5 | | 24 | V |
| $V_{cin}$ | Cin pin output voltage | | 2.7 | 3.15 | 3.6 | V |
| $I_{q\_bat}$ | Operating quiescent current into $V_{BAT}$ | Device enable, switching no load, Vin = 24 V | | | 3 | mA |
| $I_{Q\_sw}$ | Operating quiescent current into $V_O$ | $V_O$ = 35V | | | 60 | µA |
| $I_{SD}$ | Shutdown current | EN=GND | | 2 | 18 | µA |
| $V_{bat\_UVLO}$ | $V_{BAT}$ under-voltage lockout threshold | $V_{BAT}$ rising | | | 4.45 | V |
| | | $V_{BAT}$ falling | 3.9 | | | |
| $V_{bat\_hys}$ | $V_{BAT}$ under-voltage lockout hysteresis | $V_{BAT}$ rising – $V_{BAT}$ falling | | 220 | | mV |
| **EN AND DCTRL** | | | | | | |
| $V_H$ | EN pin logic high voltage | | 2.0 | | | V |
| $V_L$ | EN pin logic low voltage | | | | 0.8 | V |
| $V_H$ | DCTRL pin logic high voltage | | 2.0 | | | V |
| $V_L$ | DCTRL pin logic low voltage | | | | 0.8 | V |
| $R_{PD}$ | Pull down resistor on both pins | $V_{EN,\ DCTRL}$ = 2V | 400 | 800 | 1600 | kΩ |
| **CURRENT REGULATION** | | | | | | |
| $V_{ISET}$ | ISET pin voltage | | 1.204 | 1.229 | 1.253 | V |
| $K_{ISET}$ | Current multiple Iout/ISET | ISET current = 20 µA | 970 | 1000 | 1030 | |
| IFB | Current accuracy | ISET current = 20 µA | 19.4 | 20 | 20.6 | mA |
| $K_m$ | $(I_{max}–I_{min})/I_{AVG}$ | ISET current = 20 µA | | 1 | 2.5 | % |
| $I_{leak}$ | IFB pin leakage current | IFB voltage = 20 V on all pins | | | 3 | µA |
| $I_{IFB\_MAX}$ | Current sink max output current | IFB = 500 mV | 30 | | | mA |
| **BOOST OUTPUT REGULATION** | | | | | | |
| $V_{IFB\_L}$ | $V_O$ dial up threshold | ISET current = 20 µA | | 400 | | mV |
| $V_{IFB\_H}$ | $V_O$ dial down threshold | ISET current = 20 µA | | 700 | | mV |
| $V_{reg\_L}$ | Min Vout regulation voltage | | | | 16 | V |
| $V_{o\_step}$ | $V_O$ stepping voltage | | | 100 | 150 | mV |
| **POWER SWITCH** | | | | | | |
| $R_{PWM\_SW}$ | PWM FET on-resistance | | | 0.2 | 0.45 | Ω |
| $R_{start}$ | Start up charging resistance | $V_O$ = 0 V | 100 | | 300 | Ω |
| $V_{start\_r}$ | Isolation FET start up threshold | $V_{IN}–V_O$, $V_O$ ramp up | | 1.2 | 2 | V |
| $I_{LN\_NFET}$ | PWM FET leakage current | $V_{SW}$ = 35 V, $T_A$ = 25°C | | | 1 | µA |

## ELECTRICAL CHARACTERISTICS (continued)

$V_{BAT}$ = 10.8 V, 0.1 µF at Cin, EN = Logic High, IFB current = 20 mA, IFB voltage = 500 mV, $T_A$ = –40°C to 85°C, typical values are at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | | |
| $f_S$ | Oscillator frequency | | 0.9 | 1.0 | 1.2 | MHz |
| $D_{max}$ | Maximum duty cycle | IFB = 0 V | | 94 | | % |
| $D_{min}$ | Minimum duty cycle | | | | 7 | % |
| **OS, SC, OVP AND SS** | | | | | | |
| $I_{LIM}$ | N-Channel MOSFET current limit | D = $D_{max}$ | 1.5 | | 3 | A |
| $V_{ovp}$ | $V_O$ overvoltage threshold | Measured on the $V_O$ pin | 38 | 39 | 40 | V |
| $V_{ovp\_IFB}$ | IFB overvoltage threshold | Measured on the IFBx pin | 15 | 17 | 20 | V |
| $V_{sc}$ | Short circuit detection threshold | $V_{IN}$-$V_O$, $V_O$ ramp down | | 1.7 | 2.5 | V |
| $V_{sc\_dly}$ | Short circuit detection delay during start up | | | 32 | | ms |
| **Fault OUTPUT** | | | | | | |
| $V_{fault\_high}$ | Fault high voltage | Measured as $V_{BAT}$–$V_{Fault}$ | | 0.1 | | V |
| $V_{fault\_low}$ | Fault low voltage | Measured as $V_{BAT}$–$V_{Fault}$, sink 0.1mA, Vin = 15 V | 6 | 8 | 10 | V |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{shutdown}$ | Thermal shutdown threshold | | | 160 | | °C |
| $T_{hysteresis}$ | Thermal shutdown threshold hysteresis | | | 15 | | °C |

## PINOUT




### PIN ASSIGNMENTS

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | PGND | I | Power ground of the IC. Internally, it connects to the source of the PWM switch. |
| 2 | SW | I | This pin connects to the drain of the internal PWM switch, external Schottky diode and inductor. |
| 3 | $V_{BAT}$ | I | This pin is connected to the battery supply. It provides the pull-up voltage for the Fault pin and battery voltage signal. This is also the input to the internal LDO. |
| 4 | $V_O$ | O | This pin monitors the output of the boost regulator. Connect this pin to the anode of the WLED strings. |
| 5 | ISET | I | The resistor on this pin programs the WLED output current. |
| 6 | Cin | I | Supply voltage of the IC. It is the output of the internal LDO. Connect 0.1 µF bypass capacitor to this pin. |
| 7, 8, 9<br>12, 13, 14 | IFB1-IFB3<br>IFB4-IFB6 | I | Current sink regulation inputs. They are connected to the cathode of WLEDs. The PWM loop regulates the lowest $V_{IFB}$ to 400 mV. Each channel is limited to 30 mA current. |
| 10 | GND | I | Signal ground of the IC. |
| 11 | DCTRL | I | Dimming control logic input. The dimming frequency range is 100 Hz to 1 kHz. |
| 15 | EN | I | The enable pin to the IC. A logic high signal turns on the internal LDO and enables the IC. Therefore, do not connect the EN pin to the Cin pin. |
| 16 | Fault | I | Gate driver output for an external PFET used for fault protection. It can also be used as signal output for system fault report. |

## TYPICAL CHARACTERISTICS

### Table of Graphs

| Description (Reference to application circuit in Figure 15) | | Figure |
|---|---|---|
| DC Load Efficiency | $V_{bat}$= 5V, 10.8V, 19V; $V_O$=28.6V, 9LEDs; L=10uH | Figure 1 |
| DC Load Efficiency | $V_{bat}$= 5V, 10.8V, 19V; $V_O$=31.7V, 10LEDs; L=10uH | Figure 2 |
| PWM Dimming Efficiency | $V_{bat}$= 5V, 10.8V and 19V; $V_O$=25.5V, 8LEDs; PWM Freq = 1kHz | Figure 3 |
| PWM Dimming Efficiency | $V_{bat}$= 5V, 10.8V and 19V; $V_O$=28.6V, 9LEDs; PWM Freq = 1kHz | Figure 4 |
| PWM Dimming Efficiency | $V_{bat}$= 5V, 10.8V and 19V; $V_O$=31.7V, 10LEDs; PWM Freq = 1kHz | Figure 5 |
| PWM Dimming Efficiency | $V_{bat}$= 5V, 10.8V and 19V; $V_O$=34.8V, 11LEDs; PWM Freq = 1kHz | Figure 6 |
| Dimming Linearity | $V_{bat}$= 10.8V; $V_O$=28.6V, 9LEDs; $I_{set}$= 20µA; PWM Freq = 1kHz | Figure 7 |
| Dimming Linearity | $V_{bat}$= 10.8V; $V_O$=28.6V, 9LEDs; $I_{set}$= 20µA; PWM Freq = 200Hz | Figure 8 |
| Output Ripple | $V_O$=28.6V; $I_{set}$= 20µA; PWM Freq = 200Hz; Duty = 50% | Figure 9 |
| Switching Waveform | $V_{bat}$= 10.8V; $I_{set}$= 20µA | Figure 10 |
| Output Ripple at PWM Dimming | $V_{bat}$= 10.8V; $I_{set}$= 20µA; PWM Freq = 200Hz; Duty = 50%; $C_O$=4.7µF | Figure 11 |
| Short Circuit Protection | $V_{bat}$= 10.8V; $I_{set}$= 20µA | Figure 12 |
| Open WLED Protection | $V_{bat}$= 10.8V; $I_{set}$= 20µA | Figure 13 |
| Startup Waveform | $V_{bat}$= 10.8V; $I_{set}$= 20µA | Figure 14 |

**EFFICIENCY vs OUTPUT CURRENT**

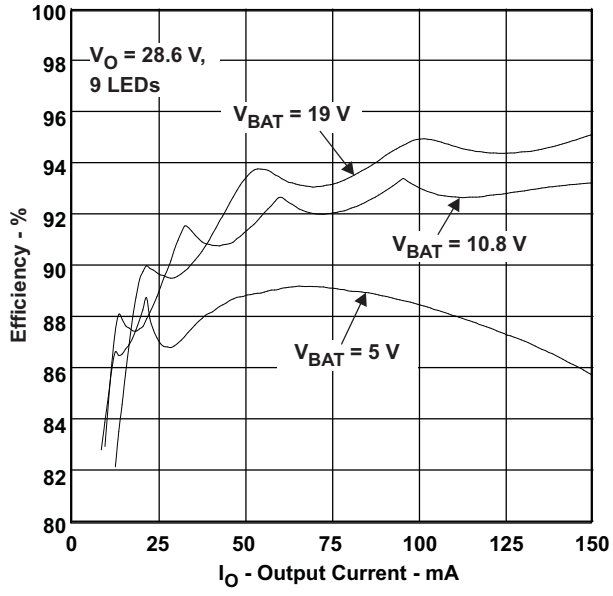



**Figure 1.**

**EFFICIENCY vs OUTPUT CURRENT**

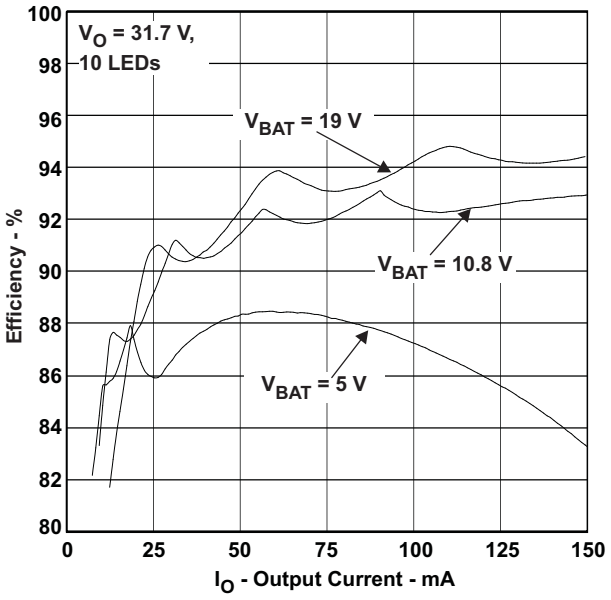



**Figure 2.**

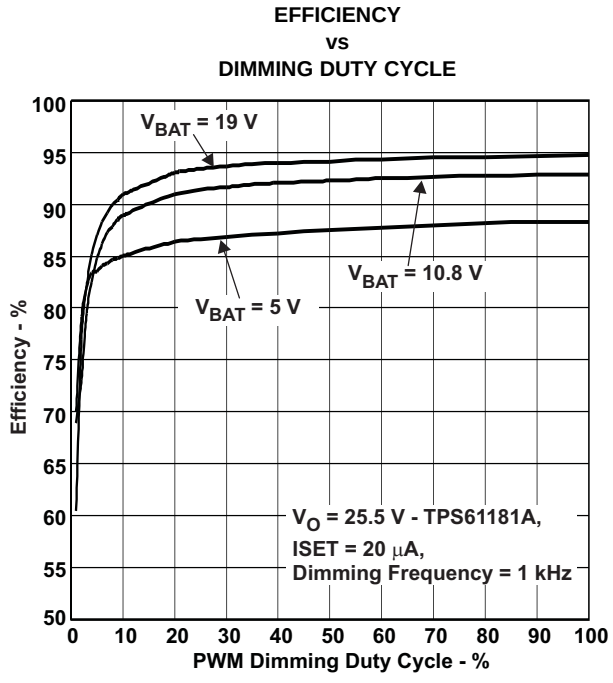



Figure 3.

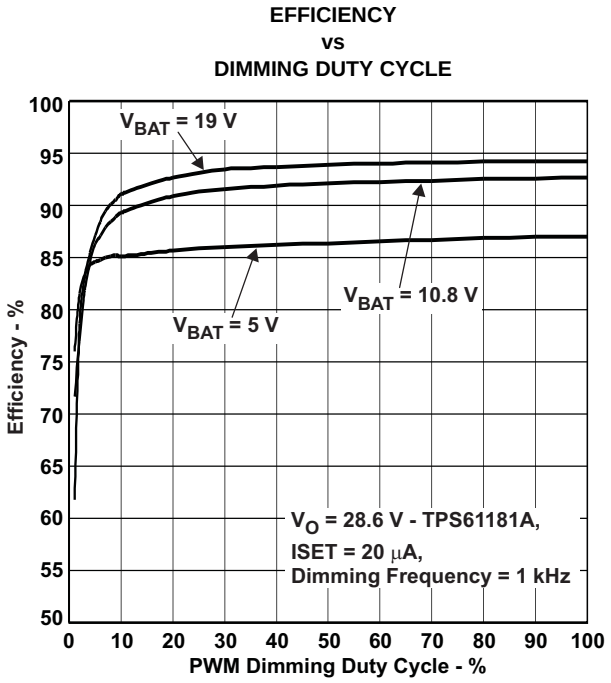



Figure 4.

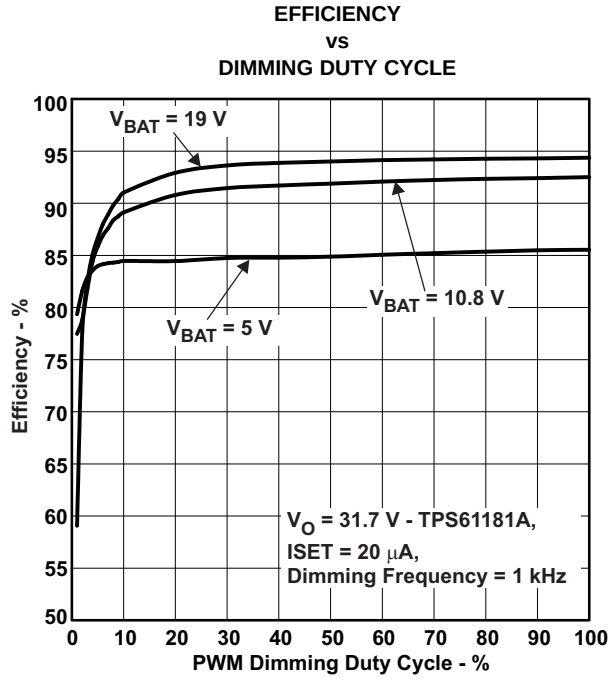



Figure 5.

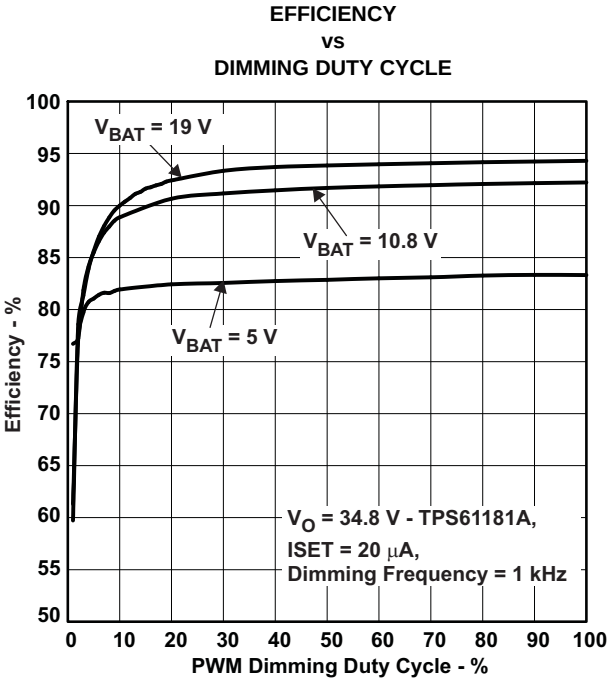



Figure 6.

PWM DIMMING linearity 1kHz

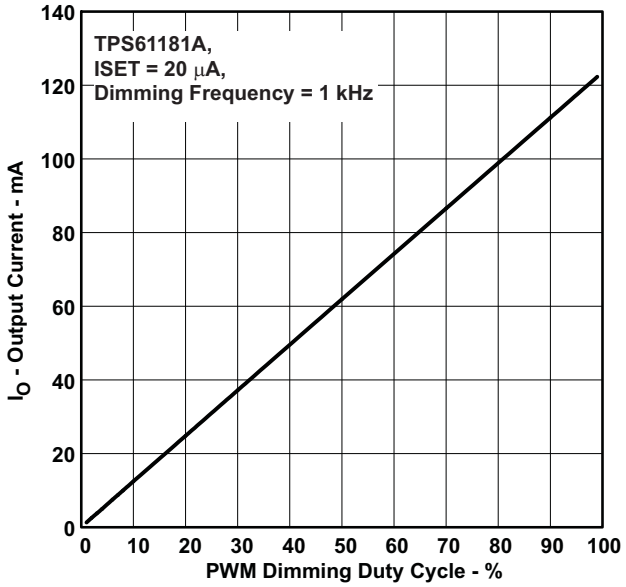



Figure 7.

PWM DIMMING LINEARITY 200Hz

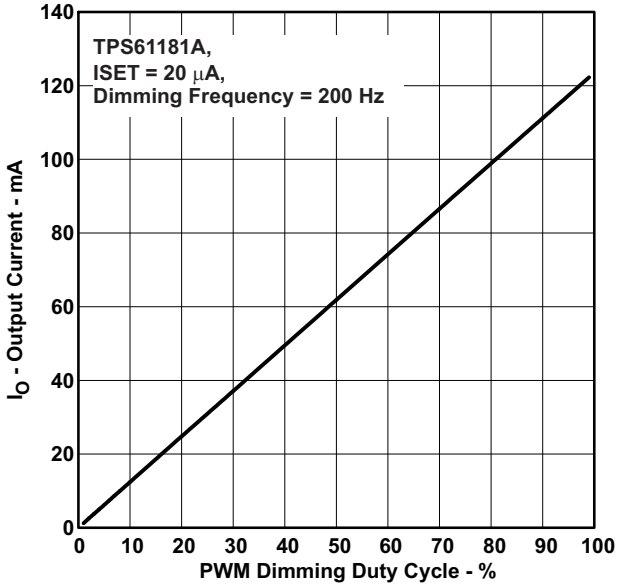



Figure 8.

PWM DIMMING OUTPUT RIPPLE $C_O$=4.7µF
vs
INPUT VOLTAGE

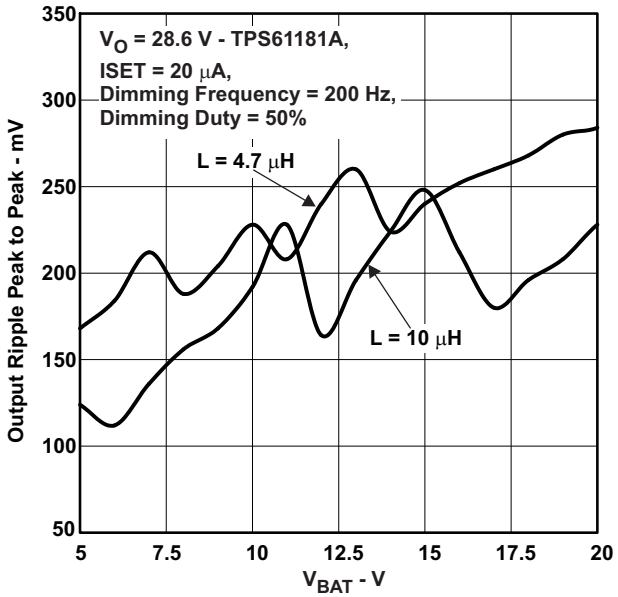



Figure 9.

SWITCHING WAVEFORM

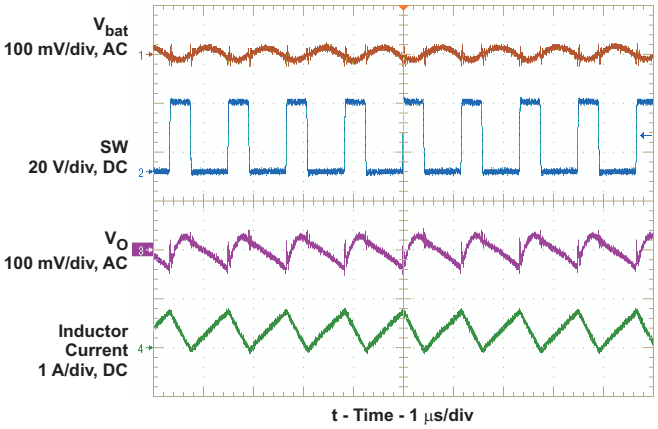



Figure 10.

OUTPUT RIPPLE AT PWM DIMMING $C_O$=4.7µF

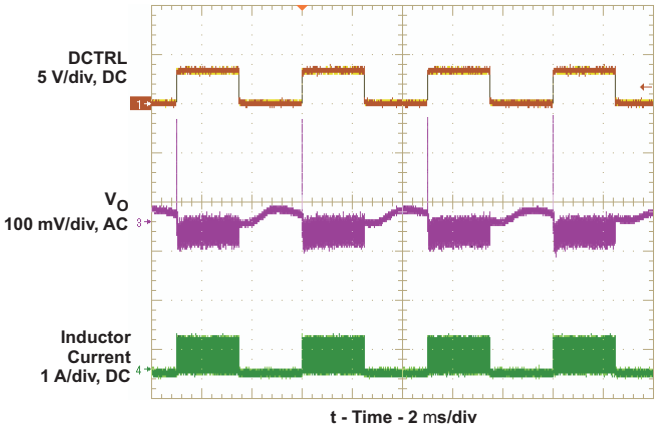



Figure 11.

OUTPUT SHORT PROTECTION

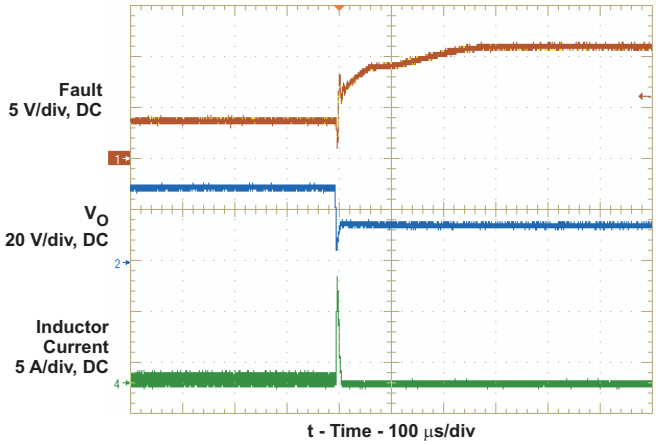



Figure 12.

OPEN WLED PROTECTION

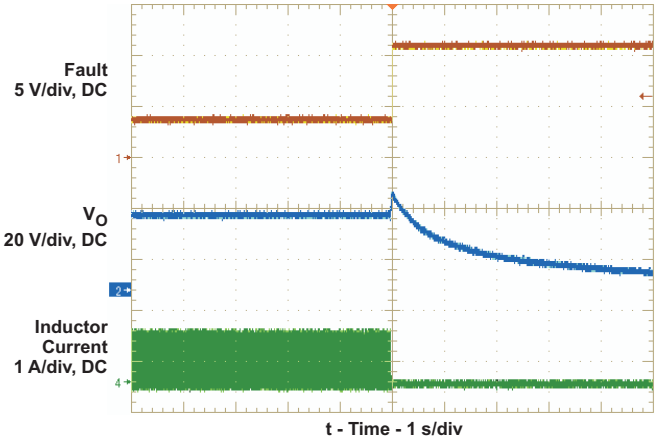



Figure 13.

STARTUP WAVEFORM

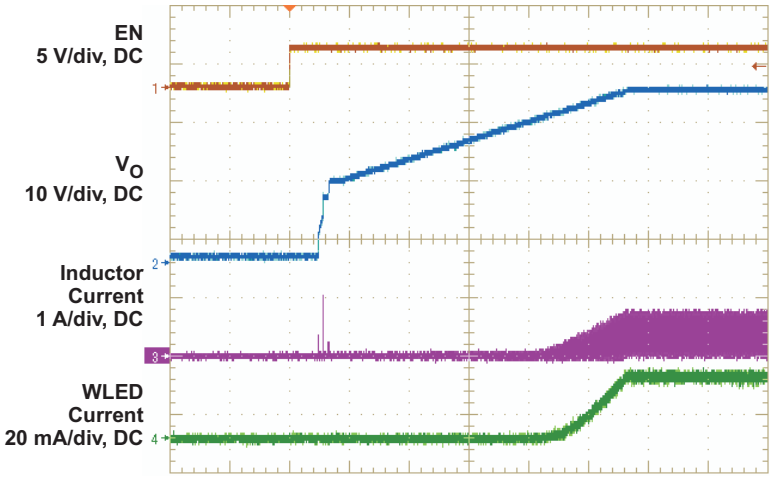
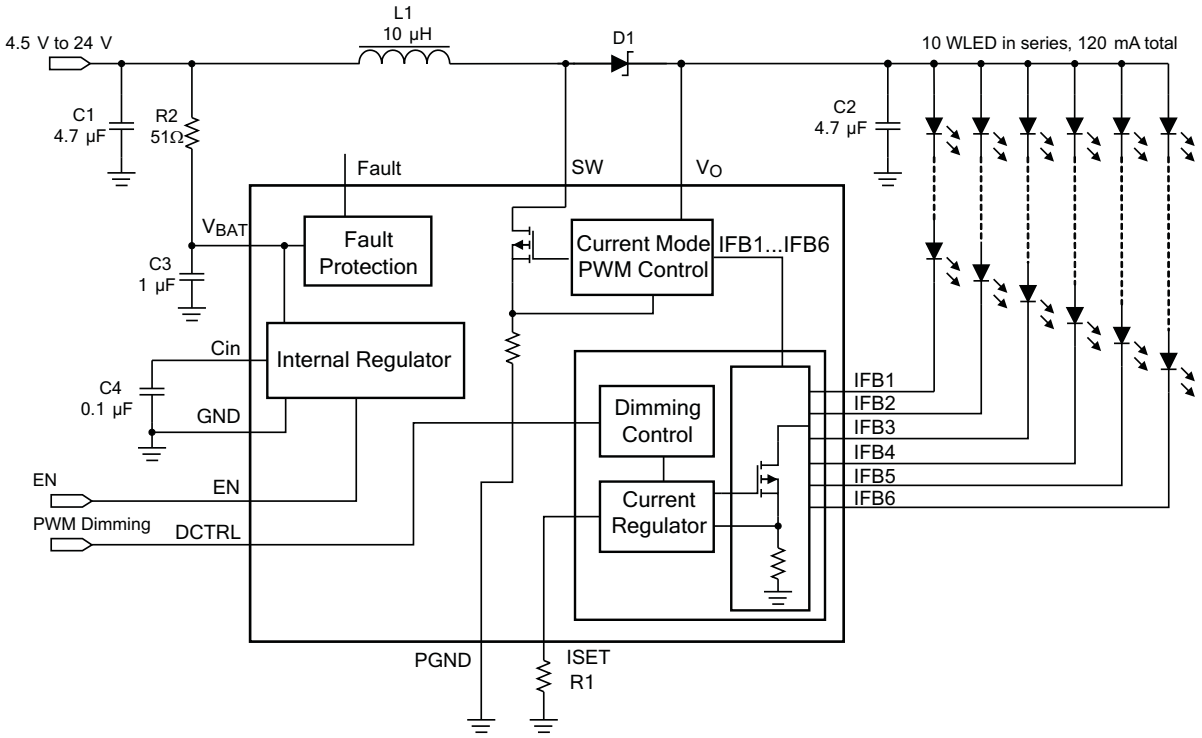



Figure 14.

## FUNCTIONAL BLOCK DIAGRAM



## DETAILED DESCRIPTION

Recently, WLEDs have gained popularity as an alternative to CCFL for backlighting media size LCD displays. The advantages of WLEDs are power efficiency and low profile design. Due to the large number of WLEDs, they are often arranged in series and parallel, and powered by a boost regulator with multiple current sink regulators. Having more WLEDs in series reduces the number of parallel strings and therefore improves overall current matching. However, the efficiency of the boost regulator declines due to the need for high output voltage. Also, there have to be enough WLEDs in series to ensure the output voltage stays above the input voltage range. Otherwise, a buck-boost (for example, SEPIC) power converter has to be adopted which could be more expensive and complicated.

The TPS61181A IC has integrated all the key function blocks to power and control up to 60 WLEDs. The devices include a 40V/1.5A boost regulator, six 30mA current sink regulators and protection circuit for over-current, over-voltage and short circuit failures. The key advantages of the devices are small solution size, low output AC ripple during PWM dimming control, and the capability to isolate the input and output during fault conditions.

### SUPPLY VOLTAGE

The TPS61181A has built-in LDO linear regulator to supply the IC analog and logic circuits. The LDO is powered up when the EN pin is high. The output of the LDO is connected to the Cin pin. A 0.1µF bypass capacitor is required for LDO's stable operation. Do not connect the Cin pin to the EN pin because this prevents the IC from starting up. In addition, avoid connecting the Cin pin to any other circuit as this could introduce noise into the IC supply voltage.

The $V_{BAT}$ connects to the input of the internal LDO, and powers the IC. The voltage on the $V_{BAT}$ pin is also the reference for the pull-up circuit of the Fault pin. In addition, it serves as the input signal to the short circuit protection. There is an under-voltage lockout on the $V_{BAT}$ pin which disables the IC when its voltage reduces to 4.2V (Typical). The IC restarts when the $V_{BAT}$ pin voltage recovers by 220mV.

### BOOST REGULATOR

The boost regulator is controlled by current mode PWM, and loop compensation is integrated inside the IC. The internal compensation ensures stable output over the full input and output voltage range. The TPS61181A switches at 1.0MHz which optimize boost converter efficiency and voltage ripple with a small form factor inductor and output capacitor.

The output voltage of the boost regulator is automatically set by the IC to minimize the voltage drop across the IFB pins. The IC automatically regulates the lowest IFB pin to 400mV, and consistently adjusts the boost output voltage to account for any changes of the LED forward voltages.

When the output voltage is too close to the input, the boost regulator may not be able to regulate the output due to the limitation of minimum duty cycle. In this case, increase the number of WLED in series or include series ballast resistors in order to provide enough headroom for the boost operation.

The TPS61181A boost regulator cannot regulate its output to voltages below 15V.

## CURRENT PROGRAM AND PWM DIMMING

The six current sink regulators can each provide a maximum of 30mA. The IFB current must be programmed to maximum WLED current using the ISET pin resistor and the following Equation 1.

$$I_{FB} = K_{ISET} \frac{V_{ISET}}{R_{ISET}} \quad (1)$$

Where

$K_{ISET}$ = Current multiple (1000 typical)

$V_{ISET}$ = ISET pin voltage (1.229 V typical)

$R_{ISET}$ = ISET pin resistor

The TPS61181A has six built-in precise current sink regulators. The current matching among the current sinks at 20mA current through is below 2.5%. This means the differential value between the maximum and minimum current of the six current sinks divided by the average current of the six is less than 2.5%.

The WLED brightness is controlled by the PWM signal on the DCTRL pin. The frequency and duty cycle of the DCTRL signal is replicated on the IFB pin current. Keep the dimming frequency in the range of 100Hz to 1kHz to avoid screen flickering and maintain dimming linearity. Screen flickering may occur if the dimming frequency is below the range. The minimum achievable duty cycle increases with the dimming frequency. For example, while a 0.1% dimming duty cycle, giving a 1000:1 dimming range, is achievable at 100 Hz dimming frequency, only 1% duty cycle, giving a 100:1 dimming range, is achievable with a 1 KHz dimming frequency, and 5% dimming duty cycle is achievable with 5KHz dimming frequency. The device could work at high dimming frequency like 20 KHz, but then only 15% duty cycle could be achievable. The TPS61181A is designed to minimize the AC ripple on the output capacitor during PWM dimming. Careful passive component selection is also critical to minimize AC ripple on the output capacitor. See APPLICATION INFORMATION for more information.

## ENABLE AND START UP

A logic high signal on the EN pin turns on the IC. For the TPS61181A, taking EN high turns on the internal LDO linear regulator which provides supply to the IC current. Then, an internal resistor, $R_{start}$ (start up charging resistor) is connected between the $V_{BAT}$ pin and $V_O$ pin to charge the output capacitor toward the $V_{BAT}$ pin voltage. The Fault pin outputs high during this time, and thus the external isolation PFET is turned off. Once the $V_O$ pin voltage is within 2 V (isolation FET start up threshold) of the $V_{BAT}$ pin voltage, $R_{start}$ is open, and the Fault pin pulls down the gate of the PFET and connects the $V_{BAT}$ voltage to the boost regulator. This operation is to prevent the in-rush current due to charging the output capacitor.

Once the isolation FET is turned on, the IC starts PWM switching to raise the output voltage above $V_{BAT}$. Soft-start is implemented by gradually ramping up the reference voltage of the error amplifier to prevent voltage over-shoot and in-rush current. See the start-up waveform of a typical example, Figure 14.

Pulling the EN pin low immediately shuts down the IC, resulting in the IC consuming less than 50µA in the shutdown mode.

## OVER-CURRENT, OVER-VOLTAGE AND SHORT-CIRCUIT PROTECTION

The TPS61181A has pulse-by-pulse over-current limit of 1.5A (min). The PWM switch turns off when the inductor current reaches this current threshold. The PWM switch remains off until the beginning of the next switching cycle. This protects the IC and external components under over-load conditions. When there is sustained over-current condition for more than 16ms ( under 100% dimming duty cycle), the IC turns off and requires POR or the EN pin toggling to restart.

Under severe over-load and/or short circuit conditions, the $V_O$ pin can be pulled below the input ($V_{BAT}$ pin). Under this condition, the current can flow directly from $V_{BAT}$ to the WLED through the inductor and schottky diode. Turning off the PWM switch alone does not limit current anymore. In this case, the TPS61181A detects the output voltage is 1.7V ($V_{sc}$,short circuit detection threshold) below the input voltage, turns off the isolation FET, and shuts down the IC. The IC restarts after input power-on reset ($V_{BAT}$ POR) or EN pin logic toggling.

During IC start up, if there is short circuit condition on the boost converter output, the output capacitor will not be charged to within 2V of $V_{BAT}$ through $R_{start}$. After 32ms ($V_{sc_dly}$short circuit detection delay during start up), the TPS61181A shuts down and does not restart until there is $V_{BAT}$ POR or EN pin toggling. The isolation FET is never turned on under the condition.

If one of the WLED strings is open, the boost output rises to over-voltage threshold (39V typical). The TPS61181A detects the open WLED string by sensing no current in the corresponding IFB pin. As a result, the IC removes the open IFB pin from the voltage feedback loop. Subsequently, the output voltage drops down and is regulated to a voltage for the connected WLED strings. The IFB current of the connected WLED strings keep in regulation during the whole transition. The IC only shuts down if it detects that all of the WLED strings are open.

If the over-voltage threshold is reached, but the current sensed on the IFB pin is below the regulation target, the IC regulates the boost output at the over-voltage threshold. This operation could occur when the WLED is turned on under cold temperature, and the forward voltages of the WLEDs exceed the over-voltage threshold. Maintaining the WLED current allows the WLED to warm up and their forward voltages to drop below the over-voltage threshold.

If any IFB pin voltage exceeds IFB over-voltage threshold (17V typical), the IC turns off the corresponding current sink and removes this IFB pin from $V_O$ regulation loop. The remaining IFB pins' current regulation is not affected. This condition often occurs when there are several shorted WLEDs in one string. WLED mismatch typically does not create such large voltage difference among WLED strings.

## IFB PIN UNUSED

If the application requires less than 6 WLED strings, one can easily disable unused IFB pins. The TPS61181A simply requires leaving the unused IFB pin open or shorting it to ground. If the IFB pin is open, the boost output voltage ramps up to $V_O$ over-voltage threshold during start up. The IC then detects the zero current string, and removes it from the feedback loop. If the IFB pin is shorted to ground, the IC detects the short immediately after IC enable, and the boost output voltage does not go up to $V_O$ over-voltage threshold. Instead, it ramps to the regulation voltage after soft start.

# APPLICATION INFORMATION

## INDUCTOR SELECTION

Because the selection of the inductor affects a power supply's steady state operation, transient behavior and loop stability, the inductor is the most important component in switching power regulator design. There are three specifications most important to the performance of the inductor: inductor value, DC resistance and saturation current. The TPS61181A ICs are designed to work with inductor values between 4.7µH and 10µH. A 4.7µH inductor may be available in a smaller or lower profile package, while 10µH may produce higher efficiency due to lower inductor ripple. If the boost output current is limited by the over-current protection of the IC, using a 10µH inductor can offer higher output current.

The internal loop compensation for the PWM control is optimized for the recommended component values, including typical tolerances. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20 to 35% from the zero current value depending on how the inductor vendor defines saturation

In a boost regulator, the inductor DC current can be calculated as

$$I_{dc} = \frac{V_O \times I_O}{V_{in} \times \eta} \quad (2)$$

Where

$V_O$ = boost output voltage

Io = boost output current

$V_{in}$ = boost input voltage

η = power conversion efficiency, use 90% for TPS61181A applications

The inductor current peak to peak ripple can be calculated as

$$I_{pp} = \frac{1}{L \times \left( \frac{1}{V_O - V_{bat}} + \frac{1}{V_{bat}} \right) \times F_S} \quad (3)$$

Where

$I_{pp}$ = inductor peak to peak ripple

L = inductor value

$F_s$= Switching frequency

$V_{bat}$= boost input voltage

Therefore, the peak current seen by the inductor is

$$I_p = I_{dc} + \frac{I_{pp}}{2} \quad (4)$$

Select the inductor with saturation current at least 25% higher than the calculated peak current. To calculate the worse case inductor peak current, use minimum input voltage, maximum output voltage and maximum load current.

Regulator efficiency is dependent on the resistance of its high current path, switching losses associated with the PWM switch and power diode. Although the TPS61181A ICs have optimized the internal switch resistance, the overall efficiency still relies on the DC resistance (DCR) of the inductor; lower DCR improves efficiency. However, there is a trade off between DCR and inductor footprint. Furthermore, shielded inductors typically have a higher DCR than unshielded ones. Table 1 lists recommended inductor models.

**Table 1. Recommended Inductor for TPS61181A**

| | L (µH) | DCR Typ (mΩ) | $I_{sat}$ (A) | Size (LXWXH mm) |
|---|---|---|---|---|
| **TOKO** | | | | |
| A915AY-4R7M | 4.7 | 38 | 1.87 | 5.2x5.2x3.0 |
| A915AY-100M | 10 | 75 | 1.24 | 5.2x5.2x3.0 |
| **TDK** | | | | |
| SLF6028T-4R7M1R6 | 4.7 | 28.4 | 1.6 | 6.0x6.0x2.8 |
| SLF6028T-100M1R3 | 10 | 53.2 | 1.3 | 6.0x6.0x2.8 |

## OUTPUT CAPACITOR SELECTION

During PWM brightness dimming, the load transient causes voltage ripple on the output capacitor. Since the PWM dimming frequency is in the audible frequency range, the ripple can produce audible noises on the output ceramic capacitor. There are two ways to reduce or eliminate this audible noise. The first option is to select PWM dimming frequency outside the audible range. This means the dimming frequency needs be to lower than 200Hz or higher than 30KHz. The potential issue with a very low dimming frequency is that WLED on/off can become visible and thus cause a flickering effect on the display. On the other hand, high dimming frequency can compromise the dimming range since the LED current accuracy and current match are difficult to maintain at low dimming duty cycle. The second option is to reduce the amount of the output ripple, and therefore minimize the audible noise.

The TPS61181A adopts a patented technology to limit output ripple even with small output capacitance. In a typical application, the output ripple is less than 200mV during PWM dimming with a 4.7µF output capacitor, and the audible noise is not noticeable. The devices are designed to be stable with output capacitor down to 1.0µF. However, the output ripple will increase with lower output capacitor.

Care must be taken when evaluating a ceramic capacitor's derating due to applied dc voltage, aging and over frequency. For example, larger form factor capacitors (in 1206 size) have their self resonant frequencies in the switching frequency range of the TPS61181A. So the effective capacitance is significantly lower. Therefore, it may be necessary to use small capacitors in parallel instead of one large capacitor.

## AUDIBLE NOISE REDUCTION

Ceramic capacitors can produce audible noise if the frequency of its AC voltage ripple is in the audible frequency range. In TPS61181A applications, both input and output capacitors are subject to AC voltage ripple during PWM brightness dimming. The ICs integrate a patented technology to minimize the ripple voltage, and thus audible noises.

To further reduce the audible noise, one effective way is to use two or three small size capacitors in parallel instead of one large capacitor. The application circuit in Figure 15 uses two 2.2-µF/25V ceramic capacitors at the input and two 1-µF/50V ceramic capacitors at the output. All of the capacitors are in 0805 package. Although the output ripple during PWM dimming is higher than with one 4.7µF in a 1206 package, the overall audible noise is lower.

In addition, connecting a 10-nF/50V ceramic capacitor between the $V_O$ pin and IFB1 pin can further reduce the output AC ripple during the PWM dimming. Since this capacitor is subject to large AC ripple, choose a small package such as 0402 to prevent it from producing noise.

## ISOLATION MOSFET SELECTION

The TPS61181A provides a gate driver to an external P-channel MOSFET which can be turned off during device shutdown or fault condition. This MOSFET can provide a true shutdown function, and also protect the battery from output short circuit conditions. The source of the PMOS should be connected to the input, and a pull up resistor is required between the source and gate of the FET to keep the FET off during IC shutdown. To turn on the isolation FET, the Fault pin is pulled low, and clamped at 8 V below the $V_{BAT}$ pin voltage.

During device shutdown or fault condition, the isolation FET is turned off, and the input voltage is applied on the

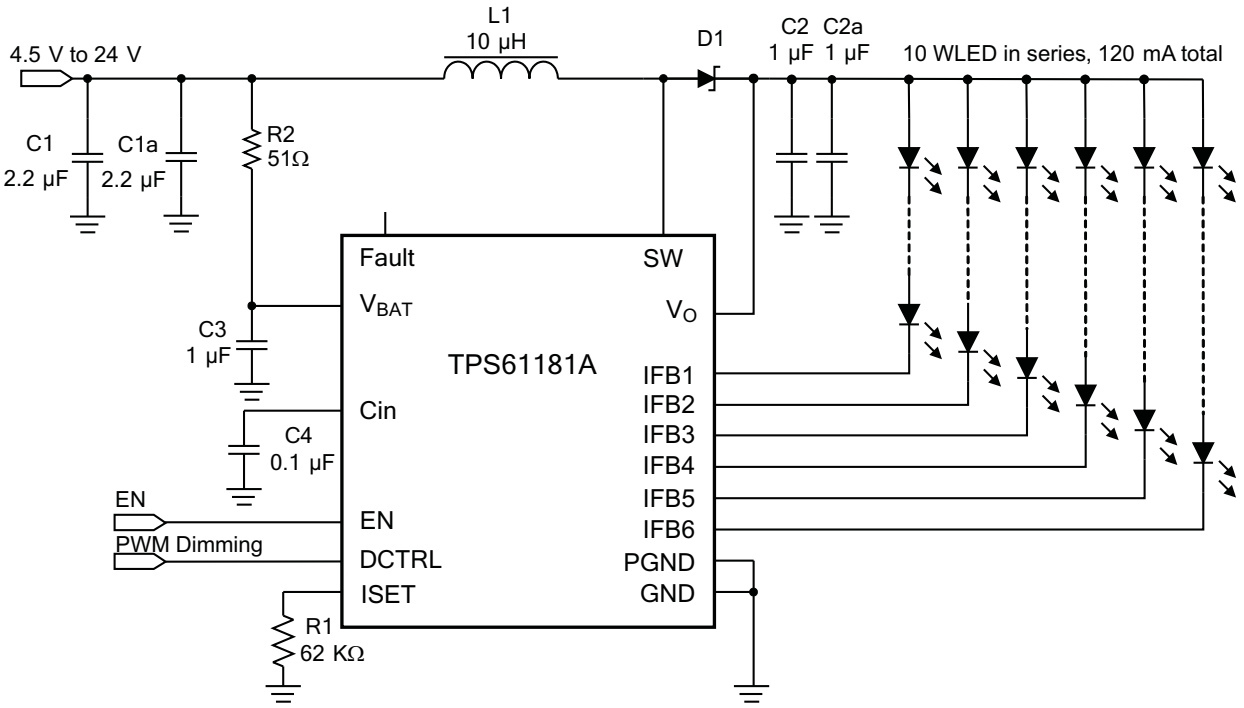
isolation MOSFET. During a short circuit condition, the catch diode (D2 in typical application circuit) is forward biased when the isolation FET is turned off. The drain of the isolation FET swings below ground. The voltage across the isolation FET can be momentarily greater than the input voltage. Therefore, select a 30V MOSFET for a 24V maximum input. The on resistance of the FET has a large impact on power conversion efficiency since the FET carries the input voltage. Select a MOSFET with $R_{ds(on)}$ less than 100mΩ to limit the power losses.

## LAYOUT CONSIDERATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor, C3 in the typical application circuit, needs not only to be close to the $V_{BAT}$ pin, but also to the GND pin in order to reduce the input ripple seen by the IC. The input capacitor, C1 in the typical application circuit, should be placed close to the inductor. The SW pin carries high current with fast rising and falling edges. Therefore, the connection between the pin to the inductor and Schottky should be kept as short and wide as possible. It is also beneficial to have the ground of the output capacitor C2 close to the PGND pin since there is large ground return current flowing between them. When laying out signal ground, it is recommended to use short traces separated from power ground traces, and connect them together at a single point, for example on the thermal pad.

Thermal pad needs to be soldered on to the PCB and connected to the GND pin of the IC. Additional thermal via can significantly improve power dissipation of the IC.

## ADDITIONAL APPLICATION CIRCUITS




C1, C1a: Murata GRM 219R61E225K
C2, C2a: Murata GRM 21BR71H105K
C3: Murata GRM 21BR71H105K
C4: Murata GRM 185R61A105K

L1: TOKO A 915AY-100 M
D1: VISHAY SS 2P5-E3/84A

**Figure 15. Audible Noise Reduction Circuit**

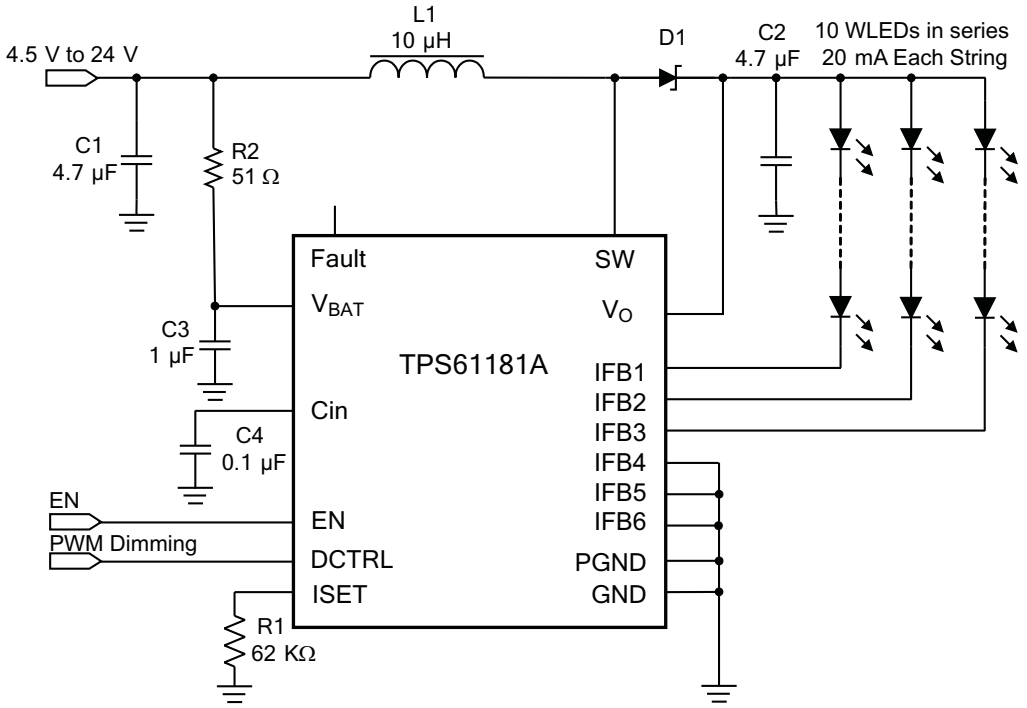



**Figure 16. TPS61181A for Three Strings of LEDs**

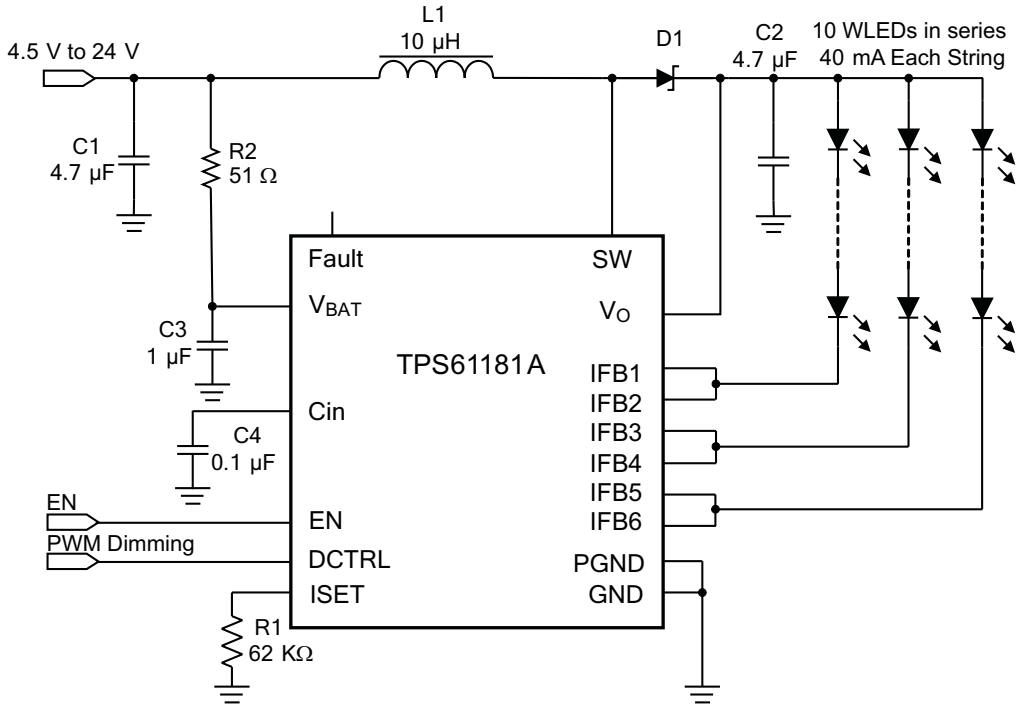



**Figure 17. TSP61181A for Three Strings of LEDs with Double Current**

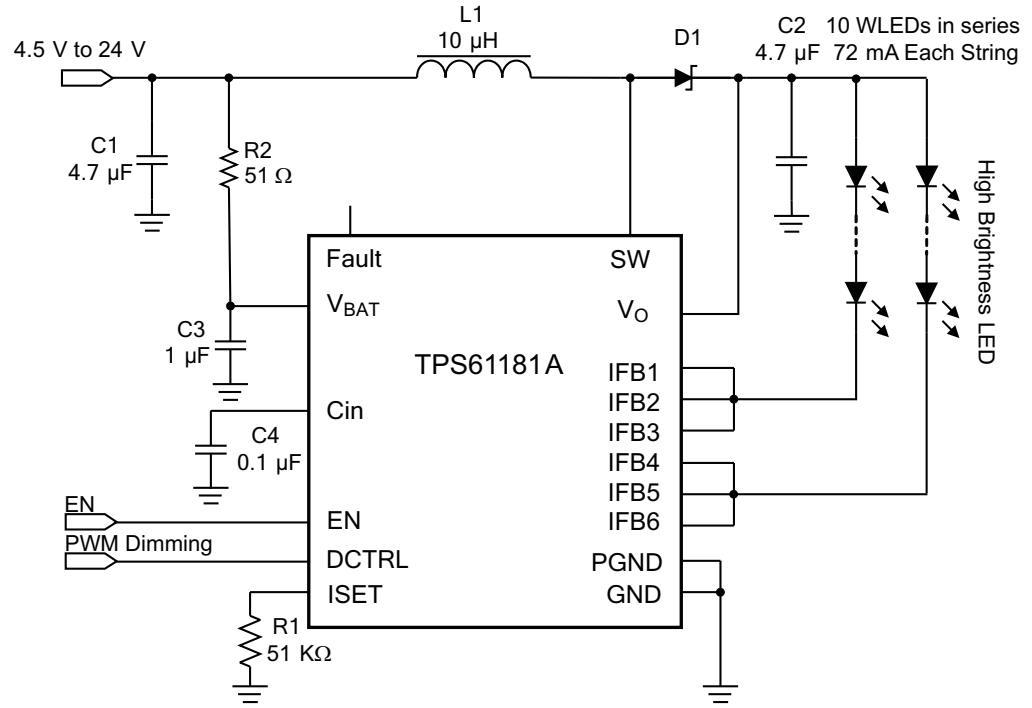



**Figure 18. TSP61181A for Two Strings High Brightness LEDs Application**

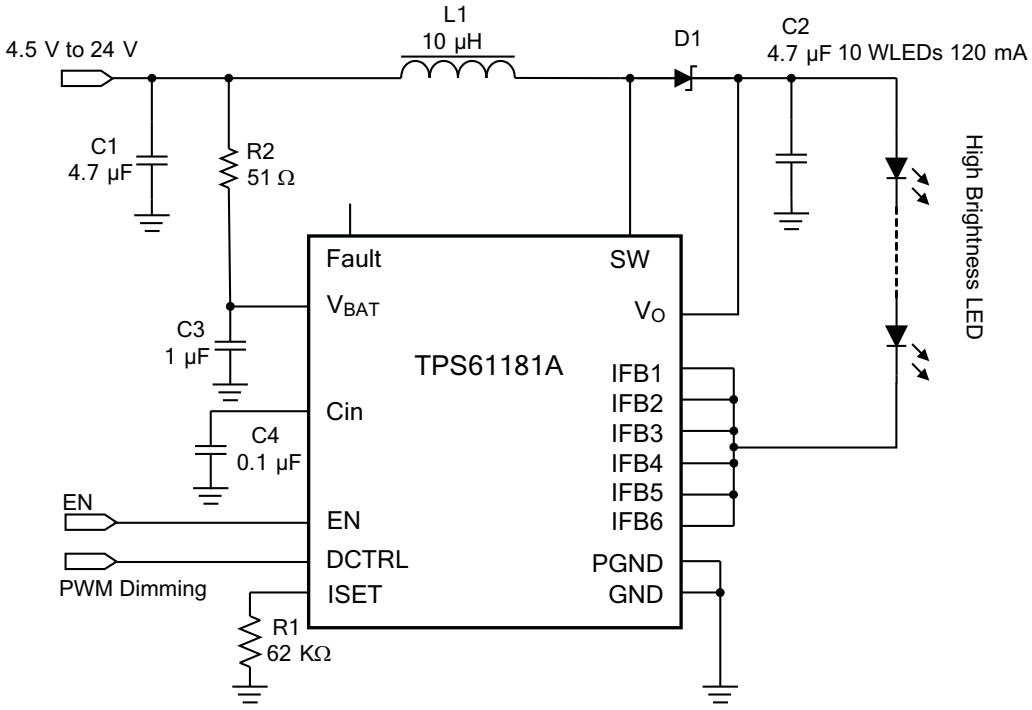



**Figure 19. TSP61181A for One String High Brightness LEDs Application**

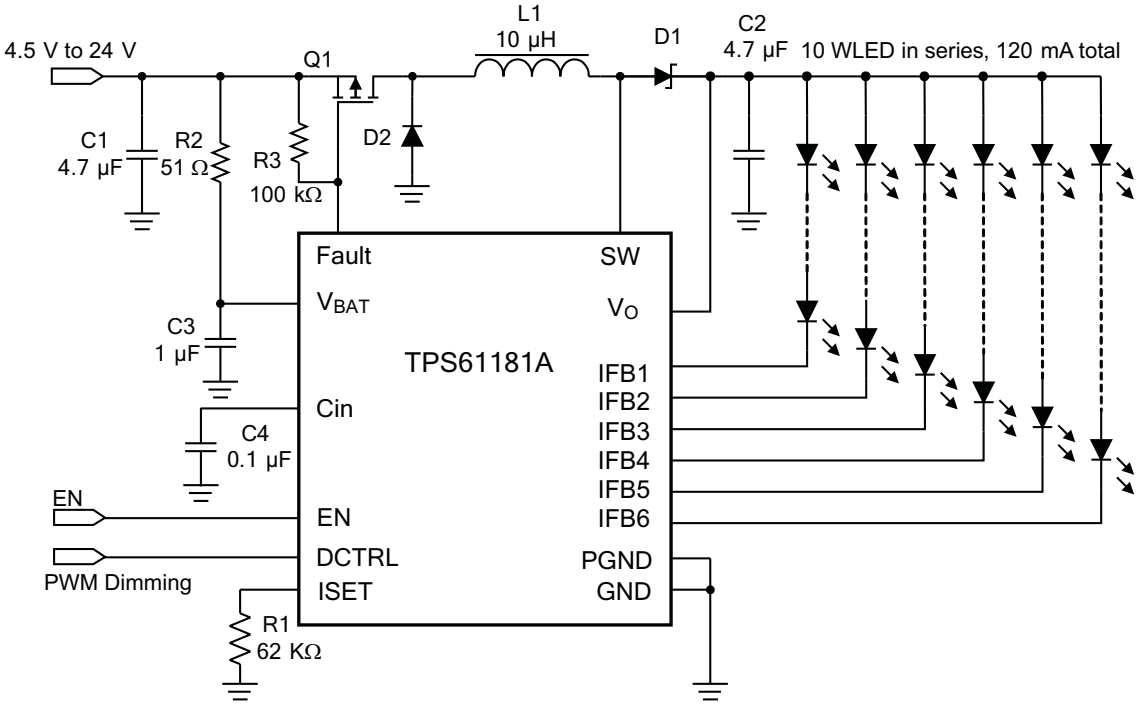



**Figure 20. TPS61181A Driving External PFET for True Shutdown Application**

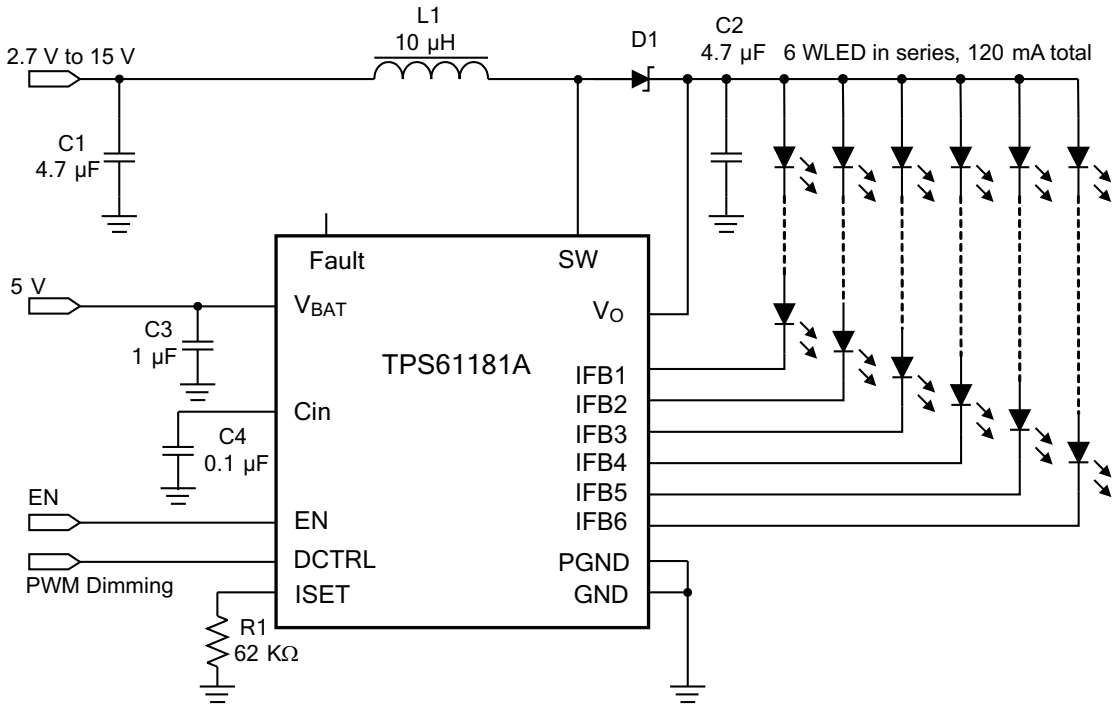



**Figure 21. TPS61181A with Separate $V_{BAT}$ Power for Low Voltage Input Application**

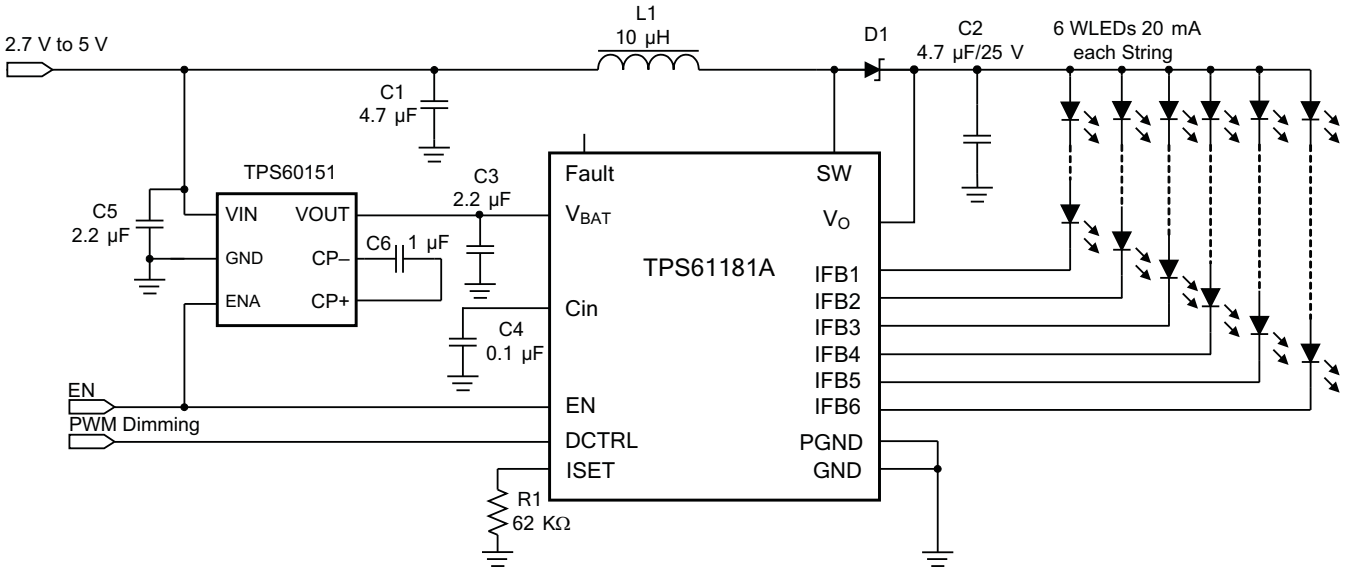



**Figure 22. TPS61181A+TPS60151 for One Cell Li-ion Battery Power Application**

## REVISION HISTORY

Note: Page numbers of current version may differ from previous version.

| Changes from Original (February) to Revision A | Page |
|---|---|
| • Deleted Voltage Range spec for "all other pins" in the Absolute Maximum Ratings table. | 2 |
| • Added $F_{PWM}$ spec. for PWM dimming frequency at $D_{PWM} \geq 1\%$ and $D_{PWM} \geq 5\%$ | 2 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| TPS61181ARTER | ACTIVE | WQFN | RTE | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TPS61181ARTET | ACTIVE | WQFN | RTE | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |

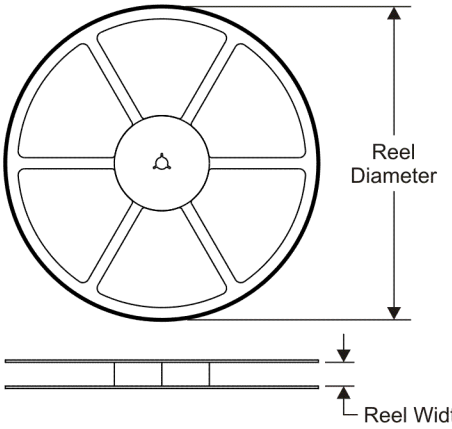
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

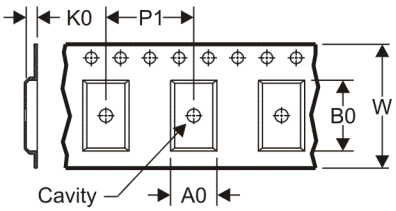
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

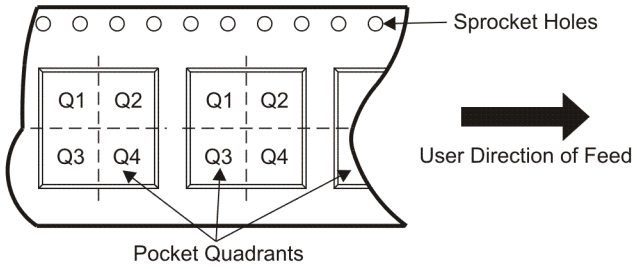



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

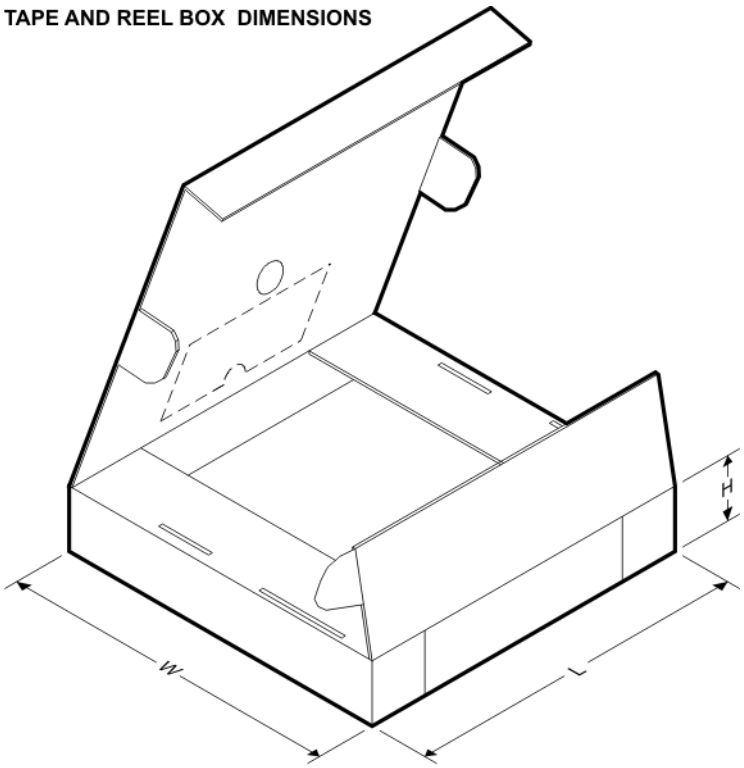
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS61181ARTER | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS61181ARTET | WQFN | RTE | 16 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

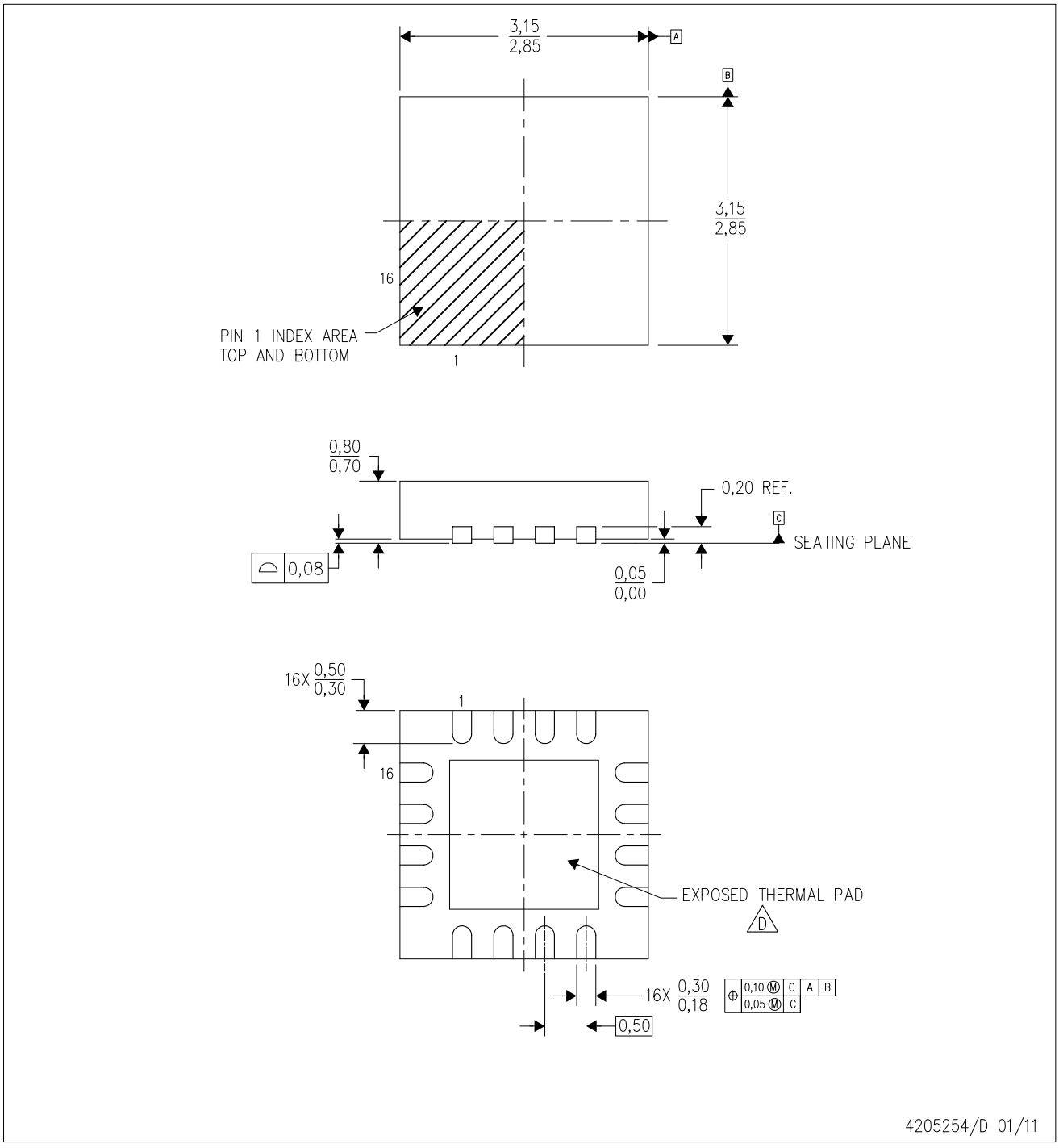
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS61181ARTER | WQFN | RTE | 16 | 3000 | 346.0 | 346.0 | 29.0 |
| TPS61181ARTET | WQFN | RTE | 16 | 250 | 190.5 | 212.7 | 31.8 |

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

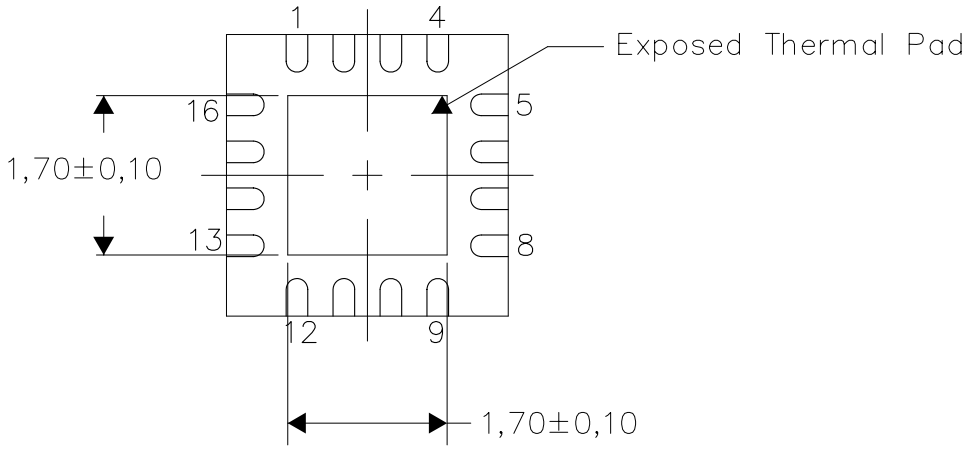
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



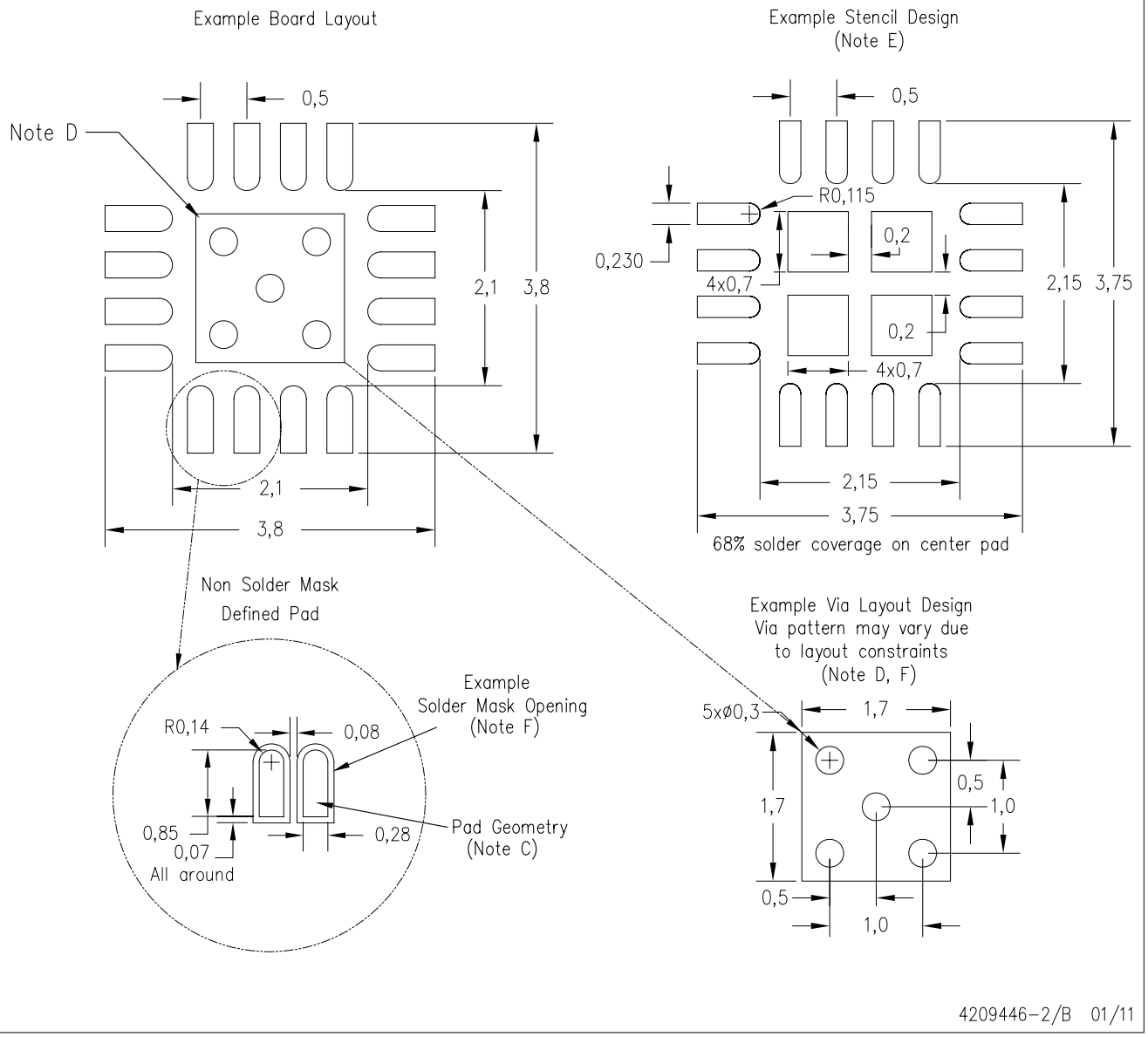

Bottom View

Exposed Thermal Pad Dimensions

4206446–3/I 01/11

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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