LOW I_Q, SINGLE BOOST, DUAL SYNCHRONOUS BUCK CONTROLLER

Check for Samples: TPS43330-Q1, TPS43332-Q1

FEATURES

- **Two Synchronous Buck Controllers**
- **One Pre-Boost Controller**
- **Input Range up to 40V, (Transients up to 60V), Operation Down to 2V when Boost is Enabled**
- **Low Power Mode I_Q: 30µA (one Buck on), 35µA (Two Bucks on)**
- **Low Shutdown Current I_{sh} < 4 µA**
- **Buck Output Range 0.9V to 11V**
- **Boost Output Selectable: 7V/10V/11V**
- **Programmable frequency and External Synchronization Range 150kHz to 600kHz**
- **Separate Enable Inputs (ENA, ENB)**
- **Frequency Spread Spectrum (TPS43332)**
- **Selectable Forced Continuous Mode or Automatic Low Power Mode at Light Loads**
- **Sense Resistor or Inductor DCR Sensing**
- **Out of Phase Switching between Buck Channels**
- **Peak Gate Drive Current 1.5 A**
- **Thermally Enhanced Package – 38-Pin HTSSOP (DAP) with PowerPad™**
- **Qualified for Automotive Applications**

APPLICATIONS

- **Automotive Start-Stop, Infotainment, Navigation Instrument Cluster Systems**
- **Industrial/Automotive Multi-Rail DC Power Distribution Systems & Electronic Control Units**

DESCRIPTION

The TPS43330-Q1/TPS43332-Q1 includes two current mode synchronous buck controllers and a voltage mode boost controller. The part is ideally suited as pre-regulator stage with low Iq requirements and systems that need to survive supply drops due to cranking events. The integrated boost controller allows the device to operate down to 2V at the input without seeing a drop on the Buck regulator output stages. At light loads, the buck controllers can be enabled to operate automatically in Low Power Mode consuming just 30µA of quiescent current.

The buck controllers have independent soft start capability and power good indicators. External MOSFET protection is provided by current fold back in the buck controllers and cycle-by-cycle current limitation in the boost controller. The switching frequency can be programmed over 150 kHz to 600 kHz or synchronized to an external clock in the same range. Additionally, the TPS43332-Q offers frequency-hopping spread spectrum operation.

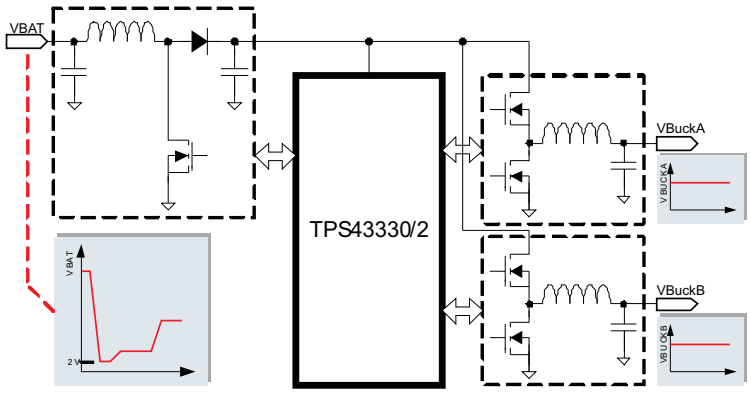


Figure 1. Typical Application Diagram

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_J	OPTION	PACKAGE(2)	ORDERABLE PART NUMBER
-40ºC to 150ºC	Frequency Hopping Spread Spectrum OFF	DAP(3)	TPS43330QDAPQ1
	Frequency Hopping Spread Spectrum ON		TPS43332QDAPQ1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) The DAP package is available in tape and reel. Add the R suffix (TPS43330QDAPR, TPS43332QDAPR) to order.

ABSOLUTE MAXIMUM RATINGS(1)

		MIN	MAX	UNIT
Voltage	Input Voltage: VIN, VBAT	–0.3	60	V
Voltage (Buck Function: Buck A and Buck B)	Enable Inputs: ENA, ENB	–0.3	60	V
	Bootstrap Inputs: CBA, CBB	–0.3	68	V
	Phase Inputs: PHA, PHB	–0.7	60	V
	Phase Inputs: PHA, PHB (for 150ns)	–1.0		V
	Feedback Inputs: FBA, FBB	–0.3	13	V
	Error amplifier outputs: COMPA, COMPB	–0.3	13	V
	High-Side MOSFET Driver: GA1-PHA, GB1-PHB	–0.3	8.8	V
	Low-Side MOSFET Drivers: GA2, GB2	–0.3	8.8	V
	Current Sense Voltage: SA1, SA2, SB1, SB2	–0.3	13	V
	Soft Start: SSA, SSB	–0.3	13	V
	Power Good Output: PGA, PGB	–0.3	13	V
	Power Good Delay: DLYAB	–0.3	13	V
	Switching Frequency Timing Resistor: RT	–0.3	13	V
	SYNC, EXTSUP	–0.3	13	V
Voltage (Boost Function)	Low-Side MOSFET Driver: GC1	–0.3	8.8	V
	Error amplifier output: COMPC	–0.3	13	V
	Enable Input: ENC	–0.3	13	V
	Current Limit Sense: DS	–0.3	60	V
	Output Voltage Select: DIV	–0.3	8.8	V
Voltage (PMOS Driver)	P-Channel MOSFET Driver: GC2	–0.3	60	V
	P-Channel MOSFET Driver: VIN-GC2	–0.3	8.8	V
	Gate Driver Supply: VREG	–0.3	8.8	V
Temperature	Junction Temperature: T_J	–40	150	°C
	Operating Temperature: T_A	–40	125	°C
	Storage Temperature: T_S	–55	165	°C
Electrostatic Discharge Ratings	Human Body Model (HBM)	±2		kV
	Charged Device Model (CDM)			V
	- FBA, FBB, RT, DLYAB	±400		
	- VBAT, ENC, SYNC, VIN	±750		
	- all other pins	±500		
	Machine Model (MM)			V
	- PGA, PGB	±150		
	- all others	±200		

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to GND.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Buck Function: Buck A and Buck B Voltage	Input Voltage: VIN, VBAT	4	40	V
	Enable Inputs: ENA, ENB	4	40	V
	Boot Inputs: CBA, CBB	4	44	V
	Phase Inputs: PHA, PHB	–0.6	40	V
	Current Sense Voltage: SA1, SA2, SB1, SB2	0	11	V
	Power Good Output: PGA, PGB	0	11	V
	Power Good Delay: DLYAB	0	6	V
	SYNC, EXTSUP	0	9	V
Boost Function	Error amplifier output: COMPC	0	6	V
	Enable Input: ENC	0	9	V
	Voltage Sense: DS		40	V
	DIV	0	6	V
Temperature Ratings	Thermal Resistance Junction to Ambient, θ_{JA} (1)	28		°C/W
	Thermal Resistance Junction to pad, θ_{JC} (2)	10		°C/W
	Operating Temperature: T_A	–40	125	°C

(1) This assumes a JEDEC JESD 51-5 standard board with thermal vias – See Power Pad section and application note from Texas Instruments SLMA002 for more information.
(2) This assumes junction to exposed pad.

DC ELECTRICAL CHARACTERISTICS

VIN = 8 V to 18 V, T_J = -40°C to 150°C (unless otherwise noted)

NO.	TEST(1)	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.0	**Input Supply**							
1.1	PT	V_{Bat}	Supply Voltage	Boost Controller enabled, after initial start up condition is satisfied	2		40	V
1.2	PT	V_{IN}	Device Operating Range	Input voltage required for device on initial start up	6.5		40	V
				Buck regulator operating range after initial start up	4		40	V
1.3	PT	$V_{IN\ UV}$	Buck Undervoltage Lockout	VIN Falling	3.5	3.6	3.8	V
				VIN Rising		3.8	4	V
1.4	PT	$V_{BAT-Off}$	Boost unlock threshold	VBAT Rising	8.2	8.5	8.8	V
1.5	PT	$I_{q\_LPM\_}$	LPM Quiescent Current: T_A = 25°C(2)	VIN = 13V, BuckA: LPM, BuckB: off		30	40	µA
				VIN = 13V, BuckB: LPM, BuckA: off				
				VIN = 13V, BuckA, B: LPM		35	45	µA
1.6	PT	I_{q_LPM}	LPM Quiescent Current: T_A = 125°C(2)	VIN = 13V, BuckA: LPM, BuckB: off		40	50	µA
				VIN = 13V, BuckB: LPM, BuckA: off				
				VIN = 13V, BuckA, B: LPM		45	55	µA
1.7	PT	I_{q_NRM}	Quiescent Current: T_A = 25°C(2)	Normal operation, SYNC = 5V				
				VIN = 13V, BuckA: CCM, BuckB: off		4.85	5.3	mA
				VIN = 13V, BuckB: CCM, BuckA: off				
				VIN = 13V, BuckA, B: CCM		7	7.6	mA
1.8	PT	I_{q_NRM}	Quiescent Current: T_A = 125°C(2)	Normal operation, SYNC = 5V				
				VIN = 13V, BuckA: CCM, BuckB: off		5	5.5	mA
				VIN = 13V, BuckB: CCM, BuckA: off				
				VIN = 13V, BuckA, B: CCM		7.5	8	mA
1.9	PT	I_{bat_sh}	Shutdown current ,T_A = 25°C	BuckA, B: off, VBat = 13V		2.5	4	µA
1.10	PT	I_{bat_sh}	Shutdown current ,T_A = 125°C	BuckA, B: off, VBat = 13V		3	5	µA
2.0	**Input voltage VBAT - Undervoltage lock out**							
2.1	PT	V_{BATUV}	Boost Input Undervoltage	VBAT falling	1.8	1.9	2	V
				VBAT rising	2.4	2.5	2.6	V
2.2	PT	$UVLO_{Hys}$	Hysteresis		500	600	700	mV
2.3	PT	$UVLO_{filter}$	Filter time			5		µs
3.0	**Input voltage VIN - Over voltage lock out**							
3.1	PT	V_{OVLO}	Overvoltage shutdown	(based on VIN sense) Rising	45	46	47	V
				Falling	43	44	45	V
3.2	PT	$OVLO_{Hys}$	Hysteresis		1	2	3	V
3.3	PT	$OVLO_{filter}$	Filter time			5		µs
4.0	**Boost Controller**							
4.1	PT	$V_{boost7-VIN}$	Boost V_{OUT} = 7V	DIV = low, VBAT = 2 V to 7 V		7		V
4.2	PT	$V_{boost7-th}$	Boost mode threshold Boost V_{OUT} = 7V	VBAT falling – Boost enable threshold	7.5	8	8.5	V
				VBAT rising – Boost disable threshold	8	8.5	9	V
				Hysteresis	0.4	0.5	0.6	V
4.3	PT	$V_{boost10-VIN}$	Boost V_{OUT} = 10V	DIV = open, VBAT = 2 V to 10 V		10		V
4.4	PT	$V_{boost10-th}$	Boost mode threshold Boost V_{OUT} = 10V	VBAT falling – Boost enable threshold	10.5	11	11.5	V
				VBAT rising – Boost disable threshold	11	11.5	12	V
				Hysteresis	0.4	0.5	0.6	V
4.5	Info	$V_{boost11-VIN}$	Boost V_{OUT} = 11V	DIV = VREG, VBAT = 2 V to 11 V		11		V

(1) PT = Production tested; CT = Characterization only, not production tested; Info = Information based on simulations and lab evaluation, not production tested
(2) Quiescent current specification is non-switching current consumption without including the current in the external feedback resistor divider.

DC ELECTRICAL CHARACTERISTICS (continued)

VIN = 8 V to 18 V, T_J = -40°C to 150°C (unless otherwise noted)

NO.	TEST(1)	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.6	Info	$V_{boost11-th}$	Boost mode threshold Boost V_{OUT} = 11V	VBAT falling – Boost enable threshold	11.5	12	12.5	V
				VBAT rising – Boost disable threshold	12	12.5	13	V
				Hysteresis	0.4	0.5	0.6	V
	Boost Switch current limit							
4.7	PT	V_{DS}	Current limit sensing	DS input with respect to PGNDA	0.175	0.2	0.225	V
4.8	Info	t_{DS}	leading edge blanking			200		ns
	Gate Driver for Boost Controller							
4.9	Info	$I_{GC1\ Peak}$	Gate driver peak current			1.5		A
4.10	PT	$R_{DS(ON)}$	Source and Sink driver	VREG = 5.8V, IGC1 current = 200mA			2	Ω
	Gate Driver for PMOS							
4.11	PT	$R_{DS\ ON}$	PMOS OFF			10	20	Ω
4.12	PT	I_{PMOS_ON}	Gate current	VIN = 13.5V, Vgs = -5V	10			mA
4.13	PT	t_{delay_ON}	Turn ON delay	C = 10nF		5	10	µs
	Boost Controller Switching frequency							
4.14	PT	$f_{sw-Boost}$	Boost Switching Frequency				$f_{SW\_Buck}/2$	kHz
4.15	PT	D_{Boost}	Boost duty cycle				90%	
	Error Amplifier (OTA) for Boost Converters							
4.16	PT	Gm_{BOOST}	Forward Transconductance	VBAT = 12V	0.8		1.35	mmho
				VBAT = 5V	0.35		0.65	
5.0	**Buck Controllers**							
5.1	PT	$V_{BuckA/B}$	Adjustable. output voltage range		0.9		11	V
5.2	PT	$V_{ref,\ NRM}$	internal reference voltage in normal mode	Measure FBX pin	0.792	0.800	0.808	V
	Info			Internal tolerance on reference	-1%		+1%	
5.3	PT	$V_{ref,\ LPM}$	internal reference voltage in low power mode	Measure FBX pin	0.784	0.800	0.816	V
	Info			Internal tolerance on reference	-2%		+2%	
5.4	PT	V_{sense}	V sense for forward current limit in CCM	Maximum sense voltage FBx = 0.75V (low duty cycles)	60	75	90	mV
5.5	PT		V sense for reverse current limit in CCM	Minimum sense voltage FBx = 1V	-65	-37.5	-23	mV
5.6	CT	$V_{I-Foldback}$	V sense for output short	Sense voltage in foldback FBx = 0V	17	32.5	48	mV
5.7	Info	t_{dead}	shoot through delay, blanking time			20		ns
5.8	CT	DC_{NRM}	Duty cycle	High side minimum on time		100		ns
	Info			Maximum duty cycle (digitally controlled)		98.75%		
5.9	CT	DC_{LPM}	Duty Cycle LPM				80%	
5.10	Info	I_{LPM_Entry}	LPM entry threshold load current as fraction of maximum set load current	The exit threshold is specified to be always higher than entry threshold		1%		
		I_{LPM_Exit}	LPM exit threshold load current as fraction of maximum set load current			10%		
	High Side external NMOS Gate Drivers for Buck Controller							
5.11	Info	I_{GX1_peak}	Gate driver peak current			1.5		A
5.12	PT	$R_{DS\ ON}$	Source and Sink driver	V_{VREG} = 5.8V, I_{GX1} current = 200mA			2	Ω
	Low Side NMOS Gate Drivers for Buck Controller							
5.13	Info	I_{GX2_peak}	Gate driver peak current			1.5		A
5.14	PT	$R_{DS\ ON}$	Source and sink driver	VREG = 5.8V, I_{GX2} current = 200mA			2	Ω
	Error Amplifier (OTA) for Buck Converters							
5.15	PT	Gm_{BUCK}	Transconductance	COMPA, COMPB = 0.8V, source/sink = 5µA, Test in feedback loop	0.72	1	1.35	mmho
5.16	PT	I_{PULLUP_FBx}	Pull-Up Current at FBx pins	FBx = 0V	50	100	200	nA
6.0	**Digital Inputs: ENA, ENB, ENC, SYNC**							
6.1	PT	V_{ih}	Higher threshold	VIN = 13V	1.7			V

DC ELECTRICAL CHARACTERISTICS (continued)

VIN = 8 V to 18 V, T_J = -40°C to 150°C (unless otherwise noted)

NO.	TEST(1)	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
6.2	PT	V_{il}	Lower threshold	VIN = 13V			0.7	V
6.3	PT	R_{ih_SYNC}	Resistance	VSYNC = 5V, SYNC: pull down resistance		500		kΩ
6.4	PT	R_{il_ENC}	Resistance	VENC = 5V, ENC: pull down resistance		500		kΩ
6.5	PT	I_{il_ENx}	pull-up current	VENx = 0V, ENA, ENB: pull up current source		0.5	2	µA

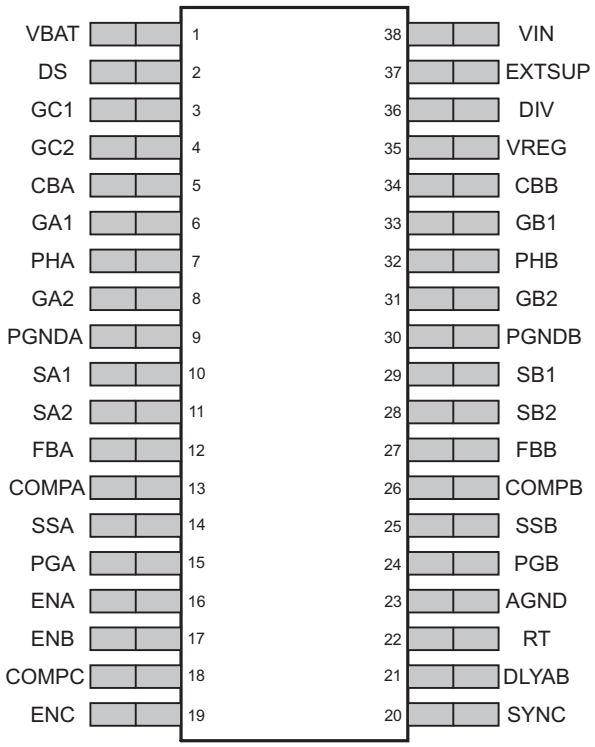
DC ELECTRICAL CHARACTERISTICS (continued)

VIN = 8 V to 18 V, T_J = -40°C to 150°C (unless otherwise noted)

NO.	TEST(1)	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
7.0	**Boost Output Voltage: DIV**							
7.1	PT	V_{ih_DIV}	Higher threshold	VREG = 5.8V	Vreg-0.2			V
7.2	PT	V_{il_DIV}	Lower threshold				0.2	V
7.3	PT	V_{oz_DIV}	open	floating		Vreg/2		V
8.0	**Switching Parameter – Buck DC-DC Controllers**							
8.1	PT	f_{SW_Buck}	Buck switching frequency	RT pin: GND	360	400	440	kHz
8.2	PT	f_{SW_Buck}	Buck switching frequency	RT pin: 60kΩ external resistor	360	400	440	kHz
8.3	PT	f_{SW_adj}	Buck adjustable range	RT pin: using external resistor	150		600	kHz
8.4	PT	f_{SYNC}	Buck synch. range	External clock input	150		600	kHz
8.5	PT	f_{SS}	Spread Spectrum spreading	TPS43332 only		5%		
9.0	**Internal Gate Driver Supply**							
9.1	PT	V_{REG}	Internal regulated supply	VIN = 8V to 18V, EXTSUP = 0V, SYNC = high	5.5	5.8V	6.1	V
			Load Regulation	I_{VREG} = 0mA to 100mA, EXTSUP = 0V, SYNC = high		0.2%	1%	
9.2	PT	$V_{REG-EXTSUP}$	Internal Regulated supply	EXTSUP = 8.5V	7.2	7.5	7.8	V
			Load Regulation	I_{EXTSUP} = 0mA to 125mA, SYNC = High EXTSUP = 8.5V to 13V		0.2	1	%
9.3	PT	$V_{EXTSUP-VREG}$	Switch over voltage	I_{VREG} = 0mA to 100mA , EXTSUP ramping positive	4.4	4.6	4.8	V
9.4	PT	$V_{EXTSUP-Hys}$	Switch over hysteresis		150		250	mV
9.5	PT	$I_{REG-Limit}$	Current Limit on VREG	EXTSUP = 0V, normal mode as well as LPM	100		400	mA
9.6	PT	$I_{REG\_EXTSUP-Limit}$	Current Limit on VREG when using EXTSUP	I_{VREG} = 0mA to 100mA, EXTSUP = 8.5V, SYNC = High	125		400	mA
10.0	**Soft Start**							
10.1	PT	I_{SSx}	Soft Start source current	SSA and SSB = 0V	0.75	1	1.25	µA
11.0	**Oscillator (RT)**							
11.1	PT	V_{RT}	Oscillator reference voltage			1.2		V
12.0	**Power Good / Delay**							
12.1	PT	PG_{pullup}	Pullup for A and B	internal pullup to Sx2		50		kΩ
12.2	PT	PG_{th1}	Power Good Threshold	FBx falling	-5	-7	-9	%
12.3	PT	PG_{hys}	Hysteresis			2%		
12.4	PT	PG_{drop}	Voltage drop	I_{PGA} = 5mA			450	mV
12.5	PT			I_{PGA} = 1mA			100	mV
12.6	PT	PG_{leak}	Leakage	VSx2 = VPGx = 13V			1	µA
12.7	PT	$t_{deglitch}$	Deglitch Time	Power Good deglitch	2		16	µs
12.8	PT	t_{delay}	Reset Delay	External capacitor = 1nF VBUCKX < PG_{th1}		1		ms
12.9	PT	t_{delay_fix}	Fixed Reset Delay	No external capacitor, pin open		20	50	µs
12.10	PT	I_{oh}	Activate current source	Current to charge external capacitor	30	40	50	µA
12.11	PT	I_{il}	Activate current sink	Current to discharge external capacitor	30	40	50	µA
13.0	**Over Temperature Protection**							
13.1	CT	$T_{shutdown}$	shutdown threshold	Junction temperature	150	165		°C
13.2	CT	T_{hys}		Hysteresis		15		°C

DEVICE INFORMATION

DAP PACKAGE
(TOP VIEW)



PIN FUNCTIONS

NO.	NAME	I/O	DESCRIPTION
1	VBAT	I	Battery input sense for the boost controller. If the boost controller is enabled and the voltage at VBAT falls below the boost threshold, the device will activate the boost controller and regulate the voltage at VIN to the programmed boost output voltage.
2	DS	I	This input monitors the voltage on the external Boost converter low-side MOSFET for over current protection. Alternatively, it can be connected to a sense resistor between the source of the low-side MOSFET and ground via a filter network for better noise immunity.
3	GC1	O	An external low-side N-channel MOSFET for the boost regulator can be driven from this output. This output provides high peak currents to drive capacitive loads. The voltage swing on this pin is provided by VREG.
4	GC2	O	A floating output drive to control the external P-channel MOSFET is available at this pin. This MOSFET can be used to bypass the boost rectifier diode or a reverse protection diode when the boost is not switching or disabled, and thus reduce power losses.
5	CBA	I	A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate drive circuitry in the buck controller BUCK A. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to re-charge.
6	GA1	O	External high-side N-channel MOSFET for the buck regulator BUCK A can be driven from these output. The output provides high peak currents to drive capacitive loads. The gate drive is referred to a floating ground reference provided by the PHA and has a voltage swing provided by CBA.
7	PHA	O	Switching terminal of the buck regulator BUCK A, providing a floating ground reference for the high-side MOSFET gate driver circuitry and is used to sense current reversal in the inductor when discontinuous mode operation is desired.
8	GA2	O	External low-side N-channel MOSFET for the buck regulator BUCK A can be driven from this output. The output provides high peak currents to drive capacitive loads. The voltage swing on this pin is provided by VREG.
9	PGNDA	O	Power ground connection to the source of the low-side N-channel MOSFETs of BUCK A.
10	SA1	I	High Impedance differential voltage inputs from the current sense element (sense resistor or inductor DCR) for each buck controller. The current sense element should be chosen to set the maximum current through the inductor based on the current limit threshold (subject to tolerances) and considering the typical characteristics across duty cycle and VIN. (SA1 positive node, SA2 negative node).
11	SA2	I	

PIN FUNCTIONS (continued)

NO.	NAME	I/O	DESCRIPTION
12	FBA	I	Feedback voltage pin for BUCK A. The buck controller regulates the feedback voltage to the internal reference of 0.8V. A suitable resistor divider network between the buck output and the feedback pin sets the desired output voltage.
13	COMPA	O	Error amplifier output of BUCK A and compensation node for voltage loop stability. The voltage at this node sets the target for the peak current through the respective inductor. This voltage is clamped on the upper and lower ends to provide current limit protection for the external MOSFETs.
14	SSA	O	Soft-start or tracking input for the buck controller BUCK A. The buck controller regulate the FBA voltage to the lower of 0.8V or the SSA pin voltage. An internal pull-up current source of 1µA is present at the pin and an appropriate capacitor connected here can be used to set the soft-start ramp interval. A resistor divider connected to another supply can also be used to provide a tracking input to this pin.
15	PGA	O	Open drain power good indicator pin for BUCK A. An internal power good comparator monitors the voltage at the feedback pin and pull this output low when the output voltage falls below 93% of the set value, or if either Vin or Vbat drops below their respective undervoltage threshold.
16	ENA	I	Enable inputs for BUCK A (active high with an internal pull up current source). An input voltage higher than 1.5V enables the controller while an input voltage lower than 0.7V disables the controller. When both ENA and ENB are low, the device is shut down and consumes less than 4µA of current.
17	ENB	I	Enable inputs for BUCK B (active high with an internal pull up current source). An input voltage higher than 1.5V enables the controller while an input voltage lower than 0.7V disables the controller. When both ENA and ENB are low, the device is shut down and consumes less than 4µA of current.
18	COMPC	O	Error amplifier output and loop compensation node of the boost regulator.
19	ENC	I	This input enables and disables the boost regulator. An input voltage higher than 1.5V enables the controller. Voltages lower than 0.7V disable the controller. When enabled, the controller will start switching as soon as VBAT falls below the boost threshold depending upon the programmed output voltage.
20	SYNC	I	If an external clock is present on this pin the device detects it and the internal PLL locks on to the external clock. This overrides the internal oscillator frequency. The device can synchronize to frequencies from 150 kHz to 600 kHz. A high logic level on this pin ensures forced continuous mode operation of the buck controllers and inhibits transition to low power mode. An open or low allows discontinuous mode operation and entry into low power mode at light loads. On the TPS43332, a high level enables frequency-hopping spread spectrum while an open or a low level disables it.
21	DLYAB	O	The capacitor at the DLYAB pin sets the power good delay interval used to de-glitch the outputs of the power good comparators. When this pin is left open, the power good delay is set to an internal default value of 20µsec typical.
22	RT	O	The operating switching frequency of the buck and boost controllers is set by connecting a resistor to ground on this pin. A short circuit to ground on this pin defaults operation to 400 kHz for the buck controllers and 200 kHz for the boost controller.
23	AGND	O	Analog Ground Reference
24	PGB	O	Open drain power good indicator pin for BUCK B. An internal power good comparator monitors the voltage at the feedback pin and pull this output low when the output voltage falls below 93% of the set value, or if either Vin or Vbat drops below their respective undervoltage threshold.
25	SSB	O	Soft-start or tracking input for the buck controller BUCK B. The buck controller regulate the FBB voltage to the lower of 0.8V or the SSB pin voltage. An internal pull-up current source of 1µA is present at the pin and an appropriate capacitor connected here can be used to set the soft-start ramp interval. A resistor divider connected to another supply can also be used to provide a tracking input to this pin.
26	COMPB	O	Error amplifier output of BUCK B and compensation node for voltage loop stability. The voltage at this node sets the target for the peak current through the respective inductor. This voltage is clamped on the upper and lower ends to provide current limit protection for the external MOSFETs.
27	FBB	I	Feedback voltage pin for BUCK B. The buck controller regulates the feedback voltage to the internal reference of 0.8V. A suitable resistor divider network between the buck output and the feedback pin sets the desired output voltage.
28	SB2	I	High Impedance differential voltage inputs from the current sense element (sense resistor or inductor DCR) for each buck controller. The current sense element should be chosen to set the maximum current through the inductor based on the current limit threshold (subject to tolerances) and considering the typical characteristics across duty cycle and VIN. (SB1 positive node, SB2 negative node).
29	SB1	I	
30	PGNDB	O	Power ground connection to the source of the low-side N-channel MOSFETs of BUCK B.
31	GB2	O	External low-side N-channel MOSFETs for the buck regulator BUCK B can be driven from this output. The output provides high peak currents to drive capacitive loads. The voltage swing on this pin is provided by VREG.
32	PHB	O	Switching terminal of the buck regulator BUCK B, providing a floating ground reference for the high-side MOSFET gate driver circuitry and is used to sense current reversal in the inductor when discontinuous mode operation is desired.

PIN FUNCTIONS (continued)

NO.	NAME	I/O	DESCRIPTION
33	GB1	O	External high-side N-channel MOSFET for the buck regulator BUCK B can be driven from these output. The output provides high peak currents to drive capacitive loads. The gate drive is referred to a floating ground reference provided by the PHB and has a voltage swing provided by CBB.
34	CBB	I	A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate drive circuitry in the buck controller BUCK B. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to re-charge.
35	VREG	O	An external capacitor on this pin is required to provide a regulated supply for the gate drivers of the buck and boost controllers. A capacitance in the order of 4.7uF is recommended. The regulator can be used such that it is either powered from VIN or EXTSUP. This pin has a current limit protection and should not be used to drive any other loads.
36	DIV	I	The status of this pin defines the output voltage of the boost regulator. A high input regulates the Boost converter at 11V, a low input sets the value at 7V and a floating pin sets 10V.
37	EXTSUP	I	EXTSUP can be used to supply the VREG regulator from one of the TPS43330/2 buck regulator rails to reduce power dissipation in cases where VIN is expected to be high. When EXTSUP is open or lower than 4.6V, the regulator is powered from VIN.
38	VIN	I	Main Input pin. This is the buck controller input pin as well as the output of the boost regulator. Additionally it powers the internal control circuits of the device.

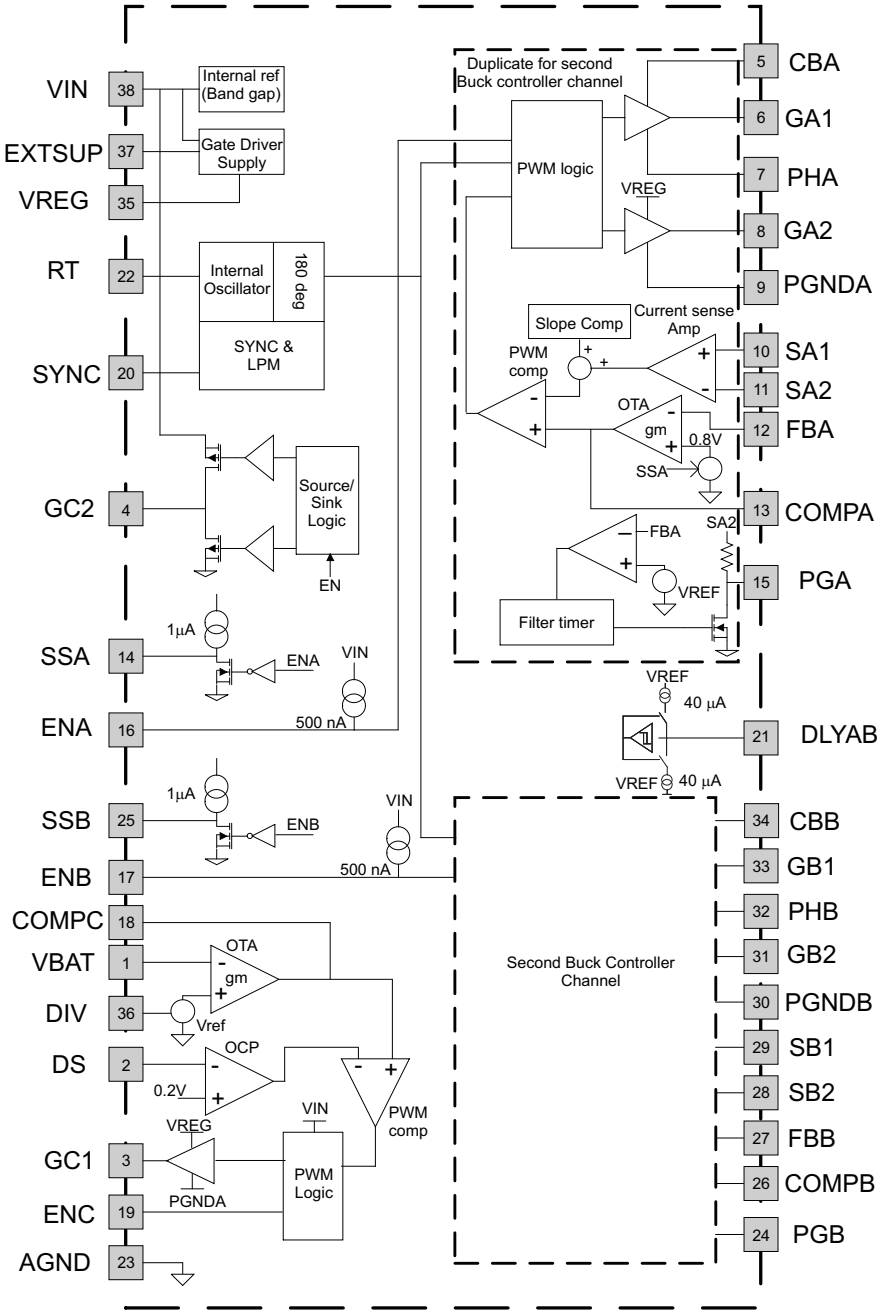


Figure 2. Functional Block Diagram

TYPICAL CHARACTERISTICS

EFFICIENCY ACROSS OUTPUT CURRENTS (BUCKS)
VIN = 12V, VOUT = 5V, SWITCHING FREQUENCY = 400kHz
INDUCTOR = 4.7µH, RSENSE = 10mΩ

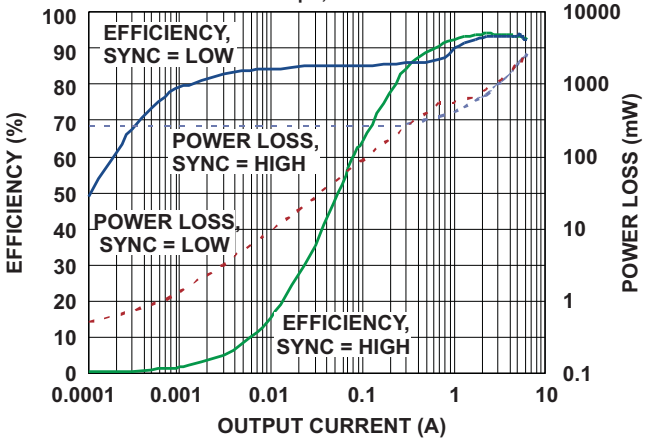


Figure 3.

INDUCTOR CURRENTS (BUCK)
VIN = 12V, VOUT = 5V, SWITCHING FREQUENCY = 400kHz
INDUCTOR = 4.7µH, RSENSE = 10mΩ

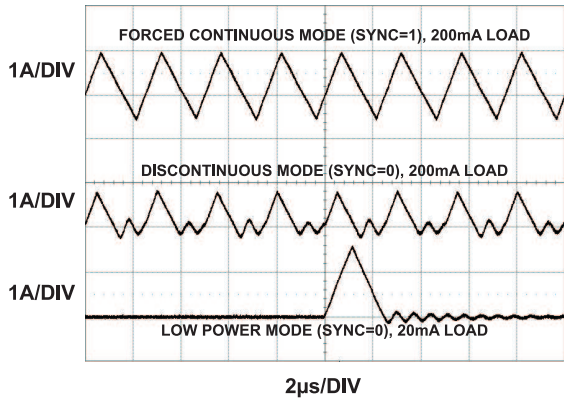


Figure 4.

BUCK LOAD STEP: FORCED CONTINUOUS MODE
(0 TO 4 A AT 2.5 A/µs)
VIN = 12 V, VOUT = 5 V, SWITCHING FREQUENCY = 400 kHz
INDUCTOR = 4.7 µH, RSENSE = 10 mΩ

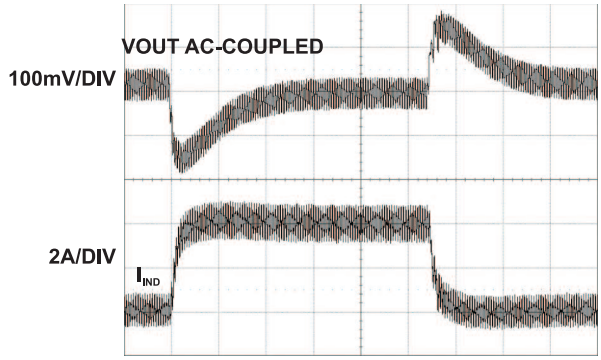


Figure 5.

SOFT-START OUTPUTS (BUCK)

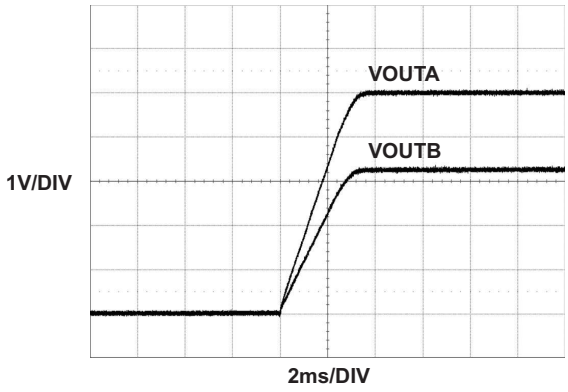


Figure 6.

BUCK LOAD STEP: LOW POWER MODE ENTRY
(4A TO 90mA AT 2.5A/µs)
VIN = 12V, VOUT = 5V, SWITCHING FREQUENCY = 400kHz
INDUCTOR = 4.7µH, RSENSE = 10mΩ

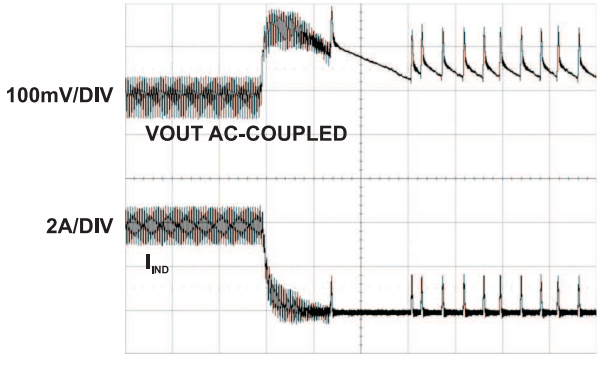


Figure 7.

BUCK LOAD STEP: LOW POWER MODE EXIT
(0.09mA TO 4A AT 2.5A/µs)
VIN = 12V, VOUT = 5V, SWITCHING FREQUENCY = 400kHz
INDUCTOR = 4.7µH, RSENSE = 10mΩ

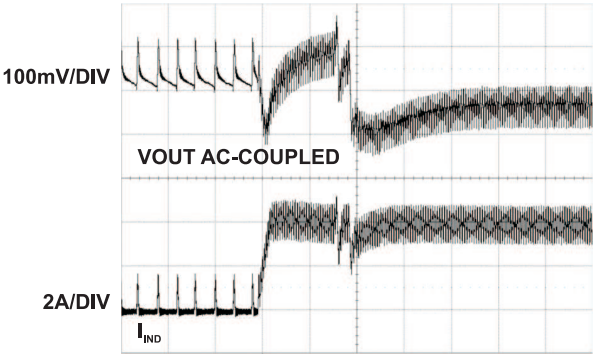


Figure 8.

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY ACROSS OUTPUT CURRENTS (BOOST)
VIN (BOOST OUTPUT) = 10V, SWITCHING FREQUENCY = 200kHz,
INDUCTOR = 1.0µH, RSENSE = 7.5mΩ

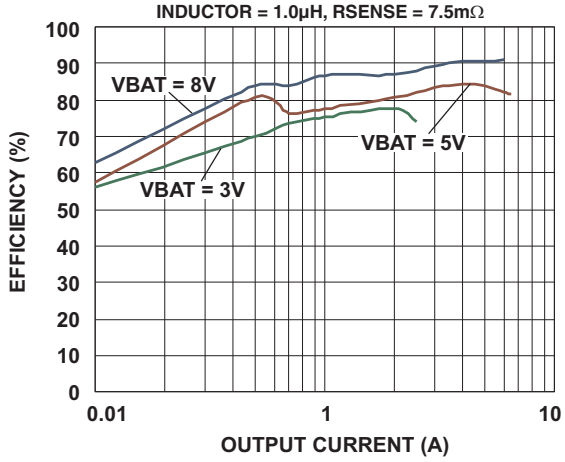


Figure 9.

LOAD STEP RESPONSE (BOOST)
(0 TO 5A AT 2.5A/µs)
VBAT (BOOST INPUT) = 5V, VIN (BOOST OUTPUT) = 10V,
SWITCHING FREQUENCY = 200kHz, INDUCTOR = 1.0µH,
RSENSE = 7.5mΩ, CIN = 440µF, COUT = 660µF

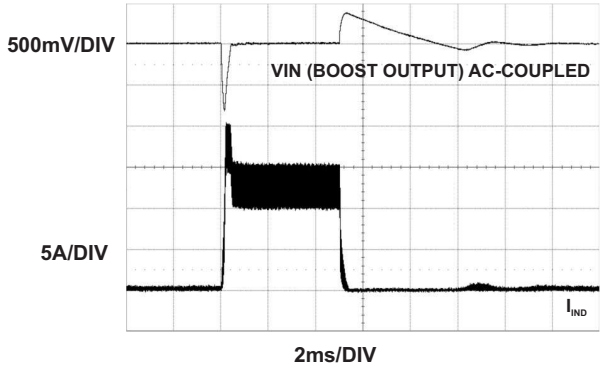


Figure 10.

CRANKING PULSE BOOST RESPONSE
(12V to 3V IN 1ms AT BUCK OUTPUTS 7.5W/11.5W)
VIN (BOOST OUTPUT) = 10V, BUCKA = 5V/1.5A, BUCKB = 3.3V/3.5A,
SWITCHING FREQUENCY = 200kHz, INDUCTOR = 1.0µH,
RSENSE = 7.5mOHM, CIN = 440µF, COUT = 660µF

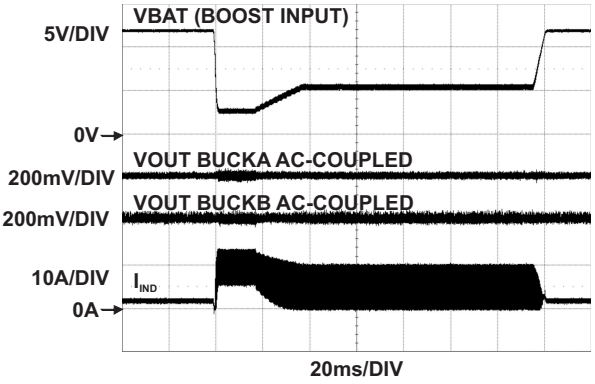


Figure 11.

CRANKING PULSE BOOST RESPONSE
(12V to 4V IN 1ms AT BOOST DIRECT OUTPUT 25W)
VIN (BOOST OUTPUT) = 10V, BUCKA = 5V/1.5A, BUCKB = 3.3V/3.5A,
SWITCHING FREQUENCY = 200kHz, INDUCTOR = 1.0µH,
RSENSE = 7.5mOHM, CIN = 440µF, COUT = 660µF

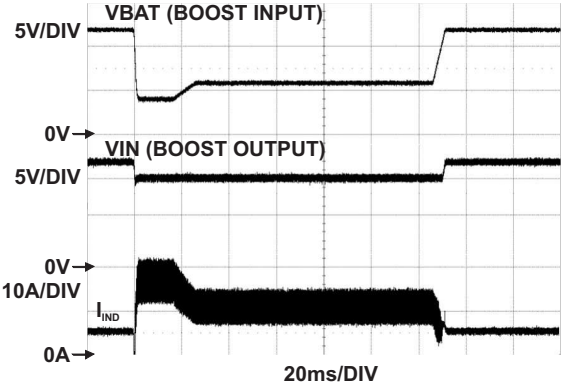


Figure 12.

INDUCTOR CURRENTS (BOOST)
VBAT (BOOST INPUT) = 5V, VIN (BOOST OUTPUT) = 10V,
SWITCHING FREQUENCY = 200kHz, INDUCTOR = 1.0µH,
RSENSE = 7.5mΩ, CIN = 440µF, COUT = 660µF

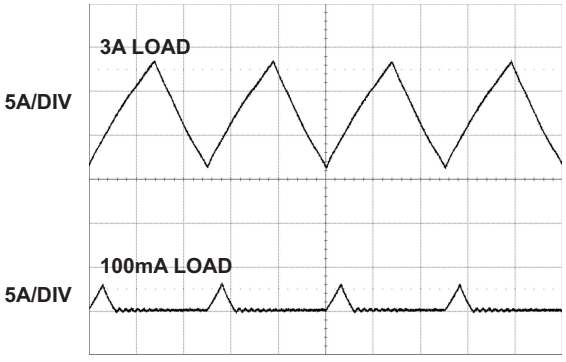


Figure 13.

TYPICAL CHARACTERISTICS (continued)

NO-LOAD QUIESCENT CURRENT ACROSS TEMPERATURE

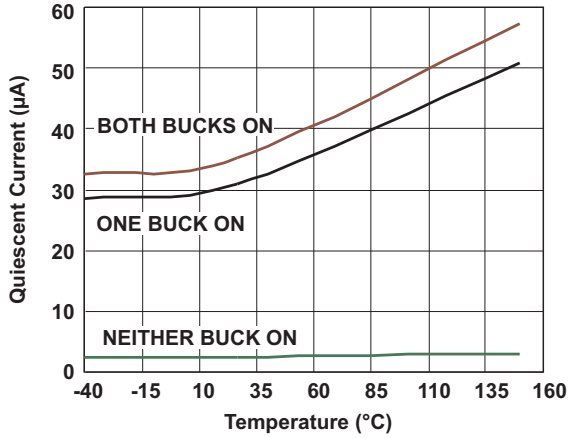


Figure 14.

BUCKx PEAK CURRENT LIMIT vs. COMPx VOLTAGE

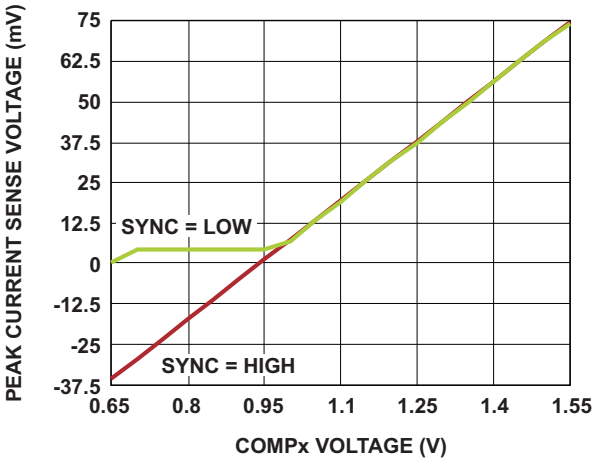


Figure 15.

CURRENT SENSE PINS INPUT CURRENT (BUCK)

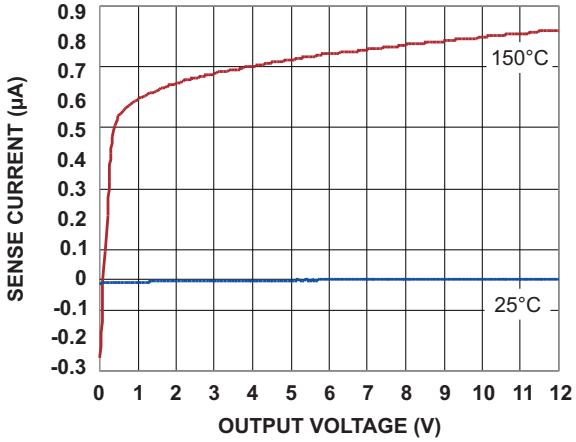


Figure 16.

FOLDBACK CURRENT LIMIT (BUCK)

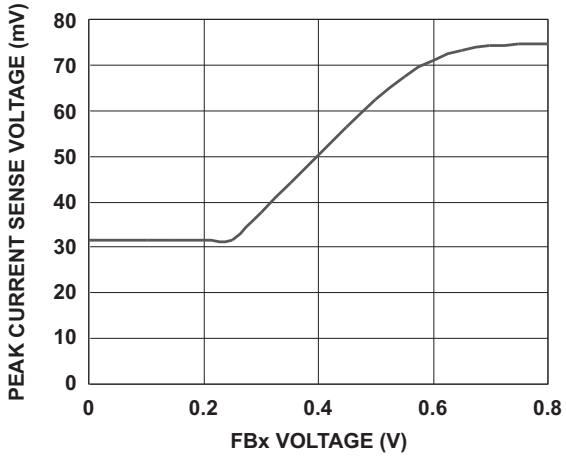


Figure 17.

REGULATED FBx VOLTAGE vs TEMPERATURE (BUCK)

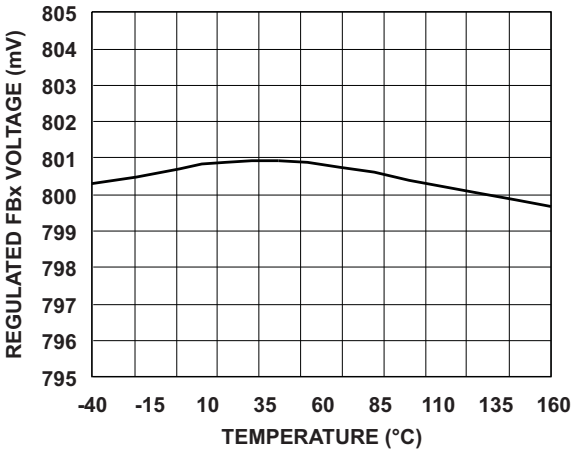


Figure 18.

CURRENT LIMIT VS DUTY CYCLE (BUCK)

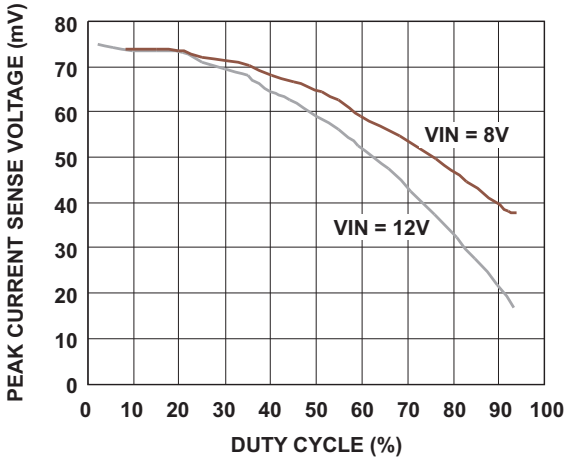


Figure 19.

DETAILED DESCRIPTION

BUCK CONTROLLERS: NORMAL MODE PWM OPERATION

Frequency Selection and External Synchronization

The buck controllers operate using constant frequency peak current mode control for optimal transient behavior and ease of component choices. The switching frequency is programmable between 150 kHz and 600 kHz depending upon the resistor value at the RT pin. A short circuit to ground at this pin sets the default switching frequency to 400 kHz. The frequency can also be set by a resistor at RT according to the formula:

$$f_{SW} = \frac{X}{RT} (X = 24k\Omega \times MHz)$$

$$f_{SW} = 24 \times \frac{10^9}{RT}$$

Equation 1 Switching Frequency

For example,

600kHz requires 40kΩ

150kHz requires 160kΩ

It is also possible to synchronize to an external clock at the SYNC pin in the same frequency range of 150 kHz to 600 kHz. The device detects clock pulses at this pin and an internal PLL locks on to the external clock within the specified range. The device can also detect a loss of clock at this pin and when this is detected it sets the switching frequency to the internal oscillator. The two buck controllers operate at identical switching frequencies 180 degrees out of phase.

Enable Inputs

The buck controllers are enabled using independent enable inputs from the ENA and ENB pins. These are high voltage pins with a threshold of 1.5V for high level and can be connected directly to the battery for self-bias. The low threshold is 0.7V. Both these pins have internal pull-up currents of 0.5µA (typical). As a result, an open circuit on these pins enables the respective buck controllers. When both buck controllers are disabled, the device is shut down and consumes a current less than 4µA.

Feedback Inputs

The output voltage is set by choosing the right resistor feedback divider network connected to the FBx (feedback) pins. This is to be chosen such that the regulated voltage at the FBx pin equals 0.8V. The FBx pins have a 100nA pull up current source as a protection feature in case the pins open up as a result of physical damage.

Soft-Start Inputs

In order to avoid large inrush currents, both buck controllers have independent programmable soft-start timer. The voltage at the SSx pins acts as the soft-start reference voltage. A 1µA pull-up current is available at the SSx pins and by choosing a suitable capacitor a ramp of the desired soft-start speed can be generated. After start-up, the pull-up current ensures that this node is higher than the internal reference of 0.8V which then becomes the reference for the buck controllers. The soft-start ramp time is defined by:

$$C_{SS} = \frac{I_{SS} \times \Delta t}{\Delta V} \quad \text{(Farads)}$$

Equation 2 SoftStart Ramp Time

Where,

I_{SS} = 1µA (typical)

ΔV = 0.8V

C_{SS} is the required capacitor for Δt, the desired soft-start time.

Alternatively the soft-start pins can be used as tracking inputs. In this case, they should be connected to the supply to be tracked via a suitable resistor divider network.

Current Mode Operation

Peak current-mode control regulates the peak current through the inductor such that the output voltage is maintained to its set value. The error between the feedback voltage at FBx and the internal reference produces a signal at the output of the error amplifier (COMPx) which serves as target for the peak inductor current. The current through the inductor is sensed as a differential voltage at Sx1-Sx2 and compared with this target during each cycle. A fall or rise in load current produces a rise or fall in voltage at FBx causing COMPx to fall or rise respectively, thus increasing/decreasing the current through the inductor until the average current matches the load. In this way the output voltage is maintained in regulation.

The top N-channel MOSFET is turned on at the beginning of each clock cycle and kept on until the inductor current reaches its peak value. Once this MOSFET is turned off, and after a small delay (shoot-through delay) the lower N-channel MOSFET is turned on until the start of the next clock cycle. In dropout operation the high-side MOSFET stays on 100%. In every fourth clock cycle the duty cycle is limited to 95% in order to charge the bootstrap capacitor at CBx. This allows a maximum duty cycle of 98.75% for the buck regulators. During dropout the buck regulator switches at one-fourth of its normal frequency.

Current Sensing and Current Limit with Foldback

The maximum value of COMPx is clamped such that the maximum current through the inductor is limited to a specified value. When the output of the buck regulator (and hence the feedback value at FBx) falls to a low value due to a short circuit/over-current condition, the clamped voltage at the COMPx successively decreases, thus providing current fold back protection. This protects the high-side external MOSFET from excess current (forward direction current limit).

Similarly, if due to a fault condition the output is shorted to a high voltage and the low-side MOSFET turns fully on, the COMPx node will drop low. It is clamped on the lower end as well in order to limit the maximum current in the low-side MOSFET (reverse direction current limit).

The current through the inductor is sensed by an external resistor. The sense resistor should be chosen such that the maximum forward peak current in the inductor generates a voltage of 75mV across the sense pins. This value is specified at low duty cycles only. At typical duty cycle conditions around 40% (assuming 5V output and 12V input), 50mV is a more reasonable value, considering tolerances and mismatches. the typical characteristics provide a guide for using the correct current limit sense voltage.

The current sense pins Sx1 and Sx2 are high impedance pins with low leakage across the entire output range. This allows DCR current sensing using the DC resistance of the inductor for higher efficiency. DCR sensing is shown in the below figure. Here the series resistance (DCR) of the inductor is used as the sense element. The filter components should be placed close to the device for noise immunity. It should be remembered that while the DCR sensing gives high efficiency, it is inaccurate due to the temperature sensitivity and a wide variation of the parasitic inductor series resistance. Hence it may often be advantageous to use the more accurate sense resistor for current sensing.

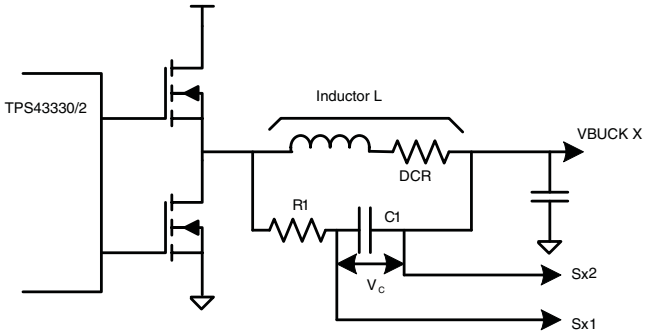


Figure 20. DCR Sensing Configuration

Slope Compensation

Optimal slope compensation which is adaptive to changes in input voltage and duty cycle allows stable operation at all conditions. For optimal performance of this circuit, the following condition must be satisfied in the choice of inductor and sense resistor:

$$\frac{L \times f_{SW}}{R_S} = 200$$

Equation 3 Inductor and Sense Resistor Choice

Where

L is the buck regulator inductor in Henry

R_S is the sense resistor in Ω

f_{sw} is the buck regulator switching frequency in Hz

Power Good Outputs and Filter Delays

Each buck controller has an independent power good comparator monitoring the feedback voltage at the FBx pins and indicating whether the output voltage has fallen below a specified power good threshold. this threshold has a typical value of 93% of the regulated output voltage. the power good indicator is available as an open drain output at the PGx pins. An internal 50kΩ pull-up resistor to Sx2 is available or an external resistor can be used. When a buck controller is shut down, the power good indicator is pulled down internally. Connecting the pull/up resistor to a rail other than the output of that particular buck channel will cause a constant current flow through the resistor when the buck controller is powered down.

In order to avoid triggering the power good indicators due to noise or fast transients on the output voltage, an internal delay circuit for de-glitching is used. Similarly, when the output voltage returns to its set value after a long negative transient, the power good indicator will be asserted high (the open-drain pin

released) after the same delay. This can be used to delay the reset to the circuits being powered from the buck regulator rail. The delay of this circuit can be programmed by using a suitable capacitor at the DLYAB pin according to the equation:

$$\frac{t_{DELAY}}{C_{DLYAB}} = \frac{1\ msec}{1\ nF}$$

Equation 4 Power Good Indicator Delay

When the DLYAB pin is open the delay is set to a default value of 20µsec typical. The power good delay timing is common to both the buck rails but the power good comparators and indicators function independently.

Light Load PFM Mode

An external clock or a high level on the SYNC pin results in forced continuous mode operation of the bucks. When the SYNC pin is low or open, the buck controllers will be allowed to operate in discontinuous mode at light loads by turning off the low-side MOSFET whenever a zero-crossing in the inductor current is detected.

In discontinuous mode, as the load decreases, the duration of the clock period when both the high-side as well the low-side MOSFET is turned off increases (deep discontinuous mode). In case the duration exceeds 60% of the clock period and VBAT > 8V, the buck controller switches to a low power operation mode. The design ensures that this typically occurs at 1% of the set full load current if the inductor and the sense resistor have been chosen appropriately as recommended in the slope compensation section.

In Low Power PFM Mode the buck monitors the FBx voltage and compares it with the 0.8V internal reference. Whenever the FBx value falls below the reference, the high-side MOSFET is turned on for a pulse-duration inversely proportional to the difference VIN-Sx2. At the end of this on-time, the high-side MOSFET is turned off and the current in the inductor decays until it becomes zero. The low-side MOSFET is not turned on. The next pulse occurs the next time FBx falls below the reference value. This results in a constant volt-second T_{on} hysteretic operation with a total device quiescent current consumption of 30µA when a single buck channel is active and 35µA when both channels are active.

As the load increases, the pulse become more and more frequent and move closer to each other until the current in the inductor becomes continuous. At this point, the buck controller returns to normal fixed frequency current mode control. Another criteria to exit the low power mode is when VIN falls low enough to require higher than 80% duty cycle of the high-side MOSFET.

The TPS43330/2 can support the full current load during low power mode until the transition to normal mode takes place. The design ensures the low power mode exit occurs at 10% (typical) of full load current if the inductor and sense resistor have been chosen as recommended. Moreover, there is always a hysteresis between the entry and exit thresholds to avoid oscillating between the two modes.

In the event that both buck controllers are active, low power mode is only possible when both buck controllers have light loads that are low enough for low power mode entry. When the boost controller is enabled, low power mode is possible only if VBAT is high enough to prevent the boost from switching and if DIV is open or set to GND. If DIV is high (VREG), low power mode is inhibited. .

Boost Controller

The boost controller has a fixed frequency voltage mode architecture and includes a cycle-by-cycle current limit protection for the external N-channel MOSFET. The switching frequency is derived from and set to one half of the buck controller switching frequency. The output voltage of the boost controller at the VIN pin is set by an internal resistor divider network and is programmable to 7V, 10V and 11V based on the low, open and high status respectively of the DIV pin. A change of the DIV-setting is not recognized, while the device is in low power mode.

The boost controller is enabled by the active-high ENC pin and is active when the input voltage at the VBAT pin has crossed the unlock threshold of 8.5V at least once. After that, the boost controller is armed and starts switching as soon as VIN falls below the value set by the DIV pin and regulates the VIN voltage. Thus, the boost regulator maintains a stable input voltage for the buck regulators during transient events such as cranking pulse at VBAT.

Whenever the voltage at the DS pin exceeds 200mV, the boost external MOSFET is turned off by pulling the CG1 pin low. By connecting the DS pin to the drain of the MOSFET or to a sense resistor between the MOSFET source and ground, cycle-by-cycle over-current protection for the MOSFET can be achieved. The on-resistance of the MOSFET or the value of the sense resistor has to be chosen in such a way that the on-state voltage at the DS does not exceed 200mV at the maximum load and minimum input voltage conditions. When sense resistor is used , a filter network is recommended to be connected between the DS pin and the sense resistor for better noise immunity.

The boost output (VIN) can also be used to supply other circuits in the system. However they should be high-voltage tolerant. The boost output is regulated to the programmed value only when VIN is low and so VIN can reach battery levels.

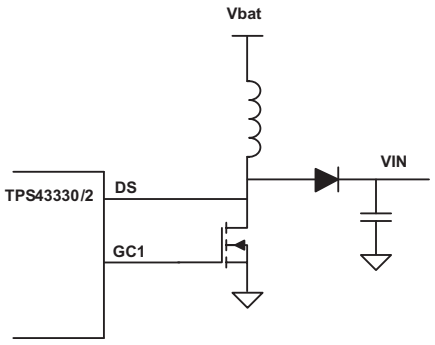


Figure 21. External Drain-Source Voltage Sensing

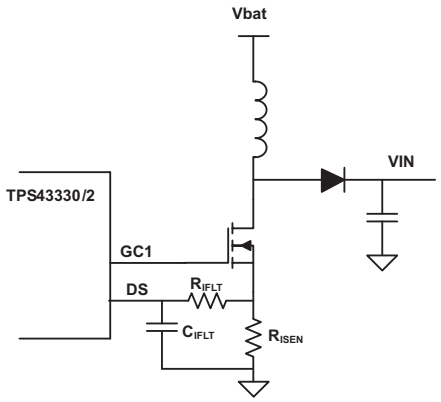


Figure 22. External Current Shunt Resistor

Frequency-Hopping Spread Spectrum (TPS43332 only)

The TPS43332 features a frequency-hopping pseudo-random spectrum spreading architecture. On this device, whenever the SYNC pin is high, the internal oscillator frequency is varied from one cycle to the next within a band of ±5% around the value programmed by the resistor at the RT pin. The implementation uses a linear feedback shift register that changes the frequency of the internal oscillator based on a digital code. The shift register is long enough to make the hops pseudo-random in nature and is designed in such a way that the frequency shifts only by one step at each cycle to avoid large jumps in the buck and boost switching frequencies.

Table 1. Frequency Hopping Control

Sync Terminal	Frequency Spread Spectrum (FSS)	Comments
External clock	Not active	Device in forced continuous mode, internal PLL locks into external clock between 150kHz and 600kHz.
Low or open	Not active	Device can enter discontinuous mode. Automatic LPM entry and Exit depending on load conditions
High	TPS43330: FSS not active	Device in forced continuous mode
	TPS43332: FSS active	

Table 2. Mode of Operation

ENABLE AND INHIBIT PINS				DRIVER STATUS		DEVICE STATUS	QUIESCENT CURRENT
ENA	ENB	ENC	SYNC	BUCK CONTROLLERS	BOOST CONTROLLER		
Low	Low	Low	X	Shutdown	disabled	Shutdown	~4 µA
Low	High	Low	Low	Buck B running	disabled	Buck B: LPM enabled	~30µA (light loads)
			High			Buck B: LPM inhibited	mA range
High	Low	Low	Low	Buck A running	disabled	Buck A: LPM enabled	~30µA (light loads)
			High			Buck A: LPM inhibited	mA range
High	High	Low	Low	Buck A&B running	disabled	Buck A/B: LPM enabled	~35µA (light loads)
			High			Buck A/B: LPM inhibited	mA range
Low	Low	Low	X	Shutdown	disabled	Shutdown	~4 µA
Low	High	High	Low	Buck B running	Boost running for VIN < set Boost Output	Buck B: LPM enabled	~50µA (no boost, light loads)
			High			Buck B: LPM inhibited	mA range
High	Low	High	Low	Buck A running	Boost running for VIN < set Boost Output	Buck A: LPM enabled	~50µA (no boost, light loads)
			High			Buck A: LPM inhibited	mA range
High	High	High	Low	Buck A&B running	Boost running for VIN < set Boost Output	Buck A/B: LPM enabled	~60µA (no boost, light loads)
			High			Buck A/B: LPM inhibited	mA range

Gate Driver Supply (VREG, EXTSUP)

The gate drivers of the buck and boost controllers are supplied from an internal linear regulator whose output (5.8V typical) is available at the VREG pin and should be decoupled using at least a 1µF ceramic capacitor. This pin has an internal current limit protection and should not be used to power any other circuits.

The VREG linear regulator is powered from VIN by default when the EXTSUP voltage is lower than 4.6V (typ.). In case VIN expected to go to high levels, there can be excessive power dissipation in this regulator, especially at high switching frequencies and when using large external MOSFET's. In this case, it is advantageous to power this regulator from the EXTSUP pin which can be connected to a supply lower than VIN but high enough to provide the gate drive. When EXTSUP is connected to a voltage greater than 4.6V, the linear regulator automatically switches to EXTSUP as its input to provide this advantage. Efficiency improvements are possible when one of the switching regulator rails from the TPS43330/2 or any other voltage available in the system is used to power the EXTSUP. The maximum voltage that should be applied to EXTSUP is 13V.

Using a large value for EXTSUP is advantageous as it provides a large gate drive and hence better on-resistance of the external MOSFET's. A 0.1µF ceramic capacitor is recommended for decoupling the EXTSUP pin when not being used.

During low power mode, the EXTSUP functionality is not available. The internal regulator operates as a shunt regulator powered from VIN and has a typical value of 7.5V. Current limit protection for VREG is available in low power mode as well.

External P-Channel Drive (GC2) and Reverse Battery Protection

The TPS43330/2 includes a gate driver for an external P-channel MOSFET which can be connected across the rectifier diode of the boost regulator. This is useful to reduce power losses when the boost controller is not switching. The gate driver provides a swing of 6V typical below the VIN voltage in order to drive a P-channel MOSFET. When VBAT falls below the boost enable threshold, the gate driver turns off the P-channel MOSFET and the diode is no longer bypassed.

The gate driver can also be used to bypass any additional protection diodes connected in series as shown in Figure 23. Figure 24 also shows a different scheme of reverse battery protection which may require only a smaller sized diode to protect the N-channel MOSFET as it conducts only for a part of the switching cycle. Since it is not always in series path, the system efficiency can be improved.

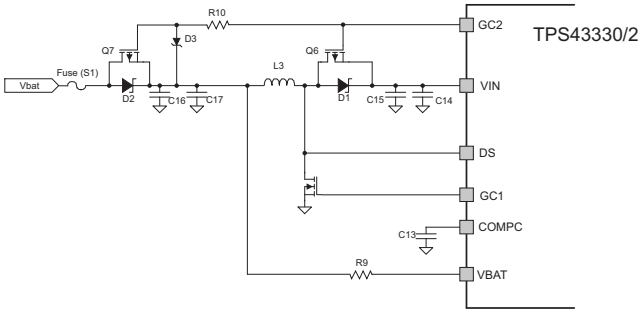


Figure 23. Reverse Battery Protection Option for Buck Boost Configuration

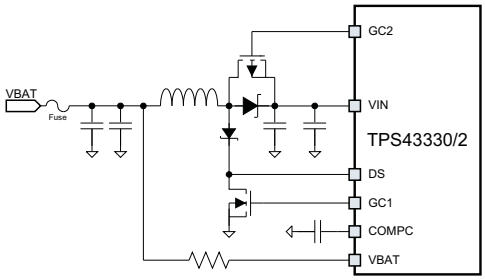


Figure 24. Reverse Battery Protection Option for Buck Boost Configuration

Undervoltage Lockout and Overvoltage Protection

The TPS43330/2 starts up at a VIN voltage of 6.5V (min). Once it has started up, the device operates down to a VIN voltage of 3.6V, below this voltage level the undervoltage lockout will disable the device. A voltage of 46V at VIN triggers the overvoltage comparator which shuts down the device. In order to prevent that transient spikes shutting down the device, the under and overvoltage protection have filter times of 5µs (typical).

When the voltages return to the normal operating region, the enabled switching regulators start including a new soft-start ramp for the buck regulators.

When the boost controller is enabled, a voltage less than 1.9V (typical) on VBAT triggers an undervoltage lockout and pulls the boost gate driver (GC1) low. As a result VIN will fall at a rate dependent on its capacitor and load, eventually triggering VIN undervoltage. A short falling transient at VBAT even lower than 2V can thus be survived, if VBAT returns to higher than 2.5V before VIN is discharged to the undervoltage threshold. This detection has a filter delay of 5µsec typical.

Thermal Protection

The TPS43330/2 protects itself from overheating using an internal thermal shutdown circuit. If the die temperature exceeds the thermal shutdown threshold of 165 degrees Celsius due to excessive power dissipation (e.g.: Due to fault conditions such as a short circuit at the gate drivers or VREG), the controllers are turned off and restarted when the temperature has fallen by 15 degrees.

APPLICATION INFORMATION

The following example illustrates the design process and component selection for the TPS43330. The design goal parameters are given in Table 3.

Table 3.

PARAMETER	VBUCK A	VBUCK B	BOOST
Input voltage	VIN 6 V to 30 V 12 V - typ	VIN 6 V to 30 V 12 V - typ	VBAT - 5 V (cranking pulse input) to 30V
Output voltage, V_O	5 V	3.3 V	10 V
Max - output current, I_O	3 A	2 A	2.5 A
Load step output tolerance, ΔV_O	±0.2 V	±0.12 V	±0.5 V
Current output load step, ΔI_O	0.1 A to 3 A	0.1 A to 2 A	0.1 A to 2.5 A
Converter switching frequency, f_{SW}	400 kHz	400 kHz	200 kHz

This is a starting point and theoretical representation of the values to be used for the application, further optimization of the components derived may be required to improve the performance of the device.

Boost Component Selection

A Boost converter operating in continuous conduction mode (CCM) has a right-half-plane (RHP) zero in its transfer function. The RHP zero is inversely related to the load current and inductor value and directly related to the input voltage. The RHP zero limits the maximum bandwidth achievable for the boost regulator. If the bandwidth is too close to the RHP zero frequency, the regulator may become unstable.

Thus, for high power systems with low input voltages, a low inductor value is chosen. This increases the amplitude of the ripple currents in the N-channel MOSFET, the inductor and the capacitors for the boost regulator. They must be designed with the ripple/RHP zero trade-off in mind and considering the power dissipation effects in the components due to parasitic series resistance.

A boost converter that operates in the discontinuous mode does not contain the RHP-zero in its transfer function. However, this needs an even lower inductor value and has high ripple currents. Also, it must be ensured that the regulator never enters the continuous conduction mode otherwise it may become unstable.

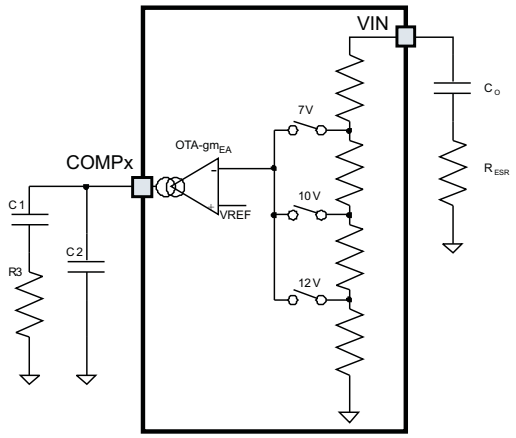


Figure 25. Boost Compensation Components

This design is done assuming continuous conduction mode. During light load conditions, the boost converter will operate in discontinuous mode without affecting stability. Hence the assumptions here cover the worst case for stability.

Boost Maximum Input Current I_{IN_MAX}

The maximum input current is drawn at the minimum input voltage and maximum load. the efficiency for VBAT = 5V at 2.5A is 80% based on the typical characteristics plot

$$P_{IN\ max} = \frac{P_{OUT}}{Efficiency} = \frac{25}{0.8} = 31.3\ W$$

Hence,

$$I_{IN\ max}\,(\text{at } V_{BAT} = 5\text{ V}) = \frac{31.3}{5} = 6.3\text{ A}$$

Boost Inductor Selection, L

Allow input ripple current of 40% of $I_{IN\ max}$ at V_{BAT} = 5 V

$$L = \frac{V_{BAT} * T_{ON}}{I_{IN\ max}} = \frac{V_{BAT}}{I_{IN\ max} * 2 * f_{SW}} = \frac{5V}{2.52A * 2 * 200kHz} = 4.9\ \mu H$$

Choose a lower value of 4 µH in order to ensure a high RHP-zero frequency while making a compromise that expects a high current ripple. Also, this can make the boost converter operate in discontinuous conduction mode where it is easier to compensate.

The inductor saturation current needs to be higher than the peak inductor current and some percentage higher than the maximum current limit value set by the external sensing resistive element.

This rating should be determined at the minimum input voltage, maximum output current and maximum core temperature for the application

Inductor Ripple Current, I_{RIPPLE}

Based on an Inductor value of 4 µH, the ripple current is approximately 3.1 A.

Peak Current in Low Side FET, I_{PEAK}

$$I_{PEAK} = I_{IN\ max} + \frac{I_{RIPPLE}}{2} = 6.3 + \frac{3.1}{2} = 7.85\ A$$

Based on this peak current value the external current sense resistor R_{SENSE} is calculated.

$$R_{SENSE} = \frac{0.2}{7.85} = 25m\Omega$$

Select 20 mΩ allowing for tolerance

The filter component values R_{IFLT} and C_{IFLT} for current sense are 1.5 kΩ and 1 nF respectively. This allows for good noise immunity.

Right Half Plane Zero RHP Frequency, f_{RHP}

$$f_{RHP} = \frac{V_{BAT\ min}}{2\pi * I_{IN\ max} * L} = 32kHz$$

Output Capacitor, C_O

To ensure stability, the output capacitor C_O is chosen such that

$$f_{LC} \le \frac{f_{RHP}}{10}$$

$$\frac{10}{2\pi * \sqrt{L * C_O}} \le \frac{V_{BAT\ min}}{2\pi * I_{IN\ max} * L}$$

$$C_O \ge \left(\frac{10 * I_{IN\ max}}{V_{BAT\ min}}\right)^2 * L = \left(\frac{10 * 6.8}{5}\right)^2 * 4\mu H$$

$$C_{O\ min} \ge 635\mu F$$

Select C_O = 660 µF.

This capacitor is usually aluminum electrolytic with ESR in the 10s of mΩ. This is good for loop stability since it provides a phase boost due to the ESR. The output filter components LC create a double pole (180 degree phase shift) at a frequency f_{LC} and the ESR of the output capacitor R_{ESR} creates a “zero“ for the modulator at frequency f_{ESR}. These frequencies can be determined by the following;

$$f_{ESR} = \frac{1}{2\pi * C_O * R_{ESR}}\ \text{Hz, assume } R_{ESR} = 40\ m\Omega$$

$$f_{ESR} = \frac{1}{2\pi * 660\mu F * 0.04}\ 6\ \text{kHz}$$

$$f_{LC} = \frac{1}{2\pi * \sqrt{L * C_O}} = \frac{1}{2\pi * \sqrt{4\mu H * 660\mu F}} = 3.1\ \text{kHz}$$

This satisfies $f_{LC} \le 0.1\ f_{RHP}$.

Bandwidth of Boost Converter, f_C

Use the following guidelines to set the frequency poles, zeroes and crossover values for trade off between stability and transient response:

$f_{LC} < f_{ESR} < f_C < f_{RHP\ Zero}$

$f_C < f_{RHP\ Zero} / 3$

$f_C < f_{SW} / 6$

$f_{LC} < f_C / 3$

Output Ripple Voltage Due to Load Transients, ΔV_O

$$\Delta Vo = R_{ESR} * \Delta Io + \frac{\Delta Io}{4 * Co * fc}$$

$$= 0.04 * 2.5 + \frac{2.5}{4 * 660\mu F * 8kHz} = 0.22V$$

Since the boost converter is active only during brief events such as a cranking pulse and the buck converters are high-voltage tolerant, a higher excursion on the boost output may be tolerable in some cases. In such cases, smaller component choices for the boost output may be used.

Selection of Components for Type II Compensation

The required loop gain for unity gain bandwidth (UGB) is

$$G = 40\log(\frac{f_c}{f_{LC}}) - 20\log(\frac{f_c}{f_{ESR}})$$

$$G = 40\log(\frac{8kHz}{3.1kHz}) - 20\log(\frac{8kHz}{3.1kHz}) = 14 \text{ dB}$$

The boost converter error amplifier (OTA) has a Gm that is proportional to the V_{BAT} voltage. This allows a constant loop response across the input voltage range and makes it easier to compensate by removing the dependency on V_{BAT}.

$$R3 = \frac{10^{\frac{G}{20}}}{85 * 10^{-6} * Vo} = 5.9k\Omega$$

$$C1 = \frac{10}{2\pi * fc * R3} = \frac{10}{2\pi * 8kHz * 5.9k\Omega} = 33nF$$

$$C2 = \frac{C1}{2\pi * R3 * C1 * (\frac{f_{SW}}{2}) - 1} = \frac{33nF}{2\pi * 5.9k\Omega * 33nF * (\frac{200kHz}{2}) - 1} = 265pF$$

Input Capacitor, C_I

The input ripple required is lower than 50 mV.

$$\Delta V_{C1} = \frac{I_{RIPPLE}}{8 * f_{SW} * C_1} = 10mV$$

$$\Delta V_{ESR} = I_{RIPPLE} * R_{ESR} = 40mV$$

Therefore our recommendation is 330µF with 10mOhm ESR.

Output Schottky Diode D1 Selection

A schottky diode with low forward conducting voltage V_F over temperature and fast switching characteristics is required to maximize efficiency. The reverse breakdown voltage should be higher than the maximum input voltage and the component should have low reverse leakage current. Additionally the peak forward current should be higher than the peak inductor current The power dissipation in the Schottky diode is given by :

$$P_D = I_{D(PEAK)} * V_F * (1 - D)$$

$$P_D = 7.85 * (1 - 0.53) = 2.2W$$

Since this is activated for low input voltage profile related to crank pulse the duration is less than 25ms

Low-Side MOSFET (BOT_SW3)

$$P_{BOOSTFET} = (I_{Pk})^2 * R_{DS(ON)}(1 + TC) * D + (\frac{V_I * I_{Pk}}{2}) * (t_r + t_f) * f_{sw}$$

$$P_{BOOSTFET} = (7.85)^2 * 0.02 * (1 + 0.4) * 0.53 + (\frac{V_I * I_{Pk}}{2}) * (20ns + 20ns) * 200KHz = 1.07W$$

The times t_r and t_f denote the rising and falling times of the switching node and are related to the gate driver strength of the TPS43330/2 and gate Miller capacitance of the MOSFET. The first term denotes the conduction losses which are minimized when the on-resistance of the MOSFET is low. The second term denotes the transition losses which arise due to the full application of the input voltage across the drain-source of the MOSFET as it turns on or off. They are higher at high output currents and low input voltages (due to the large input peak current) and when the switching time is low.

Note: The on resistance $R_{DS(ON)}$ has a positive temperature coefficient which produces the (TC=d*DeltaT) term that signifies the temperature dependence.(Temperature coefficient d is available as a normalized value from MOSFET data sheets and can be assumed to be 0.005/degrees Celsius as a starting value)

BUCKA Component Selection

Minimum ON Time, $t_{ON\ min}$

$$t_{ON\ min} = \frac{V_O}{V_{IN\ max} * f_{sw}} = \frac{5}{30 * 400kHz} = 416\,ns$$

This is higher than the min duty cycle specified (100 ns typ). Hence the minimum duty cycle is achievable at this frequency.

Current Sense Resistor R_{SENSE}

Based on the typical characteristics for V_{SENSE} limit with V_{IN} versus duty cycle, the sense limit is approximately 65 mV (at VIN = 12V and duty cycle of 5V/12V = 0.416). Allowing for tolerances and ripple currents choose V_{SENSE} max of 50mV.

$$R_{SENSE} = \frac{50mV}{3A} = 17m\Omega$$

Select 15 mΩ

Inductor Selection L

As explained in the description of the buck controllers, for optimal slope compensation and loop response, the inductor should be chosen such that:

$$L = K_{FLR} * \frac{R_{SENSE}}{fsw} = 200 * \frac{15m\Omega}{400kHz} = 7.5\mu H$$

K_{FLR} = Coil selection constant = 200

Choose a standard value of 8.2µH. For the buck converter, the inductor saturation currents and core should be chosen to sustain the maximum currents.

Inductor Ripple Current I_{RIPPLE}

At nominal input voltage of 12V, this gives a ripple current of 30% of $I_{O\ max}$ ≈ 1A.

Output Capacitor CO

Select an output capacitance C_O of 100µF with low ESR in the range of 10mΩ. This give $\Delta V_{O(Ripple)}$ ≈ 15mV and ΔV drop of ≈ 180 mV during a load step, which will not trigger the power good comparator and is within the required limits.

Bandwidth of Buck Converter f_C

Use the following guidelines to set frequency poles, zeroes and cross over values for trade off between stability and transient response

- Crossover frequency f_C between $f_{SW}/6$ and $f_{SW}/10$ Assume f_C = 50kHz
- Select the zero $f_z \approx f_C/10$
- Make the second pole $f_{P2} \approx f_{SW}/2$

Selection of Components for Type II Compensation

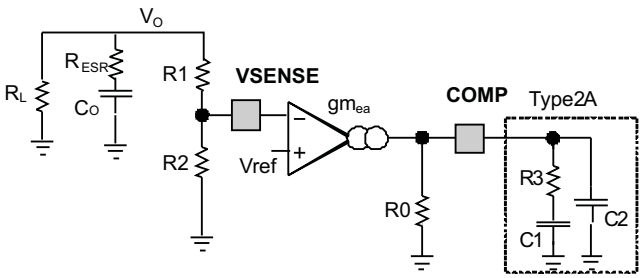


Figure 26. Buck Compensation Components

$$R3 = \frac{2\pi * f_C * V_O * C_O}{gm * K_{CFB} * V_{REF}} = \frac{2\pi * 50kHz * 5 * 100\mu F}{gm * K_{CFB} * V_{REF}} = 23.57k\Omega$$

Use standard value of R3 = 24 kΩ

Where; V_O = 5V, C_O = 100uF, gm = 1ms, V_{REF} = 0.8V

K_{CFB} = 0.125 / R_{SENSE} = 8.33 (0.125 is an internal constant)

$$C1 = \frac{10}{2\pi * R3 * f_C} = \frac{10}{2\pi * 24k\Omega * 50kHz} = 1.35nF$$

Use standard value of 1.5 nF

$$C2 = \frac{C1}{2\pi * R3 * C1(\frac{f_{SW}}{2}) - 1} = \frac{1.5nF}{2\pi * 24k\Omega * 1.5nF(\frac{400kHz}{2}) - 1} = 33pF$$

The resulting bandwidth of Buck Converter f_C

$$f_C = \frac{gm * R3 * K_{CFB}}{2\pi * C_O} * \frac{V_{REF}}{V_O} =$$

$$f_C = \frac{1ms * 24k\Omega * 8.33 * 0.8}{2\pi * 100\mu F * 5} = 50.9kHz$$

This is close to the target bandwidth of 50 kHz

The resulting zero frequency f_{Z1}

$$f_{Z1} = \frac{1}{2\pi * R3 * C1} = \frac{1}{2\pi * 24k\Omega * 1.5nF} = 4.42kHz$$

This is close to the $f_C/10$ guideline of 5 kHz

The second pole frequency f_{P2}

$$f_{P2} = \frac{1}{2\pi * R3 * C2} = \frac{1}{2\pi * 24k\Omega * 33pF} = 201kHz$$

This is close to the $f_{SW}/2$ guideline of 200 kHz. Hence all requirements for a good loop response are satisfied.

Resistor Divider Selection for setting V_O Voltage

$$\beta = \frac{V_{REF}}{V_O} = \frac{0.8}{5} = 0.16$$

Choose divider current through R1 and R2 to be 50 µA. Then

$$R1 + R2 = \frac{5V}{50\mu A} = 100k\Omega$$

And

$$\frac{R2}{R1 + R2} = 0.16$$

Therefore, R2 = 16 kΩ and R1 = 84 kΩ

BUCKB Component Selection

Using the same method as VBUCKA, the following parameters and components are realized

$$t_{ON\ min} = \frac{V_O}{V_{IN\ max} * f_{sw}} = \frac{5}{30 * 400kHz} = 416\,ns$$

This is higher than the min duty cycle specified (100 ns typ)

$$R_{SENSE} = \frac{60mV}{2A} = 30m\Omega$$

$$L = 200 * \frac{30m\Omega}{400kHz} = 15\mu H$$

ΔI_{ripple} current ≈ 0.4 A (approx.20% of $I_{O\ max}$)

Select an output capacitance C_O of 100µF with low ESR in the range of 10mΩ. This give ΔV_O (Ripple) ≈ 7.5mV and ΔV drop of ≈ 120 mV during a load step

Assume f_C = 50kHz

$$R3 = \frac{2\pi * f_C * V_O * C_O}{gm * K_{CFB} * V_{REF}}$$

$$= \frac{2\pi * 50kHz * 3.3 * 100\mu F}{1ms * 4.16 * 0.8} = 30k\Omega$$

Use standard value of R3 = 30kΩ

$$C1 = \frac{10}{2\pi * R3 * f_C} = \frac{10}{2\pi * 30k\Omega * 50kHz} = 1.2nF$$

$$C2 = \frac{C1}{2\pi * R3 * C1 * (\frac{f_{sw}}{2}) - 1}$$

$$= \frac{1.2nF}{2\pi * 30k\Omega * 1.2nF * (\frac{400kHz}{2}) - 1} = 33pF$$

$$f_C = \frac{gm * R3 * K_{CFB}}{2\pi * C_O} * \frac{V_{REF}}{V_O} =$$

$$f_C = \frac{1ms * 20k\Omega * 4.16 * 0.8}{2\pi * 100\mu F * 3.3} = 48kHz$$

This close to the target bandwidth of 50 kHz

The resulting zero frequency f_{Z1}

$$f_{Z1} = \frac{1}{2\pi * R3 * C1} = \frac{1}{2\pi * 30k\Omega * 1.2nF} = 4.4kHz$$

This close to the f_C guideline of 5kHz

The second pole frequency f_{P2}

$$f_{P2} = \frac{1}{2\pi * R3 * C2} = \frac{1}{2\pi * 30k\Omega * 33pF} = 160kHz$$

This close to the f_{SW}/2 guideline of 200 kHz

Hence all requirements for a good loop response are satisfied

Resistor Divider Selection for Setting V_O Voltage

$$\beta = \frac{V_{REF}}{V_O} = \frac{0.8}{3.3} = 0.242$$

Choose divider current through R1 and R2 to be 50 µA. Then

$$R1 + R2 = \frac{3.3V}{50\mu A} = 100k\Omega$$

And

$$\frac{R2}{R1 + R2} = 0.242$$

Therefore, R2 = 16 kΩ and R1 = 50 kΩ

BUCKX High-Side and Low-Side N-Channel MOSFETs

The gate drive supply for these MOSFET is supplied by an internal supply which is 5.8V typical under normal operating conditions. The output is a totem pole allowing full voltage drive of V_{REG} to the gate with peak output current of 1.2 A. The High-Side MOSFET is referenced to a floating node at the phase terminal (PHx) and the Low-Side MOSFET is referenced to power ground (PGx) terminal. For a particular applications these MOSFET's should be selected with consideration for the following parameters $R_{ds\ ON}$, gate charge Qg, drain to source breakdown voltage BVDSS, Maximum DC current IDC(max) and thermal resistance for the package.

The times t_r and t_f denote the rising and falling times of the switching node and are related to the gate driver strength of the TPS43330/2 and gate Miller capacitance of the MOSFET. The first term denotes the conduction losses which are minimized when the on-resistance of the MOSFET is low. The second term denotes the transition losses which arise due to the full application of the input voltage across the drain-source of the MOSFET as it turns on or off. They are lower at low currents and when the switching time is low.

$$P_{BuckTOPFET} =$$

$$(I_O)^2 * R_{DS(ON)}(1+TC) * D + (\frac{V_I * I_O}{2}) * (t_r + t_f) * f_{SW}$$

$$P_{buckLOWERFET} =$$

$$(I_O)^2 * R_{DS(ON)}(1+TC) * (1-D) + V_F * I_O * (2 * t_d) * f_{SW}$$

In addition, during the dead time t_d when both the MOSFETs are off, the body diode of the low-side MOSFET conducts, increasing the losses. This is denoted by the second term in the above equation. Using external Schottky diodes in parallel to the low-side MOSFETs of the buck converters helps to reduce this loss.

Note: The $R_{DS(ON)}$ has a positive temperature coefficient which is accounted for in the TC term for $R_{DS(ON)}$. TC = d * delta T[°C]. The temperature coefficient d is available as a normalized value from MOSFET data sheets and can be assumed to be 0.005/degrees Celsius as a starting value

Schematic

The following section summarize the previously calculated example and gives schematic + component proposals. Table 3.

Table 4. Application Example 1

PARAMETER	VBUCK A	VBUCK B	BOOST
Input voltage	VIN 6 V to 30 V 12 V - typ	VIN 6 V to 30 V 12 V - typ	VBAT - 5 V (cranking pulse input) to 30V
Output voltage, V_O	5 V	3.3 V	10 V
Max - output current, I_O	3 A	2 A	2.5 A
Load step output tolerance, ΔV_O	±0.2 V	±0.12 V	±0.5 V
Current output load step, ΔI_O	0.1 A to 3 A	0.1 A to 2 A	0.1 A to 2.5 A
Converter switching frequency, f_{SW}	400 kHz	400 kHz	200 kHz

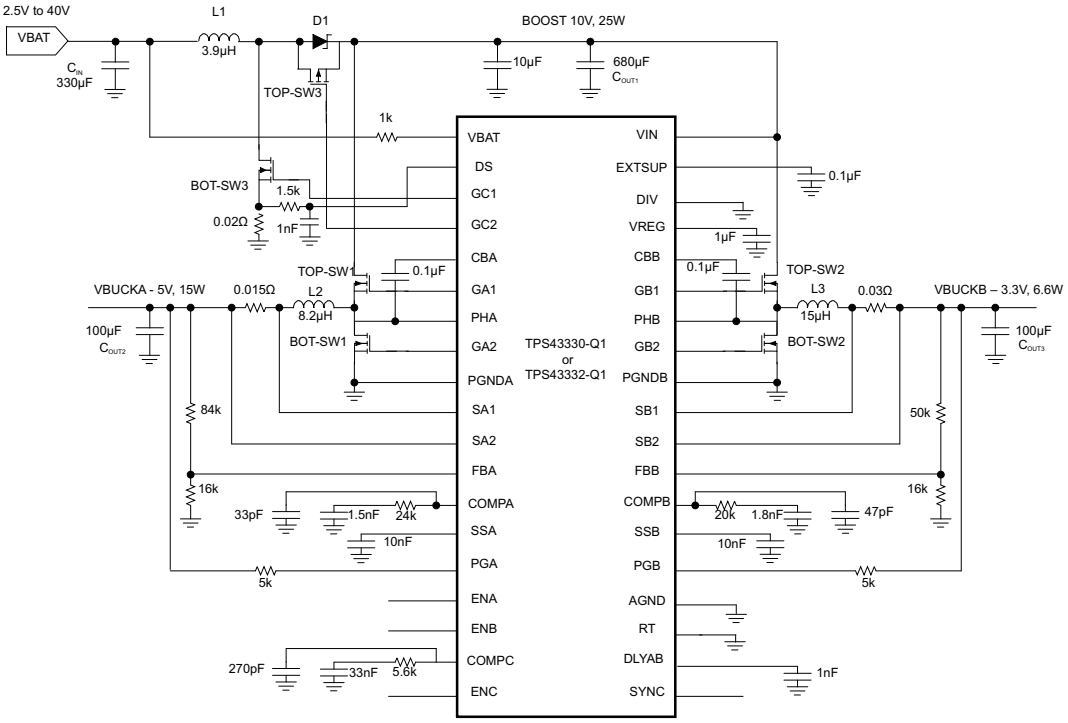


Table 5. Application Example 1 - Component Proposals

Name	Component Proposal	Value
L1	MSS1278T-392NL (Coilcraft)	4µH
L2	MSS1278T-822ML (Coilcraft)	8.2µH
L3	MSS1278T-153ML (Coilcraft)	15µH
D1	SK103 (Micro Commercial Components)	
TOP_SW3	IRF7416 (International Rectifier)	
TOP_SW1, TOP_SW2	Si4840DY-T1-E3 (Vishay)	
BOT_SW1, BOT_SW2	Si4840DY-T1-E3 (Vishay)	
BOT_SW3	IRFR3504ZTRPBF (International Rectifier)	
COUT1	EEVFK1J681M (Panasonic)	680µF
COUT2,3	ECASD91A107M010K00 (Murata)	100µF
CIN	EEEFK1V331P (Panasonic)	330µF

Table 6. Application Example 2

PARAMETER	VBUCK A	VBUCK B	BOOST
Input voltage	VIN 5 V to 30 V 12 V - typ	VIN 6 V to 30 V 12 V - typ	VBAT - 5 V (cranking pulse input) to 30V
Output voltage, V_O	5 V	3.3 V	10 V
Max - output current, I_O	2.7 A	5 A	3 A
Load step output tolerance, ΔV_O	±0.2 V	±0.12 V	±0.5 V
Current output load step, ΔI_O	0.1 A to 2.7 A	0.1 A to 5 A	0.1 A to 3 A
Converter switching frequency, f_{SW}	300 kHz	300 kHz	150 kHz

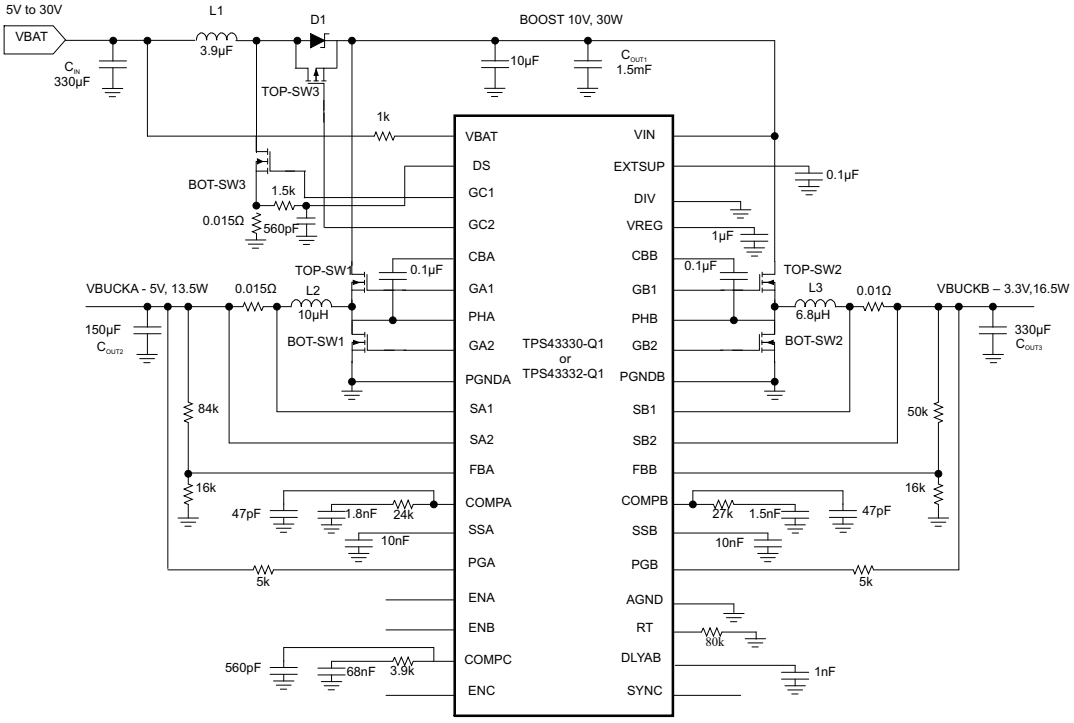


Table 7. Application Example 2 - Component Proposals

Name	Component Proposal	Value
L1	MSS1278T-392NL (Coilcraft)	3.9µH
L2	MSS1278T-103ML (Coilcraft)	10µH
L3	MSS1278T-682ML (Coilcraft)	6.8µH
D1	SK103 (Micro Commercial Components)	
TOP_SW3	IRF7416 (International Rectifier)	
TOP_SW1, TOP_SW2	Si4840DY-T1-E3 (Vishay)	
BOT_SW1, BOT_SW2	Si4840DY-T1-E3 (Vishay)	
BOT_SW3	IRFR3504ZTRPBF (International Rectifier)	
COUT1	EEVFK1V152M (Panasonic)	1.5mF
COUT2	ECASD91A157M010K00 (Murata)	150µF
COUT3	ECASD90G337M008K00 (Murata)	330µF
CIN	EEEFK1V331P (Panasonic)	330µF

Table 8. Application Example 3

PARAMETER	VBUCK A	VBUCK B	BOOST
Input voltage	VIN 5 V to 30 V 12 V - typ	VIN 6 V to 30 V 12 V - typ	VBAT - 5 V (cranking pulse input) to 30V
Output voltage, V_O	5 V	2.5 V	10 V
Max - output current, I_O	3 A	1 A	2 A
Load step output tolerance, ΔV_O	±0.2 V	±0.12 V	±0.5 V
Current output load step, ΔI_O	0.1 A to 3 A	0.1 A to 1 A	0.1 A to 2 A
Converter switching frequency, f_{SW}	400 kHz	400 kHz	200 kHz

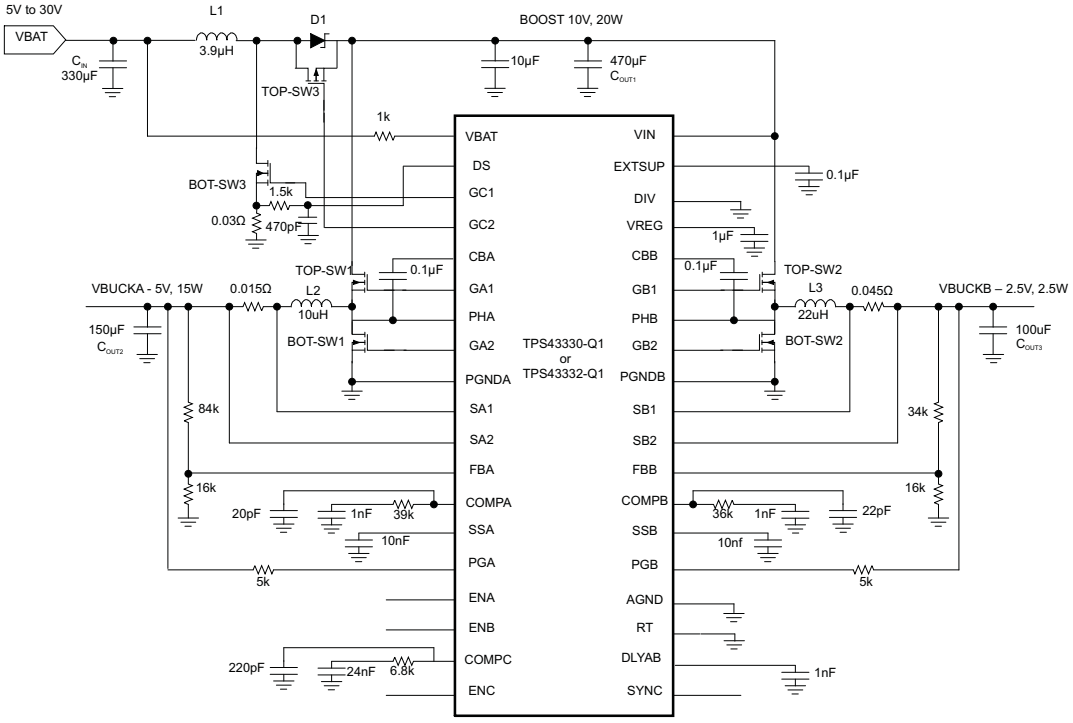


Table 9. Application Example 3 - Component Proposals

Name	Component Proposal	Value
L1	MSS1278T-392NL (Coilcraft)	3.9µH
L2	MSS1278T-822ML (Coilcraft)	8.2µH
L3	MSS1278T-223ML (Coilcraft)	22µH
D1	SK103 (Micro Commercial Components)	
TOP_SW3	IRF7416 (International Rectifier)	
TOP_SW1, TOP_SW2	Si4840DY-T1-E3 (Vishay)	
BOT_SW1, BOT_SW2	Si4840DY-T1-E3 (Vishay)	
BOT_SW3	IRFR3504ZTRPBF (International Rectifier)	
COUT1	EEVFK1V471Q (Panasonic)	470µF
COUT2	ECASD91A157M010K00 (Murata)	150µF
COUT3	ECASD40J107M015K00 (Murata)	100µF
CIN	EEEFK1V331P (Panasonic)	330µF

Power Dissipation De-Rate Profile 32 pin HTTSOP package with power PAD

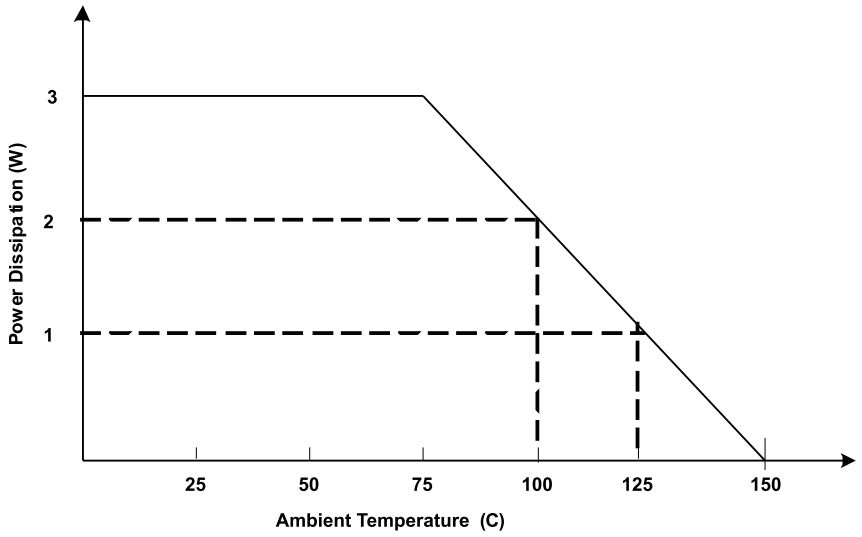


Figure 27. Power dissipation de rating profile based on high K Jedec PCB

PCB Layout Guidelines

Grounding and PCB Circuit Layout Considerations

Boost converter

1. The path formed from the input capacitor to the inductor and BOT_SW3 with low side current sense resistor should have short leads and PC trace lengths. The same applies for the trace from the inductor to the Schottky Diode D1 to the COUT1 capacitors. The negative terminal of the input capacitor and the negative terminal of the sense resistor be connected together with short trace lengths.
2. The over current sensing shunt resistor may require noise filtering and this capacitor should be close to the IC pin.

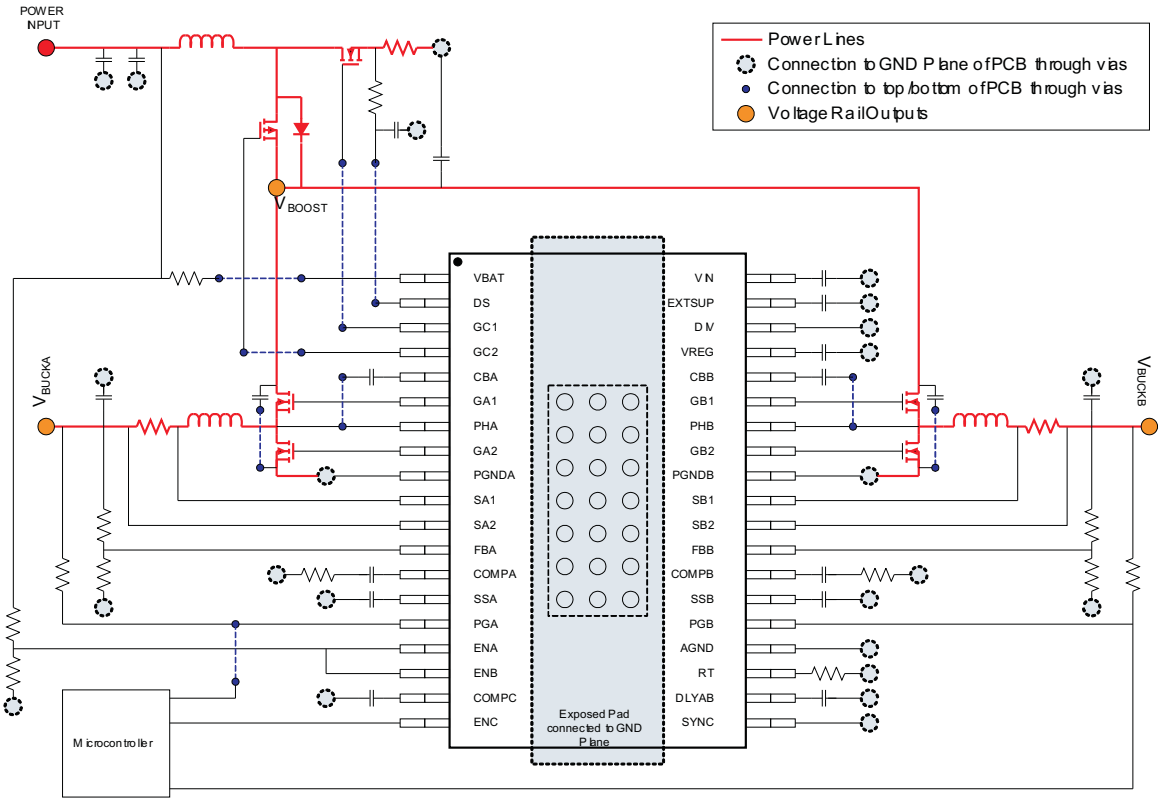
Buck Converter

1. Connect the drain of TOP_SW1 and TOP_SW2 together with positive terminal of the input capacitor COUT1. The trace length between these terminals should be short.
2. Connect a local decoupling capacitor between Drain of TOP_SWx and Source of BOT_SWx.
3. The Kelvin current sensing for the shunt resistor should have minimum trace spacing and routed together. Any filtering capacitors for noise should be placed near the IC pins.
4. The resistor divider for sensing output voltage is connected between the positive terminal of the respective output capacitor and COUT2 or COUT3 and the IC signal ground. These components and the traces should not be routed near any switching nodes or high current traces.

Other Considerations

1. PGNDx and AGND should be shorted to thermal pad. Use a star ground configuration if connecting to non ground plane system. Use tie-ins for EXTSUP capacitor, compensation network ground and voltage sense feedback ground networks to this start ground.
2. Connect compensation network between compensation pins and IC signal ground. Connect the oscillator resistor (frequency setting) between the RT pin and IC signal ground. These sensitive circuits should NOT be located near the dv/dt nodes; these include the gate drive outputs, phase pins and boost circuits (bootstrap).
3. Reduce the surface area of the high current carrying loops to a minimum, by ensuring optimal component placement. Ensure the bypass capacitors are located as close as possible to their respective power and ground pins.

PCB Layout


POWER INPUT
Power Lines
Connection to GND Plane of PCB through vias
Connection to top/bottom of PCB through vias
Voltage Rail Outputs
VBOOST
VBUCKA
VBUCKB
VBAT
DS
GC1
GC2
CBA
GA1
PHA
GA2
PGNDA
SA1
SA2
FBA
COMPA
SSA
PGA
ENA
ENB
COMPC
ENC
VIN
EXTSUP
DIV
VREG
CBB
GB1
PHB
GB2
PGNDB
SB1
SB2
FBB
COMPB
SSB
PGB
AGND
RT
DLYAB
SYNC
Exposed Pad connected to GND Plane
Microcontroller

PACKAGING INFORMATION

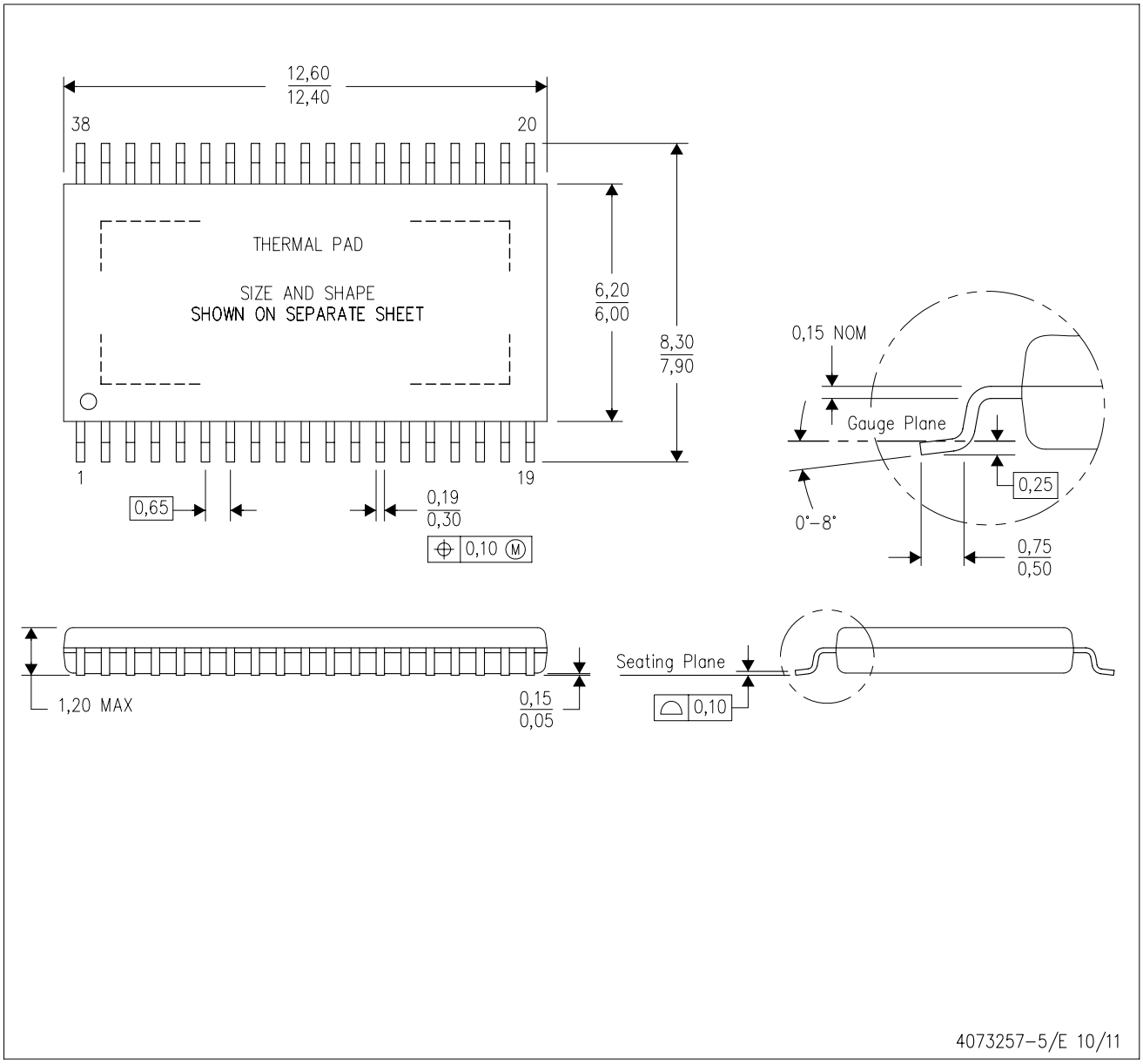
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS43330QDAPRQ1	ACTIVE	HTSSOP	DAP	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS43332QDAPRQ1	ACTIVE	HTSSOP	DAP	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DAP (R–PDSO–G38) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153 Variation DDT–1.

PowerPAD is a trademark of Texas Instruments.

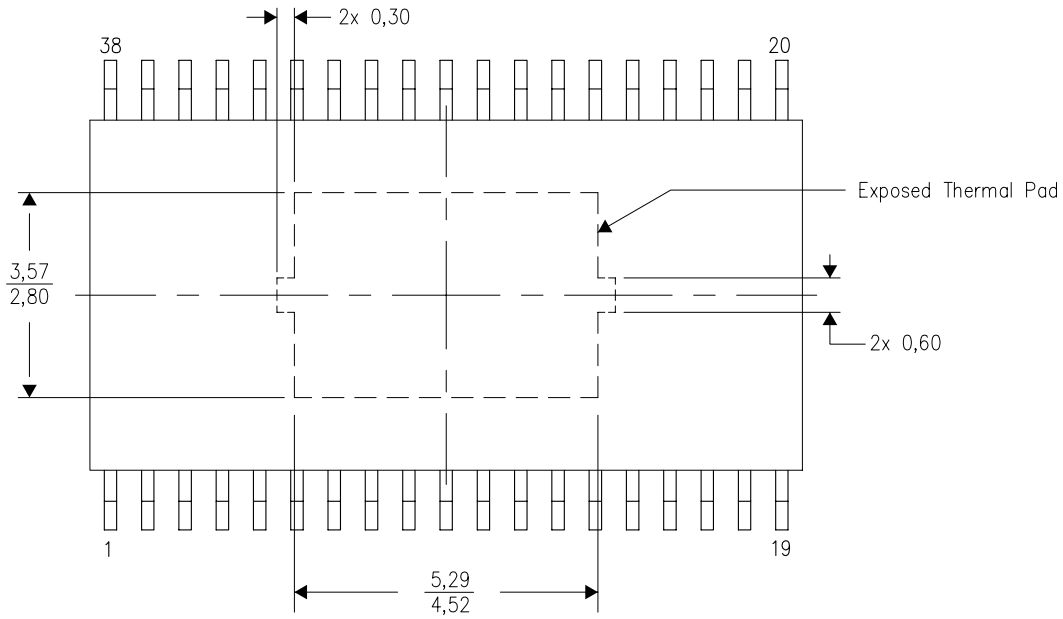
DAP (R–PDSO–G38) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206319–9/J 02/12

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Insrtuments.

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