

TLP716

Plasma display panel.
High Speed Interface.
Factory Automation .

The TOSHIBA TLP716 consists of a GaAlAs light emitting diode and a high speed photodetector. This unit is 6-lead SDIP. TLP716 is 50% smaller than 8PIN DIP and has suited the safety standard reinforced insulation class. So, mounting area in safety standard required equipment can be reduced.

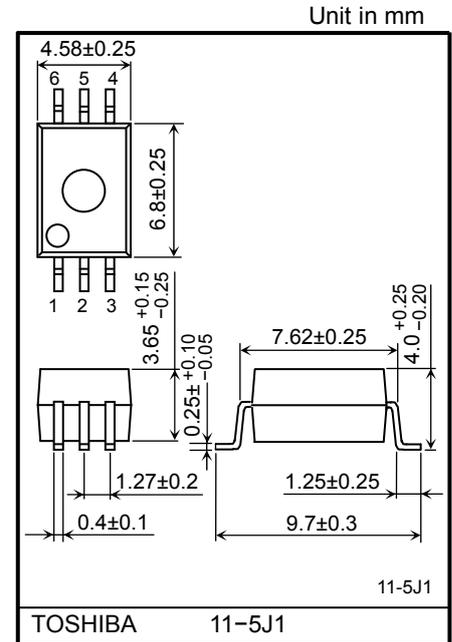
- Inverter Logic (totempole output)
- Package Type : SDIP6
- Guaranteed Performance Over Temperature : -40~100°C
- Power Supply Voltage : 4.5~5.5 V
- Input Thresholds Current : IFHL=6.5 mA(max.)
- Propagation delay Time (tpHL/ tpLH) : 75 ns(max.)
- Switching speed : 15 MBd(typ.) (NRZ)
- Common mode transient immunity : 10 kV/us(min.)
- Isolation voltage : 5000 Vrms(min.)
- UL Recognized :UL1577, File No.E67349
- Option (D4)
 TÜV Approved : EN60747-5-2
 Maximum Operating Insulation Voltage : 890 V_{PK}
 Highest Permissible Over Voltage : 8000 V_{PK}
(Note):When a EN60747-5-2 approved type is needed, Please designate "Option(D4)"

- Construction Mechanical Rating

	7.62 mm pitch standard type	10.16 mm pitch TLPXXXXF type
Creepage Distance	7.0 mm (min)	8.0 mm (min)
Clearance	7.0 mm (min)	8.0 mm (min)
Insulation Thickness	0.4 mm (min)	0.4 mm (min)

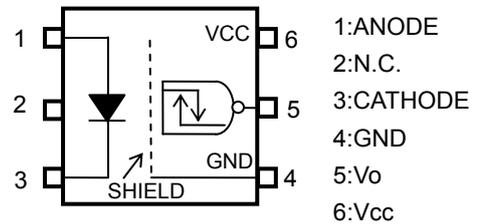
Truth Table

Input	LED	Tr1	Tr2	Output
H	ON	OFF	ON	L
L	OFF	ON	OFF	H

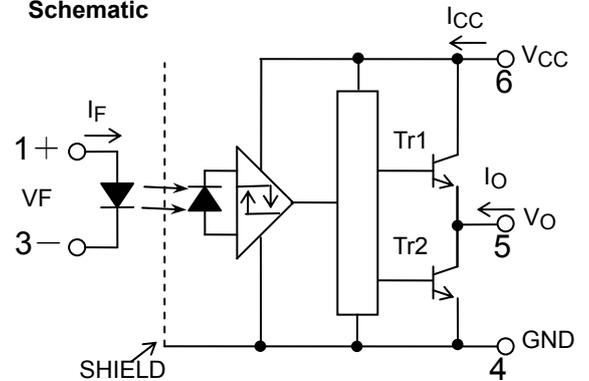


Weight : 0.26 g (typ.)

Pin Configuration (Top View)



Schematic



0.1 μF bypass capacitor must be connected between pins 6 and 4. (Note 4)

Absolute Maximum Ratings (Ta=25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current (Ta ≤ 85°C)	IF	20	mA
	Forward Current Derating (Ta > 85°C)	ΔIF/ΔTa	-0.5	mA/°C
	Peak Transient Forward Current (Note1)	IFPT	1	A
	Reverse Voltage	VR	5	V
	Junction Temperature	Tj	125	°C
DETECTOR	Output Current (Ta ≤ 85°C)	IO	10	mA
	Output Current Derating (Ta > 85°C)	ΔIO /ΔTa	-0.25	mA/°C
	Output Voltage (Vo ≤ Vcc)	VO	-0.5~6	V
	Supply Voltage	VCC	-0.5~6	V
	Power Dissipation (Ta ≤ 85°C)	PD	40	mW
	Power Dissipation Derating (Ta > 85°C)	ΔPo/ΔTa	-1	mW/°C
	Junction Temperature	Tj	125	°C
Operating Temperature Range		Topr	-40~100	°C
Storage Temperature Range		Tstg	-55~125	°C
Lead Solder Temperature(10s)		Tsol	260	°C
Isolation Voltage (AC, 1min., R.H. ≤ 60%, Ta=25°C) (Note2)		BVs	5000	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Current , ON	IF(ON)	8	12	18	mA
Input Voltage , OFF	VF(OFF)	0	—	0.8	V
Supply Voltage (*) (Note3, Note4)	VCC	4.5	5	5.5	V

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

(*) This item denotes operating ranges, not meaning of recommended operating conditions.

The correlation between input current and switching speed and drive circuit (reference information).

Input Current (IF)	TEST CIRCUIT	Typical Switching Speed
12mA	1 (Page 4)	14 – 16 MBd
8mA	1 (Page 4)	11 – 13 MBd
8mA	2 (Page 4, with Speed up capacitor)	16 – 20 MBd

Note 1: Pulse width $PW \leq 1 \mu s, 300 \text{ pps}$.

Note 2: Device Considered a two terminal device : pins 1,2 and 3 shorted together and pins 4,5 and 6 shorted together.

Note 3: The detector of this product requires a power supply voltage (VCC) of 4.5 V or higher for stable operation. If the VCC is lower than this value, an Icc may increase, or an output may be unstable. Be sure to use the product after checking the supply current, and the operation of a power-on/-off.

Note 4: A ceramic capacitor(0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

Electrical Characteristics

(Unless otherwise specified, $T_a = -40$ to $100^\circ C, V_{CC} = 4.5 \sim 5.5V$)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP. *	MAX.	UNIT
Input Forward Voltage	VF	IF=10mA, $T_a = 25^\circ C$	—	1.65	1.8	V
Temperature Coefficient of Forward Voltage	$\Delta VF / \Delta T_a$	IF=10mA	—	-2.0	—	mV/ $^\circ C$
Input Reverse Current	IR	VR=5V, $T_a = 25^\circ C$	—	—	10	μA
Input Capacitance	CT	V=0V, f=1MHz, $T_a = 25^\circ C$	—	45	—	pF
Logic Low Output Voltage	VOL	IOL=1.6mA, IF=12mA, VCC=5V	—	—	0.4	V
Logic High Output Voltage	VOH	IOH=-0.02mA, VF=1.05V, VCC=5V	4.0	—	—	V
Logic Low Supply Current	ICCL	IF=12mA	—	—	5.0	mA
Logic High Supply Current	ICCH	VF=0V	—	—	5.0	mA
Input Current Logic Low Output	IFHL	IO=1.6mA, VO<0.4V	—	—	6.5	mA
Input Voltage Logic High Output	VFLH	IO=-0.02mA, VO>4.0V	0.8	—	—	V

*All typical values are at $T_a = 25^\circ C, V_{CC} = 5V, I_{F(ON)} = 12mA$ unless otherwise specified

Isolation Characteristics ($T_a = 25^\circ C$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Capacitance input to output	C_S	$V_S = 0V, f = 1MHz$ (Note 2)	—	0.8	—	pF
Isolation resistance	R_S	R.H. $\leq 60\%, V_S = 500V$ (Note 2)	1×10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	AC, 1 minute	5000	—	—	V_{rms}
		AC, 1 second, in oil	—	10000	—	Vdc
		DC, 1 minute, in oil	—	10000	—	

Switching Characteristics

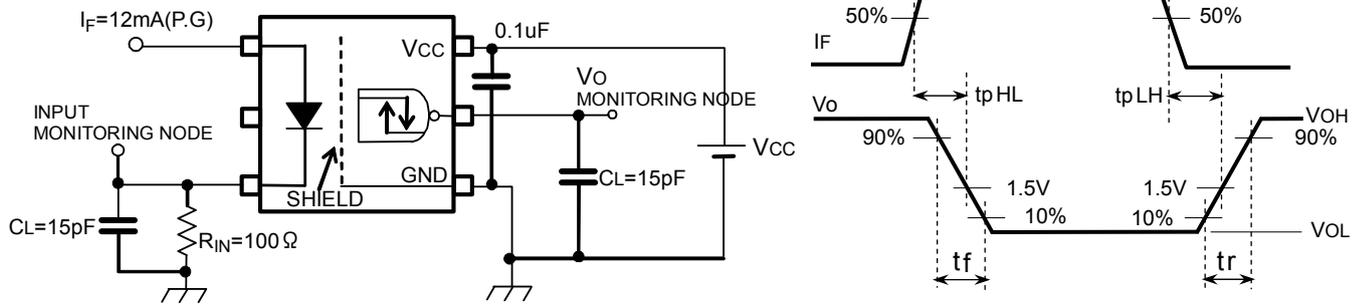
(Unless otherwise specified, $T_a = -40$ to 100°C , $V_{CC} = 4.5 \sim 5.5\text{V}$)

CHARACTERISTIC	SYMBOL	TEST -CIRCUIT	CONDITION		MIN.	TYP.	MAX.	UNIT
propagation Delay Time to Logic Low output	tpHL	1	IF=0→12mA	RIN=100Ω	—	—	75	ns
propagation Delay Time to Logic High output	tpLH		IF=12→0mA	CL=15pF (Note 5)	—	—	75	ns
propagation Delay Time to Logic Low output	tpHL	2	VIN=0→5V (IF=0→8mA)	RIN=430Ω	—	—	65	ns
propagation Delay Time to Logic High output	tpLH		VIN=5→0V (IF=8→0mA)	CIN=33pF CL=15pF (Note 5)	—	—	65	ns
Switching Time Dispersion between ON and OFF	tpLH-tpHL	1	IF=12mA RIN=100Ω, CL=15pF (Note 5)		—	—	45	ns
Output Fall Time (90 ~ 10%)	tf		IF=0→12mA	RIN=100Ω	—	15	—	ns
Output Rise Time (10 ~ 90%)	tr		IF=12→0mA	CL=15pF (Note 5)	—	15	—	ns
Common Mode transient Immunity at High Level Output	CMH	3	VCM=1000Vp-p, IF=0mA, VO(Min)=4V, Ta=25°C		10000	—	—	V/us
Common Mode transient Immunity at Low Level Output	CML		VCM=1000Vp-p, IF=12mA, VO(Max)=0.4V, Ta=25°C		-10000	—	—	V/us

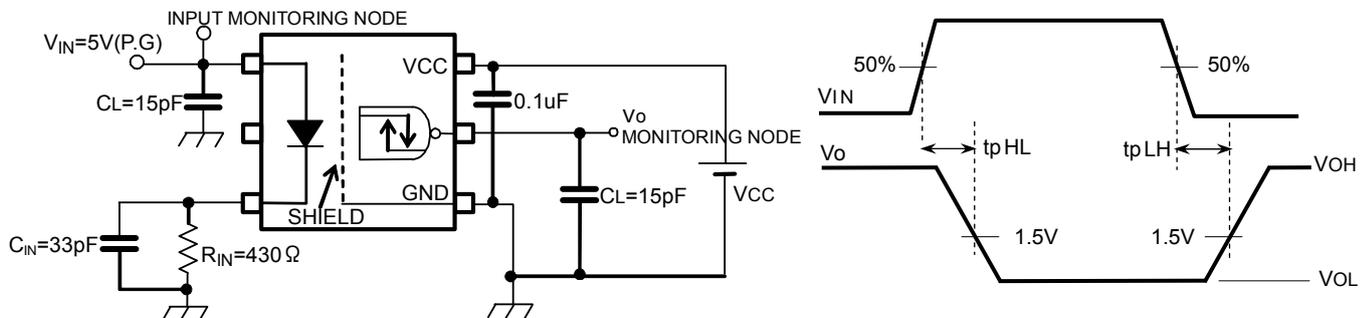
*All typical values are at $T_a = 25^\circ\text{C}$

Note 5: CL is approximately 15pF which includes probe and Jig/stray wiring capacitance.

TEST CIRCUIT 1 : tpLH , tpHL



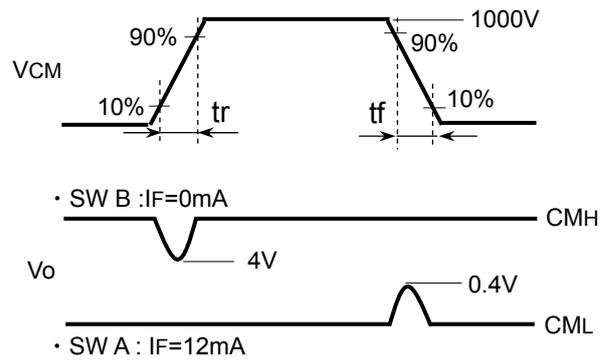
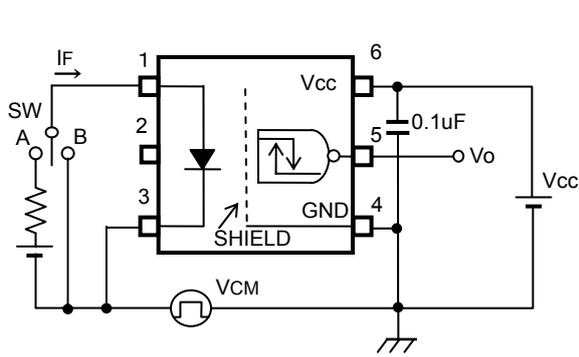
TEST CIRCUIT 2 : tpLH , tpHL



The PROBE and JIG capacitances are included in CL.

(P.G) : Pulse Generator

TEST CIRCUIT 3 : Common-Mode Transient Immunity Test Circuit



$$CMH = \frac{800(V)}{tr(\mu s)} \quad CML = -\frac{800(V)}{tf(\mu s)}$$

CM_L (CM_H) is the maximum rate of fall (rise) of the common mode voltage that can be sustained with the output voltage in the low (high) state.

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20070701-EN

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