TOSHIBA

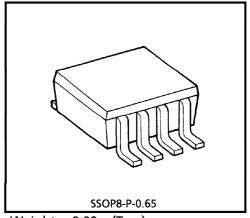
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T C 7 W 1 2 5 F U

DUAL BUS BUFFER

The TC7W125FU is a high speed C²MOS DUAL BUS BUFFERS fabricated with silicon gate C²MOS technology. It achieve the high speed operation similar to equivalent LSTTL while maintaining the C²MOS low power dissipation.

The require 3-state control input \overline{G} to be set high to place the output into the high impedance. All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Weight: 0.02g (Typ.)

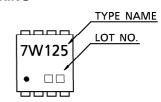
FEATURES

- High Speed $\cdots t_{pd} = 10$ ns (Typ.) at $V_{CC} = 5V$
- Low Power Dissipation $\cdots I_{CC} = 2\mu A$ (Max.) at $Ta = 25^{\circ}C$
- High Noise Immunity········· V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- Output Drive Capability 15 LSTTL Loads
- Symmetrical Output Impedance $\cdots \cdot |I_{OH}| = I_{OL} = 6mA$ (Min.)
- Balanced Propagation Delays $\cdots \cdots t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range ····· V_{CC} (opr) = 2∼6V

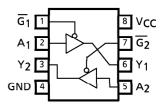
MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V _{CC}	- 0.5~7	V
DC Input Voltage	V _{IN}	-0.5~V _{CC} +0.5	V
DC Output Voltage	Vout	-0.5~V _{CC} +0.5	\ \
Input Diode Current	ΙΚ	± 20	mA
Output Diode Current	loк	± 20	mA
DC Output Current	IOUT	±35	mA
DC V _{CC} /Ground Current	lcc	± 37.5	mA
Power Dissipation	PD	300	mW
Storage Temperature	T _{stg}	-65∼150	°C
Lead Temperature (10s)	TL	260	°C

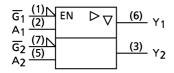
MARKING



PIN ASSIGNMENT (TOP VIEW)



LOGIC DIAGRAM



TRUTH TABLE

INP	UTS	OUTPUTS
G	Α	Υ
Н	Х	Z
L	┙	L
L	Н	Н

X : Don't Care Z : High Impedance

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	Vcc	2~6	V
Input Voltage	V _{IN}	0~V _{CC}	٧
Output Voltage	Vout	0~V _{CC}	٧
Operating Temperature	T _{opr}	-40~85	°C
		$0 \sim 1000 \text{ (V}_{CC} = 2.0\text{V)}$	
Input Rise and Fall Time	t _r , t _f	$0 \sim 500 \ (V_{CC} = 4.5V)$	ns
		$0 \sim 400 \ (V_{CC} = 6.0V)$	

DC ELECTRICAL CHARACTERISTICS

DADAMETED	TEST		TEST COMPITION		Ta = 25°C			Ta = −40~85°C			
PARAMETER SYMBOL		CIR- TEST CONDITION [Vcc	MIN.	TYP.	MAX.	MIN.	MAX.	UNIT	
High-Level Input					2.0	1.5	_	_	1.5	_	
Voltage	V _{IH}	—		_	4.5	3.15	—	_	3.15	—	V
					6.0	4.2			4.2		
Low-Level Input			_		2.0		_	0.5	—	0.5	
Voltage	VIL	-			4.5		—	1.35	—	1.35	V
				Γ	6.0			1.8		1.8	
			V _{IN} = V _{IH} or V _{IL}		2.0	1.9	2.0	<u> </u>	1.9	—	
High-Level				$I_{OH} = -20\mu A$	4.5	4.4	4.5	<u> </u>	4.4	—	
Output Voltage	Voн	_			6.0	5.9	6.0	_	5.9		V
Cutput Voltage				$I_{OH} = -6mA$	4.5	4.18	4.31	_	4.13	—	
				$I_{OH} = -7.8 mA$	6.0	5.68	5.80	_	5.63	_	
			V _{IN} = V _{IL}	 I _{OL} = 20μΑ	2.0	_	0.0	0.1	—	0.1	
Low-Level					4.5		0.0	0.1	—	0.1	
	VOL	l —			6.0	_	0.0	0.1	—	0.1	V
Output Voltage				I _{OL} = 6mA	4.5	_	0.17	0.26	_	0.33	
				I _{OL} = 7.8mA	6.0	_	0.18	0.26	—	0.33	
3-State Output Off-State Current	loz	_	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		6.0	_	_	±0.5	_	± 5.0	
Input Leakage Current	IN	_	V _{IN} = V _{CC} or GND		6.0	_	_	±0.1	_	± 1.0	μ A
Quiescent Supply Current	lcc	_	V _{IN} = V _{CC} or GND		6.0	_	_	2.0	_	20.0	

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6ns$)

	CVMDOL	TEST CIR- CUIT	TEST			Ta = 25°C			Ta = − 40~85°C		
PARAMETER SYI	SYMBOL		CONDITION	CL	Vcc	MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
Output Transition t					2.0	_	20	60	_	75	
Output Transition Time	t _{TLH}	_	_	50	4.5		6	12	_	15	
Tillie	^t THL				6.0	_	5	10	_	13	
					2.0		30	90	_	115	
				50	4.5	<u> </u>	11	18	—	23	
Propagation	^t PLH		_		6.0	_	10	15	_	20	
Delay Time	^t pHL		_		2.0		42	130	_	165	
				150	4.5	_	14	26	—	33	
					6.0	_	12	22	_	28	ns
			— R _L = 1kΩ	50	2.0		30	90	_	115	113
Output Enable t _{pZL} Time t _{pZH}					4.5	_	11	18	 	23	
	^t pZL				6.0		10	15	_	20	
	^t pZH			150	2.0	_	42	130	_	165	
					4.5	_	14	26	_	33	
					6.0	_	12	22	_	28	
Output Disable	+		$ R_L = 1k\Omega$	50	2.0		24	100	_	125	
1	^t pLZ	_			4.5	_	12	20	 —	25	
	^t pHZ				6.0	_	10	17	_	21	
Input Capacitance	c_IN	-	_	-	_		5	10	_	10	
Output Capacitance	C _{OUT}	l	_		_	_	10	_	_	_	pF
Power Dissipation Capacitance	C _{PD}	_	Note (1)			_	32	_		_	

Note (1): CpD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

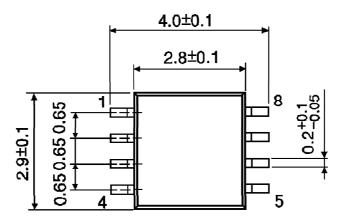
Average operating current can be obtained by the equation:

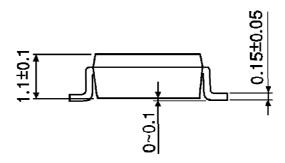
ICC (opr) = CpD·VCC·fIN + ICC / 2 (per Gate)

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PACKAGE DIMENSIONS

SSOP8-P-0.65 Unit: mm





Weight: 0.02g (Typ.)

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000707EBA

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