TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHC165F, TC74VHC165FN, TC74VHC165FS, TC74VHC165FT

8 - BIT SHIFT REGISTER (P - IN, S - OUT)

The TC74VHC165 is an advanced high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8 - bit shift register with a gated clock input. When the SHIFT/ $\overline{\text{LOAD}}$ input is held high, the serial data input is enabled and the eight frip-frops perform serial shifting with each clock pulse.

When the SHIFT/LOAD input is held low, the parallel data is loaded synchronously into the register at positive going transition of the clock pulse.

The CK-INH input should be shifted high only when the CK input is held high.

An Input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES :

- High Speed $\cdots f_{MAX} = 150 MHz(typ.)$ at $V_{CC} = 5V$
- Low Power Dissipation $\dots I_{CC} = 4\mu A(Max.)$ at Ta = 25°C
- High Noise Immunity $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$ (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays.... $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range V_{CC} (opr) = 2V ~ 5.5V
- Pin and Function Compatible with 74ALS165

IEC LOGIC SYMBOL



961001EBA2

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TRUTH TABLE

		INPUTS	-		INTERNAL OUTPUTS		OUTPUT				
<u>SHIFT/</u> LOAD	CLOCK INH	CLOCK	SERIAL IN	PARALLEL A ······ H	QA	QB	QH	QH			
L	Х	Х	X	a h	а	b	h	h			
Н	L	ſ	н	Х	Н	QAn	QGn	QGn			
Н	L	<u> </u>	L	Х	L	QAn	QGn	QGn			
Н		L	Н	X	Н	QAn	QGn	QGn			
Н	<u> </u>	L	L	X	L	QAn	QGn	QGn			
Н	X	Н	X	X	NO CHANGE						
Н	Н	Х	Х	Х	NO CHANGE						

X : Don't Care a h : The level of steady state input voltage at inputs A through H respectively QAn~QGn : The level of QA~QG, respectively, before the most recent positive transition of the CK.

TIMING CHART



⁹⁶¹⁰⁰¹EBA2'

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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V _{cc}	-0.5~7.0	V
DC Input Voltage	VIN	-0.5~7.0	V
DC Output Voltage	V _{OUT}	-0.5~V _{CC} +0.5	V
Input Diode Current	Ι _{ικ}	- 20	mA
Output Diode Current	Ι _{οκ}	± 20	mA
DC Output Current	I _{OUT}	±25	mA
DC V _{CC} /Ground Current	I _{cc}	± 50	mA
Power Dissipation	P _D	180	mW
Storage Temperature	T _{stg}	-65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V _{cc}	2.0~5.5	V
Input Voltage	VIN	0~5.5	V
Output Voltage	V _{OUT}	0~V _{cc}	V
Operating Temperature	T _{opr}	- 40~85	°C
Input Rise and Fall Time	dt/dv	0~100 (V _{CC} = 3.3 ± 0.3V) 0~20 (V _{CC} = 5±0.5V)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V _{cc}	Т	a = 25°	С	Ta = — 4	40∼85°C	UNIT	
PARAIVIETER	STIVIBUL			(V)	MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level				2.0	1.50	—	—	1.50	—		
Input Voltage	VIH			3.0~ 5.5	V _{cc} × 0.7	_	_	V _{cc} × 0.7	_	V	
Low - Level				2.0		-	0.50	—	0.50		
Input Voltage	VIL			3.0~ 5.5	—	-	$V_{cc} \times 0.3$	—	$V_{cc} \times 0.3$	V	
	V _{OH}			50.0	2.0	1.9	2.0	—	1.9	—	
High - Level Output Voltage		V _{1 N} =	$I_{OH} = -50 \mu A$	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4	_	V	
		V _{IH} or V _{IL}	$I_{OH} = -4mA$ $I_{OH} = -8mA$	3.0 4.5	2.58 3.94	_	_	2.48 3.80	_		
	V _{OL}		V _{1N} =	l _{oL} = 50μA	2.0 3.0	_	0.0 0.0	0.1	_	0.1 0.1	
Low - Level Output Voltage				4.5	—	0.0	0.1	—	0.1	V	
output voltage		V _{IH} or V _{IL}	I _{OL} = 4mA I _{OL} = 8mA	3.0 4.5	-		0.36 0.36	_	0.44 0.44		
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND		0~5.5	-	—	±0.1	—	± 1.0		
Quiescent Supply Current	I _{cc}	$V_{IN} = V_{CC}$ or GN	ID	5.5	-	_	4.0	_	40.0	μΑ	

TIMING	REQUIREMENTS	(Input	t _r = t _f = 3ns)
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PARAMETER	SYMBOL	TEST CONDITION		Ta = 25° _C	Ta = −40~85°C	UNIT
	STIVIBOL		V _{cc} (V)	LIMIT	LIMIT	
Minimum Pulse Width (CK, CK INH)	t _{W (L)} t _{W (H)}		3.3 ± 0.3 5.0 ± 0.5	6.0 4.0	7.0 4.0	
Minimum Pulse Width (S/L)	tw (L)		3.3±0.3 5.0±0.5	7.5 5.0	9.0 6.0	
Minimum Set - up Time (PI – S / \overline{L})	ts		3.3 ± 0.3 5.0 ± 0.5	7.5 5.0	8.5 5.0	
Minimum Set - up Time (SI—CK, CK INH)	ts		3.3±0.3 5.0±0.5	5.0 4.0	6.0 4.0	nc
Minimum Set - up Time (S/I—CK, CK INH)	ts		3.3±0.3 5.0±0.5	5.0 4.0	6.0 4.0	ns
Minimum Hold Time ($PI-S/\overline{L}$)	t _h		3.3±0.3 5.0±0.5	0.5 1.0	0.5 1.0	
Minimum Hold Time (SI—CK, CK INH)	t _h		3.3±0.3 5.0±0.5	0.0 0.5	0.0 0.5	
Minimum Hold Time (S/Ī—CK, CK INH)	t _h		3.3±0.3 5.0±0.5	0.0 0.5	0.0 0.5	
Minimum Removal Time (CK INH-CK) (CK-CK INH)	t _{rem}		3.3±0.3 5.0±0.5	5.0 3.5	5.0 3.5	

PARAMETER	CV/MPOL	TEST	T CONDITION		Ta = 25°C			Ta = − 40~85°C		UNIT
FARAIVIETER	SYMBOL		V _{cc} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
		t _{pLH}	3.3 ± 0.3	15	—	9.9	15.4	1.0	18.0	
Propagation Delay Time	t _{pLH}			50	—	12.4	18.9	1.0	21.5	
$(CK, CK INH - QH, \overline{QH})$	t _{pHL}		5.0 ± 0.5	15	—	6.6	9.9	1.0	11.5	
			$ 5.0 \pm 0.5 $	50	—	8.1	11.9	1.0	13.5	
			3.3 ± 0.3	15	—	9.9	15.8	1.0	18.5	
Propagation Delay Time	t _{pLH}		3.3 ± 0.3	50	_	12.4	12.4 19.3	1.0	22.0	- ns
$(S/\overline{L}-QH, \overline{QH})$	t _{pHL}		5.0 ± 0.5	15	—	6.7	9.9	1.0	11.5	
				50	—	8.2	11.9	1.0	13.5	
			3.3±0.3	15	_	9.2	14.1	1.0	16.5	
Propagation Delay Time	t _{pLH}			50	—	11.7	17.6	1.0	20.0	
$(H-QH, \overline{QH})$	t _{pHL}		5.0 ± 0.5	15	—	5.9	9.0	1.0	10.5	
				50	—	7.4	11.0	1.0	12.5	
			3.3 ± 0.3	15	65	85	—	55	—	- MHz
Maximum Clock Frequency	f	f _{MAX}		50	60	105	—	50	—	
Maximum clock riequency	'MAX		5.0 ± 0.5	15	110	150	—	90	-	
				50	95	130	—	85	—	
Input Capacitance	C _{IN}				_	4	10	-	10	nF
Power Dissipation Capacitance	C _{PD}	(Note 1)			_	50	_	_	—	- pF

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

 $I_{CC \text{ (opr.)}} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

INPUT EQUIVALENT CIRCUIT







Unit in mm



SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150-1.27)



SSOP 16PIN OUTLINE DRAWING (SSOP16-P-225-0.65B)

Unit in mm

Unit in mm



TSSOP 16PIN OUTLINE DRAWING (TSSOP16-P-0044-0.65)



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