

STL135N8F7AG

Automotive-grade N-channel 80 V, 3.15 mΩ typ., 130 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

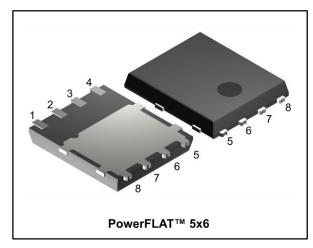
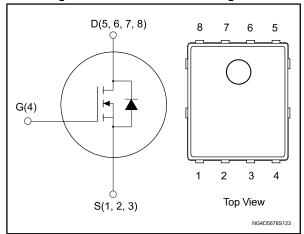


Figure 1: Internal schematic diagram



Features

Order code	V _{DS} R _{DS(on)} max.		I _D	Ртот
STL135N8F7AG	80 V	3.6 mΩ	130 A	135 W

- Designed for automotive applications and AEC-Q101 qualified
- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness
- Wettable flank package

Applications

• Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low onstate resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STL135N8F7AG	135N8F7	PowerFLAT™ 5x6	Tape and reel

Contents STL135N8F7AG

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STL135N8F7AG Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	±20	V
I _D ⁽¹⁾	Drain current (continuous) at T _{case} = 25 °C	130	۸
ייטו	Drain current (continuous) at T _{case} = 100 °C	93	Α
I _{DM} ⁽¹⁾⁽²⁾	Drain current (pulsed)	560	Α
I _D (3)	Drain current (continuous) at T _{pcb} = 25 °C	26	А
ID(°)	Drain current (continuous) at T _{pcb} = 100 °C	19	A
I _{DM} ⁽²⁾⁽³⁾	Drain current (pulsed)	104	Α
P _{TOT} ⁽¹⁾	Total dissipation at T _{case} = 25 °C	135	W
P _{TOT} (3)	Total dissipation at T _{pcb} = 25 °C	4.8	W
E _{AS} ⁽⁴⁾	Single pulse avalanche energy	1.2	J
T _{stg}	Storage temperature range	FF to 175	°C
T _j Operating junction temperature range		-55 to 175	°C

Notes:

Table 3: Thermal data

Symbol	Parameter Value		Unit
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	31.3	°C/W
R _{thj-case}	Thermal resistance junction-case	1.1 °C/	

Notes:

 $^{^{(1)}}$ This value is rated according to $R_{\text{thj-c}}.$

⁽²⁾ Pulse width is limited by safe operating area.

 $^{^{(3)}}$ This value is rated according to $R_{\text{thj-pcb}}$

 $^{^{(4)}}$ Starting T_j = 25 °C, I_D = 13 A, V_{DD} = 50 V

⁽¹⁾ When mounted on a 1-inch² FR-4 board, 2oz Cu, t < 10 s

Electrical characteristics STL135N8F7AG

2 Electrical characteristics

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(T_{case} = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit	
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	80			V	
	Zaro goto voltogo droin	$V_{GS} = 0 \text{ V}, V_{DS} = 80 \text{ V}$			1		
IDSS	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 80 \text{ V},$ $T_j = 125 \text{ °C}$			10	μΑ	
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = 20 V			100	nΑ	
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	2.5		4.5	V	
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 13 A		3.15	3.6	mΩ	

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Ciss	Input capacitance		-	6800	-	
Coss	Output capacitance	$V_{DS} = 40 \text{ V}, f = 1 \text{ MHz},$	-	1350	-	pF
C _{rss}	Reverse transfer capacitance	Ves = 0 V	-	95	1	'
Qg	Total gate charge	$V_{DD} = 40 \text{ V}, I_D = 26 \text{ A},$	-	103	-	
Q _{gs}	Gate-source charge	V _{GS} = 10 V (see Figure 14: "Test circuit for gate charge	-	35	-	nC
Q _{gd}	Gate-drain charge	behavior")	-	28	1	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = 40 \text{ V}, I_D = 13 \text{ A R}_G = 4.7 \Omega,$	-	30	-	
tr	Rise time	V _{GS} = 10 V (see Figure 13: "Test	-	28	-	
t _{d(off)}	Turn-off delay time	circuit for resistive load switching times" and Figure 18: "Switching	-	73	-	ns
t _f	Fall time	time waveform")	-	30	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Isp	Source-drain current		-		26	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		104	Α
V _{SD} ⁽²⁾	Forward on voltage	V _{GS} = 0 V, I _{SD} = 26 A	-		1.2	V
t _{rr}	Reverse recovery time	$I_{SD} = 26 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	47		ns
Qrr	Reverse recovery charge	V _{DD} = 64 V (see Figure 15: "Test circuit for inductive load	-	66		nC
I _{RRM}	Reverse recovery current	switching and diode recovery times")	-	2.8		А

Notes:

 $^{^{\}left(1\right) }$ Pulse width is limited by safe operating area.

 $^{^{(2)}}$ Pulse test: pulse duration = 300 $\mu s,$ duty cycle 1.5%.

2.1 Electrical characteristics (curves)

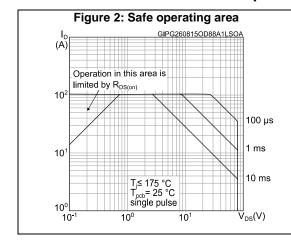


Figure 3: Thermal impedance K GIPG2608150D88A1LZTH δ =0.5 δ =0.2 δ =0.05 δ =0.01 δ =0.02 δ =0.01 δ =0.01 δ =0.02 δ =0.01 δ =0.01 δ =0.02 δ =0.01 δ =0.02 δ =0.01 δ =0.02 δ =0.01 δ =0.01 δ =0.02 δ =0.01 δ =0.02 δ =0.01 δ =0.02 δ =0.03 δ =0.04 δ =0.05 δ =0.02 δ =0.05 δ =0.02 δ =0.05 δ =0.05 δ =0.02 δ =0.05 δ =0.05 δ =0.02 δ =0.05 δ =0

Figure 4: Output characteristics

GIPG2608150D88A1LOCH

(A)

V_{GS} = 8,9,10 V

V_{GS} = 7 V

250

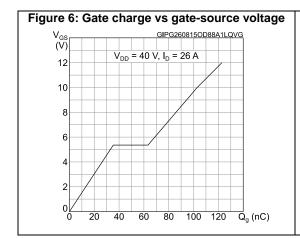
150

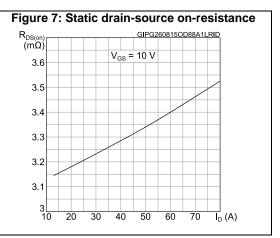
100

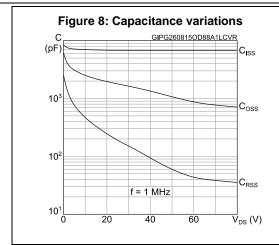
V_{GS} = 6 V

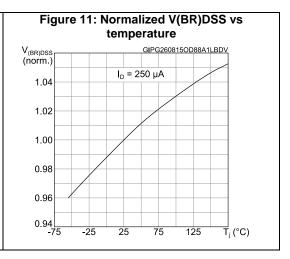
0

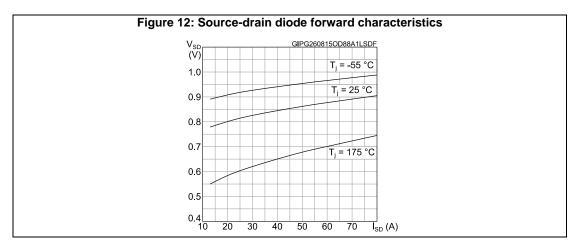
1 2 3 4 5 V_{DS} (V)











Test circuits STL135N8F7AG

3 Test circuits

Figure 13: Test circuit for resistive load switching times

Figure 14: Test circuit for gate charge behavior

12 V 47 KΩ 100 Ω D.U.T.

12 V 47 KΩ VGD

14 VGD

14 VGD

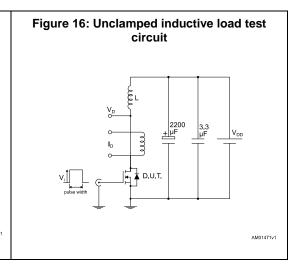
15 VGD

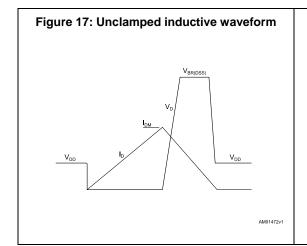
16 CONST 100 Ω D.U.T.

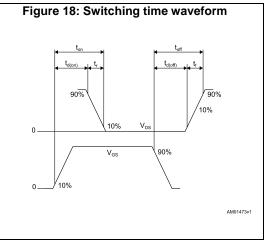
17 VGD

18 V

Figure 15: Test circuit for inductive load switching and diode recovery times







Package information 4

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

PowerFLAT™ 5x6 WF type C package information 4.1

BOTTOM VIEW D3 5 E7 Detail A E3 Scale 3:1 0.04 0.08 D5(x4) L(x4) b(x8) SIDE VIEW A Detail A TOP VIEW 8231817_WF_typeC_r12

Figure 19: PowerFLAT™ 5x6 WF type C package outline

577

Table 8: PowerFLAT™ 5x6 WF type C mechanical data

	able 8: PowerFLA1 *** 5x6	mm	
Dim.	Min.	Тур.	Max.
А	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
С	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.0	5.20
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
е		1.27	
Е	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.2	0.325	0.450
E7	0.85	1.00	1.15
K	1.05		1.35
L	0.90	1.00	1.10
L1	0.175	0.275	0.375
θ	0°		12°

STL135N8F7AG Package information

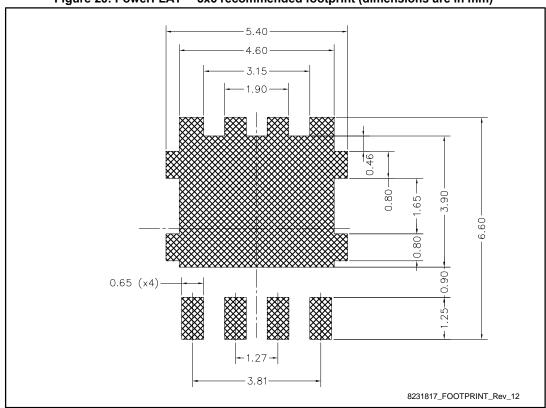


Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)

4.2 PowerFLAT™ 5x6 WF packing information

Figure 21: PowerFLAT™ 5x6 WF tape

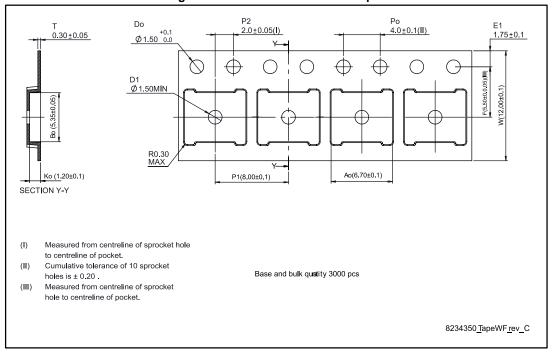


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

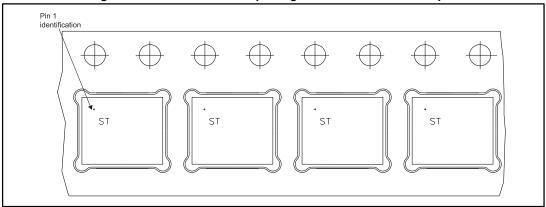
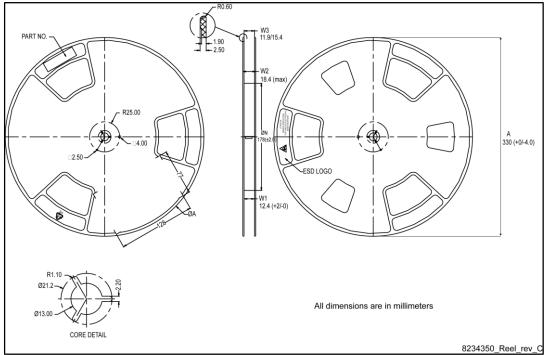


Figure 23: PowerFLAT™ 5x6 reel



STL135N8F7AG Revision history

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
07-Sep-2015	1	First release.
15-Sep-2015	2	Minor text edits. On cover page: - updated Title and Features
26-Jan-2016	3	Updated Table 2: "Absolute maximum ratings" and Section 4.1: "PowerFLAT™ 5x6 WF type C package information".

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