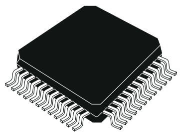
STDVE001A

Adaptive single 3.4 Gbps TMDS/HDMI signal equalizer

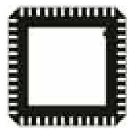
Preliminary Data

Features

- Compatible with the high-definition multimedia interface (HDMI) v1.3 digital interface
- Conforms to the transition minimized differential signaling (TMDS) voltage standard on input and output channels
- 340 MHz maximum clock speed operation supports all video formats with deep color at maximum refresh rates
- 3.4 Gbps data rate per channel
- Fully automatic adaptive equalizer for cables lengths up to 25 m
- Single supply V_{CC}: 3.135 to 3.465 V
- ESD: ±8 KV contact for all I/Os
- Integrated open-drain I^2C buffer for display data channel (DDC)
- 5.3 V tolerant DDC and HPD I/Os
- Lock-up free operation of I^2C bus
- 0 to 400 kHz clock frequency for I^2C bus
- Low capacitance of all the channels
- Equalizer regenerates the incoming attenu-ated TMDS signal
- Buffer drives the TMDS outputs over long PCB track lengths
- Low output skew and jitter
- Tight input thresholds reduce bit error rates
- On-chip selectable 50 Ω input termination
- Low ground bounce
- Data and control inputs provide undershoot clamp diode
- Evaluation kit is available



TQFP48



QFN48

Description

The STDVE001A integrates a 4-channel 3.4 Gbps TMDS equalizer. High-speed data paths and flow-through pinout minimize the internal device jitter and simplify the board layout.

The equalizer overcomes the intersymbol interference (ISI) jitter effects from lossy cables. The buffer/driver on the output can drive the TMDS output signals over long distances. In addition to this, STDVE001A integrates the 50 Ω termination resistor on all the input channels to improve performance and reduce board space. The device can be placed in a low-power mode by disabling the output current drivers. The STDVE001A is ideal for advanced TV and STB applications supporting HDMI/DVI standard. The differential signal from the HDMI/DVI ports can be routed through the STDVE001A to guarantee good signal quality at the HDMI receiver. Designed for very low skew, jitter and low I/O capacitance, the switch preserves the signal integrity to pass the stringent HDMI compliance requirements.

Table 1. Device summary

Order code	Operating temperature	Package	Packaging
STDVE001ABTR	-40°C to 85°C	TQFP48	Tape and reel
STDVE001AQTR	-40°C to 85°C	QFN48	Tape and reel

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Figure 1. STDVE001A block diagram

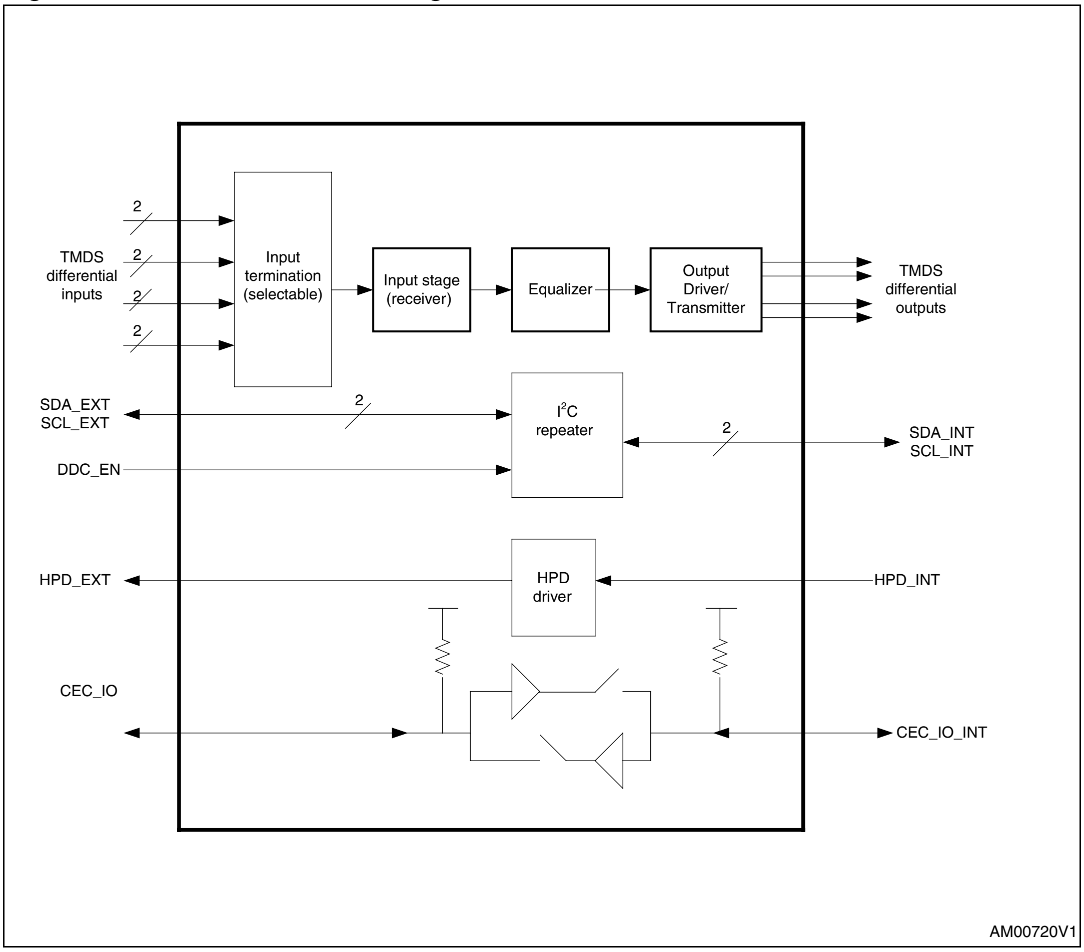


Figure 2. Equalizer functional diagram (one signal pair)

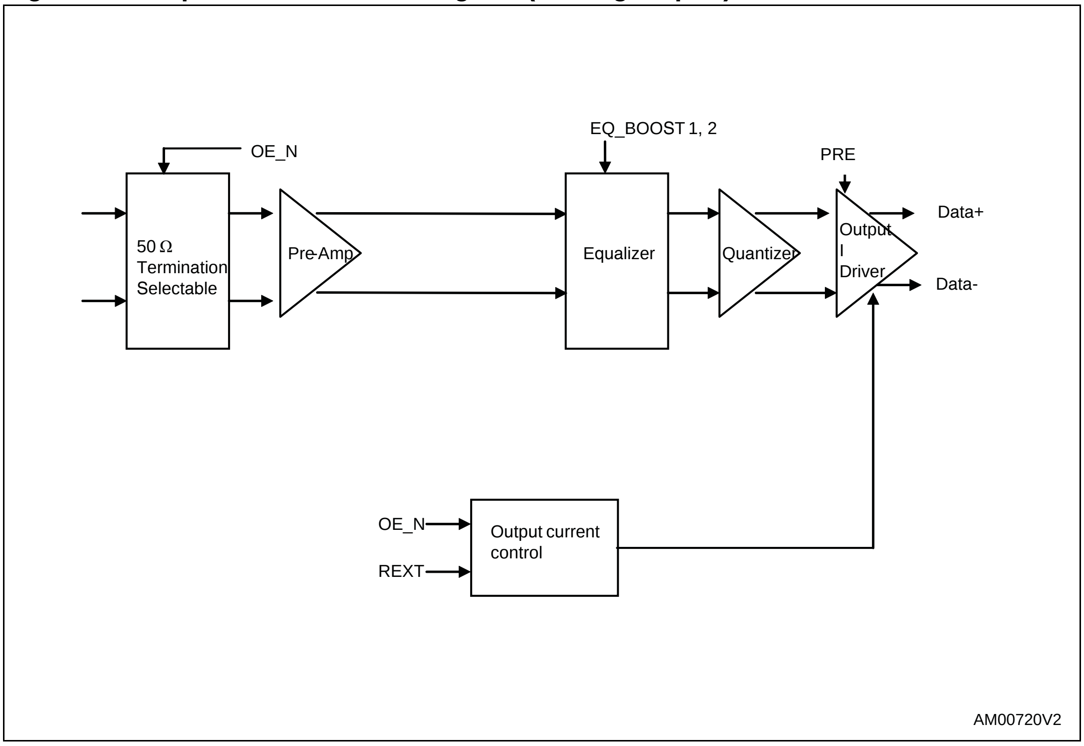
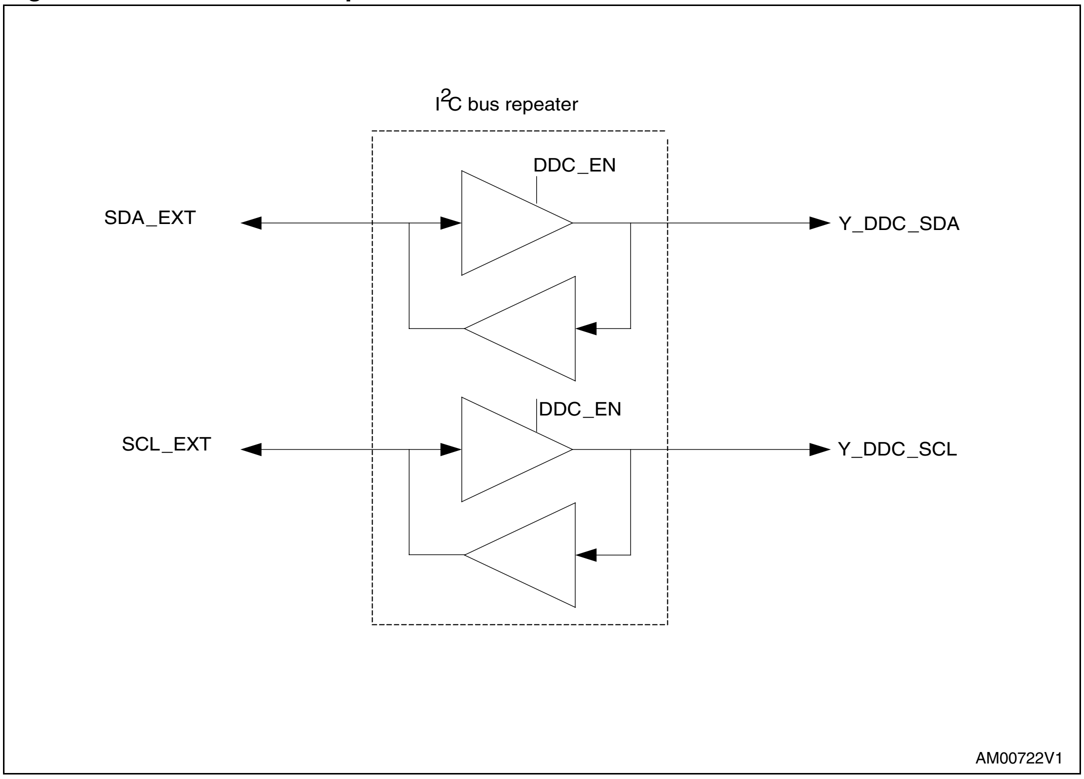
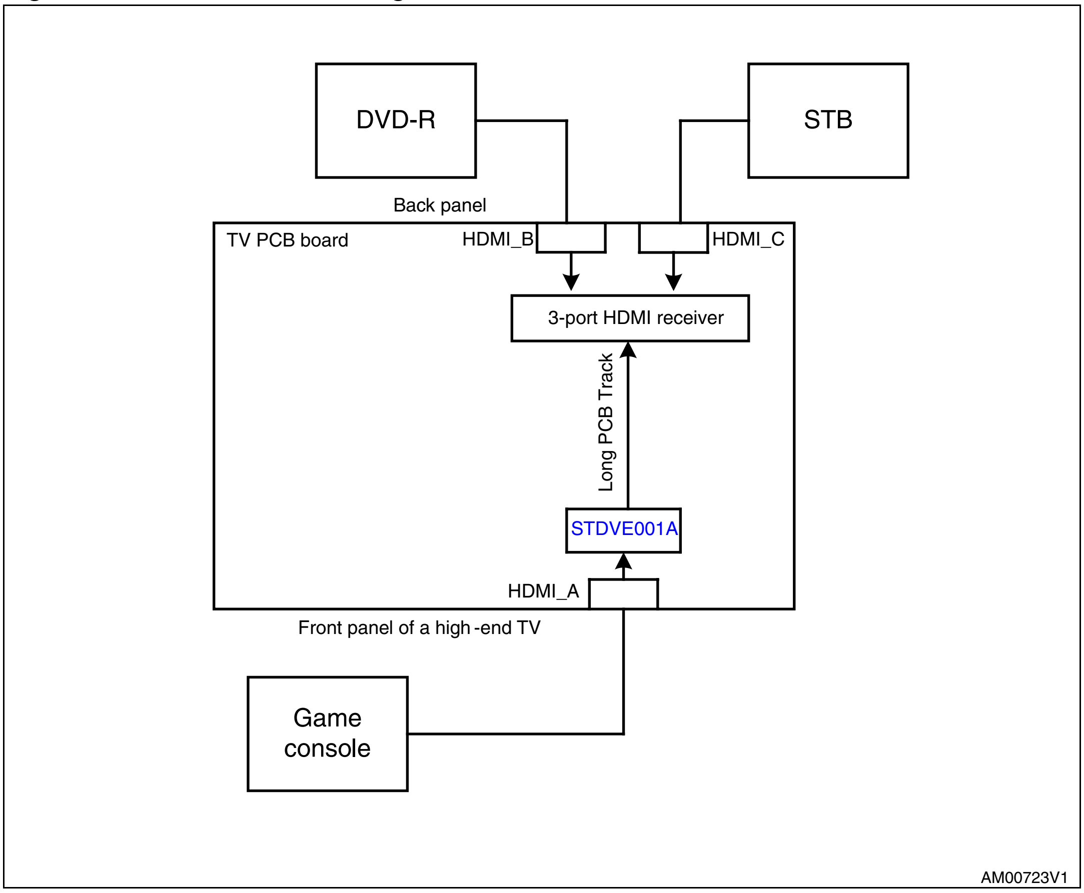


Figure 3. DDC I^2C bus repeater



1.1 Application diagrams

Figure 4. STDVE001A in a digital TV



2 Pin configuration

Figure 5. Pin configuration (TQFP48 package)

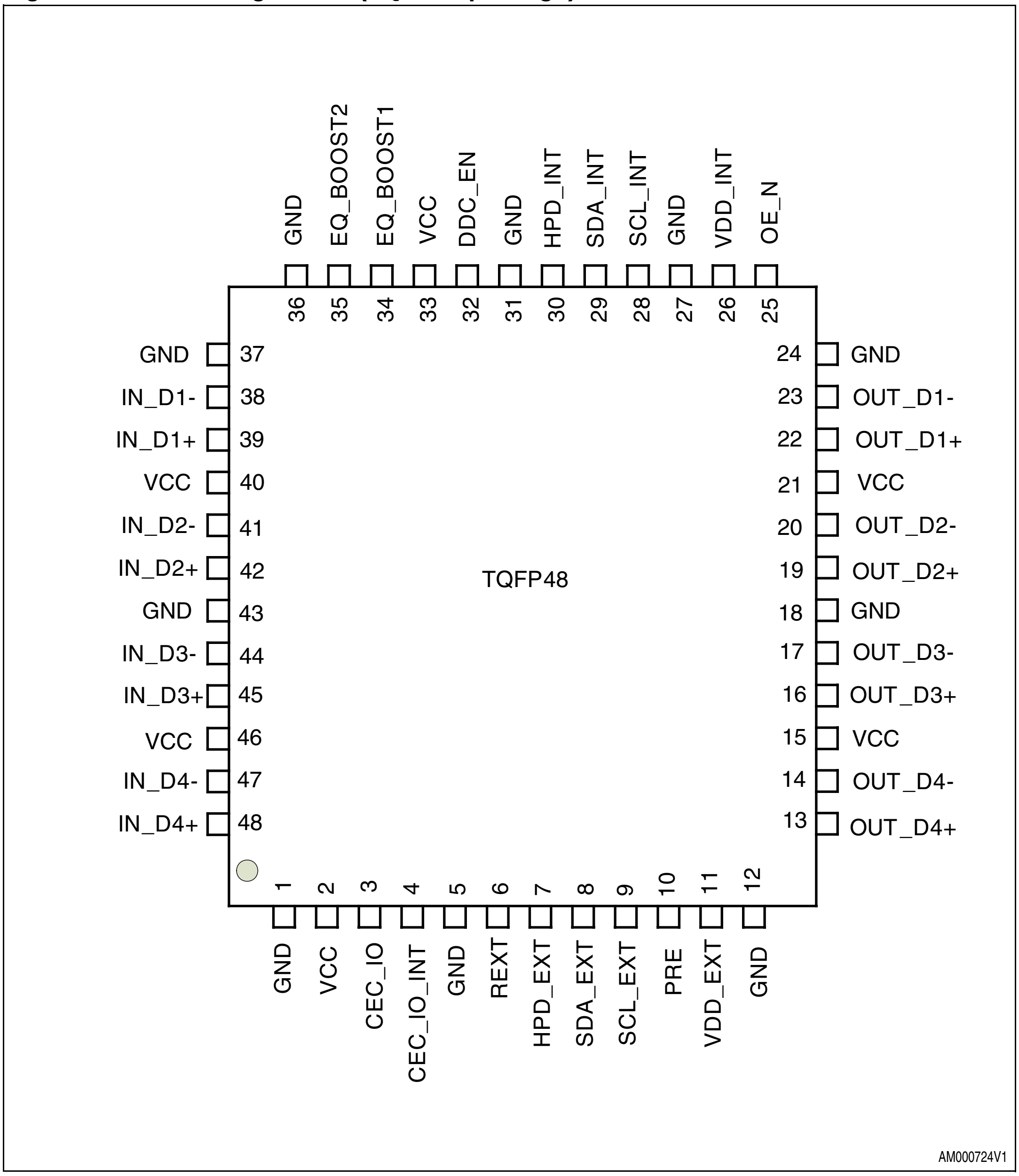


Figure 6. Pin configuration (QFN48 package)

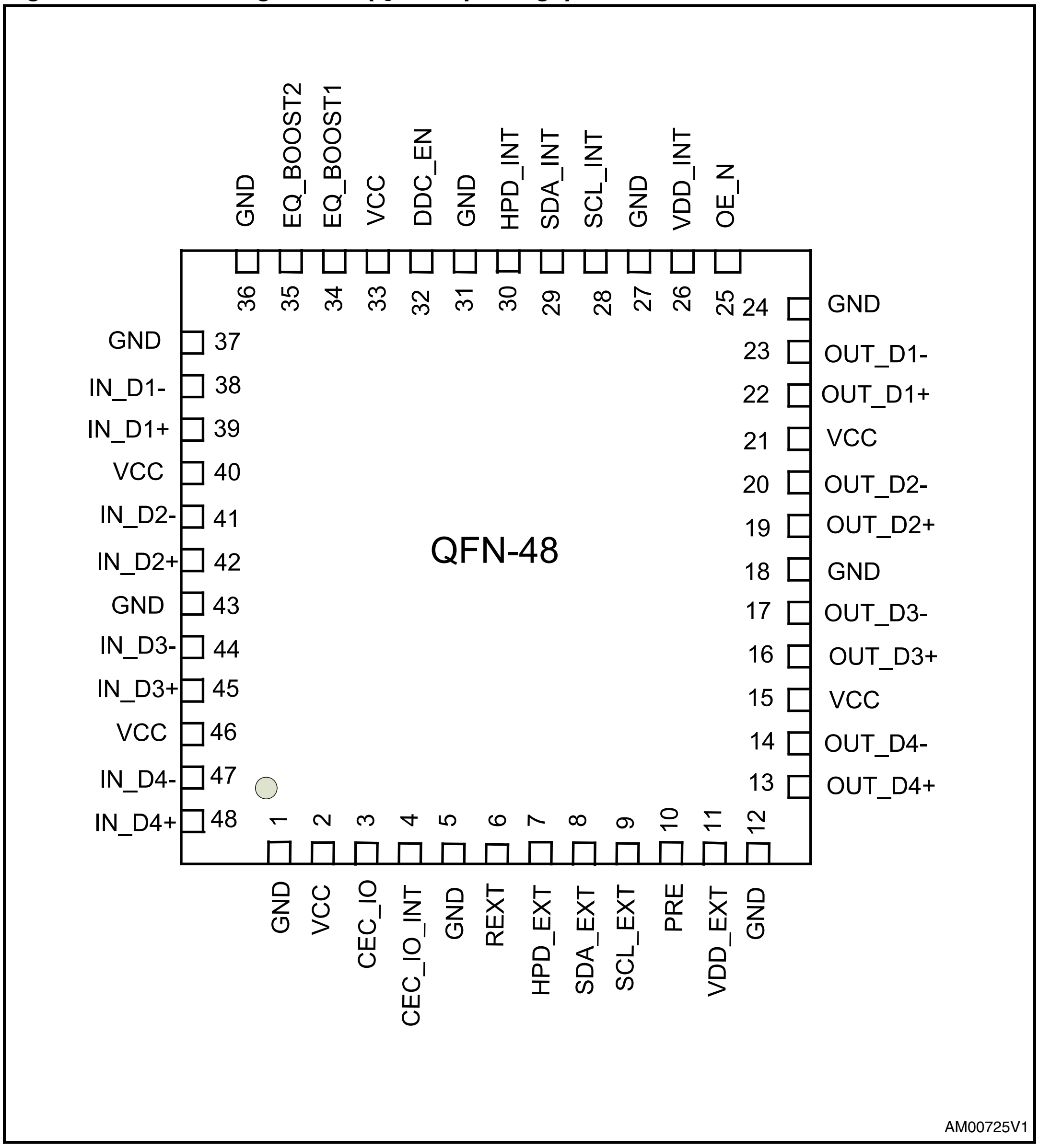


Table 2. Pin description

<table>
<tr><th>Pin number</th><th>Pin name</th><th>Type</th><th colspan="2">Function</th></tr>
<tr><td>1</td><td>GND</td><td>Power</td><td colspan="2">Ground</td></tr>
<tr><td>2</td><td>VCC</td><td>Power</td><td colspan="2">3.3 V±5% DC supply</td></tr>
<tr><td>3</td><td>CEC_IO</td><td>I/O</td><td colspan="2">CEC signal to/from the connector end</td></tr>
<tr><td>4</td><td>CEC_IO_INT</td><td>I/O</td><td colspan="2">CEC signal to/from TV end</td></tr>
<tr><td>5</td><td>GND</td><td>Power</td><td colspan="2">Ground</td></tr>
<tr><td>6</td><td>REXT</td><td>Analog</td><td colspan="2">Connect to GND through a 4.7 KΩ ± 1% precision reference resistor. Sets the output current to generate the output voltage compliant with TMDS</td></tr>
<tr><td>7</td><td>HPD_EXT</td><td>Output</td><td colspan="2">0 to 5.0 V (nominal) output signal. Hot plug detector output. Open drain output. Connect an external resistor according to the HDMI specification.</td></tr>
<tr><td>8</td><td>SDA_EXT</td><td>I/O</td><td colspan="2">DDC data I/O. Pulled-up by external termination to V_{DD}.</td></tr>
<tr><td>9</td><td>SCL_EXT</td><td>I/O</td><td colspan="2">DDC clock I/O. Pulled-up by external termination to V_{DD}.</td></tr>
<tr><td rowspan="4">10</td><td rowspan="4">PRE</td><td rowspan="4">Input</td><td colspan="2">TMDS output de-emphasis adjustment</td></tr>
<tr><th>PRE</th><th>Output de-emphasis</th></tr>
<tr><td>0 V</td><td>0 dB</td></tr>
<tr><td>3.3 V</td><td>3 dB</td></tr>
<tr><td>11</td><td>VDD_EXT</td><td>Power</td><td colspan="2">DC supply for DDC, HPD and CEC (can be 5V or 3.3V or unconnected)</td></tr>
<tr><td>12</td><td>GND</td><td>Power</td><td colspan="2">Ground</td></tr>
<tr><td>13</td><td>OUT_D4+</td><td>Output</td><td colspan="2">HDMI 1.3 compliant TMDS output. OUT_D4+ makes a differential output signal with OUT_D4-.</td></tr>
<tr><td>14</td><td>OUT_D4-</td><td>Output</td><td colspan="2">HDMI 1.3 compliant TMDS output. OUT_D4- makes a differential output signal with OUT_D4+.</td></tr>
<tr><td>15</td><td>VCC</td><td>Power</td><td colspan="2">3.3V±10% DC supply</td></tr>
<tr><td>16</td><td>OUT_D3+</td><td>Output</td><td colspan="2">HDMI 1.3 compliant TMDS output. OUT_D3+ makes a differential output signal with OUT_D3-.</td></tr>
<tr><td>17</td><td>OUT_D3-</td><td>Output</td><td colspan="2">HDMI 1.3 compliant TMDS output. OUT_D3- makes a differential output signal with OUT_D3+.</td></tr>
<tr><td>18</td><td>GND</td><td>Power</td><td colspan="2">Ground</td></tr>
<tr><td>19</td><td>OUT_D2+</td><td>Output</td><td colspan="2">HDMI 1.3 compliant TMDS output. OUT_D2+ makes a differential output signal with OUT_D2-.</td></tr>
<tr><td>20</td><td>OUT_D2-</td><td>Output</td><td colspan="2">HDMI 1.3 compliant TMDS output. OUT_D2- makes a differential output signal with OUT_D2+.</td></tr>
<tr><td>21</td><td>VCC</td><td>Power</td><td colspan="2">3.3V±10% DC supply</td></tr>
</table>

Table 2. Pin description (continued)

<table>
<tr><th>Pin number</th><th>Pin name</th><th>Type</th><th colspan="3">Function</th></tr>
<tr><td>22</td><td>OUT_D1+</td><td>Output</td><td colspan="3">HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1-.</td></tr>
<tr><td>23</td><td>OUT_D1-</td><td>Output</td><td colspan="3">HDMI 1.3 compliant TMDS output. OUT_D1- makes a differential output signal with OUT_D1+.</td></tr>
<tr><td>24</td><td>GND</td><td>Power</td><td colspan="3">Ground</td></tr>
<tr><td rowspan="4">25</td><td rowspan="4">OE_N</td><td rowspan="4">Input</td><td colspan="3">Active low enable signal</td></tr>
<tr><td>OE_N</td><td>N_D termination</td><td>IOUT_D outputs</td></tr>
<tr><td>1</td><td>High-Z</td><td>High-Z</td></tr>
<tr><td>0</td><td>50 Ω</td><td>Active</td></tr>
<tr><td>26</td><td>VDD_INT</td><td>Power</td><td colspan="3">DC supply for DDC, HPD and CEC (can be 5V or 3.3V or unconnected)</td></tr>
<tr><td>27</td><td>GND</td><td>Power</td><td colspan="3">Ground</td></tr>
<tr><td>28</td><td>SCL_INT</td><td>I/O</td><td colspan="3">DDC Clock I/O. Pulled-up by external termination to VCC.</td></tr>
<tr><td>29</td><td>SDA_INT</td><td>I/O</td><td colspan="3">DDC Data I/O. Pulled-up by external termination to VCC.</td></tr>
<tr><td>30</td><td>HPD_INT</td><td>Input</td><td colspan="3">Sink side, Low-frequency, 0V to 5V (nominal) hot plug detector input signal.

Voltage high indicates “plugged” state; voltage low indicates “unplugged” state.

High : 5V power signal asserted from source to sink and EDID is ready
Low : No 5V power signal is asserted from source to sink or EDID is not ready</td></tr>
<tr><td>31</td><td>GND</td><td>Power</td><td colspan="3">Ground</td></tr>
<tr><td>32</td><td>DDC_EN</td><td>Input</td><td colspan="3">I^2C repeater enable signal</td></tr>
<tr><td></td><td></td><td></td><td colspan="2">DDC_EN</td><td>I2C repeater</td></tr>
<tr><td></td><td></td><td></td><td colspan="2">0 V</td><td>Disabled, high-Z</td></tr>
<tr><td></td><td></td><td></td><td colspan="2">3.3 V</td><td>Enabled, active</td></tr>
<tr><td>33</td><td>VCC</td><td>Power</td><td colspan="3">3.3 V±10% DC supply</td></tr>
</table>

Table 2. Pin description (continued)

<table>
<tr><th>Pin number</th><th>Pin name</th><th>Type</th><th colspan="3">Function</th></tr>
<tr><td rowspan="6">34-35</td><td rowspan="6">EQ_BOOST1, EQ_BOOST2</td><td rowspan="6">Input</td><td colspan="3">TMDS input equalization selector (control pin).</td></tr>
<tr><td>EQ_BOOST 2</td><td>EQ_BOOST 1</td><td>Setting at 825 MHz</td></tr>
<tr><td>0</td><td>0</td><td>11 dB</td></tr>
<tr><td>0</td><td>1</td><td>9 dB</td></tr>
<tr><td>1</td><td>0</td><td>4 dB</td></tr>
<tr><td>1</td><td>1</td><td>16 dB</td></tr>
<tr><td>36</td><td>GND</td><td>Power</td><td colspan="3">Ground</td></tr>
<tr><td>37</td><td>GND</td><td>Power</td><td colspan="3">Ground</td></tr>
<tr><td>38</td><td>IN_D1-</td><td>Input</td><td colspan="3">HDMI 1.3 compliant TMDS input. IN_D1- makes a differential pair with IN_D1+.</td></tr>
<tr><td>39</td><td>IN_D1+</td><td>Input</td><td colspan="3">HDMI 1.3 compliant TMDS input. IN_D1+ makes a differential pair with IN_D1-.</td></tr>
<tr><td>40</td><td>VCC</td><td>Power</td><td colspan="3">3.3V±10% DC supply</td></tr>
<tr><td>41</td><td>IN_D2-</td><td>Input</td><td colspan="3">HDMI 1.3 compliant TMDS input. IN_D2- makes a differential pair with IN_D2+.</td></tr>
<tr><td>42</td><td>IN_D2+</td><td>Input</td><td colspan="3">HDMI 1.3 compliant TMDS input. IN_D2+ makes a differential pair with IN_D2-.</td></tr>
<tr><td>43</td><td>GND</td><td>Power</td><td colspan="3">Ground</td></tr>
<tr><td>44</td><td>IN_D3-</td><td>Input</td><td colspan="3">HDMI 1.3 compliant TMDS input. IN_D3- makes a differential pair with IN_D3+.</td></tr>
<tr><td>45</td><td>IN_D3+</td><td>Input</td><td colspan="3">HDMI 1.3 compliant TMDS input. IN_D3+ makes a differential pair with IN_D3-.</td></tr>
<tr><td>46</td><td>VCC</td><td>Power</td><td colspan="3">3.3V±10% DC supply</td></tr>
<tr><td>47</td><td>IN_D4-</td><td>Input</td><td colspan="3">HDMI 1.3 compliant TMDS input. IN_D4- makes a differential pair with IN_D4+.</td></tr>
<tr><td>48</td><td>IN_D4+</td><td>Input</td><td colspan="3">HDMI 1.3 compliant TMDS input. IN_D4+ makes a differential pair with IN_D4-.</td></tr>
</table>

3 Functional description

The STDVE001A routes physical layer signals for high bandwidth digital video and is compatible with low voltage differential signaling standard like TMDS. The device passes the differential inputs from a video source to a common display when it is in the active mode of operation. The device conforms to the TMDS standard on both inputs and outputs.

The low on-resistance and low I/O capacitance of the switch in STDVE001A result in a very small propagation delay. Additionally, it supports the DDC, HPD and CEC signaling.

The I^2C interface of the enabled input port is linked to the I^2C interface of the output port, and the hot plug detector (HPD) of the enabled input port is output to HPD_EXT.

3.1 Adaptive equalizer

The equalizer dramatically reduces the intersymbol interference (ISI) jitter and attenuation from long or lossy transmission media. The inputs present high impedance when the device is not active or when V_{CC} is absent or 0 V. In all other cases, the 50 Ω termination resistors on input channels are present.

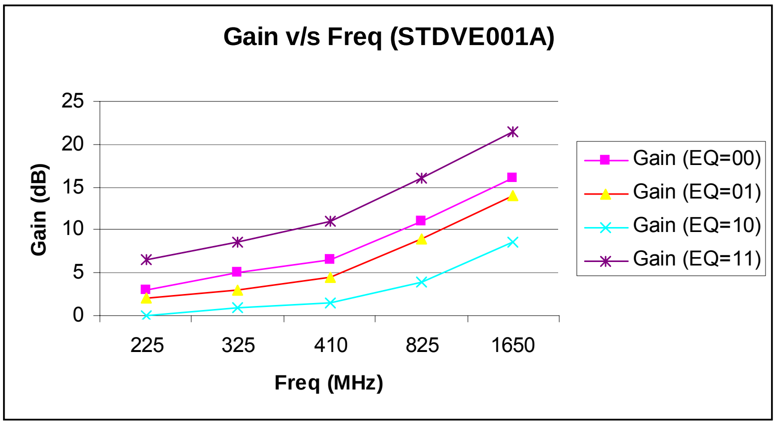
This circuit helps to improve the signal eye pattern significantly. Shaping is performed by the gain stage of the equalizer to compensate the signal degradation and then the signals are driven on to the output ports.

The equalizer is fully adaptive and automatic in function providing smaller gain at low frequencies and higher gain at high frequencies. The default setting of EQ = 00 is recommended on EQ pins for optimized operation.

Table 3. Adaptive equalizer gain with frequency

Freq (MHz)	Gain in dB (EQ=00)	Gain in dB (EQ=01)	Gain in dB (EQ=10)	Gain in dB (EQ=11)
225	3	2	0	6.5
325	5	3	1	8.5
410	6.5	4.5	1.5	11
825	11	9	4	16
1650	16	14	8.5	21.5

Figure 7. STDVE001A gain vs. frequency



The equalizer of STDVE001A is fully adaptive and automatic in function. The default setting of EQ = 00 is recommended for optimal operation. The equalizer performance is optimized for all frequencies over the cable lengths from 1m to 25 m at EQ = 00. If cable lengths greater than 25 m are desired in application, then EQ = 11 setting is recommended. The other two EQ settings of 01 and 10 are provided simply for fine-tuning purposes and can be used for very short external cables or PCB traces only if deemed necessary.

Input termination

The STDVE001A integrates precise 50 Ω ± 5% termination resistors, pulled up to V_{CC}, on all its differential input channels. External terminations are not required. This gives better performance and also minimizes the PCB board space. These on-chip termination resistors should match the differential characteristic impedance of the transmission line. Since the output driver consists of current steering devices, an output voltage is not generated without a termination resistor. Output voltage levels are dependent on the value of the total termination resistance. The STDVE001A produces TMDS output levels for point-to-point links that are doubly terminated (100 Ω at each end). With the typical 10 mA output current, the STDVE001A produces an output voltage of 3.3 – 0.5 V = 2.8 V when driving a termination line terminated at each end. The input terminations are selectable thus saving power for the unselected ports.

Output buffers

Each differential output of the STDVE001A drives external 50 Ω load (pull-up resistor) and conforms to the TMDS voltage standard. The output drivers consist of 10 mA differential current-steering devices.

The driver outputs are short-circuit current limited and are high-impedance to ground when OE_N = H or the device is not powered. The current steering architecture requires a resistive load to terminate the signal to complete the transmission loop from V_{CC} to GND through the termination resistor. Because the device switches the direction of the current flow and not voltage levels, the output voltage swing is determined by V_{CC} minus the voltage drop across the termination resistor. The output current drivers are controlled by the OE_N pin and are turned off when OE_N is a high. A stable 10 mA current is derived by accurate internal current mirrors of a stable reference current which is generated by band-gap voltage across the REXT. The differential output driver provides a typical 10 mA current sink capability, which provides a typical 500 mV voltage drop across a 50 Ω termination resistor.

TMDS voltage levels

The TMDS interface standard is a signaling method intended for point-to-point communication over a tightly controlled impedance medium. The TMDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise. The device is capable of detecting differential signals as low as 100 mV within the entire common mode voltage range.

3.2 Operating modes

Table 4. OE_N operating modes

Input			Output		Function
OE_N	IN+	IN-	OUT+	OUT-	
L	H	L	H	L	Active mode
L	L	H	L	H	Active mode
H	X	X	Hi-Z	Hi-Z	Low power mode

The OE_N input activates a hardware power down mode. When the power down mode is active (OE_N = H), all input and output buffers and internal bias circuitry are powered-off and disabled.

Outputs are tri-stated in power-down mode. When exiting power-down mode, there is a delay associated with turning on band-references and input/output buffer circuits.

Note that the OE_N pin is only used to disable the TMDS paths in the chip to same maximum amount of current. It does not affect the HPD, DDC and CEC portions. The DDC is controlled only by the DDC_EN pin whereas the HPD and CEC are always active as long as the supply to the chip is present.

3.3 HPD pins

The input pin HPD_INT is 5 V tolerant, allowing direct connection tp 5 V signals. The output HPD pin has open-drain structure so that the disabled HPD output is driven to GND whereas the enabled HPD port has the same polarity as the HPD_INT. Note that the HPD output should have an external pull-up resistor connected to +5 V from the HDMI source.

3.4 DDC channels

The DDC channels are designed together with a bi-directional buffer so as to ensure the voltage levels on the I^2C lines are met even after long capacitive cables. This feature eliminates the errors during EDID and HDCP reading.

3.5 I^2C DDC line repeater

The device contains two identical bi-directional open-drain, non-inverting buffer circuits that enable I^2C DDC bus lines to be extended without degradation in system performance. The STDVE001A buffers both the serial data (DDC SDA) and serial clock (DDC SCL) on the I^2C bus, while retaining all the operating modes and features of the I^2C system. This enables two buses of 400 pF bus capacitance to be connected in an I^2C application. These buffers are operational from a supply V of 3.0 V to 3.6 V.

The I^2C bus capacitance limit of 400 pF restricts the number of devices and bus length. The STDVE001A enables the system designer to isolate the two halves of a bus, accommodating more I^2C devices or longer trace lengths. It can also be used to run two buses, one at 5 V and the other at 3.3 V or a 400 kHz and 100 kHz bus, where the 100 kHz bus is isolated when 400 kHz operation of the other bus is required. The STDVE001A can be used to run the I^2C bus at both 5 V and 3.3 V interface levels.

The DDC_EN acts as the enable for the DDC buffer. The DDC_EN line should not change state during an I^2C operation, because disabling during bus operation hangs the bus and enabling port may through a bus cycle could confuse the I^2C ports being enabled. The DDC_EN input should change state only when the global bus and repeater port are in idle state, to prevent system failures.

The output low levels for each internal buffer are approximately 0.5 V, but the input voltage of each internal buffer must be 70 mV or more below the output low level, when the output internally is driven low. This prevents a lock-up condition from occurring when the input low condition is released.

As with the standard I^2C system, pull up resistors are required to provide the logic high levels on the buffered bus. The STDVE001A has standard open collector configuration of the I^2C bus. The size of the pull up resistors depends on the system, but each side of the repeater must have a pull up resistor.

This part is designed to work with standard mode and fast mode I^2C devices. Standard mode I^2C devices only specify 3 mA output drive, this limits the termination current to 3 mA in a generic I^2C system where standard mode devices and multiple masters are possible. Under certain conditions, higher termination currents can be used.

3.6 Power-down condition

The OE_N pin can be used to disable the device. Also there is no ESD protection dode to supply on any of the IOs. This prevents a reverse current flow condition when the main box is switched off while the TV is switched on.

The OE_N is used to disable most of the internal circuitry of STDVE001A that puts the device in a low power mode of operation.

3.7 Bias

The bandgap reference voltage over the external R_{EXT} reference resistor sets the internal bias reference current. This current and its factors (achieved by employing highly accurate and well matched current mirror circuit topologies) are generated on-chip and used by several internal modules. The 10 mA current used by the transmitter block is also generated using this reference current. It is important to ensure that the R_{EXT} value is within the ±1% tolerance range of its typical value.

Table 5. Bias parameter

Parameter	Min	Typ	Max	Unit
Bandgap voltage		1.2		V

The output voltage swing depends on 3 components: supply voltage ($V_{supply)}$, termination resistor (R_T) and current drive (I_{drive}). The supply voltage can vary from 3.3 V ±5%, termination resistor can vary from 50 Ω ±10%.

The voltage on the output is given by:

$V_{supply} - I_{drive} \times R_T$.

The variation on I_{drive} must be controlled to ensure that the voltage on HDMI output is within the HDMI specification under all conditions.

This is achieved when:

400 mV $\leq I_{drive} \times R_T \leq$ 600 mV with typical value centered at 500 mV.

3.8 Timing between HPD and DDC

It is important to ensure that the I^2C DDC interface is ready by the time the HPD detection is complete.

As soon as the discovery is finished by the HPD detection, the configuration data is exchanged between a source and sink through the I^2C DDC interface. The STDVE003 Afs DDC interface is ready for communication as soon as the power supply to the chip is present and stable. When the desired port is enabled and the chip is out of shutdown mode, the I^2C DDC lines can be used for communication.

Thus, as soon as the HPD detection sequence is complete, the DDC interface can be readily used. There is no delay between the HPD detection and I^2C DDC interface to be ready.

3.9 CEC

The CEC channel is a dedicated single pin bus and electrically translates to a bi-directional buffer used to ensure that the electrical specs of the CEC are met even with high capacitance on the single CEC line. The pull-up resistor of 26K? is integrated on either sides of the buffer. The CEC is used for AV control of the electronic devices connected in a HDMI cluster. The drive of the buffer is set to meet the requirements of the CEC. This is optionally used for higher-level user functions such as automatic set-up tasks or tasks typically associated with infrared remote control usage.

The CEC line is continuously monitored during the power-on state and is not monitored during powered-off state. In powered off state, the CEC line should not be pulled low and it should not affect the CEC communication between other devices. The maximum capacitance on the CEC lines can be 7.2nF.

4 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage to ground		-0.5 to +4.0	V
V_I	DC input voltage (TMDS ports)		1.7 to +4.0	V
	OE_N, DDC_EN, PRE, EX_BOOST1, EX_BOOST2		-0.5 to +4.0	V
	SDA_INT, SCL_INT, SDA_EXT, SCL_EXT, HPD_INT, HPD_EXT		-0.5 to +6.0	V
I_O	DC output current		120	mA
T_{STG}	Storage temperature		-65 to +150	°C
T_L	Lead temperature (10 sec)		300	°C
V_{ESD}	Electrostatic discharge voltage on all IOs	Contact discharge as per IEC61000-4-2 standard	±8	kV

Table 7. Thermal data

Symbol	Parameter	TQFP48 QFN48	Unit
Θ_{JA}	Thermal coefficient (junction-ambient)	48	°C/W

4.1 Recommended operating conditions

4.2 DC electrical characteristics

T_A = -40 to +85 °C, V_{CC} = 3.3 V ± 5% [a]

Table 8. Power supply characteristics

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		3.135	3.3	3.465	V
I_{CC}	Supply current	All inputs/outputs are enabled. Inputs are terminated with 50 Ω to V_{CC}. V_{CC} = 3.465 V Data rate = 3.4 Gbps		130		mA

Table 9. DC specifications for TMDS differential inputs

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V_{TH}	Differential input high threshold (peak-to-peak)	V_{CC} = 3.465 V over the entire V_{CMR}		0	150	mV
V_{TL}	Differential input low threshold	V_{CC} = 3.465 V over the entire V_{CMR}	-150	0		mV
V_{ID}	Differential input voltage (peak-to-peak)(1)	V_{CC} = 3.465 V	150		1560	mV
V_{CMR}	Common mode voltage range		V_{CC} - 0.3		V_{CC} - 0.04	V
C_{IN}	Input capacitance	IN+ or IN- to GND F = 1 MHz		3.5		pF

1. Differential output voltage is defined as | (OUT+ - OUT-) |.
Differential input voltage is defined as | (IN+ - IN-) |.

a. Typical parameters are measured at V_{CC} = 3.3 V, T_A = +25 °C.

Table 10. DC specifications for TMDS differential ouputs

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V_{OH}	Single-ended high level output voltage		V_{CC}-10		V_{CC}+10	mV
V_{OL}	Single-ended low level output voltage		V_{CC}-600		V_{CC}-400	mV
V_{swing}	Single ended output swing voltage	V_{CC} = 3.3 V R_{TERM} = 50 Ω	400	500	600	mV
V_{OD}	Differential output voltage (peak-to-peak)(1)	V_{CC} = 3.3 V R_{TERM} = 50 Ω	800	1000	1200	mV
I_{OH}	Differential output high level current		0		50	µA
I_{OL}	Differential output low level current		8	10	12	mA
$\|I_{SC}\|$	Output driver short-circuit current (continuous)	OUT± = GND through a 50 Ω resistor. See *Figure 12*			12	mA
C_{OUT}	Output capacitance	OUT+ or OUT- to GND when tri-state F = 1 MHz		5.5		pF

1. Differential output voltage is defined as | (OUT+ - OUT-) |. Differential input voltage is defined as | (IN+ - IN-) |

Table 11. DC specifications for OE_N, EQ_BOOST, EQ_BOOST2, PRE, DDC_EN inputs

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V_{IH}	HIGH level input voltage	High level guaranteed	2.0			V
V_{IL}	LOW level input voltage	Low level guaranteed	-0.5		0.8	V
V_{IK}	Clamp diode voltage	V_{CC} = 3.465 V I_{IN} = -18 mA	-1.2	-0.8		V
I_{IH}	Input high current	V_{CC} = 3.465 V V_{IN} = V_{CC}	-5		+5	µA
I_{IL}	Input low current	V_{CC} = 3.465 V V_{IN} = GND	-5		+5	µA
C_{IN}	Input capacitance	Pin to GND F = 1 MHz		3.5		pF

Table 12. Input termination resistor

Symbol	Parameter	Test condition	Value			Unit
R_{TERM}	Differential input termination resistor on IN± channels relative to V_{CC}	I_{IN} = -10 mA	45	50	55	Ω

Table 13. External reference resistor

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
R_{EXT}	Resistor for TMDS compliant voltage swing range	Tolerance for R = ±1%		4.7		KΩ

Table 14. DDC I/O pins

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$V_{I(DDC)}$	Input voltage		GND		5.3	V

Table 14. DDC I/O pins

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$I_{I(leak)}$	Input leakage current	V_{CC} = 3.465 V Input port= 5.3 V Output port = 0.0 V Switch is isolated			6	µA
		V_{CC} = 3.465 V Input port = 3.3 V Output port = 0.0 V Switch is isolated			2	µA
$C_{I/O}$	Input/output capacitance	V_I = 0 V F = 1 MHz Switch disabled		5		pF
		V_I = 0 V F = 1 MHz Switch enabled		9		pF

Table 15. Status pins (HPD_INT)

Symbol	Parameter	Test condition	Value Min	Value Typ	Value Max	Unit
V_{IH}	High level input voltage	V_{CC} = 3.3 V High level guaranteed	2.0		5.3	V
V_{IL}	Low level input voltage	V_{CC} = 3.3 V Low level guaranteed	GND		0.8	V
$I_{I(leak)}$	Input leakage current	V_{CC} = 3.465 V Output = 5.3 V			4	µA
		V_{CC} = 3.465 V Output = 3.3 V			2	µA

Table 16. Status pins (HPD_EXT)[1]

Symbol	Parameter	Test condition	Value Min	Value Typ	Value Max	Unit
V	Voltage		GND		5.3	V
$C_{I/O}$	Input/output capacitance	V_I = 0 V F = 1 MHz Switch disabled		5		pF
		V_I = 0 V F = 1 MHz Switch enabled		9		pF
V_{OL}	Output low voltage (open drain I/Os)	V_{CC} = 3.3 V I_{OL} = 8 mA			0.4	V

1. Typical parameters are measured at V_{CC} = 3.3 V, T_A = +25 °C.

4.3 DC electrical characteristics (I^2C repeater)

(T_A = -40 to +85 °C, V_{CC} = 3.3 V ± 5%, GND = 0 V; unless otherwise specified)

Table 17. Supplies

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V_{CC}	DC supply voltage		3.135	3.3	3.465	V

Table 18. Input/output SDA, SCL

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V_{IH}	High level input voltage		0.7 V_{CC}		5.3	V
V_{IL}	Low level input voltage(1)		-0.5		0.3 V_{CC}	V
V_{ILc}	Low level input voltage contention(1)		-0.5		0.4	V
V_{IK}	Input clamp voltage	I_I = -18 mA	–	–	-1.2	V
I_{IL}	Input current low (SDA, SCL)	Input current low (SDA, SCL)	–	–	1	µA
I_{IH}	Input current high (SDA, SCL)	V_I = 3.465 V (SDA, SCL)	–	–	10	µA
		V_I = 5.3 V (SDA, SCL)	–	–	10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA			0.4	V
		I_{OL} = 6 mA			0.65	V
I_{OH}	Output high level leakage current	V_O = 3.6 V; driver disabled	–	–	10	µA
		V_O = 5.3 V; driver disabled	–	–	10	µA
C_I	Input capacitance	V_I = 3 V or 0 V	–	6	7(2)	pF

1. V_{IL} specification is for the first low level seen by the SDA/SCL lines. V_{ILc} is for the second and subsequent low levels seen by the SDA/SCL lines.
2. The SCL/SDA C_I is about 200 pF when V_{CC} = 0 V. The STDVE001A should be used in applications where power is secured to the repeater but an active bus remains on either set of the SDA/SCL pins.

4.4 DC electrical characteristics (CEC)

(TA = -40 to +85 °C, VCC = 3.3V ± 5%, GND=0V; unless otherwise specified)

Table 19. DC electrical characteristics (CEC)

Symbol	Parameter	Test condition	Value			
			Min	Typ	Max	Unit
V_{CC}	DC supply voltage		3.135	3.3	3.465	V
V_{OL}	Logic 0 output		0.0		0.6	V
V_{OH}	Logic 1 output		2.5		3.63	V
$V_{HL(th)}$	High to low input V treshold for logic ‘0’			Vcec(‘0’) ≥ 0.8		V
$V_{LH(th)}$	Low to high input V treshold for logic ‘1’			Vcec(‘1’) ≥ 2.0		V
V_{hys}	Typical input hysteresis(1)			0.4		V
T_r	Maximum rise time (10% to 90%)	C_L= 7.2 nF			250	µs
T_f	Maximum fall time (90% to 10%)	C_L= 7.2 nF			50	µs
RPU	Internal pull-up resistor(2)		23.4	26	28.6	KΩ
I_{OFF}	CEC IO current in upowered state	V_{CC} = 0.0 V			1.8	µA

1. Input hysteresis is normally supplied by the microprocessor input circuit. In this case, additional hysteresis circuitry is not needed.
2. The internal device pull-up should be disconnected from the line when the device is powered-off.

4.5 Dynamic switching characteristics[b]

T_A = -40 to +85 °C, V_{CC} = 3.3 V ± 5%, R_{TERM} = 50 Ω ± 5%, C_L = 5 pF).

Typical values are at T_A = +25 °C and V_{CC} = 3.3 V.

Table 20. Clock and data rate

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
f_{CK}	Clock frequency (1/10th of the differenttial data rate)		25		340	MHz
D_{rate}	Signaling rate				3.4	Gbps

Table 21. Differential output timings

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
t_r	Differential data and clock output rise/fall times	20% to 80% of V_{OD}	75	150	240	ps
t_f		80% to 20% of V_{OD}	75	150	240	ps
t_{PLH}	Differential low to high propagation delay	Alternating 1 and 0 pattern at slow and fast data rates Measure at 50% V_{OD} between input to output	250		800	ps
t_{PHL}	Differential high to low propagation delay		250		800	ps

Table 22. Skew times

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$t_{SK(O)}$	Inter-pair channel-to-channel output skew				100	ps
$t_{SK(P)}$	Pulse skew	$\lvert t_{PLH} - t_{PHL} \rvert$		25	80	ps
$t_{SK(D)}$	Intra-pair differential skew				44	ps
$t_{SK(CC)}$	Output channel to channel skew	Difference in propagation delay (t_{PLH} or t_{PHL}) among all output channels		50	125	ps

b. *The timing values in this section are tested during characterization and are guaranteed by design and simulation. Not tested in production.*

Table 23. Turn-on and turn-off times

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
t_{ON}	TMDS output enable time	Time from OE_N to OUT± change from tri-state to active		12	20	ns
t_{OFF}	TMDS output disable time	Time from OE_N to OUT± change from active to tri-state		6	10	ns

Table 24. DDC I/O pins

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
Refer to *Section 4.6*						

Table 25. Status pins (HPD_INT, HPD_EXT, OE_N)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$t_{PD(HPD)}$	Propagation delay (from Y_HPD to the active port of HPD)	C_L = 10 pF, R_{PU} = 1 KΩ		150		ns
$T_{ON/OFF}$	Switch time (from port select to the latest valid status of HPD)	C_L = 10 pF		50		ns

Table 26. Jitter

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
t_{JIT}	Total jitter(1)	PRBS pattern at 1.6 Gbps (800 MHz)		35		ps (p-p)

1. Total jitter is measured peak-to-peak with a histogram including 3500 window hits. Stimulus and fixture jitter has been subtracted. Input differential voltage = V_{ID} = 500 mV, PRBS random pattern at 1.65 Gbps, t_r=t_f=50 ps (20% to 80%). Jitter parameter is not production-tested but guaranteed through characterization on a sample-to-sample basis.

4.6 Dynamic switching characteristics (I^2C repeater)

T_A = -40 to +85 °C, V_{CC} = 3.3 V ± 5%.

Typical values are at T_A = +25 °C and V_{CC} = 3.3 V.

.

Table 27. I^2C repeater(1)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
f_{SCL}	I^2C clock frequency	Standard mode			100	kHz
		Fast mode			400	kHz
t_{LOW}	Low duration on SCL pin	100 KHz See *Figure 20* Voltage on line = 5V Cmax=400 pF, Rmax = 2 K Depends on input signal rise time. Includes the 20 % time intervals on both transitions.	4.7			µs
		400 KHz See *Figure 20* Voltage on line = 5V Cmax = 400 pF, Rmax = 2 K Depends on input signal rise time. Includes the 20 % time intervals on both transitions.	1.3			µs
t_{LOW}	Low duration on SCL pin	100 KHz See *Figure 20* Voltage on line = 3.3 V Cmax = 400 pF, Rmax = 2 K Depends on input signal rise time. Includes the 20 % time intervals on both transitions.	4.7			µs
		400 KHz See *Figure 20* Voltage on line = 3.3 V, Cmax = 400 pF, Rmax = 2 K Depends on input signal rise time. Includes the 20 % time intervals on both transitions.	1.3			µs

Table 27. I²C repeater(1) (continued)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
t_{HIGH}	High duration on SCL pin	100 KHz See *Figure 20* Voltage on line = 5 V Cmax = 400 pF, Rmax = 2 K Depends on input signal rise time. Includes the 20 % time intervals on both transitions	4.0			µs
		400 KHz See *Figure 20* Voltage on line = 5 V Cmax = 400 pF, Rmax=2 K Depends on input signal rise time. Includes the 20 % time intervals on both transitions	0.6			µs
t_{HIGH}	High duration on SCL pin	100 KHz Refer section 14.12, Voltage on line = 3.3 V Cmax = 400 pF, Rmax = 2 K Depends on input signal rise time. Includes the 20 % time intervals on both transitions	4.0			µs
		400 KHz See *Figure 20* Voltage on line = 3.3 V, Cmax=400 pF, Rmax = 2 K Depends on input signal rise time. Includes the 20 % time intervals on both transitions	0.6			µs
t_{PHL}	Propagation delay	400 KHz Waveform 1 (*Figure 18*) Voltage on line = 5 V, Cmax = 400 pF, Rmax = 2 K			250	µs
t_{PLH}	Propagation delay	400 KHz Waveform 1 (*Figure 18*) Voltage on line = 5 V, Cmax = 400 pF, Rmax = 2 K			300	µs
t_{PHL}	Propagation delay	400 KHz Waveform 1 (*Figure 18*) Voltage on line = 3.3 V, Cmax = 400 pF, Rmax = 2 K			250	ns

Table 27. I^{2}C repeater[1] (continued)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
t_{PLH}	Propagation delay	400 KHz Waveform 1 (*Figure 18*) Voltage on line = 3.3 V, Cmax = 400 pF, Rmax = 2 K			450	ns
t_{PHL}	Propagation delay	100 KHz Waveform 1 (*Figure 18*) Voltage on line = 5 V, Cmax = 400 pF, Rmax = 2 K			250	ns
t_{PLH}	Propagation delay	100 KHz Waveform 1 (*Figure 18*) Voltage on line = 5 V, Cmax = 400 pF, Rmax = 2 K			300	ns
t_{PHL}	Propagation delay	100 KHz Waveform 1 (*Figure 18*) Voltage on line = 3.3 V, Cmax = 400 pF, Rmax = 2 K			250	ns
t_{PLH}	Propagation delay	100 KHz Waveform 1 (*Figure 18*) Voltage on line = 3.3 V, Cmax = 400 pF, Rmax = 2 K			450	ns
t_f	Output fall time	400 KHz Waveform 1 (*Figure 18*)[2] Voltage on line = 5 V Cmax = 400 pF, Rmax = 2 K			300	ns
		400 KHz Waveform 1[2] Voltage on li ne = 3.3 V Cmax = 400pF, Rmax = 2 K			300	ns
t_f	Output fall time	100 KHz Waveform 1 (*Figure 18*) [2] Voltage on line = 5 V Cmax = 400 pF, Rmax = 2 K			300	ns
		100 KHz Waveform 1 (*Figure 18*)[2] Voltage on line = 3.3 V Cmax = 400 pF, Rmax = 2 K			300	ns

Table 27. I²C repeater(1) (continued)

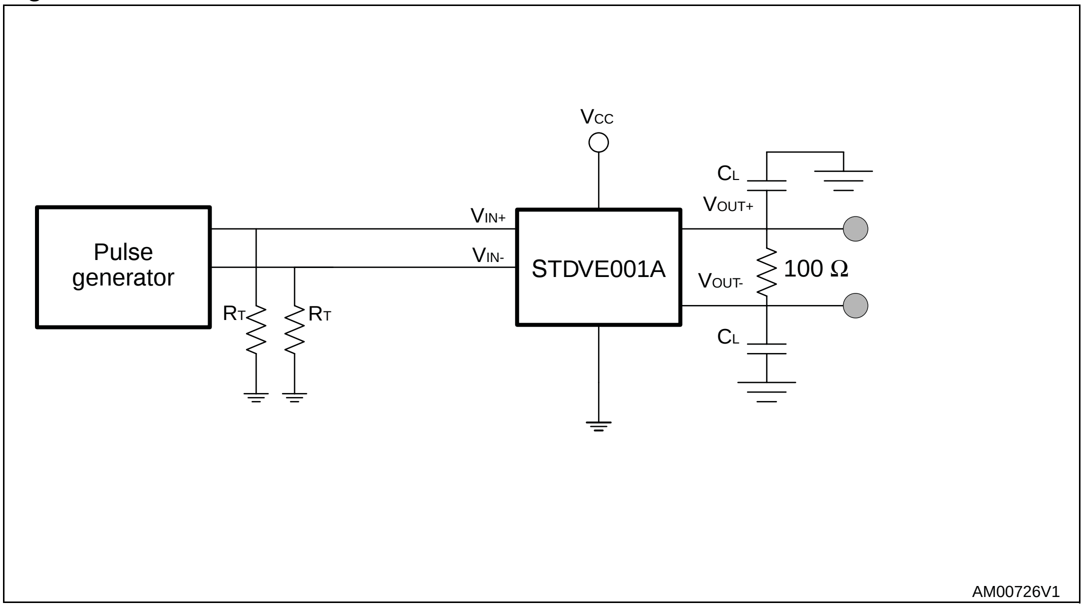
Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
t_r	Output rise time	400 KHz Waveform 1 (*Figure 18*)(2) Voltage on line = 5 V Cmax = 400 pF, Rmax = 2 K			300	ns
		400 KHz Waveform 1 (*Figure 18*)(2) Voltage on line = 3.3 V Cmax = 400 pF, Rmax = 2 K			300	ns
t_r	Output rise time	100 KHz Waveform 1,(2) Voltage on line = 5 V Cmax = 400 pF, Rmax = 2 K			1000	ns
		100 KHz Waveform 1 (*Figure 18*)(2) Voltage on line = 3.3 V Cmax = 400 pF, Rmax = 2 K			1000	ns

1. All the timing values are tested during characterization and are guaranteed by design and simulation. Not tested in production.
2. The t_r transition time is specified with maximum load of 2 kΩ pull-up resistance and 400 pF load capacitance. Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times. Refer to *Figure 10*.

Table 28. ESD performance

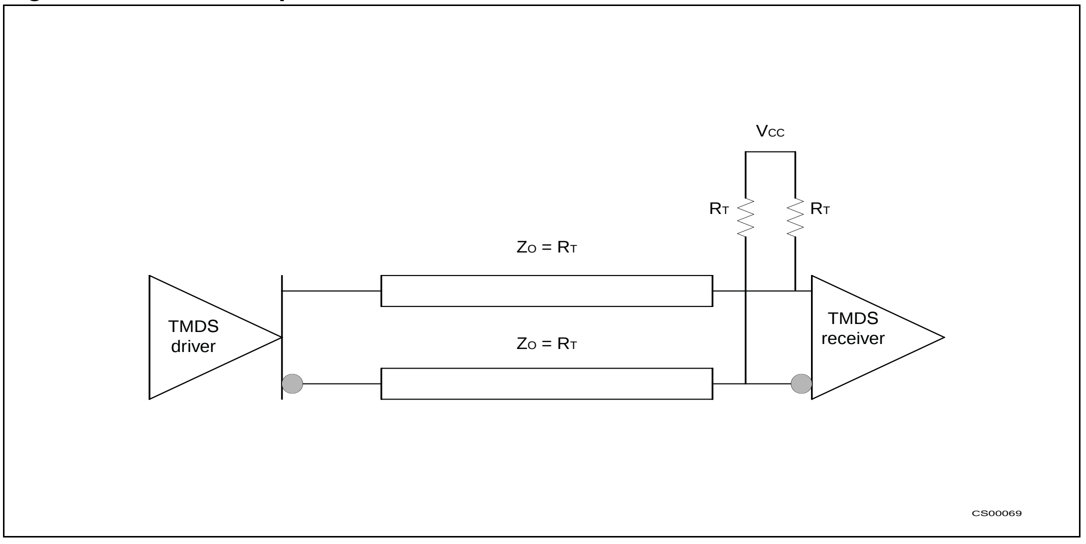
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ESD	All I/Os	Contact discharge as per IEC61000-4-2 standard		8		kV

Figure 8. Test circuit for electrical characteristics



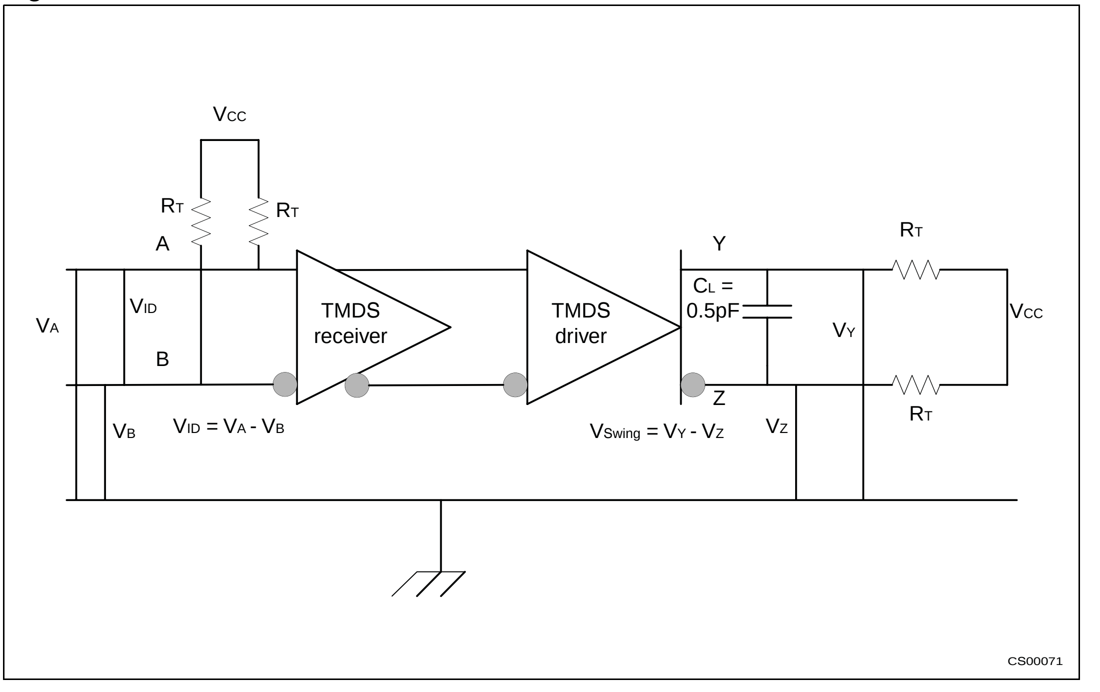
1. C_L = load capacitance: include jig and probe capacitance.
2. R_T = termination resistance; should be equal to Z_{OUT} of the pulse generator.

Figure 9. TMDS output driver



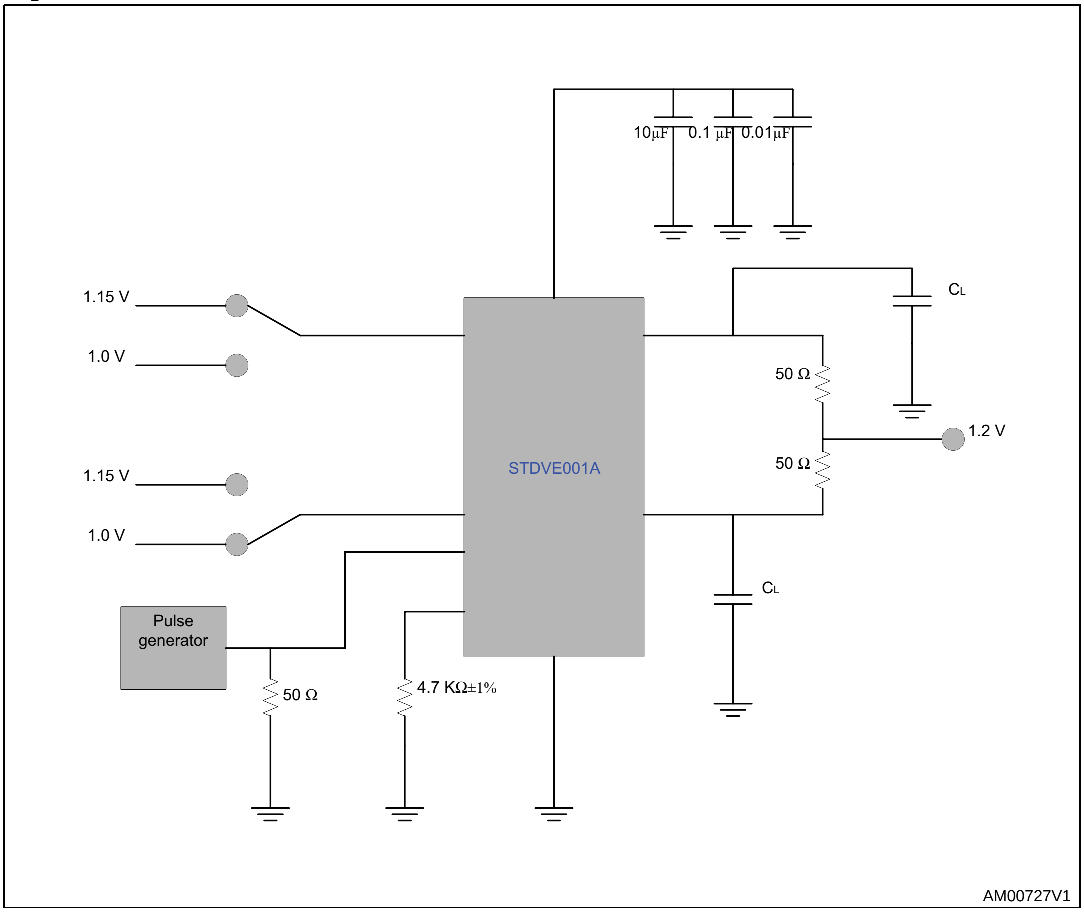
1. Z_O = characteristic impedance of the cable.
2. R_T = termination resistance: should be equal to Z_O of the cable. Both are equal to 50_W.

Figure 10. Test circuit for HDMI receiver and driver



1. $R_T = 50\ \Omega$

Figure 11. Test circuit for turn off and turn off times



1. C_L = 5 pF

Figure 12. Test circuit for short circuit output current

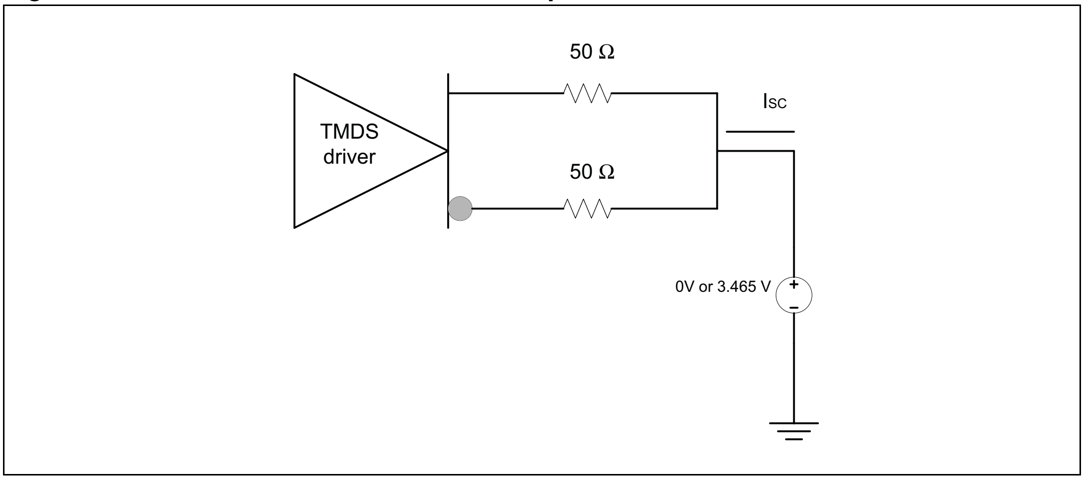


Figure 13. Propagation delays

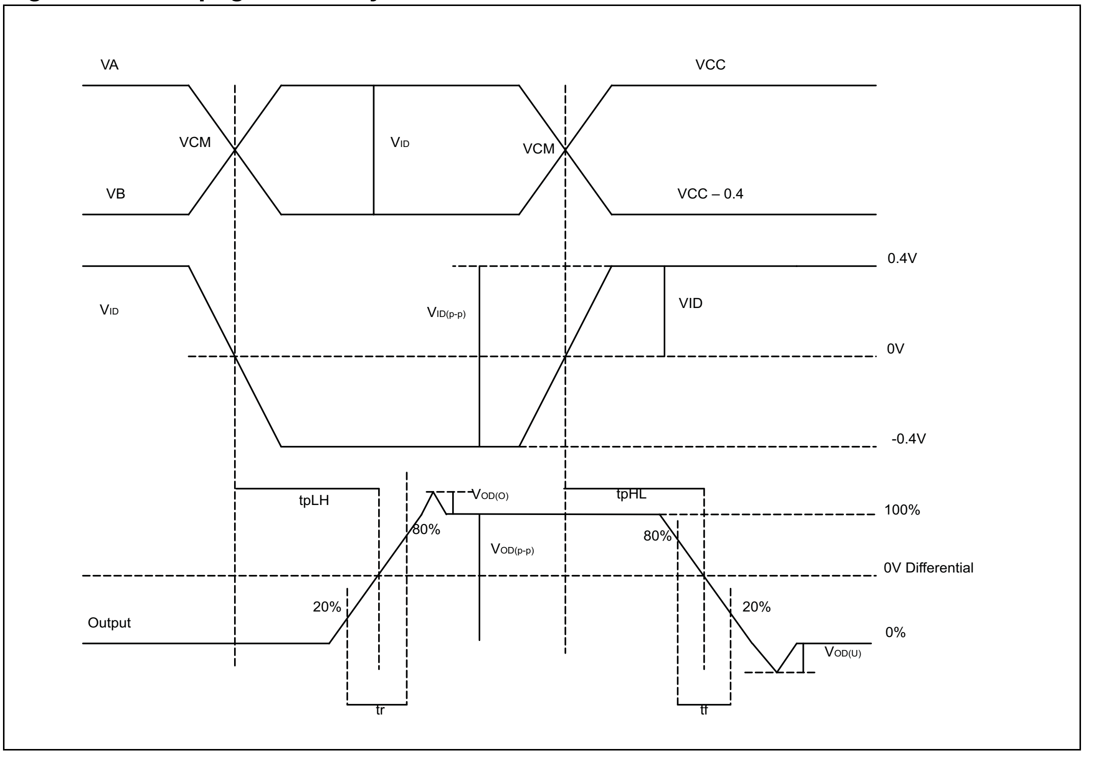


Figure 14. Turn-on and turn-off times

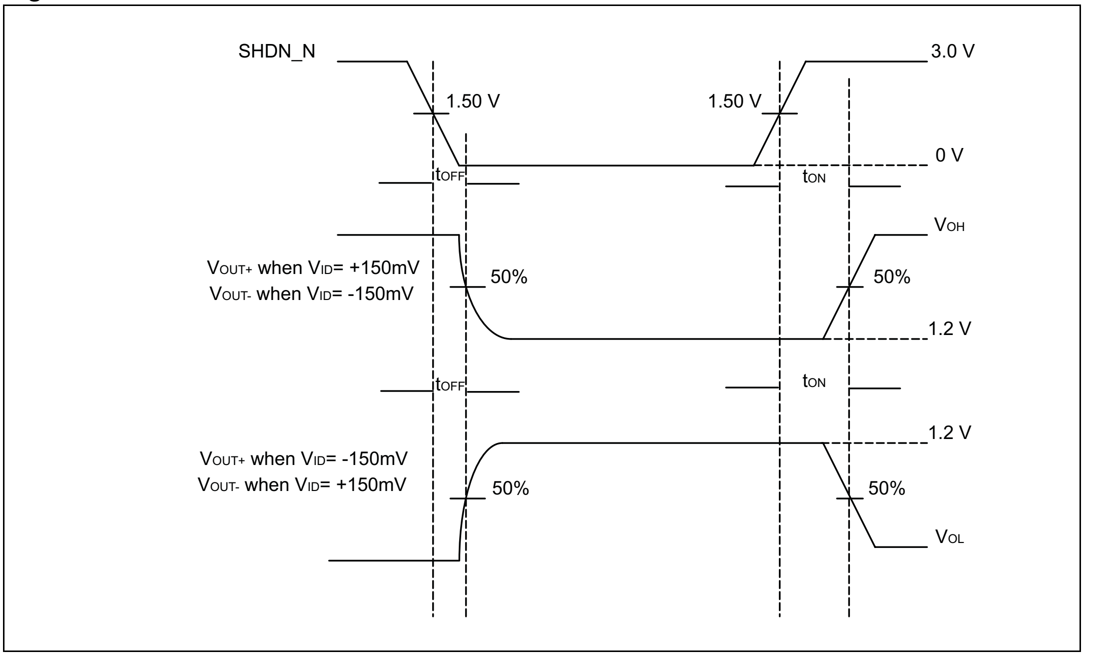


Figure 15. TSK(O)

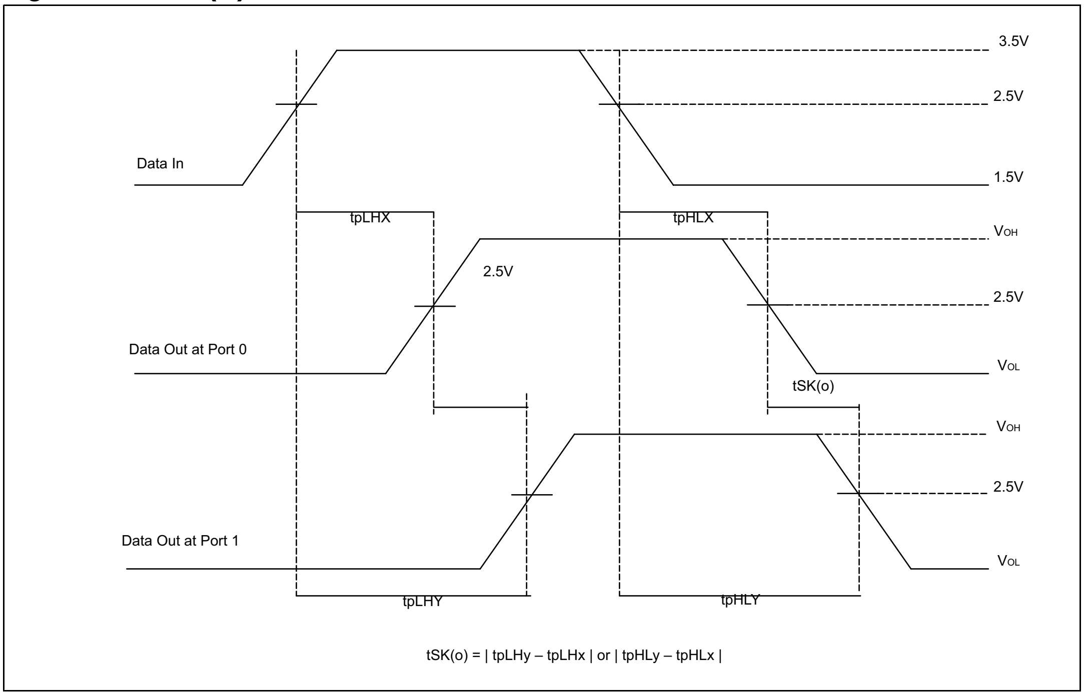


Figure 16. TSK(P)

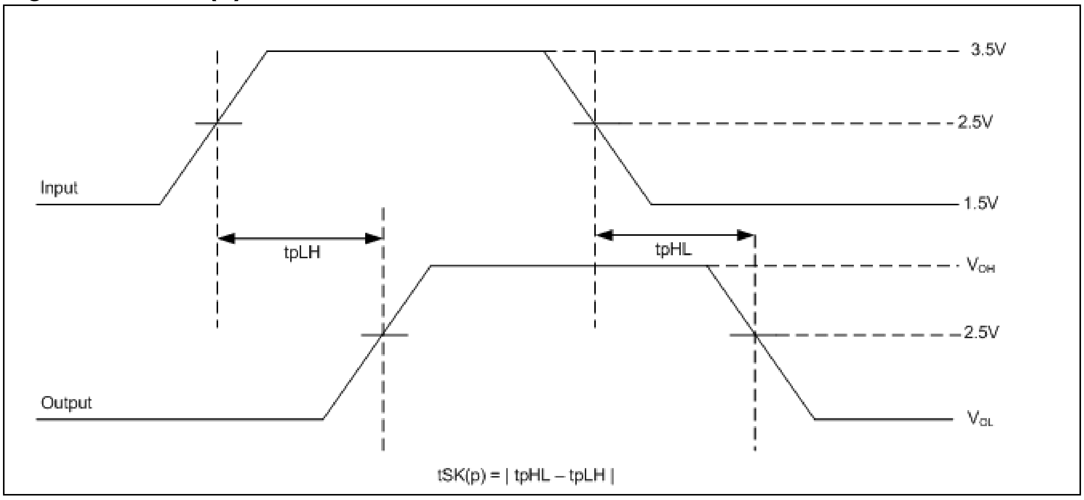


Figure 17. TSK(D)

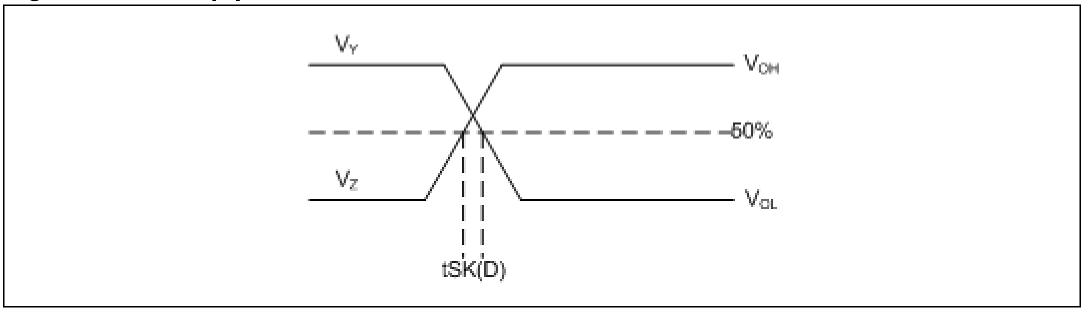


Figure 18. AC waveform 1 (I^2C lines)

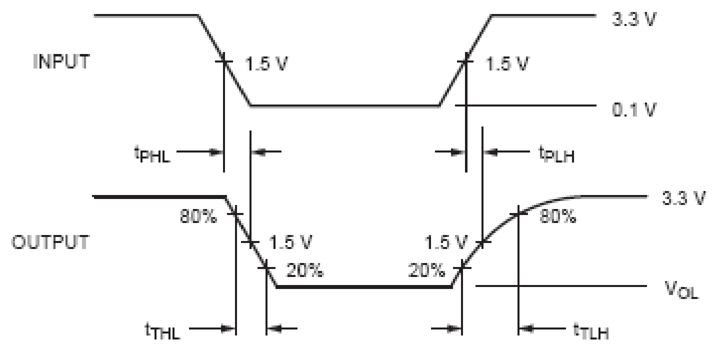
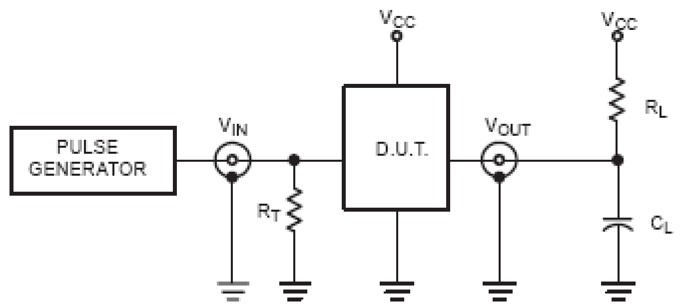


Figure 19. Test circuit for AC measurements (I^2C lines)



Test Circuit for Open Drain Outputs

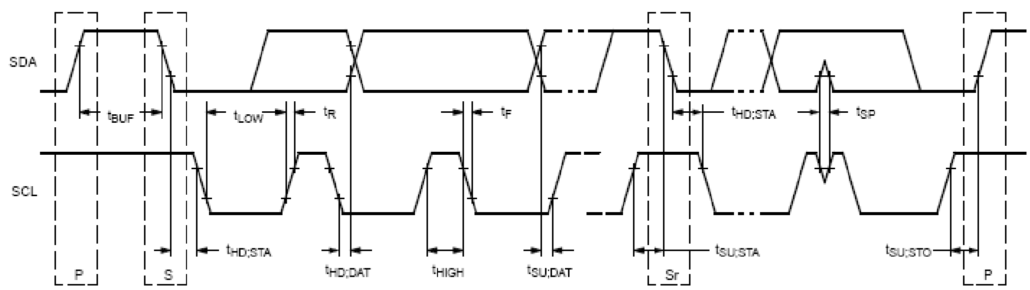
DEFINITIONS

R_L = Load resistor; 1.35 kΩ

C_L = Load capacitance includes jig and probe capacitance; 7 pF

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Figure 20. I^2C bus timing



5 Application information

5.1 Power supply sequencing

Proper power-supply sequencing is advised for all CMOS devices. It is recommended to always apply V_{CC} before applying any signals to the input/output or control pins.

5.2 Power supply requirements

Bypass each of the V_{CC} pins with 0.1 µF and 1 nF capacitors in parallel as close to the device as possible, with the smaller-valued capacitor as close to the V_{CC} pin of the device as possible.

All V_{CC} pins can be tied to a single 3.3 V power source. A 0.01 µF capacitor is connected from each V_{CC} pin directly to ground to filter supply noise. The maximum power supply variation can only be ±5% as per the HDMI specifications.

The maximum tolerable noise ripple on 3.3 V supply must be within a specified limit.

5.3 Differential traces

The high-speed TMDS inputs are the most critical parts for the device. There are several considera-tions to minimize discontinuities on these transmission lines between the connectors and the device.

(a) Maintain 100-Ω differential transmission line impedance into and out of the STDVE001A.

(b) Keep an uninterrupted ground plane below the high-speed I/Os.

(c) Keep the ground-path vias to the device as close as possible to allow the shortest return current path.

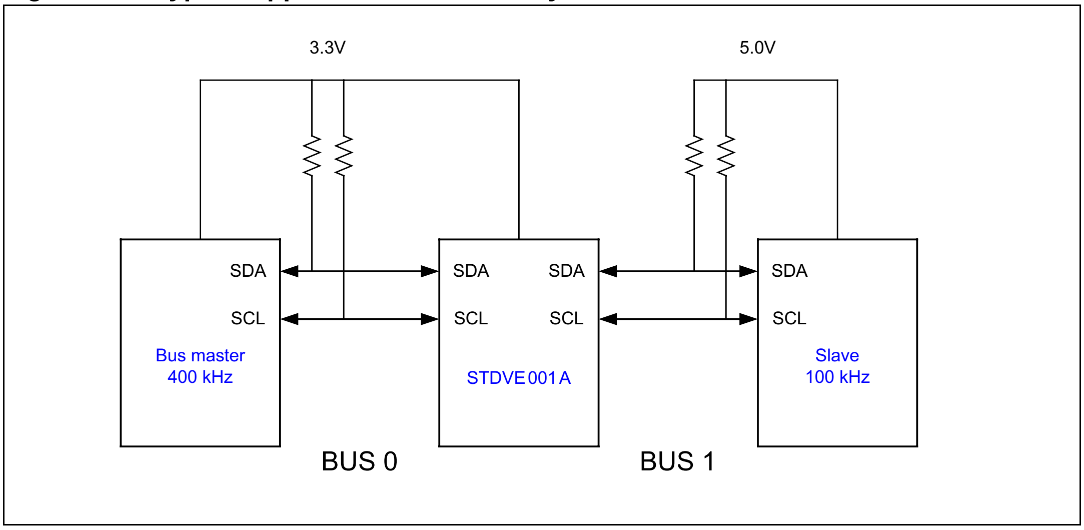
(d) Layout of the TMDS differential inputs should be with the shortest stubs from the connectors.

Output trace characteristics affect the performance of the STDVE001A. Use controlled impedance traces to match trace impedance to both the transmission medium impedance and termination resistor. Run the differential traces close together to minimize the effects of the noise. Reduce skew by matching the electrical length of the traces. Avoid discontinuities in the differential trace layout. Avoid 90 degree turns and minimize the number of vias to further prevent impedance discontinuities.

5.3.1 I²C lines application information

A typical application is shown in the figure below. In the example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 5 V bus. Both buses run at 100 kHz unless the slave bus is isolated and then the master bus can run at 400 kHz. Master devices can be placed on either bus.

Figure 21. Typical application of I²C bus system



The STDVE001A DDC lines are 5 V tolerant; so it does not require any extra circuitry to translate between the different bus voltages.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 22. TQFP48 (7 x 7 mm) package outline

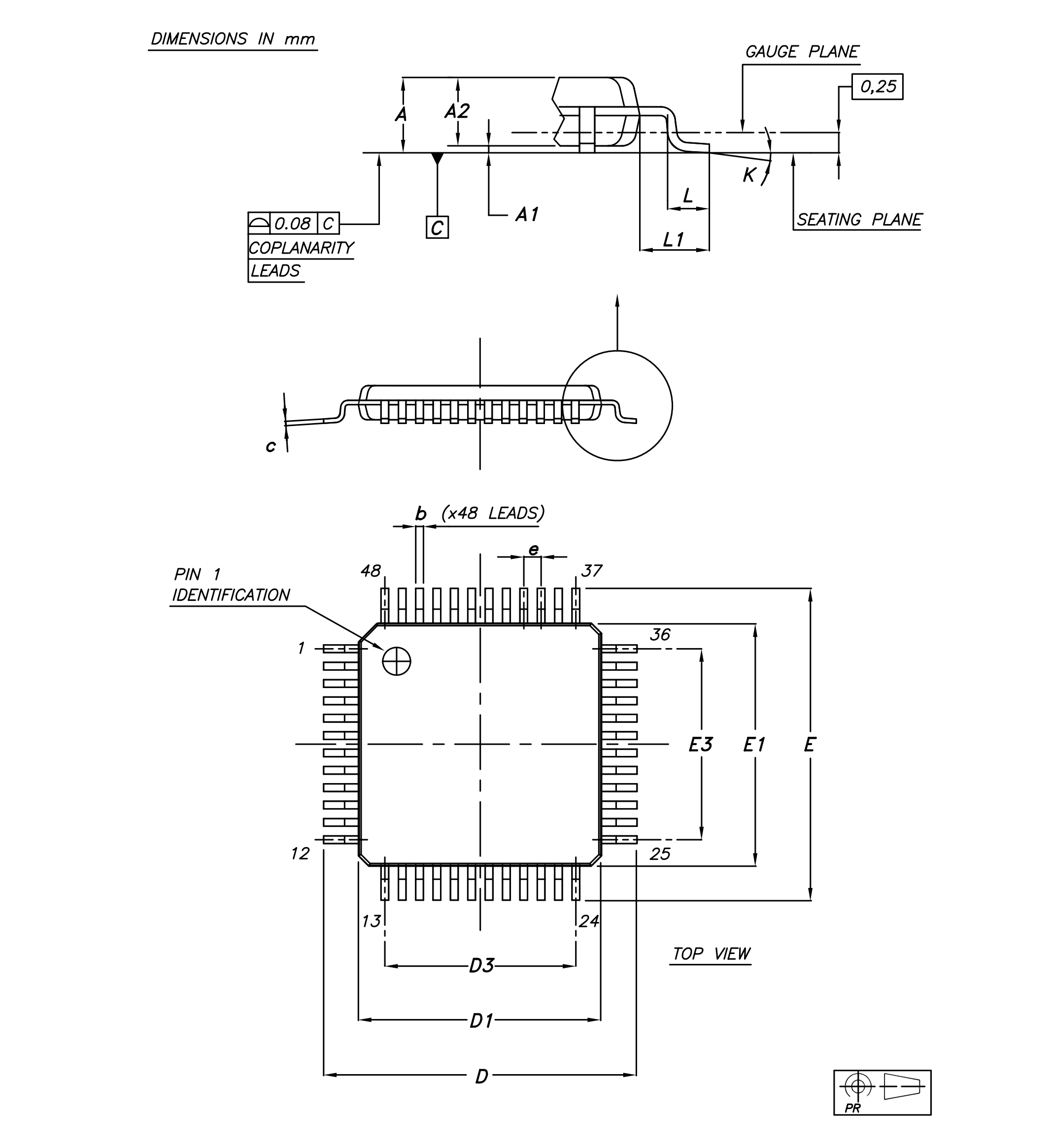


Table 29. TQFP48 (7 x 7 mm) mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A			
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
L	0.45	0.60	0.75
L1		1.00	
T	0.70	0.15	0.20
T1	0.10	0.13	1.15
a	0°		7°
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
e		0.500	
ccc / ddd		0.08	

Figure 23. TQFP48 (7 x 7 mm) footprint recommendation

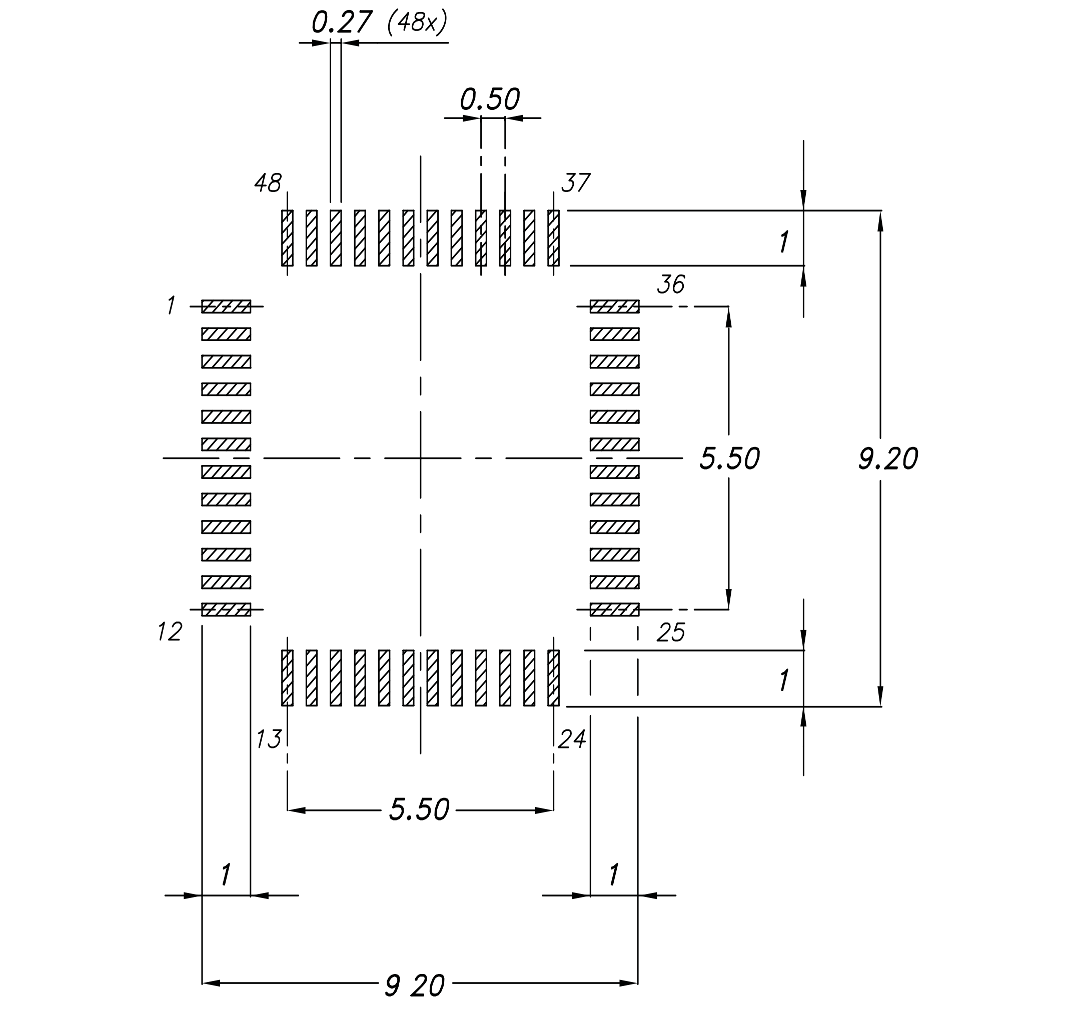
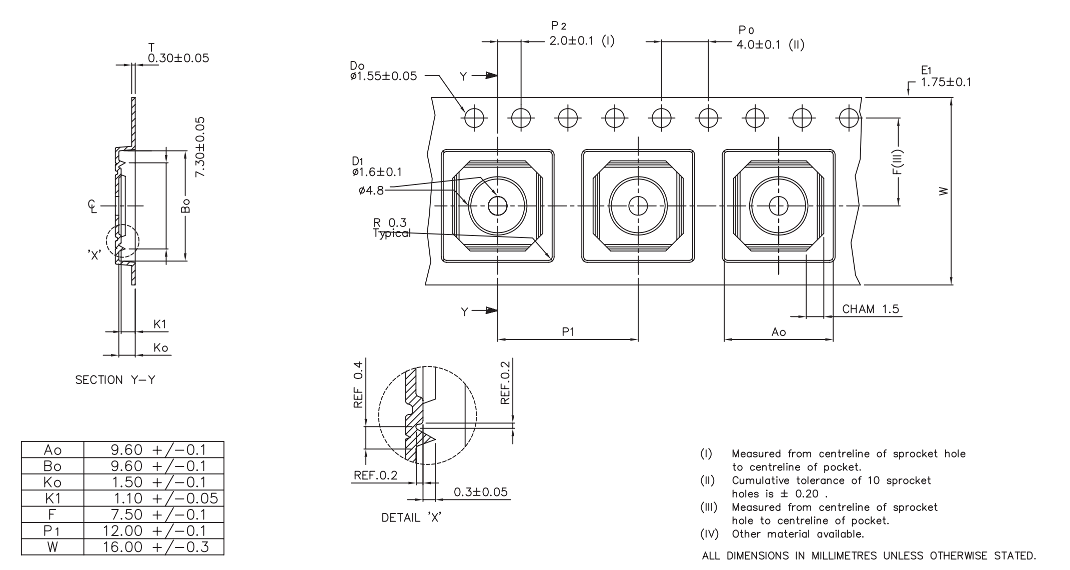


Figure 24. TQFP48 (7 x 7 mm) tape and reel information



Ao	9.60 +/−0.1
Bo	9.60 +/−0.1
Ko	1.50 +/−0.1
K1	1.10 +/−0.05
F	7.50 +/−0.1
P1	12.00 +/−0.1
W	16.00 +/−0.3

Figure 25. QFN48 (7 x 7 mm) package outline

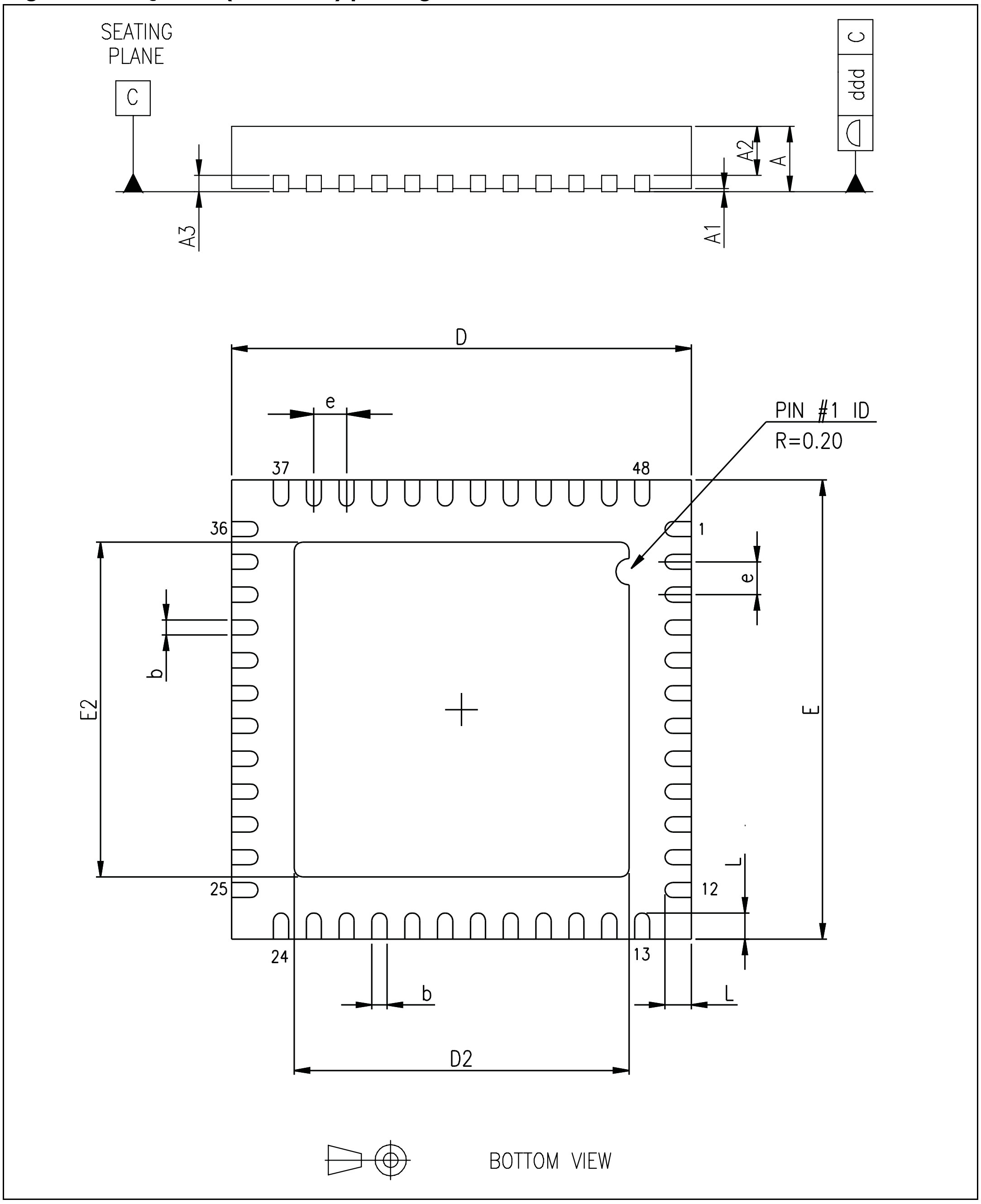


Table 30. QFN48 (7 x 7 mm) package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.90	1.00
A1		0.02	0.05
A2		0.65	1.00
A3		0.25	
b	0.18	0.23	0.30
D	6.85	7.00	7.15
D2	2.25	4.70	5.25
E	6.85	7.00	7.15
E2	2.25	4.70	5.25
e	0.45	0.50	0.55
L	0.30	0.40	0.50
ddd			0.08

7 Revision history

Table 31. Document revision history

Date	Revision	Changes
02-Jul-2008	1	Initial release.
21-Jul-2008	2	Modified: *Figure 2* and *Section 3: Functional description on page 13* Replaced ‘equation’ with ‘equalizer in the Features section.