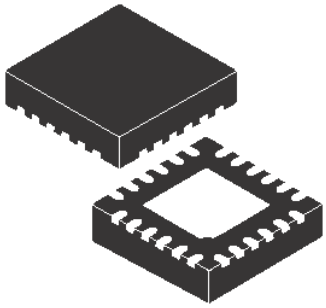
ST8034HN, ST8034HC

24-pin smartcard interfaces

Datasheet - production data



QFN24 4 x 4 x 0.8 mm

Features

- Complete smartcard interface
- ISO 7816, NDS and EMV 4.3 payment systems compatible
- Three protected half-duplex bidirectional buffered I/O lines to the smartcard
- 5 V, 3 V or 1.8 V supply voltage for the smartcard (V_{CC}), pin-selectable. Ensures controlled V_{CC} rise and fall times and provides smart overload detection with glitch immunity.
- Very low power consumption in deep shutdown mode
- Chip select function allows the device interface to be isolated from the microcontroller signals - allows parallel combination of the card interface devices (ST8034HC)
- Card clock generation by integrated crystal oscillator or from external clock source
- Card clock frequency up to 20 MHz, programmable by CLKDIV1 and CLKDIV2 pins (ST8034HN) or by CLKDIV pin (ST8034HC), with synchronous frequency changes
- Automatic activation and deactivation sequences initiated by the microcontroller
- Emergency deactivation sequences initiated by a card supply short-circuit, card take-off, falling V_{DD}, V_{DDP}, or $V_{DD(INTF)}$ or by the interface device overheating
- Voltage supply supervisors
  - with a fixed threshold (V_{DD}, V_{DDP})
  - with an external resistor divider to set the $V_{DD(INTF)}$ threshold (PORADJ pin)
- Multipurpose card status signal $\overline{OFF}$
- Non-inverted card reset pin RST driven by the RSTIN input
- Thermal and short-circuit protection of all card contacts
- Card presence detection contacts debounced
- Enhanced card side ESD protection of 8 kV
- Space saving QFN24 4 x 4 x 0.8 mm package
- Temperature range -25 to +85 °C

Applications

Smartcard readers for

- Set-top boxes
- Pay-TV
- Identification
- Banking
- Tachographs

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1 Description

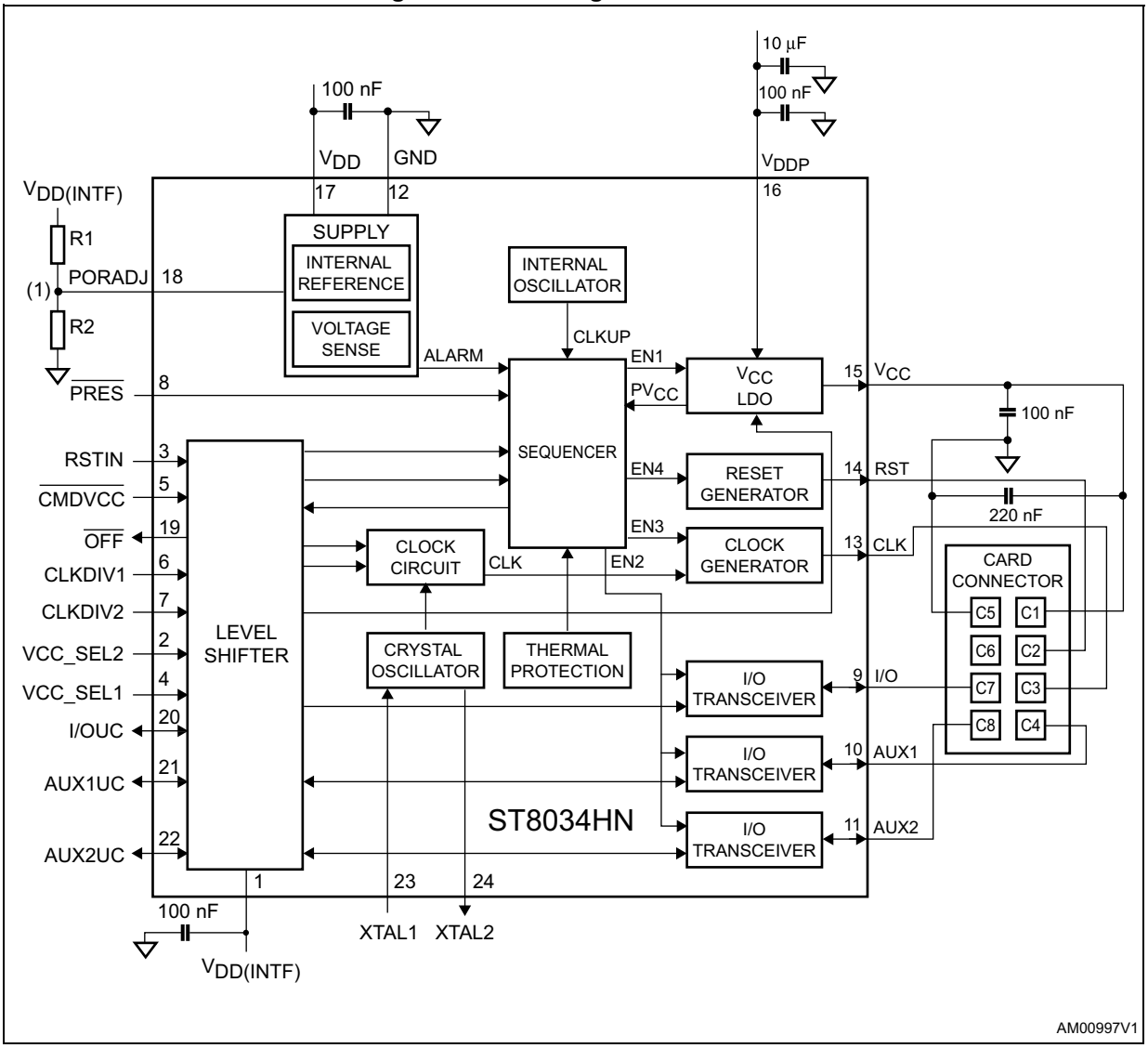
The ST8034HN and ST8034HC devices are complete low-cost analog interfaces for asynchronous and synchronous smartcards operating at a supply voltage of 5 V, 3 V or 1.8 V. The ST8034HN and ST8034HC devices can be placed between the card and the microcontroller to provide all supply, protection, detection and control functions, with just a few external components.

Table 1. Device summary

Order code	PORADJ	V_{CC} selection pins	Chip select	CLKDIV inputs	NDS compliant	Package	Shipment	Package topmark
ST8034HNQR	⋁	⋁		2	⋁	QFN24 4 x 4 x 0.85 mm, 0.5 mm pitch	Tape and reel	8034HN
ST8034HCQR	⋁	⋁	⋁	1	⋁	QFN24 4 x 4 x 0.85 mm, 0.5 mm pitch	Tape and reel	8034HC

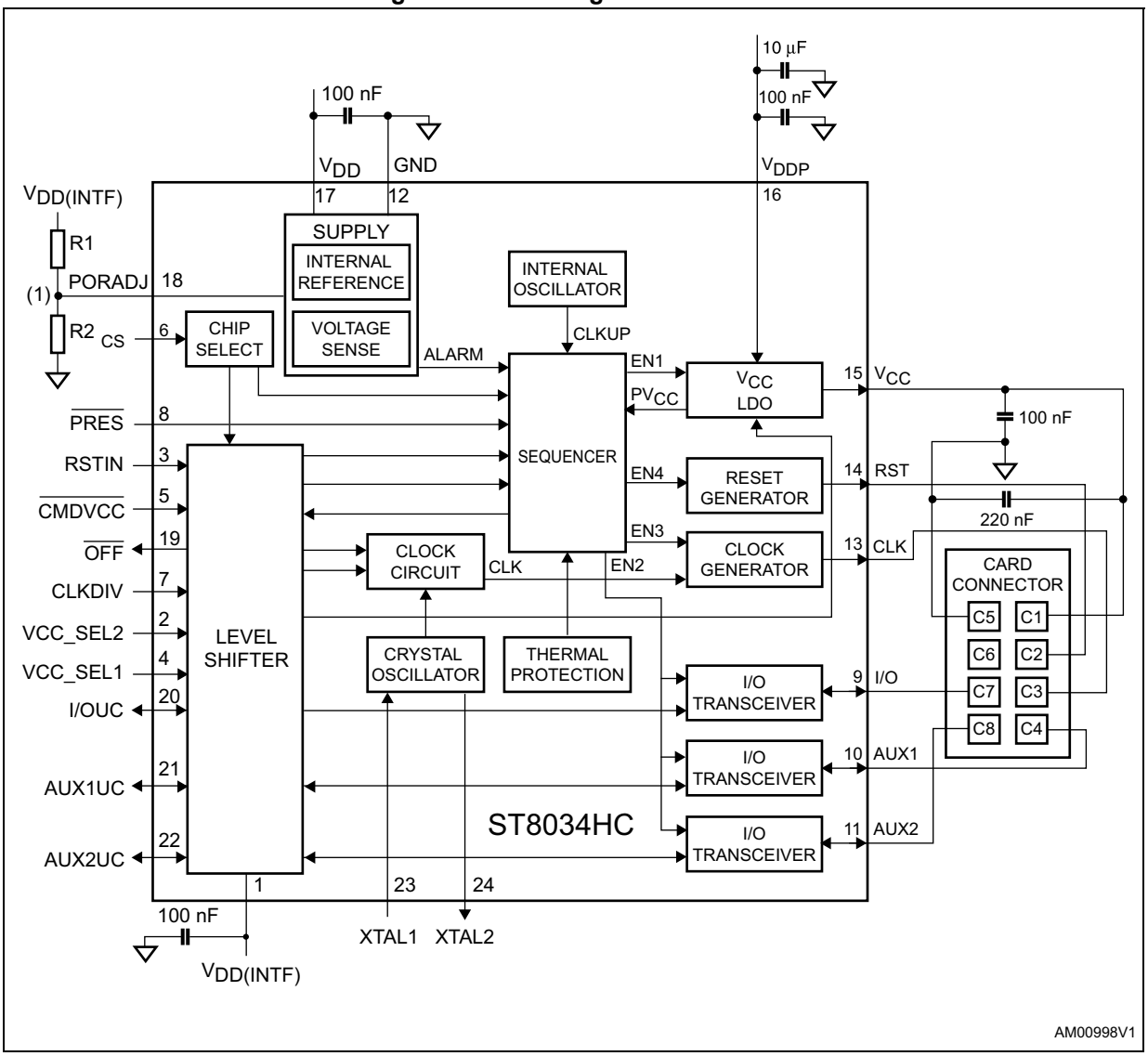
2 Block diagrams

Figure 1. Block diagram ST8034HN



1. Optional external resistor divider. If not used, connect the PORADJ pin to $V_{DD(INTF)}$ for a direct $V_{DD(INTF)}$ voltage monitoring.

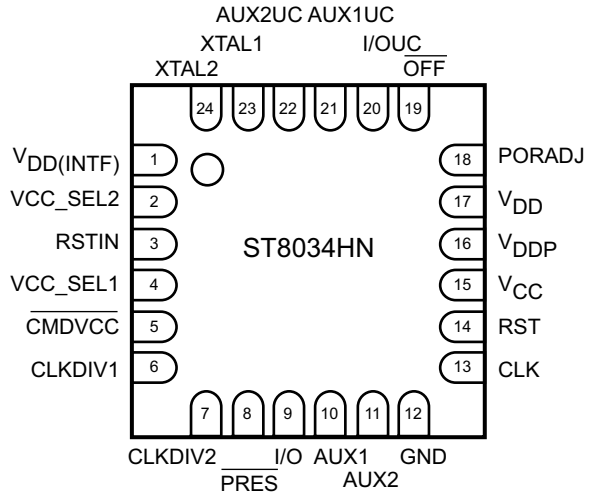
Figure 2. Block diagram ST8034HC



1. Optional external resistor divider. If not used, connect the PORADJ pin to $V_{DD(INTF)}$ for a direct $V_{DD(INTF)}$ voltage monitoring.

3 Pin description

Figure 3. Pin connections ST8034HN (top-through view)



QFN24 - 4 x 4 x 0.8 mm, 0.5 mm pitch. Thermal pad not connected.

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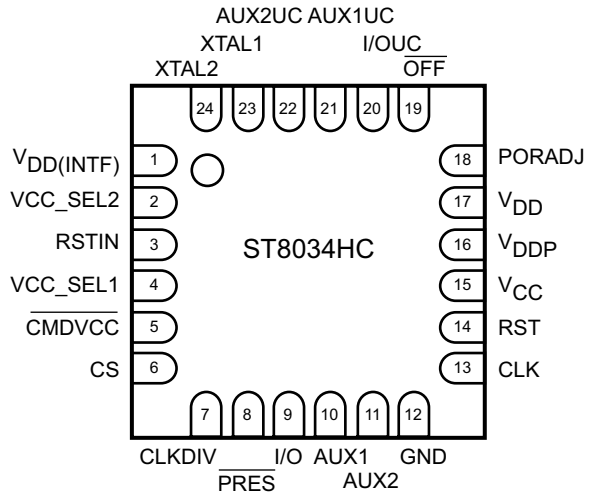
Figure 4. Pin connections ST8034HC (top-through view)



QFN24 - 4 x 4 x 0.8 mm, 0.5 mm pitch. Thermal pad not connected.

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Table 2. Pin description ST8034HN and ST8034HC

Pin number	Symbol	Ref. supply	Function
1	$V_{DD(INTF)}$	$V_{DD(INTF)}$	Microcontroller interface supply voltage
2	VCC_SEL2	$V_{DD(INTF)}$	V_{CC} selection control signal 5 V or 3 V (see *Table 13 on page 27*)
3	RSTIN	$V_{DD(INTF)}$	Card reset input from microcontroller; active high
4	VCC_SEL1	$V_{DD(INTF)}$	V_{CC} selection control signal 1.8 V, overrides VCC_SEL2 (see *Table 13 on page 27*)
5	$\overline{CMDVCC}$	$V_{DD(INTF)}$	Activation sequence start, input (from microcontroller, active low)
6	CLKDIV1	$V_{DD(INTF)}$	CLK frequency division control input (together with CLKDIV2), see *Table 12 on page 21* (ST8034HN)
	CS	$V_{DD(INTF)}$	Chip select input. High = device active, low = all microcontroller interface pins in high impedance (ST8034HC)
7	CLKDIV2	$V_{DD(INTF)}$	CLK frequency division control (together with CLKDIV1), see *Table 12 on page 21* (ST8034HN)
	CLKDIV	$V_{DD(INTF)}$	CLK frequency division control, see *Table 12 on page 21* (ST8034HC)
8	$\overline{PRES}$	$V_{DD(INTF)}$	Card presence input (active low: $\overline{PRES}$ low = card is present). Debounced.
9	I/O	V_{CC}	Card input/output data line (C7); internal 9 kΩ pull-up resistor to V_{CC}
10	AUX1	V_{CC}	Auxiliary card input/output data line (C4); internal 9 kΩ pull-up resistor to V_{CC}
11	AUX2	V_{CC}	Auxiliary card input/output data line (C8); internal 9 kΩ pull-up resistor to V_{CC}
12	GND		Ground
13	CLK	V_{CC}	Clock to card (C3)
14	RST	V_{CC}	Card reset, output (C2)
15	V_{CC}		Supply voltage for the card, output (C1)
16	V_{DDP}		LDO supply voltage input (for V_{CC} generation)
17	V_{DD}		Control logic supply voltage input
18	PORADJ	$V_{DD(INTF)}$	Power-on reset threshold adjustment input (with an optional external resistor divider)
19	$\overline{OFF}$	$V_{DD(INTF)}$	Interrupt to microcontroller (active low output); internal 20 kΩ pull-up resistor to $V_{DD(INTF)}$
20	I/OUC	$V_{DD(INTF)}$	Microcontroller data I/O line (with internal 10 kΩ pull-up resistor connected to $V_{DD(INTF)}$)
21	AUXUC1	$V_{DD(INTF)}$	Auxiliary microcontroller input/output data line; internal 10 kΩ pull-up resistor to $V_{DD(INTF)}$
22	AUXUC2	$V_{DD(INTF)}$	Auxiliary microcontroller input/output data line; internal 10 kΩ pull-up resistor to $V_{DD(INTF)}$
23	XTAL1	V_{DD}	Crystal or external clock input
24	XTAL2	V_{DD}	Crystal connection (leave this pin open if external clock is used)

4 Maximum ratings

Table 3. Absolute maximum ratings(1), (2)

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply voltage, logic	-0.3	6	V
V_{DDP}	Supply voltage, power	-0.3	6	V
$V_{DD(INTF)}$	Supply voltage, interface	-0.3	6	V
V_{IN}	Input voltage on XTAL1, XTAL2, RSTIN, I/OUC, AUX1UC, AUX2UC, CLKDIV1, CLKDIV2, CS, VCC_SEL1, VCC_SEL2, PORADJ, CMDVCC, OFF, PRES, I/O, AUX1, and AUX2 pins	-0.3	6	V
$V_{ESD\ (HBM)}$	Human body model (HBM) on card lines - I/O, RST, V_{CC}, CLK, and PRES pins	-8	8	kV
	Human body model (HBM), all other pins	-2	2	kV
$V_{ESD\ (MM)}$	Machine model (MM), all pins	-200	200	V
$V_{ESD\ (FCDM)}$	Field charged device model (FCDM), all pins	-500	500	V
P_{TOT}	Total power dissipation (T_A = -25 to +85 °C)		0.25	W
$T_{J(MAX)}$	Maximum operating junction temperature		125	°C
T_{STG}	Storage temperature range	-55	150	°C

1. Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
2. All card contacts are protected against short-circuit to any other card contact.

Table 4. Thermal data

Symbol	Parameter	Test conditions	Typ.	Unit
R_{THJA}	Thermal resistance junction-ambient temperature (multilayer test board - JEDEC standard)	QFN24	47	°C/W

Table 5. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Max.	Unit
T_A	Ambient temperature range		-25	85	°C

5 Electrical characteristics

Electrical characteristics over recommended operating conditions

Table 6. Supply voltages

Symbol	Parameter	Test conditions(1)	Min.	Typ.	Max.	Unit
Device supply voltages						
V_{DD}	Supply voltage, logic		2.7	3.3	3.6(2)	V
V_{DDP}	Supply voltage, power	V_{CC} = 5 V	4.85	5	5.5	V
		V_{CC} = 3 V or 1.8 V	3	3.3	5.5	
$V_{DD(INTF)}$	Supply voltage, microcontroller interface		1.6	3.3	V_{DD} +0.3(3)	V
I_{DD}	Supply current, logic	Shutdown mode			35	µA
		Deep shutdown mode			12	
		Active mode			2	mA
I_{DDP}	Supply current, power	Shutdown mode, f_{XTAL} stopped			5	µA
		Active mode, $f_{CLK} = f_{XTAL}/2$, no I_{CC} load			1.5	mA
		Active mode, $f_{CLK} = f_{XTAL}/2$, I_{CC} = 65 mA			70	
$I_{DD(INTF)}$	Supply current, interface	Shutdown mode			6	µA
		Active mode			2	mA
Card supply voltage						
V_{CC}	Card supply voltage (output)(4)	Active mode, V_{CC} = 5 V, I_{CC} < 65 mA	4.75	5.0	5.25	V
		With current pulses of 40 nAs at I_{CC} < 200 mA, t < 400 ns(5)	4.65	5.0	5.25	
		Active mode, V_{CC} = 3 V, I_{CC} < 65 mA	2.85	3.05	3.15	
		With current pulses of 40 nAs at I_{CC} < 200 mA, t < 400 ns(5)	2.76		3.20	
		Active mode, V_{CC} = 1.8 V, I_{CC} < 65 mA	1.71	1.83	1.89	
		With current pulses of 15 nAs at I_{CC} < 200 mA, t < 400 ns(5)	1.66		1.94	
I_{CC}	Card supply current (refer also to *Table 10: Protection characteristics on page 17*)	V_{CC} = 5 V, 3 V or 1.8 V			65	mA
		V_{CC} shorted to GND	90	120	150	
C_{VCC}	V_{CC} decoupling capacitor (4)	V_{CC} to GND	160	320	530	nF
SR	V_{CC} slew rate (rising or falling)(4)	V_{CC} = 5 V	0.055	0.180	0.300	V/µs
		V_{CC} = 3 V	0.040	0.180	0.300	
		V_{CC} = 1.8 V	0.025	0.180	0.300	

Table 6. Supply voltages (continued)

Symbol	Parameter	Test conditions[1]	Min.	Typ.	Max.	Unit
$V_{CC(SHDN)}$	V_{CC} output voltage in shutdown mode	No load	-0.1		0.1	V
		I_{CC} = 1 mA	-0.1		0.3	
$I_{CC(SHDN)}$	V_{CC} output current in shutdown mode	V_{CC} connected to GND			-1	mA
Device supply voltages monitoring						
V_{TH}	Falling supply voltage threshold	V_{DD} pin	2.3	2.4	2.5	V
		V_{DDP} pin (V_{CC} = 5 V)	3.0	4.1	4.4	
		V_{DDP} pin (V_{CC} = 3 V or 1.8 V)	2.3	2.4	2.5	
		PORADJ pin	1.20	1.24	1.29	
V_{HYS}	Hysteresis on supply voltage threshold	V_{DD} pin	50	100	150	mV
		V_{DDP} pin (V_{CC} = 5 V)	100	200	350	
		V_{DDP} pin (V_{CC} = 3 V or 1.8 V)	50	100	150	
		PORADJ pin	10	20	30	
$I_{I(PORADJ)}$	Input current, PORADJ pin		-1		1	µA
t_W	Power-on or undervoltage reset pulse width (minimum)		5.1	8	10.2	ms

1. T_A = 25 °C, V_{DD} = 3.3 V, V_{DDP} = 5 V, $V_{DD(INTF)}$ = 3.3 V, f_{XTAL} = 10 MHz, unless otherwise noted.
2. The device can operate at V_{DD} supply voltage up to 5.5 V, however the specified parameters (mainly related to current consumption) are guaranteed in the basic V_{DD} range 2.7 to 3.6 V.
3. The device can operate at $V_{DD(INTF)}$ supply voltage up to 5.5 V, however the specified parameters (mainly related to current consumption and input currents) are guaranteed in the basic $V_{DD(INTF)}$ range 1.6 to 3.6 V.
4. Two low ESR (< 350 mΩ) ceramic capacitors for V_{CC} decoupling recommended: 100 nF ± 20% (up to 330 nF ± 20%) close to the ST8034 and 100 nF ± 20% (up to 330 nF ± 20%) close to the card.
5. These current pulses are filtered by the decoupling capacitors on the V_{CC} pin, therefore for the LDO just the mean value matters.

Table 7. Card interface

Symbol	Parameter	Test conditions[1]	Min.	Typ.	Max.	Unit
Data lines to the card (I/O, AUX1, AUX2 pins)[2]						
t_D	Delay time	Falling edge on pin I/O to falling edge on I/OUC or vice versa			200	ns
$t_{W(PU)}$	Pull-up pulse width		100		400	ns
f_{IO}	Input/output frequency				1	MHz
C_I	Input capacitance				10	pF
V_O	Output voltage in shutdown mode	No load	0		0.1	V
		I_O = 1 mA	0		0.3	V
I_O	Output current in shutdown mode	I/O connected to GND			-1	mA
V_{OL}	Output voltage low	I_{OL} = 1 mA	0		0.3	V
		$I_{OL} \geq$ 15 mA (current limit)	V_{CC} - 0.4		V_{CC}	
V_{OH}	Output voltage high	No load	0.9 V_{CC}		V_{CC} + 0.1	V
		I_{OH} < -40 µA, 5 V or 3 V	0.75 V_{CC}		V_{CC} + 0.1	
		I_{OH} < -20 µA, 1.8 V	0.75 V_{CC}		V_{CC} + 0.1	
		$I_{OH} \geq$ -15 mA (current limit)	0		0.4	
V_{IL}	Input voltage low		-0.3		0.8	V
V_{IH}	Input voltage high	V_{CC} = 5 V	0.6 V_{CC}		V_{CC} + 0.3	V
		V_{CC} = 3 V or 1.8 V	0.7 V_{CC}		V_{CC} + 0.3	
V_{HYS}	Hysteresis	I/O pin		50		mV
I_{IL}	Input current low	I/O pin, V_{IL} = 0 V			750	µA
I_{IH}	Input current high	I/O pin, V_{IH} = V_{CC}			10	µA
$t_{R(I)}$	Input rise time	V_{IL} max. to V_{IH} min.			0.15	µs
$t_{R(O)}$	Output rise time	$C_L \leq$ 80 pF, 10% to 90%, 0 V to V_{CC}			0.1	µs
$t_{F(I)}$	Input fall time	V_{IL} max. to V_{IH} min.			0.15	µs
$t_{F(O)}$	Output fall time	$C_L \leq$ 80 pF, 10% to 90%, 0 V to V_{CC}			0.1	µs
R_{PU}	Pull-up resistance to V_{CC}		7	9	11	kΩ
I_{PU}	Pull-up current (one-shot circuit active)	V_{OH} = 0.9 V_{CC}	-8	-6	-4	mA
Reset output to the card (RST pin)						
V_O	Output voltage in shutdown mode	No load	0		0.1	V
		I_O = 1 mA	0		0.3	
I_O	Output current in shutdown mode	RST connected to GND			-1	mA
t_D	Delay time	Between RSTIN and RST; RST enabled			2	µs

Table 7. Card interface (continued)

Symbol	Parameter	Test conditions[1]	Min.	Typ.	Max.	Unit
V_{OL}	Output voltage low	I_{OL} = 200 µA, V_{CC} = 5 V	0		0.3	V
		I_{OL} = 200 µA, V_{CC} = 3 V or 1.8 V	0		0.2	
		I_{OL} = 20 mA (current limit)	V_{CC} - 0.4		V_{CC}	
V_{OH}	Output voltage high	I_{OH} = -200 µA	0.9 V_{CC}		V_{CC}	V
		I_{OH} = -20 mA (current limit)	0		0.4	
t_R	Rise time	C_L = 100 pF			0.1	µs
t_F	Fall time	C_L = 100 pF			0.1	
Clock output to the card (CLK pin)						
V_O	Output voltage in shutdown mode	No load	0		0.1	V
		I_O = 1 mA	0		0.3	
I_O	Output current in shutdown mode	CLK connected to GND			-1	mA
V_{OL}	Output voltage low	I_{OL} = 200 µA	0		0.3	V
		I_{OL} = 70 mA (current limit)	V_{CC} - 0.4		V_{CC}	
V_{OH}	Output voltage high	I_{OH} = -200 µA	0.9 V_{CC}		V_{CC}	V
		I_{OH} = -70 mA (current limit)	0		0.4	
t_R	Rise time[3]	C_L = 30 pF			16	ns
t_F	Fall time[3]	C_L = 30 pF			16	ns
f_{CLK}	Frequency on pin CLK	Operational	0		20	MHz
DC	Duty cycle[3]	C_L = 30 pF	45		55	%
SR	Slew rate (rise and fall, C_L = 30 pF)	V_{CC} = 5 V	0.2			V/ns
		V_{CC} = 3 V or 1.8 V	0.12			
Card detection input ($\overline{\text{PRES}}$ pin)[4]						
V_{IL}	Input voltage low		-0.3		0.3 $V_{DD(INTF)}$	V
V_{IH}	Input voltage high		0.7 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.3	V
V_{HYS}	Hysteresis			0.14 $V_{DD(INTF)}$		V
I_{IL}	Input current low	0 < V_{IL} < $V_{DD(INTF)}$			5	µA
I_{IH}	Input current high	0 < V_{IH} < $V_{DD(INTF)}$			5	µA

1. T_A = 25 °C, V_{DD} = 3.3 V, V_{DDP} = 5 V, $V_{DD(INTF)}$ = 3.3 V, f_{XTAL} = 10 MHz, unless otherwise noted.
2. With an internal 9 kΩ pull-up resistor to V_{CC}.
3. For rise and fall times and duty cycle definitions, see *Figure 5 on page 18*.
4. $\overline{\text{PRES}}$ is active low, with an internal current source of 1.25 µA (pull-up) to $V_{DD(INTF)}$.

Table 8. Microcontroller interface

Symbol	Parameter	Test conditions[1]	Min.	Typ.	Max.	Unit
Data lines to the microcontroller (I/OUC, AUX1UC, AUX2UC pins)[2]						
t_D	Delay time	Falling edge on pin I/O to falling edge on I/OUC or vice versa			200	ns
$t_{W(PU)}$	Pull-up pulse width		100		400	ns
f_{IO}	Input/output frequency				1	MHz
C_I	Input capacitance				10	pF
V_{OL}	Output voltage low	I_{OL} = 1 mA	0		0.3	V
V_{OH}	Output voltage high	No load	0.9 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.1	V
		$I_{OH} \leq$ -40 µA; $V_{DD(INTF)}$ > 2 V	0.75 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.1	
		$I_{OH} \leq$ -20 µA; $V_{DD(INTF)}$ < 2 V	0.75 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.1	
V_{IL}	Input voltage low		-0.3		0.3 $V_{DD(INTF)}$	V
V_{IH}	Input voltage high		0.7 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.3	V
V_{HYS}	Hysteresis	I/OUC pin		0.14 $V_{DD(INTF)}$		V
I_{IL}	Input current low	V_{IL} = 0 V			500	µA
I_{IH}	Input current high	$V_{IH} = V_{DD(INTF)}$			10	µA
R_{PU}	Pull-up resistance to $V_{DD(INTF)}$		8	10	12	kΩ
I_{PU}	Pull-up current (one-shot circuit active)	V_{OH} = 0.9 $V_{DD(INTF)}$	-1			mA
$t_{R(I)}$	Input rise time	V_{IL} max. to V_{IH} min.			0.15	µs
$t_{R(O)}$	Output rise time	$C_L \leq$ 30 pF, 10% to 90%, 0 V to $V_{DD(INTF)}$			0.1	µs
$t_{F(I)}$	Input fall time	V_{IL} max. to V_{IH} min.			0.15	µs
$t_{F(O)}$	Output fall time	$C_L \leq$ 30 pF, 10% to 90%, 0 V to $V_{DD(INTF)}$			0.1	µs
Device control inputs (CLKDIV1, CLKDIV2, RSTIN, VCC_SEL1, VCC_SEL2, CS pins)[3]						
V_{IL}	Input voltage low		-0.3		0.3 $V_{DD(INTF)}$	V
V_{IH}	Input voltage high		$V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.3	V
V_{HYS}	Hysteresis			0.14 $V_{DD(INTF)}$		V

Table 8. Microcontroller interface (continued)

Symbol	Parameter	Test conditions[1]	Min.	Typ.	Max.	Unit
I_{IL}	Input current low				1	µA
I_{IH}	Input current high				1	µA
Control input $\overline{CMDVCC}$[4]						
V_{IL}	Input voltage low		-0.3		0.3 $V_{DD(INTF)}$	V
V_{IH}	Input voltage high		0.7 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.3	V
V_{HYS}	Hysteresis			0.14 $V_{DD(INTF)}$		V
I_{IL}	Input current low	V_{IL} = 0 V			1	µA
I_{IH}	Input current high	$V_{IH} = V_{DD(INTF)}$			1	µA
$f_{\overline{CMDVCC}}$	Frequency at $\overline{CMDVCC}$ pin				100	Hz
$\overline{OFF}$ output[5]						
V_{OL}	Output voltage low	I_{OL} = 2 mA	0		0.3	V
V_{OH}	Output voltage high	I_{OH} = -15 µA	0.75 $V_{DD(INTF)}$			V
R_{PU}	Pull-up resistance to $V_{DD(INTF)}$		16	20	24	kΩ

1. T_A = 25 °C, V_{DD} = 3.3 V, V_{DDP} = 5 V, $V_{DD(INTF)}$ = 3.3 V, f_{XTAL} = 10 MHz, unless otherwise noted.
2. With an internal 10 kΩ pull-up resistor to $V_{DD(INTF)}$.
3. For clock frequency division control (CLKDIV), see *Table 12 on page 21*.
4. $\overline{CMDVCC}$ is active low.
5. $\overline{OFF}$ is an NMOS open drain, with an internal 20 kΩ pull-up resistor to $V_{DD(INTF)}$. The pull-up is connected only when used (i.e. when $\overline{OFF}$ = high), otherwise disconnected.

Table 9. Clock circuits

Symbol	Parameter	Test conditions(1)	Min.	Typ.	Max.	Unit
Internal oscillator						
$f_{OSC(INT)LOW}$	Internal oscillator frequency	Shutdown mode	100	150	200	kHz
$f_{OSC(INT)}$		Active state	2	2.7	3.2	MHz
Crystal oscillator (XTAL1 and XTAL2 pins)						
C_{EXT}	External capacitances	XTAL1 and XTAL2 to GND (according to the crystal or resonator specification)			15	pF
f_{XTAL}	External crystal frequency	Card clock reference, crystal oscillator	2		26	MHz
f_{EXT}	External clock frequency	External clock on XTAL1	0.032		26	MHz
$t_{R(fEXT)}$	External clock frequency rise time	External clock on XTAL1			10	ns
$t_{F(fEXT)}$	External clock frequency fall time	External clock on XTAL1			10	ns
V_{IL}	Input voltage low	Crystal oscillator	-0.3		0.3 V_{DD}	V
		External clock on XTAL1	-0.3		0.3 $V_{DD(INTF)}$	
V_{IH}	Input voltage high	Crystal oscillator	0.7 V_{DD}		V_{DD} + 0.3	V
		External clock on XTAL1	0.7 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.3	

1. T_A = 25 °C, V_{DD} = 3.3 V, V_{DDP} = 5 V, $V_{DD(INTF)}$ = 3.3 V, f_{XTAL} = 10 MHz, unless otherwise noted.

Table 10. Protection characteristics

Symbol	Parameter	Test conditions(1)	Min.	Typ.	Max.	Unit
I_{OLIM}	Output current limit(2)	I/O pin	-15		15	mA
		CLK pin	-70		70	
		RST pin	-20		20	
$I_{SD(VCC)}$	Limit and shutdown card supply current	V_{CC} pin	90	120	150	mA
T_{SD}	Shutdown junction temperature			150		°C

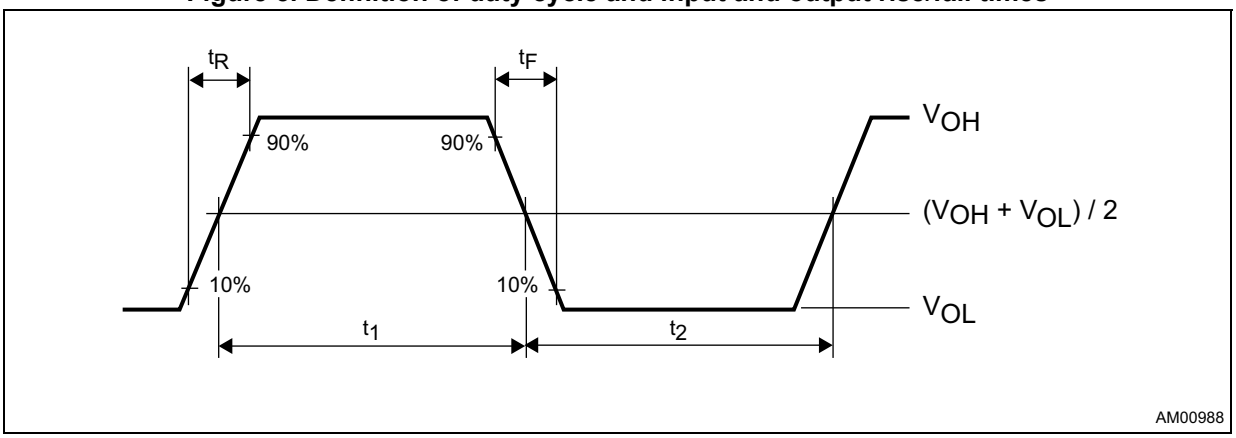
1. T_A = 25 °C, V_{DD} = 3.3 V, V_{DDP} = 5 V, $V_{DD(INTF)}$ = 3.3 V, f_{XTAL} = 10 MHz, unless otherwise noted.
2. All card contacts are protected against short-circuit to any other card contact.

Table 11. Timing characteristics

Symbol	Parameter	Test conditions[1]	Min.	Typ.	Max.	Unit
t_{ACT}	Activation time	See *Figure 10 on page 24*	2090		4160	µs
t_{DEACT}	Deactivation time	See *Figure 11 on page 25*	35	90	250	µs
$t_{D(START)}$, $t_{D(END)}$	Delay time, CLK sent to card using an external clock	$t_{D(START)} = t_3$, see *Figure 10 on page 24*	2090		4112	µs
		$t_{D(END)} = t_5$, see *Figure 10 on page 24*	2120		4160	
t_{DEB}	Debounce time	$\overline{PRES}$ pin	3.2	4.5	6.4	ms

1. T_A = 25 °C, V_{DD} = 3.3 V, V_{DDP} = 5 V, $V_{DD(INTF)}$ = 3.3 V, f_{XTAL} = 10 MHz, unless otherwise noted.

Figure 5. Definition of duty cycle and input and output rise/fall times



Duty cycle (DC) = $t_1 / (t_1 + t_2)$.

6 Functional description

Throughout this document it is assumed that the reader is familiar with ISO7816 terminology.

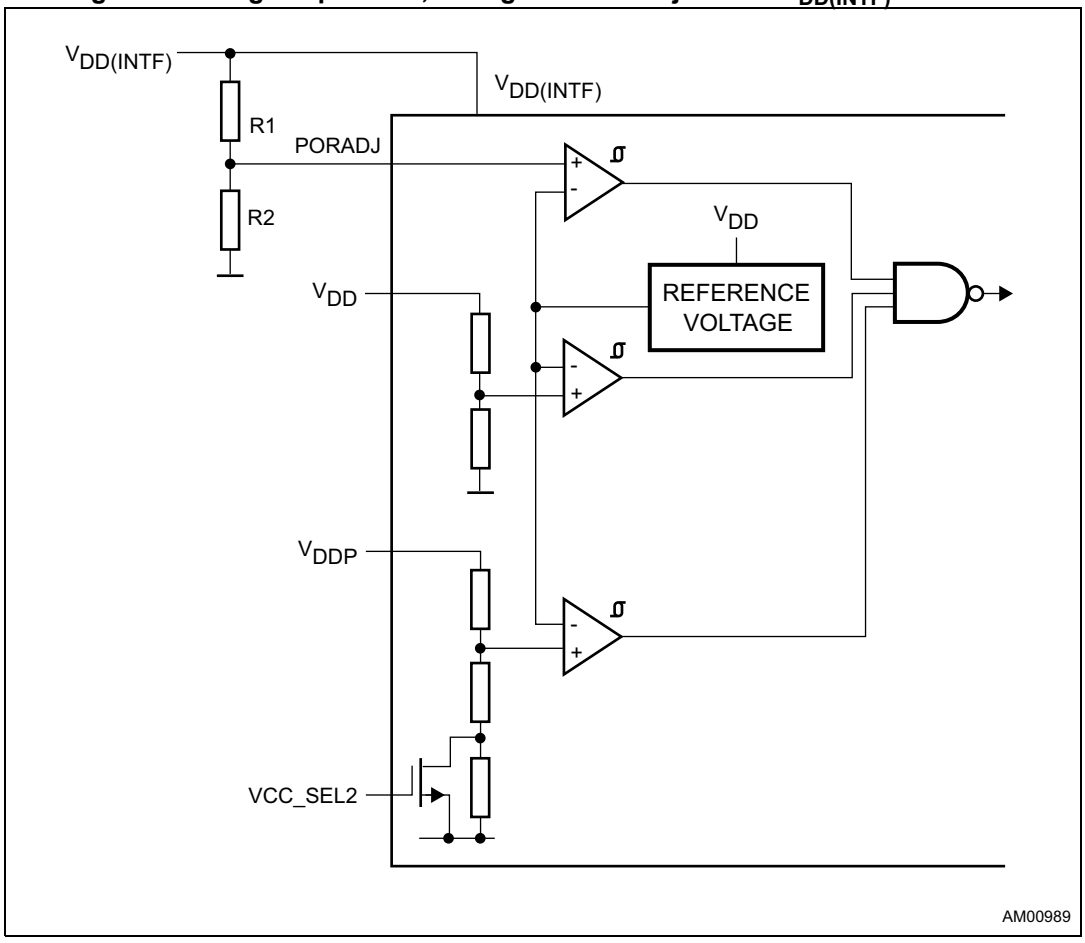
6.1 Power supplies

All interface signals to the host microcontroller are referenced to $V_{DD(INTF)}$. All card contacts remain inactive during power-up or power-down. After powering up the device, $\overline{OFF}$ output remains low until $\overline{CMDVCC}$ input is set high and $\overline{PRES}$ input is low. During power-down, $\overline{OFF}$ output goes low when V_{DDP} falls below the V_{DDP} falling threshold voltage. The internal oscillator clock frequency $f_{OSC(INT)}$ is used only during the activation sequence. When the card is not activated ($\overline{CMDVCC}$ input is high), the internal oscillator is in low frequency mode to reduce power consumption.

Power-on sequence: supply voltages may be applied to the ST8034 in any sequence.

6.2 Voltage supervisor

Figure 6. Voltage supervisor, configured with adjustable $V_{DD(INTF)}$ threshold



The voltage supervisor monitors the V_{DDP}, V_{DD}, and $V_{DD(INTF)}$ voltages and provides both power-on reset (POR) and supply dropout detection during a card session. The supervisor threshold voltages for V_{DDP} and V_{DD} are set internally, and $V_{DD(INTF)}$ is set externally by an external resistor divider on the PORADJ pin, which provides additional voltage monitoring flexibility (this pin can be used for monitoring any external voltage, with adjustable threshold):

Undervoltage (UVLO) threshold adjustment on the PORADJ input with the resistor divider:

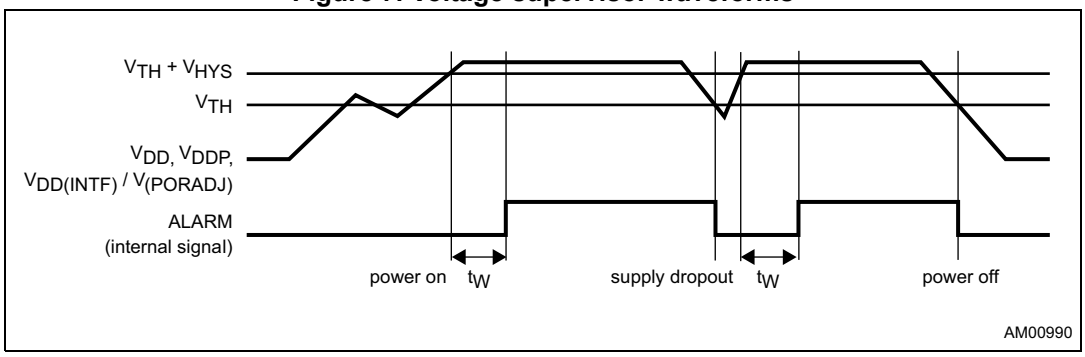
$V_{DD(INTF)}$ UVLO threshold (falling) = (R1+R2)/R2 x $V_{TH(PORADJ)}$

$V_{DD(INTF)}$ UVLO threshold (rising) = (R1+R2)/R2 x ($V_{TH(PORADJ)}$ + $V_{HYST(PORADJ)}$)

If the external resistor divider is not used, connect the PORADJ pin to $V_{DD(INTF)}$, then $V_{DD(INTF)}$ UVLO threshold = $V_{TH(PORADJ)}$.

As long as V_{DDP}, V_{DD} or $V_{DD(INTF)}$ is less than the corresponding V_{TH} + V_{HYS}, the device remains inactive irrespective of the command line levels. After V_{DDP}, V_{DD}, and $V_{DD(INTF)}$ has reached a level higher than the corresponding V_{TH} + V_{HYS}, the device still remains inactive for the duration of t_W, a defined reset pulse of approximately 8 ms (t_W = 1024 x 1/$f_{OSC(INT)LOW}$) when the output of the supervisor keeps the control logic in reset state. This is used to maintain the device in shutdown mode during the supply voltage power-on, see *Figure 7*. A deactivation sequence is performed when either V_{DD}, V_{DDP} or $V_{DD(INTF)}$ falls below the corresponding V_{TH}.

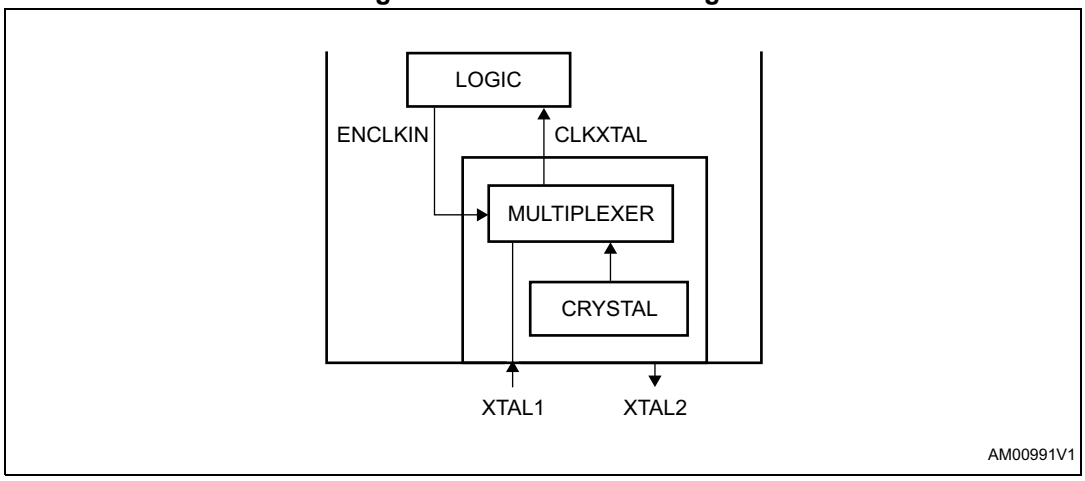
Figure 7. Voltage supervisor waveforms



6.3 Clock circuits

The clock signal for the card (CLK output) is either provided by an external clock signal connected to the XTAL1 pin or generated by a crystal connected between the XTAL1 and XTAL2 pins. The ST8034 automatically detects if an external clock is connected to XTAL1, which eliminates the need for a separate clock source selection pin. Automatic clock source detection is performed on each activation command (falling edge of $\overline{\text{CMDVCC}}$). The presence of an external clock on the XTAL1 pin is checked during a time window defined by the internal oscillator. If the external clock is detected, the crystal oscillator is stopped. If the clock is not detected, the crystal oscillator is started. When the external clock is used, the clock signal must be present on the XTAL1 pin before the $\overline{\text{CMDVCC}}$ falling edge. If the external clock is used, connect it to XTAL1 input and leave the XTAL2 pin floating. The XTAL1 pin can not be left floating, either a crystal or an external clock source needs to be connected, or the XTAL1 pin needs to be grounded.

Figure 8. External clock usage



The clock frequency is selected by the CLKDIV1 and CLKDIV2 pins and is f_{XTAL}, $f_{XTAL}/2$, $f_{XTAL}/4$ or $f_{XTAL}/8$ in the case of the ST8034HN or either f_{XTAL} or $f_{XTAL}/2$ in the case of the ST8034HC, selected by the CLKDIV pin, see *Table 12*.

The frequency change is synchronous, meaning that after transition on the CLKDIV input, the present clock period is completed and after that the new whole clock period starts, therefore no clock period is shortened during the frequency switchover.

If an external crystal is used, the duty cycle on the CLK pin should be between 45% and 55%. If an external clock is connected to the XTAL1 pin, its duty cycle must be between 48% and 52% so that the CLK output duty cycle is between 45% and 55%.

Table 12. Clock frequency selection

ST8034HN		
CLKDIV1 pin level	**CLKDIV2 pin level**	**CLK frequency**
Low	Low	$f_{XTAL}/8$
Low	High	$f_{XTAL}/4$
High	High	$f_{XTAL}/2$
High	Low	f_{XTAL}
ST8034HC		
CLKDIV pin level		**CLK frequency**
High		$f_{XTAL}/2$
Low		f_{XTAL}

6.4 Input and output circuits

When the I/O and I/OUC pins are pulled high by a 9 kΩ resistor between I/O and V_{CC} and/or 10 kΩ resistor between I/OUC and $V_{DD(INTF)}$, both lines enter the idle state. The I/O pin is referenced to V_{CC} and the I/OUC pin to $V_{DD(INTF)}$, which allows operation at V_{CC} level different from $V_{DD(INTF)}$ level.

The first side on which a falling edge occurs becomes the master. An anti-latch circuit disables falling edge detection on the other side, making it the slave. After a time delay t_D, the logic 0 present on the master side is sent to the slave side. When the master side returns logic 1, the slave side sends logic 1 during time delay ($t_{W(PU)}$). After this sequence, both master and slave sides return to their idle states.

The active pull-up feature (one-shot circuit) ensures fast low to high transitions, making the ST8034 outputs capable of delivering more than 1 mA, up to an output voltage of 0.9 V_{CC}, at a load of 80 pF. At the end of the active pull-up pulse, the output voltage is dependent on the internal pull-up resistor value and load current. The current sent to and received from the card's I/O lines is limited to 15 mA at a maximum frequency of 1 MHz.

6.5 Shutdown mode

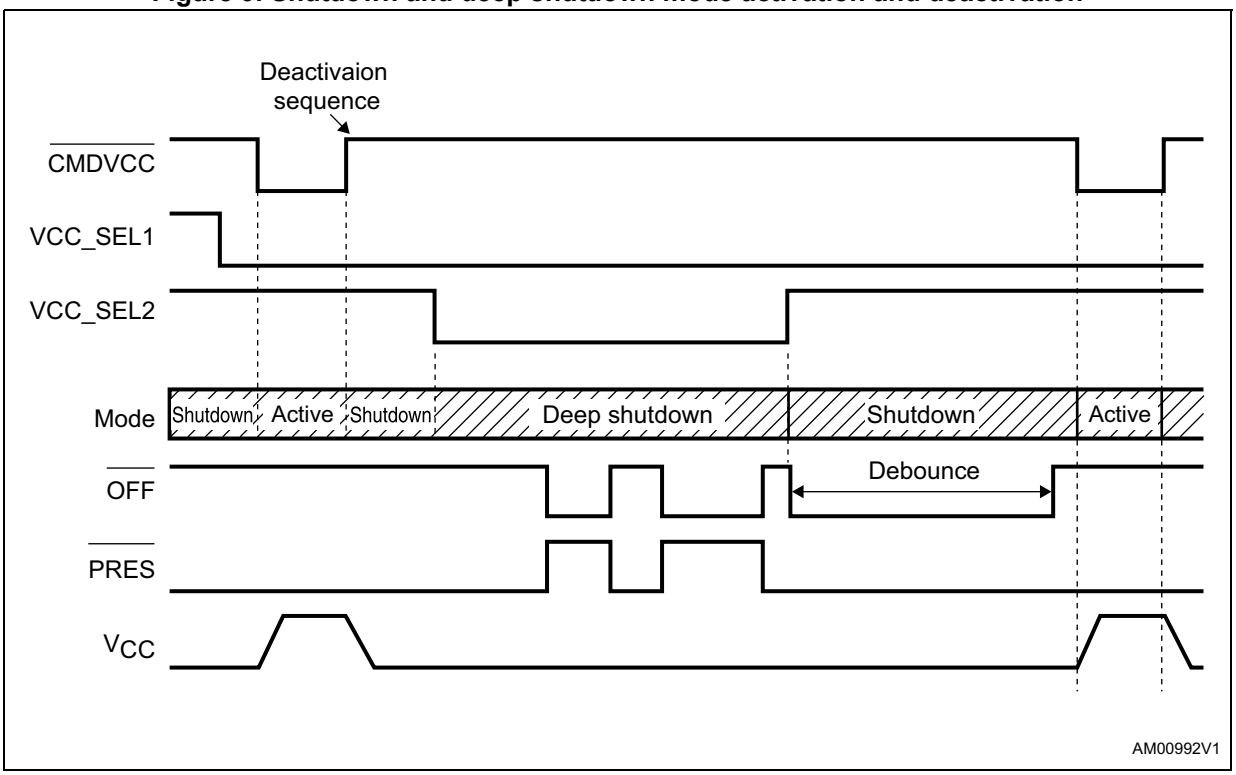
After a power-on reset, if $\overline{\text{CMDVCC}}$ is high, the ST8034 enters shutdown mode, ensuring only the minimum number of circuits are active while the ST8034 waits for the microcontroller to start a session.

- All card contacts are inactive. The impedance between the contacts and GND is approximately 200 Ω
- I/OUC, AUX1UC, AUX2UC pins are in high impedance with the 10 kΩ pull-up resistor connected to $V_{DD(INTF)}$
- The voltage generators are stopped
- The voltage supervisor is active
- The internal oscillator runs at its lowest frequency ($f_{OSC(INT)LOW}$).

6.6 Deep shutdown mode

When the smartcard reader is inactive, the ST8034HN and ST8034HC enter a deep shutdown mode if the $\overline{\text{CMDVCC}}$ pin is forced high and the VCC_SEL1 and VCC_SEL2 pins are low. In deep shutdown mode, all circuits are disabled and the $\overline{\text{OFF}}$ pin follows the status of the $\overline{\text{PRES}}$ pin. Changing the status of either $\overline{\text{CMDVCC}}$, VCC_SEL1 or VCC_SEL2 exits the deep shutdown mode, see *Figure 9*.

Figure 9. Shutdown and deep shutdown mode activation and deactivation



6.7 Activation sequence

The following device activation sequence is applied when using an external clock, also see *Figure 10*:

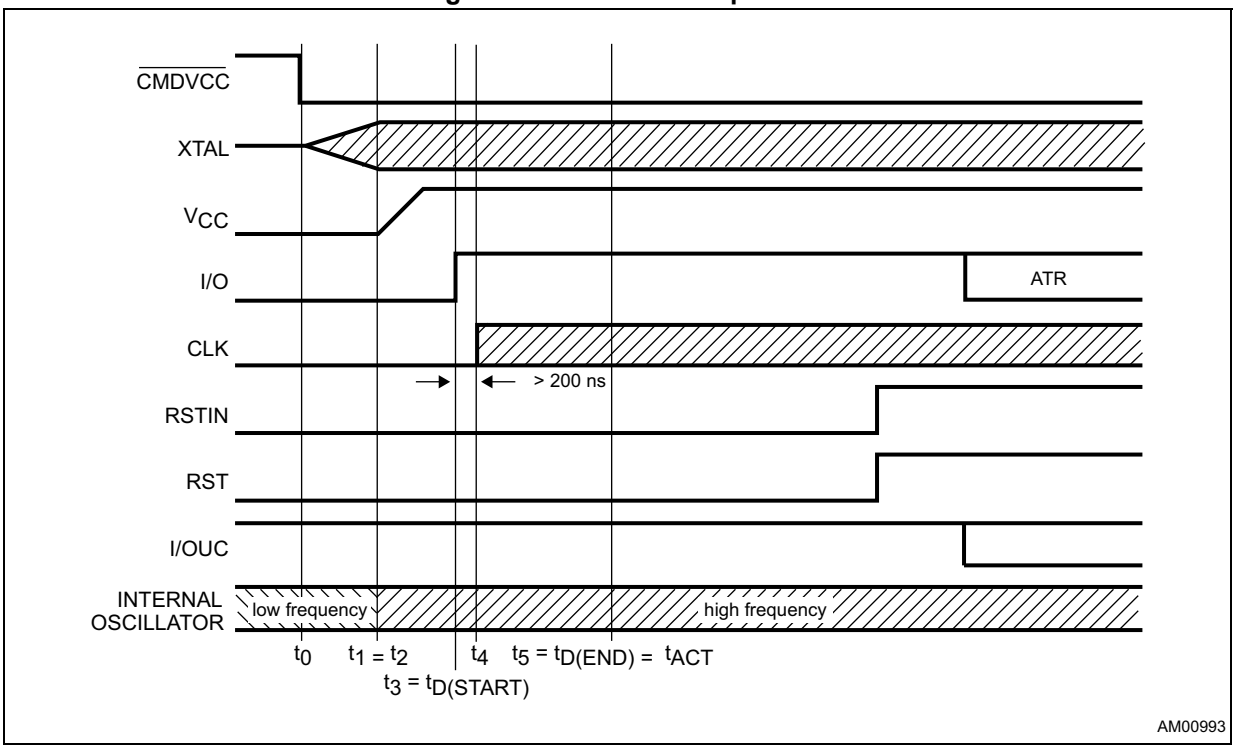
1. $\overline{\text{CMDVCC}}$ is pulled low (t_0).
2. The internal oscillator is triggered (t_0).
3. The internal oscillator changes to high frequency (t_1).
4. V_{CC} rises from 0 V to 1.8 V or to 3 V or to 5 V on a controlled slope (t_2).
5. I/O, AUX1, AUX2 are driven high (t_3).
6. The clock on the CLK output is applied to the C3 contact (t_4).
7. RST is enabled (t_5).

Time delays

- $t_1 = t_0 + 384 \times 1/f_{OSC(INT)LOW}$
- $t_2 = t_1$
- t_3 ($t_{D(START)}$) = t_1 + 17T/2
- t_4 = driven by host microcontroller; > t_3 and < t_5
- t_5 ($t_{D(END)}$) = t_1 + 23T/2.

T = 64 x $1/f_{OSC(INT)}$.

Figure 10. Activation sequence



6.8 Deactivation sequence

When a session ends, the microcontroller sets $\overline{CMDVCC}$ high. The ST8034 device then executes an automatic deactivation sequence by counting the sequencer back to the inactive state (see *Figure 11*):

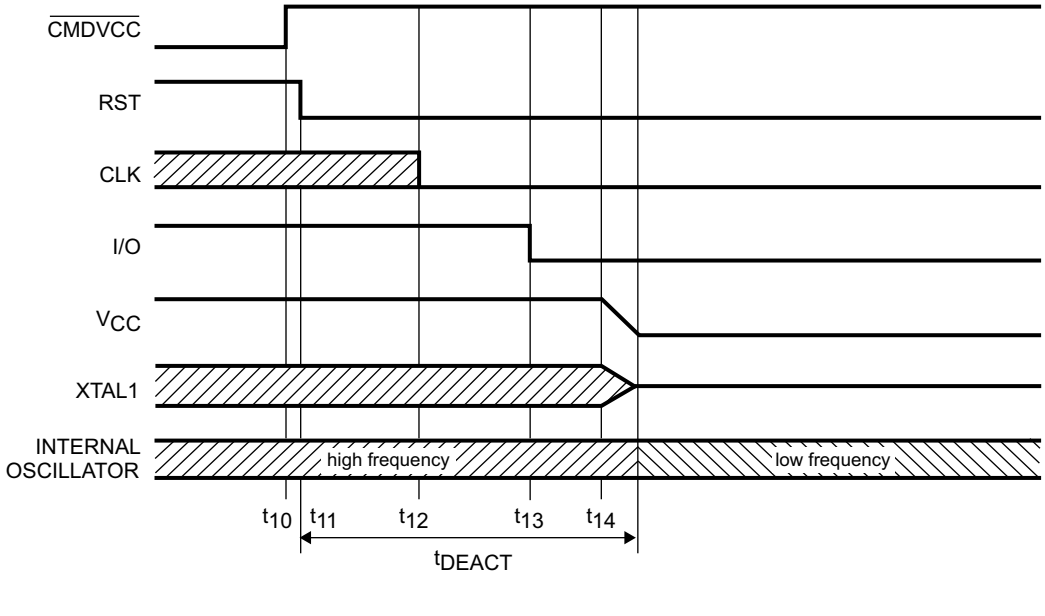
1. RST goes low (t_{11}).
2. The clock is stopped, CLK is low (t_{12}).
3. I/O, AUX1, AUX2 are pulled low (t_{13}).
4. V_{CC} falls to 0 V (t_{14}). The deactivation sequence is completed when V_{CC} reaches its inactive state.
5. V_{CC} < 0.4 V (t_{DEACT}).
6. All card contacts become low impedance to GND. The I/OUC, AUX1UC and AUX2UC pins remain pulled up to $V_{DD(INTF)}$ by the internal 10 kΩ pull-up resistor.
7. The internal oscillator returns to its low frequency mode.

Time delays

- $t_{11} = t_{10} + 3T / 64$
- $t_{12} = t_{11} + T / 2$
- $t_{13} = t_{11} + T$
- $t_{14} = t_{11} + 3T / 2$
- $t_{DEACT} = t_{11} + 3T / 2 + V_{CC}$ fall time.

$T = 64 \times 1/f_{OSC(INT)}$.

Figure 11. Deactivation sequence



6.9 V_{CC} generator

The LDO on the V_{CC} output is capable of supplying up to 65 mA continuously at any selected V_{CC} value (5 V, 3 V or 1.8 V). This output is overcurrent protected by the current limiter with a limit threshold value of 120 mA typ., with a glitch immunity allowing overcurrent pulses up to 200 mA with duration up to several microseconds not causing a deactivation (the average current value must stay below the specified current limit, see *Table 6 on page 11* and *Table 10 on page 17*).

A 100 nF capacitor (min.) with ESR < 350 mΩ should be tied to GND near the V_{CC} pin and another low ESR 100 nF capacitor (min.) should be tied to GND also on the card side, near the card reader contact C1.

6.10 Fault detection

The fault conditions monitored by the device are:

- Short-circuit or overcurrent on the V_{CC} pin
- Card removal during transaction
- V_{DD} falling
- V_{DDP} falling
- $V_{DD(INTF)}$ falling
- Overheating.

There are two different fault detection situations:

- Outside card session ($\overline{CMDVCC}$ pin is high): the $\overline{OFF}$ pin is low if the card is not in the reader and high if the card is in the reader. Any voltage drop on V_{DD}, V_{DDP} or $V_{DD(INTF)}$ is detected by the voltage supervisor. This generates an internal power-on reset pulse but does not act upon the $\overline{OFF}$ pin signal. The card is not powered-up and short-circuits or overheating are not detected.
- In card session ($\overline{CMDVCC}$ pin is low): when the $\overline{OFF}$ pin goes low, the fault detection circuit triggers the automatic emergency deactivation sequence (see *Figure 12*).

On card insertion or removal, bouncing can occur on the card presence switch (i.e. on the $\overline{PRES}$ signal). Therefore a debouncing feature is integrated into the ST8034 (4.5 ms typically, t_{DEB} = 640 × 1/$f_{OSC(INT)LOW}$). See *Figure 13*.

On card insertion, the $\overline{OFF}$ pin goes high after the debounce time has elapsed. When the card is extracted, the automatic card deactivation sequence is performed on the first high to low transition on the $\overline{PRES}$ pin. After this, the $\overline{OFF}$ pin goes low.

Figure 12. Deactivation sequence after card removal

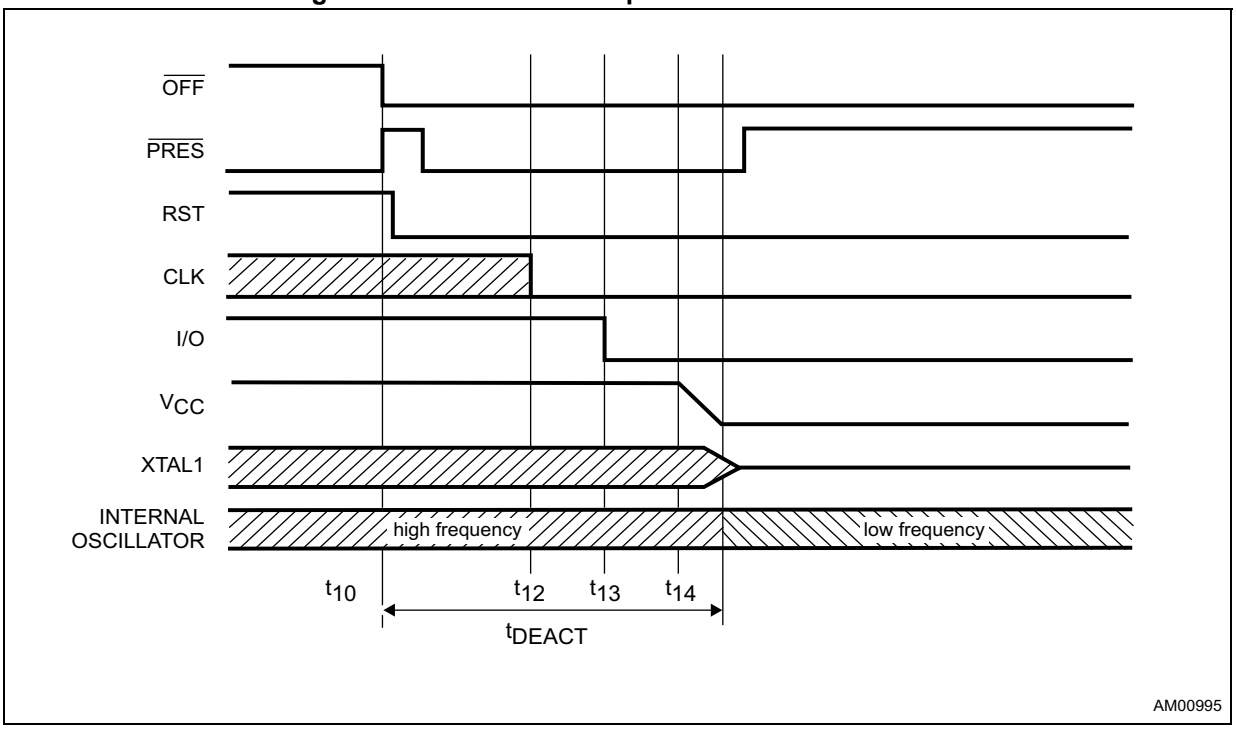
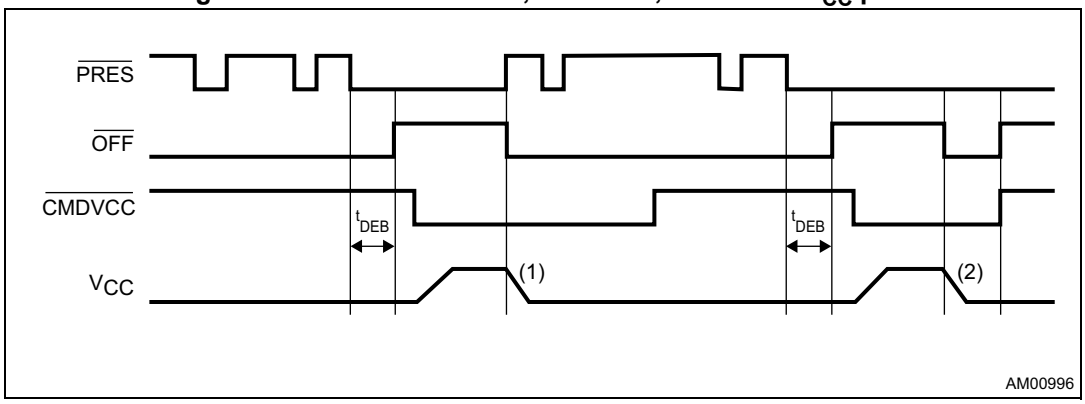


Figure 13. Debounce at $\overline{OFF}$, $\overline{CMDVCC}$, $\overline{PRES}$ and V_{CC} pins



1. Deactivation caused by card withdrawal.
2. Deactivation caused by short-circuit on card side.

6.11 VCC_SEL pin-programmed card supply voltage (V_{CC})

The card supply voltage (V_{CC}) is selected by the VCC_SEL1 and VCC_SEL2 inputs, see *Table 13*.

Table 13. V_{CC} selection by VCC_SEL1, VCC_SEL2 pins

VCC_SEL1 pin level	VCC_SEL2 pin level	V_{CC}
Low	x(1)	1.8 V
High	High	5 V
High	Low	3 V

1. x = “don't care”. However keep in mind that combination VCC_SEL1 = VCC_SEL2 = GND and $\overline{CMDVCC}$ = high initiates deep shutdown mode.

6.12 Chip select (ST8034HC only)

The chip select (CS) input pin of the ST8034HC replaces the CLKDIV1 pin and is active high, meaning normal operation of the device when CS is in logic high state. When the CS pin goes low, the status of the ST8034HC device is frozen (i.e. status of control inputs RSTIN, $\overline{CMDVCC}$, CLKDIV, VCC_SEL1 and VCC_SEL2 is latched) and the I/OUC, AUX1UC, and AUX2UC pins on the microcontroller interface go into high impedance mode (with pull-up resistors to $V_{DD(INTF)}$), not transferring any data to or from the card. The $\overline{OFF}$ output pin also goes into high impedance mode. This allows the microcontroller to share interface pins among multiple smartcard interfaces connected in parallel. Status and all the ST8034HC device functions (including the card) are maintained for immediate use when the CS goes high again. For this reason clock input is not affected by the chip select, the clock is provided to the ST8034HC device and to the card even when the CS is low.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 14. QFN24 4 x 4 x 0.8 mm, 0.5 mm pitch package outline

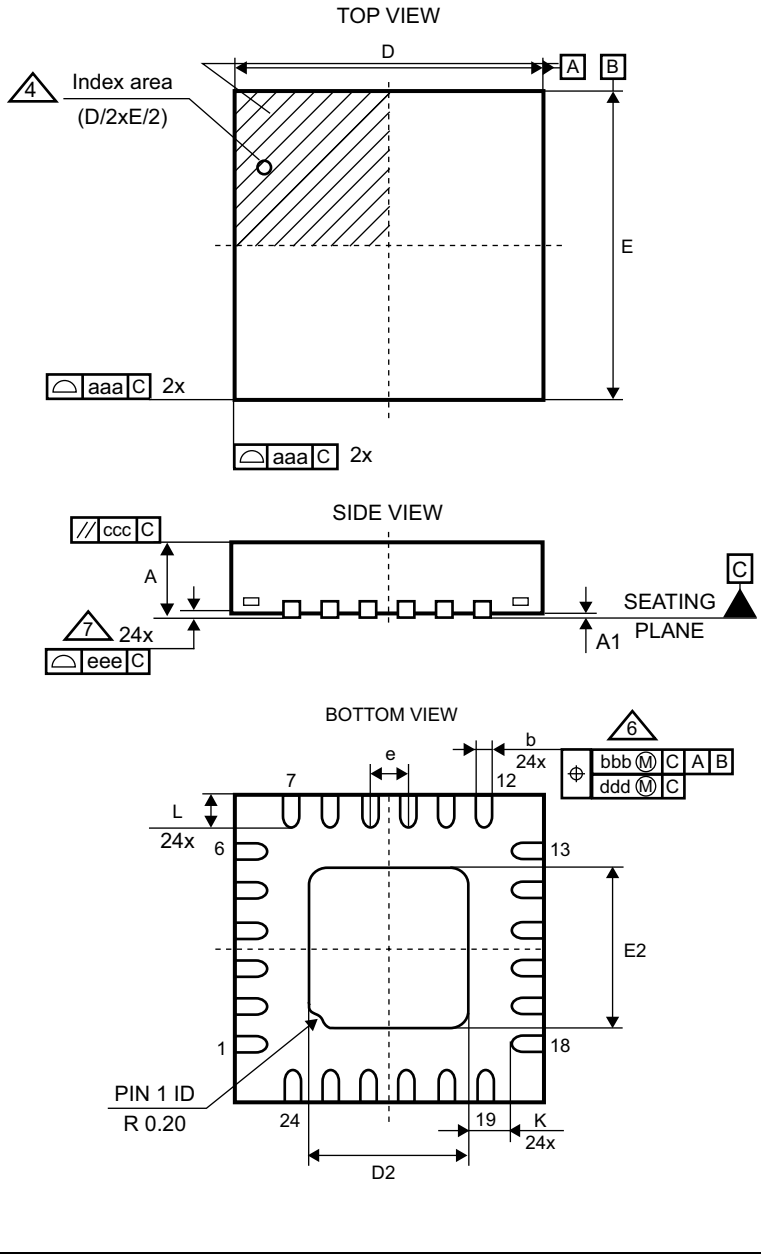
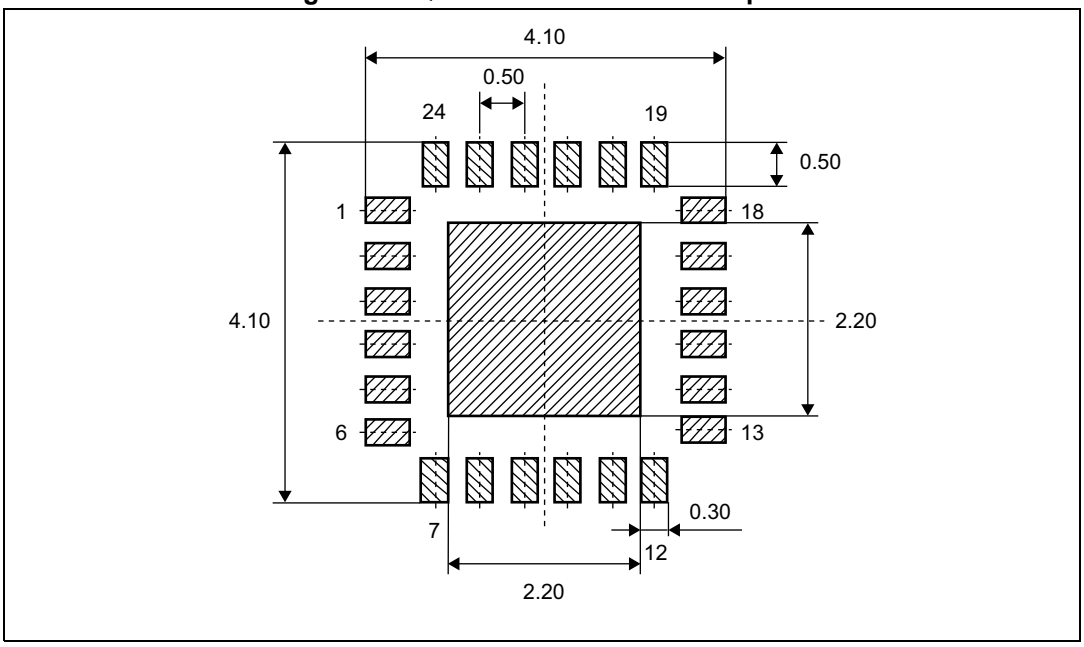


Table 14. QFN24 4 x 4 x 0.8 mm, 0.5 mm pitch package mechanical data(1), (2)

Symbol	Dimensions (mm)			Note
	Min.	Typ.	Max.	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
b	0.18	0.25	0.30	(3)
D	3.90	4.00	4.10	
E	3.90	4.00	4.10	
e		0.5 ref.		
D2	1.95	2.10	2.20	
E2	1.95	2.10	2.20	
K	0.20	-	-	
L	0.30	0.40	0.50	
aaa	0.05	0.05		
bbb	0.10	0.10		
ccc	0.10	0.10		
ddd	0.05	0.05		
eee	0.08	0.08		

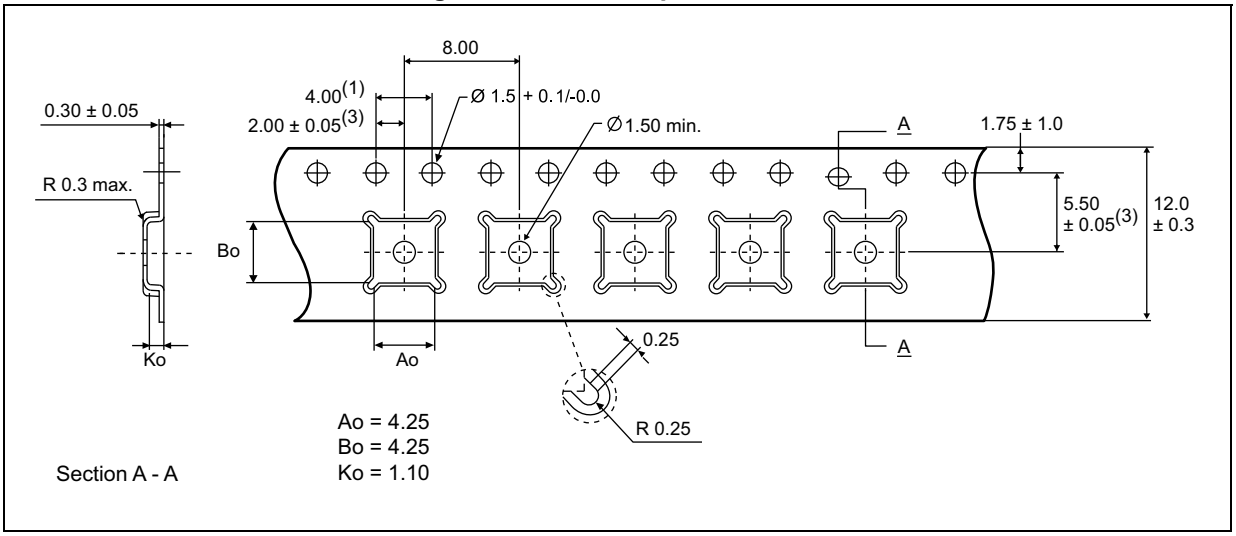
1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. The location of the terminal #1 identifier is within the hatched area.
3. Dimension b applies to metallized terminal. If the terminal has a radius on its end, dimension b should not be measured in that radius area.

Figure 15. QFN24 recommended footprint



8 Tape and reel information

Figure 16. Carrier tape for QFN24



1. 10 sprocket hole pitch cumulative tolerance ± 0.2.
2. Camber in compliance with EIA 481.
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Table 15. Tape and reel specification for QFN24

Quantity per reel	Carrier tape		Cover tape		Lockreel 7 / 13"	
	Part no. (vendor)	Description	Part no. (vendor)	Description	Part no. (vendor)	Description
3000	434146 (Cpak)	Carrier tape 12 mm width, 8 mm pitch	437150 (Cpak)	Cover tape 9.2 mm width	434543 (peak)	13" lockreel

9 Revision history

Table 16. Document revision history

Date	Revision	Changes
22-Apr-2013	1	Initial release.
22-Oct-2013	2	Updated title on page 1 (removed ST8034HN and ST8034HC). Updated *Table 1 on page 5* (removed note 1). Minor modifications throughout document.

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