DISCRETE SEMICONDUCTORS

DATA SHEET

PEMH13; **PUMH13** NPN/NPN resistor-equipped transistors; R1 = 4.7 kΩ, R2 = 47 kΩ

Product data sheet Supersedes data of 2003 Nov 07 2004 Apr 14



NPN/NPN resistor-equipped transistors; R1 = 4.7 k Ω , R2 = 47 k Ω

PEMH13; PUMH13

FEATURES

- Built-in bias resistors
- · Simplifies circuit design
- · Reduces component count
- · Reduces pick and place costs.

APPLICATIONS

- · Low current peripheral driver
- Replacement of general purpose transistors in digital applications
- . Control of IC inputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{CEO}	collector-emitter voltage	_	50	V
Io	output current (DC)	_	100	mA
TR1	NPN	_	-	-
TR2	NPN	_	_	_
R1	bias resistor	4.7		kΩ
R2	bias resistor	47	-	kΩ

DESCRIPTION

NPN/NPN resistor-equipped transistors (see "Simplified outline, symbol and pinning" for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE MARKING CODE		PACKAGE		MARKING CODE	PNP/PNP	NPN/PNP
TIFE NOWIBER	PHILIPS	EIAJ	WARKING CODE	COMPLEMENT	COMPLEMENT		
PEMH13	SOT666	-	21	PEMB13	PEMD13		
PUMH13	SOT363	SC-88	H0* ⁽¹⁾	PUMB13	PUMD13		

Note

- 1. * = p: Made in Hong Kong.
 - * = t: Made in Malaysia.
 - * = W: Made in China.

SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING		
TIPE NOMBER	SIMPLIFIED OUTLINE AND STMBOL	PIN	DESCRIPTION	
PEMH13 PUMH13	6 5 4 R1 R2 TR1	1 2 3 4 5	emitter TR1 base TR1 collector TR2 emitter TR2 base TR2	
	Top view MHC650	6	collector TR1	

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ORDERING INFORMATION

TYPE NUMBER		PACKAGE	
TIPE NOWIBER	NAME DESCRIPTION		VERSION
PEMH13	 plastic surface mounted package; 6 leads 		SOT666
PUMH13	 plastic surface mounted package; 6 leads 		SOT363

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transis	tor			-	-
V_{CBO}	collector-base voltage	open emitter	_	50	V
V _{CEO}	collector-emitter voltage	open base	_	50	V
V _{EBO}	emitter-base voltage	open collector	_	10	V
Vı	input voltage positive		_	+30	V
	negative		_	- 5	V
I _O	output current (DC)		_	100	mA
I _{CM}	peak collector current		_	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT363	note 1	_	200	mW
	SOT666	notes 1 and 2	_	200	mW
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		_	150	°C
T _{amb}	operating ambient temperature		-65	+150	°C
Per device					
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT363	note 1	_	300	mW
	SOT666	notes 1 and 2	_	300	mW

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Notes

- 1. Device mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.
- 2. Reflow soldering is the only recommended soldering method.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Per transis	tor			
R _{th(j-a)}	thermal resistance from junction to ambient	T _{amb} ≤ 25 °C		
	SOT363	note 1	625	K/W
	SOT666	notes 1 and 2	625	K/W
Per device				
R _{th(j-a)}	thermal resistance from junction to ambient	T _{amb} ≤ 25 °C		
	SOT363	note 1	416	K/W
	SOT666	notes 1 and 2	416	K/W

Notes

- 1. Device mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.
- 2. Reflow soldering is the only recommended soldering method.

CHARACTERISTICS

 T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT			
Per transis	Per transistor								
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0 A	_	_	100	nA			
I _{CEO}	collector-emitter cut-off current	V _{CE} = 30 V; I _B = 0 A	_	_	1	μΑ			
		$V_{CE} = 30 \text{ V}; I_{B} = 0 \text{ A}; T_{j} = 150 ^{\circ}\text{C}$	_	_	50	μΑ			
I _{EBO}	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_{C} = 0 \text{ A}$	_	_	170	μΑ			
h _{FE}	DC current gain	$V_{CE} = 5 \text{ V}; I_{C} = 10 \text{ mA}$	100	_	_				
V _{CEsat}	collector-emitter saturation voltage	$I_C = 5 \text{ mA}; I_B = 0.25 \text{ mA}$	_	_	100	mV			
$V_{i(off)}$	input-off voltage	$V_{CE} = 5 \text{ V}; I_{C} = 100 \mu\text{A}$	_	0.6	0.5	V			
$V_{i(on)}$	input-on voltage	$V_{CE} = 0.3 \text{ V}; I_{C} = 5 \text{ mA}$	1.3	0.9	_	V			
R1	input resistor		3.3	4.7	6.1	kΩ			
<u>R2</u> R1	resistor ratio		8	10	12				
C _c	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = i_e = 0 \text{ A};$ f = 1 MHz	-	_	2.5	pF			

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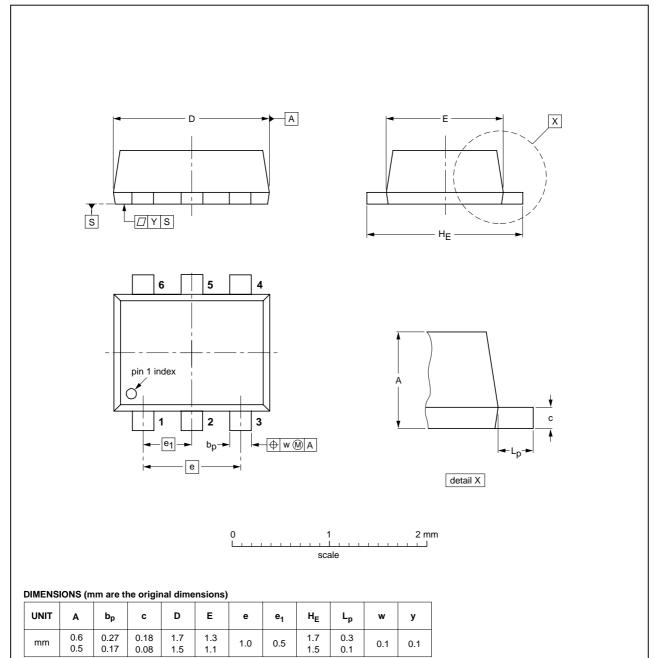
NPN/NPN resistor-equipped transistors; R1 = 4.7 k Ω , R2 = 47 k Ω

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PACKAGE OUTLINES

Plastic surface-mounted package; 6 leads

SOT666



REFERENCES			EUROPEAN	ISSUE DATE	
IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
					-04-11-08- 06-03-16
-	IEC	IEC JEDEC	IEC JEDEC JEITA	IEC JEDEC JEITA	IEC JEDEC JEITA PROJECTION

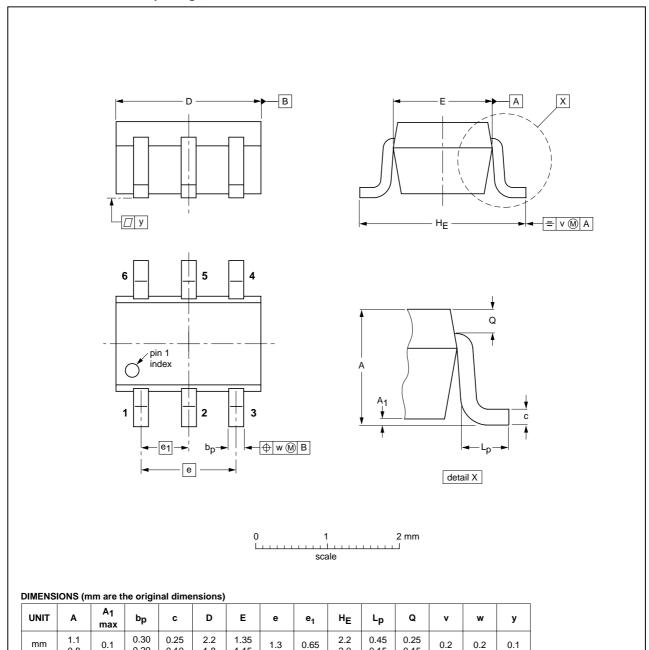
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NPN/NPN resistor-equipped transistors; R1 = 4.7 k Ω , R2 = 47 k Ω

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Plastic surface-mounted package; 6 leads

SOT363



OUTLINE	REFERENCES			EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT363			SC-88			04-11-08 06-03-16

0.15

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0.10

1.15

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DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

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NXP Semiconductors

Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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Printed in The Netherlands R75/03/pp8 Date of release: 2004 Apr 14 Document order number: 9397 750 13092

