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Team Nexperia



PMV45EN

N-channel TrenchMOS logic level FET Rev. 2 — 7 November 2011

Product data sheet

Product profile 1.

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications.

1.2 Features and benefits

■ Logic-level compatible

■ Trench MOSFET technology

Very fast switching

1.3 Applications

Battery management

High-speed switching

1.4 Quick reference data

Quick reference data Table 1.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C	-	-	30	V
I _D	drain current	$T_{sp} = 25 \text{ °C}$; $V_{GS} = 10 \text{ V}$; see <u>Figure 1</u> ; see <u>Figure 3</u>	-	-	5.4	Α
V_{GS}	gate-source voltage		-20	-	20	V
Static charac	cteristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 2 \text{ A}; T_j = 25 ^{\circ}\text{C}; \text{ see}$ Figure 9; see Figure 10	-	35	42	mΩ

Pinning information 2.

Table 2. **Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source		D
3	D	drain	1 2	G_(ISA)
			SOT23 (TO-236AB)	mbb076 S



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3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMV45EN	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PMV45EN	%4N

^{[1] % =} placeholder for manufacturing site code

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C	-	30	V
V_{DGR}	drain-gate voltage	$T_j \ge 25$ °C; $T_j \le 150$ °C; $R_{GS} = 20$ kΩ	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I _D	drain current	T_{sp} = 100 °C; V_{GS} = 10 V; see <u>Figure 1</u>	-	3.4	Α
		T_{sp} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u> ; see <u>Figure 3</u>	-	5.4	Α
I _{DM}	peak drain current	$T_{sp} = 25 \text{ °C}$; pulsed; $t_p \le 10 \mu\text{s}$; see Figure 3	-	21.6	Α
P _{tot}	total power dissipation	T _{sp} = 25 °C; see <u>Figure 2</u>	-	2	W
T _{stg}	storage temperature		-55	150	°C
Tj	junction temperature		-55	150	°C
Source-drain	diode				
Is	source current	$T_{sp} = 25 ^{\circ}C$	-	1.7	Α
I _{SM}	peak source current	T_{sp} = 25 °C; pulsed; $t_p \le 10 \ \mu s$	-	6.9	Α

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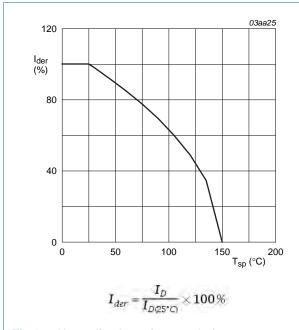


Fig 1. Normalized continuous drain current as a function of solder point temperature

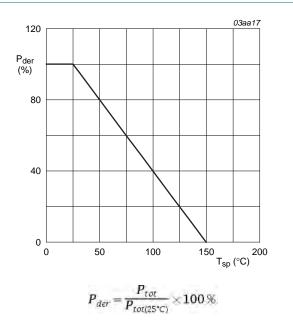
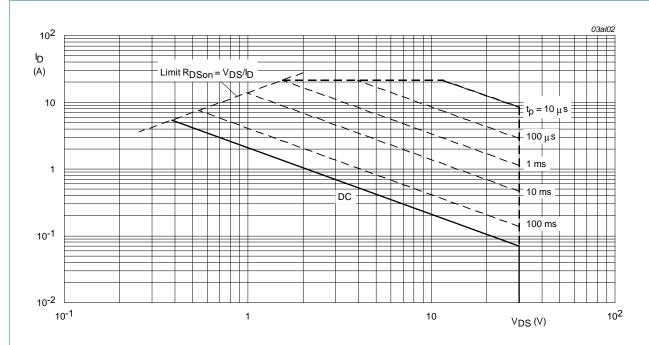


Fig 2. Normalized total power dissipation as a function of solder point temperature



 $T_{SP} = 25^{\circ}C; I_{DM}$ is single pulse; $V_{GS} = 10V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

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6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	N	/lin	Тур	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-		-	60	K/W

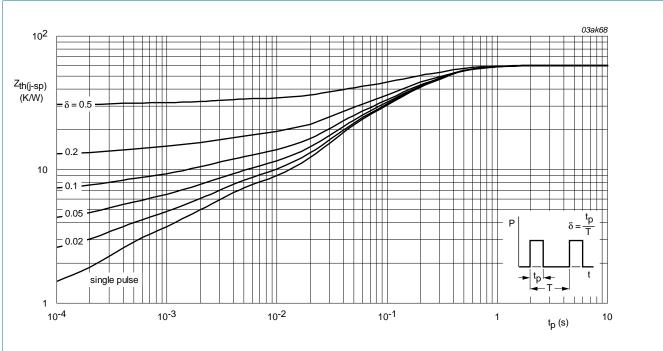


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

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7. Characteristics

Table 7. Characteristics

Table 7.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
V _{(BR)DSS}	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	30	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ °C}$; see Figure 8	1	1.5	2	V
		$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 150 \text{ °C}$; see Figure 8	0.6	-	-	V
		$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = -55 \text{ °C}$; see Figure 8	-	-	2.2	V
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 ^{\circ}\text{C}$	-	-	100	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nA
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$; $I_D = 2 \text{ A}$; $T_j = 25 \text{ °C}$; see Figure 9; see Figure 10	-	35	42	mΩ
		$V_{GS} = 10 \text{ V}$; $I_D = 2 \text{ A}$; $T_j = 150 \text{ °C}$; see Figure 9; see Figure 10	-	59.5	71.4	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 1.5 \text{ A}; T_j = 25 ^{\circ}\text{C}; \text{ see}$ Figure 9; see Figure 10	-	45	54	mΩ
Dynamic	characteristics					
Q _{G(tot)}	total gate charge	$I_D = 3 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$	-	9.4	-	nC
Q _{GS}	gate-source charge	T _j = 25 °C; see <u>Figure 11</u>	-	1.2	-	nC
Q_{GD}	gate-drain charge		-	1.9	-	nC
C _{iss}	input capacitance	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	350	-	pF
C _{oss}	output capacitance	$T_j = 25 ^{\circ}\text{C}$	-	70	-	pF
C _{rss}	reverse transfer capacitance		-	50	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 15 \text{ V}; R_L = 15 \Omega; V_{GS} = 10 \text{ V};$	-	5	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	7	-	ns
t _{d(off)}	turn-off delay time		-	16	-	ns
t _f	fall time		-	5.5	-	ns
Source-di	rain diode					
V_{SD}	source-drain voltage	$I_S = 1.5 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ °C}$; see Figure 12	-	0.79	1.2	V

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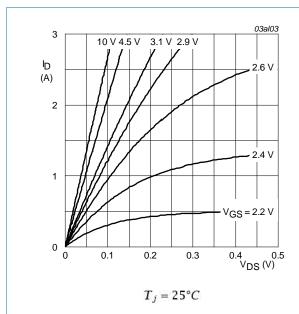


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

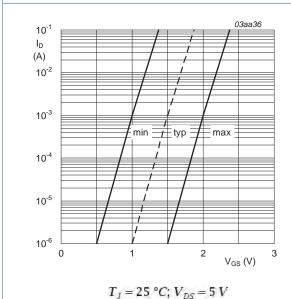


Fig 7. Sub-threshold drain current as a function of gate-source voltage

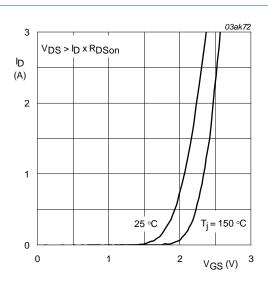


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

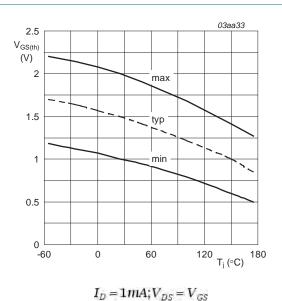


Fig 8. Gate-source threshold voltage as a function of junction temperature

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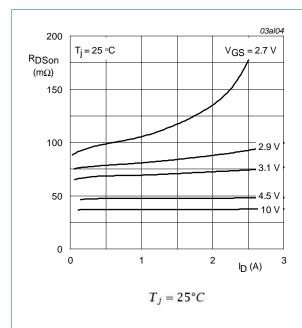


Fig 9. Drain-source on-state resistance as a function of drain current; typical values

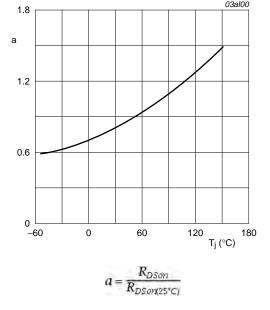


Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature

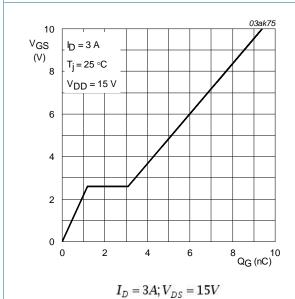


Fig 11. Gate-source voltage as a function of gate charge; typical values

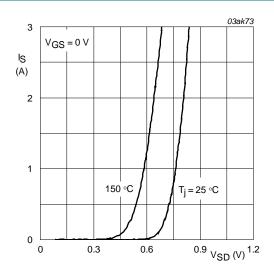


Fig 12. Source current as a function of source-drain voltage; typical value

 $T_j = 25^{\circ}C \text{ and } 150^{\circ}C; V_{GS} = 0V$

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8. Package outline

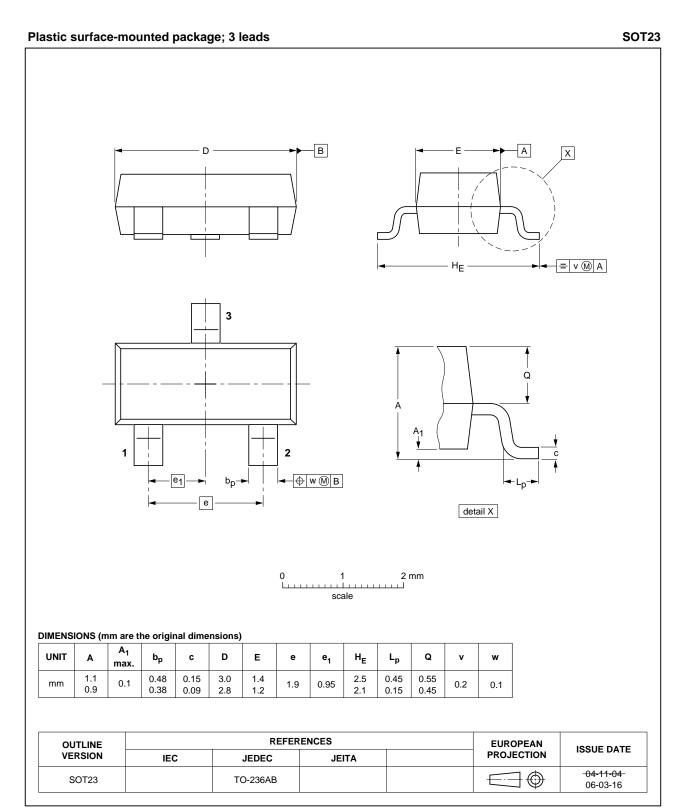


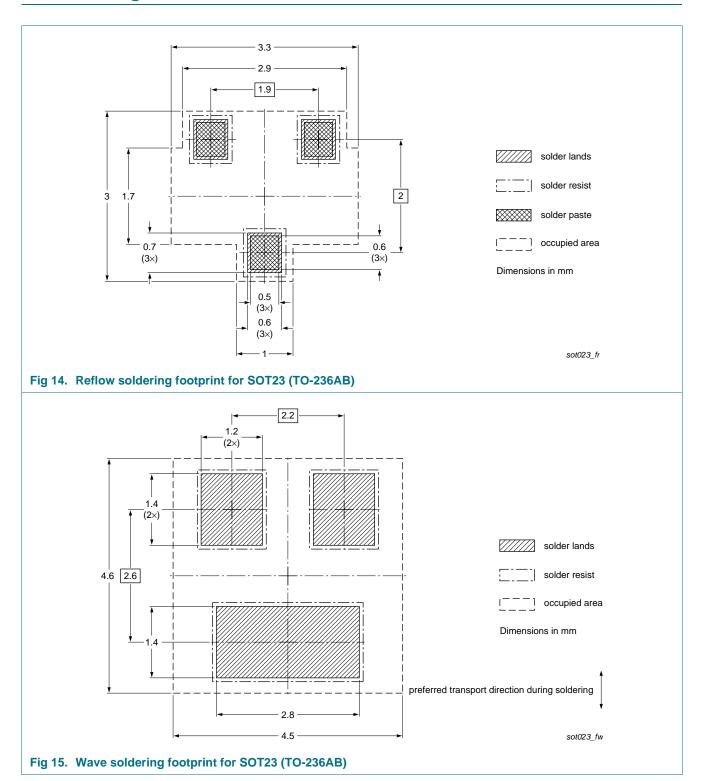
Fig 13. Package outline SOT23 (TO-236AB)

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9. Soldering



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10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMV45EN v.2	20111107	Product data sheet	-	PMV45EN v.1
Modifications:	NXP Semiconducto			
	 Legal texts have be 	een adapted to the new c	ompany name where app	propriate.
	 1 "Product profile" 	: updated		
	 3 "Ordering inform 	nation": added		
	 4 "Marking": added 	d		
	Fig 13.: updated			
	• <u>9 "Soldering"</u> : add	ed		
	• 11 "Legal informat	ion": updated		
PMV45EN v.1	20030115	Product data sheet	-	-

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11. Legal information

11.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design
- [2] The term 'short data sheet' is explained in section "Definitions"
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