

#### Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <a href="http://www.nxp.com">http://www.nxp.com</a>, <a href="http://www.semiconductors.philips.com/">http://www.nxp.com</a>, <a href="http://www.nexperia.com">http://www.nexperia.com</a>, <a href="http://www.nexperia.com">http://www.nexperia.com</a>,

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use salesaddresses@nexperia.com (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © Nexperia B.V. (year). All rights reserved.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia



# **NUP1301**

# Ultra low capacitance ESD protection array Rev. 01 — 11 May 2009

**Product data sheet** 

# **Product profile**

# 1.1 General description

Ultra low capacitance ElectroStatic Discharge (ESD) protection array in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package designed to protect one signal line in rail-to-rail configuration from the damage caused by ESD and other transients.

#### 1.2 Features

- ESD protection of one signal line (rail-to-rail configuration)
- Ultra low diode capacitance: C<sub>d</sub> = 0.6 pF
- Very low reverse leakage current: ≤ 30 nA
- ESD protection up to 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge);  $I_{PP}$  = 11 A at  $t_p$  = 8/20 μs
- AEC-Q101 qualified

### 1.3 Applications

- Telecommunication networks
- Video line protection
- Microcontroller protection
- I<sup>2</sup>C-bus protection
- Antenna power supply
- Analog audio
- Class-D amplifier

#### 1.4 Quick reference data

Table 1. Quick reference data

T<sub>amb</sub> = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per diode						
$V_{RRM}$	repetitive peak reverse voltage		-	-	80	V
C <sub>d</sub>	diode capacitance	f = 1 MHz; $V_R = 0 V$	-	0.6	0.75	pF
I <sub>R</sub>	reverse current	$V_{R} = 80 \text{ V}$	-	-	100	nA



# **Ultra low capacitance ESD protection array**

# 2. Pinning information

Table 2. Pinning

I GIDIO E.	;	9		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND	ground		
2	$V_{CC}$	supply voltage	3	3
3	I/O	input/output	1	1 2

# 3. Ordering information

Table 3. Ordering information

Type number	Package	Package		
	Name	Description	Version	
NUP1301	-	plastic surface-mounted package; 3 leads	SOT23	

# 4. Marking

Table 4. Marking

Type number	Marking code <sup>[1]</sup>
NUP1301	LJ*

<sup>[1] \* = -:</sup> made in Hong Kong

# 5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per diode					
$V_{RRM}$	repetitive peak reverse voltage		-	80	V
$V_R$	reverse voltage		-	80	V
I <sub>F</sub>	forward current		<u>[1]</u> _	215	mA
I <sub>FRM</sub>	repetitive peak forward current	$t_p \leq 1 \text{ ms; } \delta \leq 0.25$	-	500	mA

<sup>\* =</sup> p: made in Hong Kong

<sup>\* =</sup> t: made in Malaysia

<sup>\* =</sup> W: made in China

### Ultra low capacitance ESD protection array

**Table 5.** Limiting values ...continued
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
I <sub>FSM</sub> non-repetitive peak forward current	•	square wave	[2]		
	forward current	t <sub>p</sub> = 1 μs	-	4	Α
		t <sub>p</sub> = 1 ms	-	1	Α
		t <sub>p</sub> = 1 s	-	0.5	Α
Per device					
P <sub>PP</sub>	peak pulse power	$t_p = 8/20 \ \mu s$	[3][4]	220	W
I <sub>PP</sub>	peak pulse current	$t_p = 8/20 \ \mu s$	[3][4]	11	Α
P <sub>tot</sub>	total power dissipation	$T_{amb} \le 25  ^{\circ}C$	[5][6]	250	mW
Tj	junction temperature		-	150	°C
T <sub>amb</sub>	ambient temperature		-55	+150	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

<sup>[1]</sup> Pulse test:  $t_p \le 300 \ \mu s; \ \delta \le 0.02$ .

Table 6. ESD maximum ratings

Symbol	Parameter	Conditions	М	in Max	Unit
V <sub>ESD</sub>	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1][2]	30	kV
		machine model	-	400	V
		MIL-STD-883 (human body model)	-	10	kV

<sup>[1]</sup> Device stressed with ten non-repetitive ESD pulses.

Table 7. ESD standards compliance

Standard	Conditions
IEC 61000-4-2; level 4 (ESD)	> 15 kV (air); > 8 kV (contact)
MIL-STD-883; class 3B (human body model)	> 8 kV

<sup>[2]</sup>  $T_i = 25$  °C prior to surge.

<sup>[3]</sup> Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.

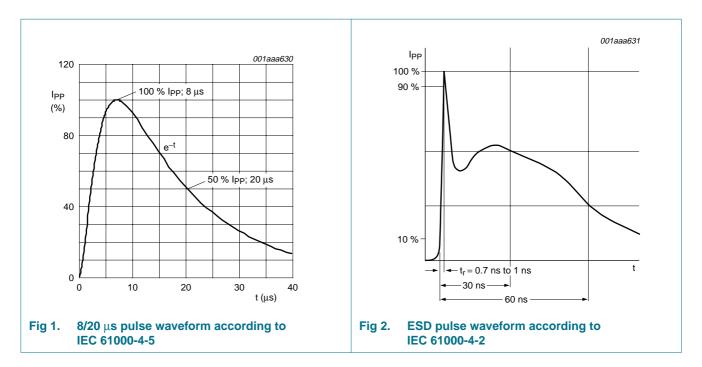
<sup>[4]</sup> Measured from pin 3 to pins 1 and 2 (pins 1 and 2 are connected).

<sup>[5]</sup> Single diode loaded.

<sup>[6]</sup> Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

<sup>[2]</sup> Measured from pin 3 to pins 1 and 2 (pins 1 and 2 are connected).

# **Ultra low capacitance ESD protection array**



# 6. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per devic	e					
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1][2]	-	500	K/W
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point		-	-	360	K/W

<sup>[1]</sup> Single diode loaded.

<sup>[2]</sup> Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

# **Ultra low capacitance ESD protection array**

# 7. Characteristics

Table 9. Electrical characteristics

 $T_{amb}$  = 25 °C unless otherwise specified.

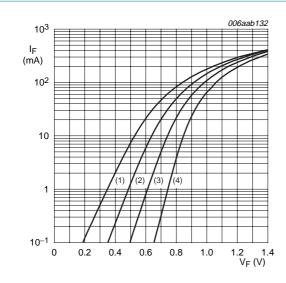
Tamb = 25 O unicos otherwise specifica.							
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per diode	)						
$V_{BR}$	breakdown voltage	$I_R = 100 \mu A$		100	-	-	V
V <sub>F</sub>	forward voltage		[1]				
		I <sub>F</sub> = 1 mA		-	-	715	mV
		I <sub>F</sub> = 10 mA		-	-	855	mV
		$I_F = 50 \text{ mA}$		-	-	1	V
		I <sub>F</sub> = 150 mA		-	-	1.25	V
I <sub>R</sub>	reverse current						
		V <sub>R</sub> = 25 V		-	-	30	nA
		V <sub>R</sub> = 80 V		-	-	100	nA
		$V_R = 25 \text{ V};$ $T_j = 150 ^{\circ}\text{C}$		-	-	25	μΑ
		$V_R = 80 \text{ V};$ $T_j = 150 ^{\circ}\text{C}$		-	-	35	μΑ
C <sub>d</sub>	diode capacitance	$f = 1 MHz; V_R = 0 V$		-	0.6	0.75	pF
Per devic	е						
V <sub>CL</sub>	clamping voltage	I <sub>PP</sub> = 1 A	[2][3]	-	-	3	V
		I <sub>PP</sub> = 11 A	[2][3]	-	-	20	V

<sup>[1]</sup> Pulse test:  $t_p \le 300~\mu s;~\delta \le 0.02.$ 

<sup>[2]</sup> Non-repetitive current pulse  $8/20~\mu s$  exponential decay waveform according to IEC 61000-4-5.

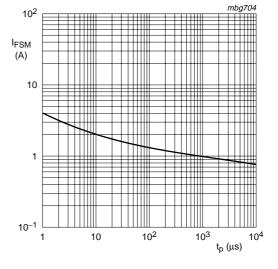
<sup>[3]</sup> Measured from pin 3 to pins 1 and 2 (pins 1 and 2 are connected).

### **Ultra low capacitance ESD protection array**



- (1)  $T_{amb} = 150 \, ^{\circ}C$
- (2)  $T_{amb} = 85 \, ^{\circ}C$
- (3)  $T_{amb} = 25 \, ^{\circ}C$
- (4)  $T_{amb} = -40 \, ^{\circ}C$

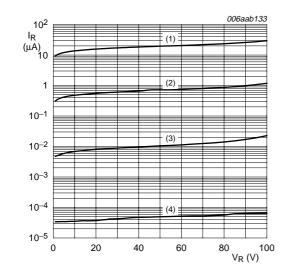
Fig 3. Forward current as a function of forward voltage; typical values



Based on square wave currents.

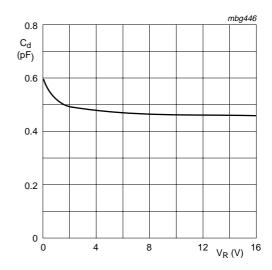
 $T_i = 25$  °C; prior to surge

Fig 4. Non-repetitive peak forward current as a function of pulse duration; typical values



- (1)  $T_{amb} = 150 \, ^{\circ}C$
- (2)  $T_{amb} = 85 \,^{\circ}C$
- (3)  $T_{amb} = 25 \, ^{\circ}C$
- (4)  $T_{amb} = -40 \, ^{\circ}C$

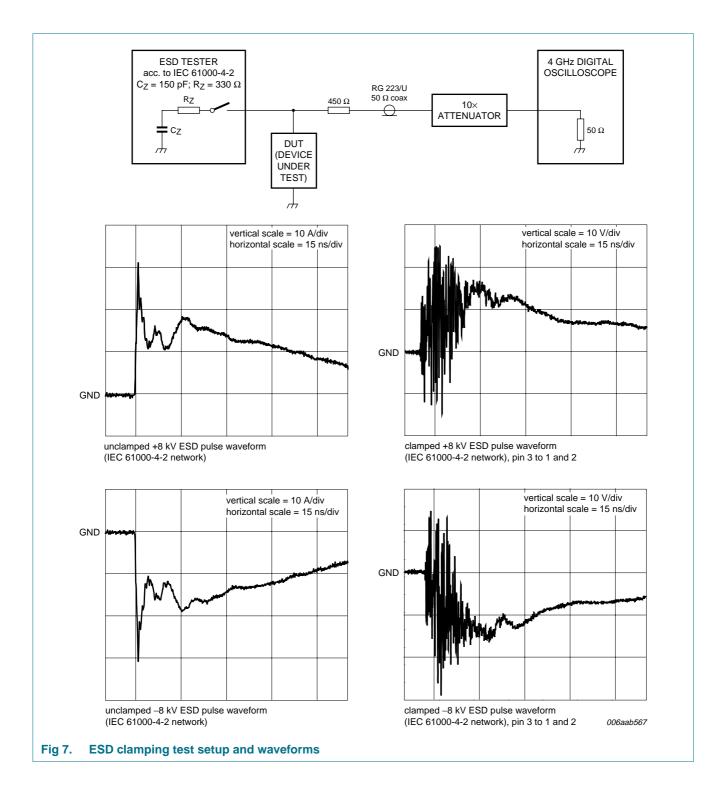
Fig 5. Reverse current as a function of reverse voltage; typical values



 $T_{amb} = 25 \, ^{\circ}C; f = 1 \, MHz$ 

Fig 6. Diode capacitance as a function of reverse voltage; typical values

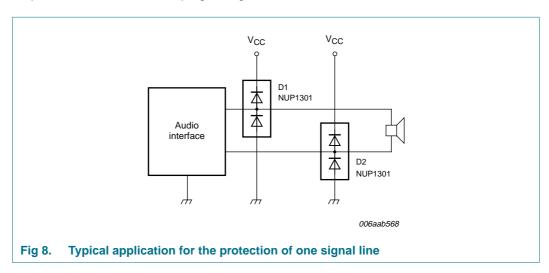
### **Ultra low capacitance ESD protection array**



**Ultra low capacitance ESD protection array** 

# 8. Application information

Protection of a single (high-speed) data line in rail-to-rail configuration. The protected data line is connected to pin 3. Pin 1 is connected to ground (GND) and pin 2 is connected to the supply rail (supply voltage  $V_{CC}$ .) When the transient voltage exceeds the forward voltage drop of one diode, the transient is directed either to the supply rail or to GND. The advantages of these solutions are: low line capacitance (0.6 pF typically), fast response time, and low clamping voltage.



#### Circuit board layout and protection device placement:

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- 1. Place the NUP1301 as close to the input terminal or connector as possible.
- 2. The path length between the NUP1301 and the protected line should be minimized.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

#### 9. Test information

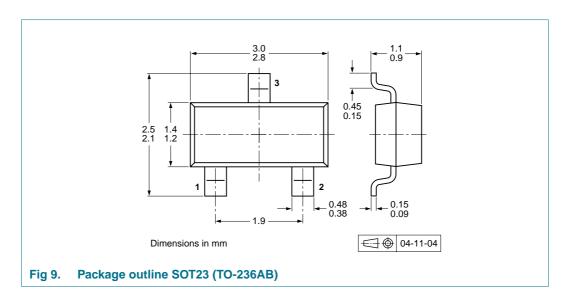
#### 9.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

NUP1301\_1 © NXP B.V. 2009. All rights reserved.

### **Ultra low capacitance ESD protection array**

# 10. Package outline



# 11. Packing information

Table 10. Packing methods

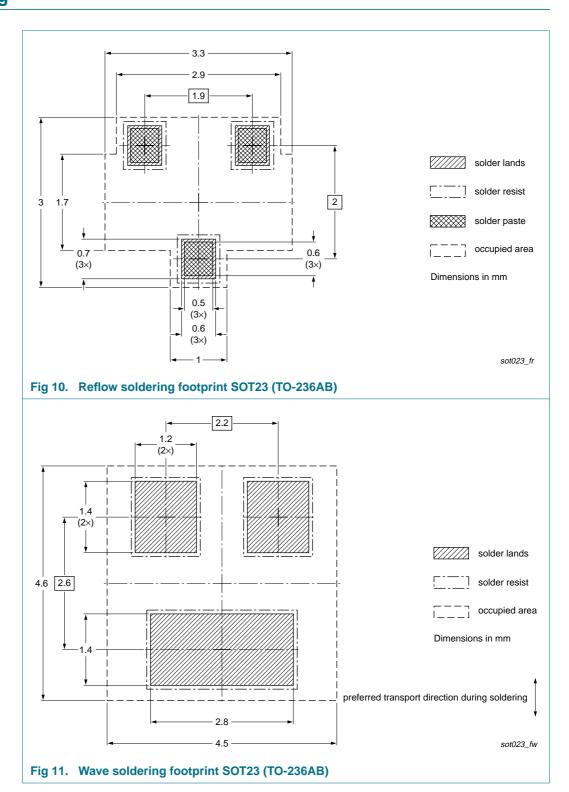
The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing	Packing quantity	
			3000	10000	
NUP1301	SOT23	4 mm pitch, 8 mm tape and reel	-215	-235	

<sup>[1]</sup> For further information and the availability of packing methods, see Section 15.

### **Ultra low capacitance ESD protection array**

# 12. Soldering



Ultra low capacitance ESD protection array

# 13. Revision history

### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NUP1301_1	20090511	Product data sheet	-	-

#### **Ultra low capacitance ESD protection array**

# 14. Legal information

#### 14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <a href="http://www.nxp.com">http://www.nxp.com</a>.

#### 14.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 14.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <a href="http://www.nxp.com/profile/terms">http://www.nxp.com/profile/terms</a>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

#### 14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

#### 15. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

NUP1301\_1 © NXP B.V. 2009. All rights reserved.

### **Ultra low capacitance ESD protection array**

# 16. Contents

1	Product profile
1.1	General description
1.2	Features
1.3	Applications
1.4	Quick reference data 1
2	Pinning information 2
3	Ordering information
4	Marking 2
5	Limiting values
6	Thermal characteristics 4
7	Characteristics 5
8	Application information 8
9	Test information 8
9.1	Quality information 8
10	Package outline 9
11	Packing information 9
12	Soldering 10
13	Revision history
14	Legal information
14.1	Data sheet status
14.2	Definitions
14.3	Disclaimers
14.4	Trademarks12
15	Contact information 12
16	Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2009.

All rights reserved.

For more information, please visit: http://www.nxp.com For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 11 May 2009 Document identifier: NUP1301\_1