# **MOSFET** - N-Channel Shielded Gate PowerTrench®

150 V, 5.0 mΩ, 139 A

## NTP5D0N15MC

#### **Features**

- Shielded Gate MOSFET Technology
- Max  $R_{DS(on)} = 5.0 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 97 \text{ A}$
- 50% Lower Qrr than other MOSFET Suppliers
- Lowers Switching Noise/EMI
- 100% UIL Tested
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

#### **Typical Applications**

- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage		$V_{DSS}$	150	V	
Gate-to-Source Voltage			V <sub>GS</sub>	±20	V
Continuous Drain Current R <sub>θJC</sub> (Note 2)	Steady State			139	Α
Power Dissipation $R_{\theta JC}$ (Note 2)	State		P <sub>D</sub>	214	W
Continuous Drain Current R <sub>θJA</sub> (Notes 1, 2)	Steady State	T <sub>Δ</sub> = 25°C	I <sub>D</sub>	15	Α
Power Dissipation R <sub>θJA</sub> (Notes 1, 2)	State	, ,	P <sub>D</sub>	2.4	W
Pulsed Drain Current	$T_A = 25^{\circ}C, t_p = 100 \mu s$		I <sub>DM</sub>	818	Α
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	
Single Pulse Drain–to–Source Avalanche Energy ( $I_L = 26  A_{pk},  L = 3  mH$ )		E <sub>AS</sub>	1014	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

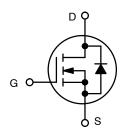
- 1. Surface-mounted on FR4 board using a 1 in<sup>2</sup>, 2 oz. Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.



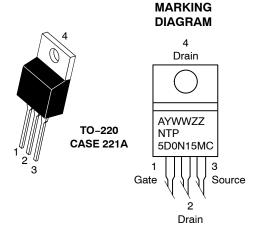
#### ON Semiconductor®

#### www.onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
150 V	5.0 mΩ @ 10 V	139 A



**N-CHANNEL MOSFET** 



NTP5D0N15MC = Specific Device Code

A = Assembly Location

Y = Year WW = Work Week ZZ = Lot Traceability

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NTP5D0N15MC	TO-220 (Pb-Free)	800 / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 2)	$R_{ hetaJC}$	0.7	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{ hetaJA}$	62.5	

#### **ELECTRICAL CHARACTERISTICS** (T<sub>1</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condi	tion	Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		150			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /	I <sub>D</sub> = 250 μA, ref to 25°C			76		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 120 V				1.0	μΑ
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS}$	= ±20 V			±100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D =$	= 532 μΑ	2.5		4.5	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>	I <sub>D</sub> = 532 μA, re	f to 25°C		-8.5		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub>	<sub>0</sub> = 97 A		4.2	5	mΩ
Forward Transconductance	9FS	V <sub>DS</sub> = 10 V, I <sub>D</sub>	= 97 A		146		S
CHARGES, CAPACITANCES & GATE RESIS	STANCE						
Input Capacitance	C <sub>ISS</sub>				6300		
Output Capacitance	C <sub>OSS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 75 V			1900		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>				13		
Gate-Resistance	$R_{G}$				1.1	2.2	Ω
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 75 V; I <sub>D</sub> = 97 A			75		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>				18		
Gate-to-Source Charge	$Q_{GS}$				31		
Gate-to-Drain Charge	$Q_{GD}$				10		
Plateau Voltage	$V_{GP}$				5.4		V
Output Charge	Q <sub>OSS</sub>	V <sub>DD</sub> = 75 V, V <sub>GS</sub> = 0 V			227		nC
SWITCHING CHARACTERISTICS (Note 3)							
Turn-On Delay Time	t <sub>d(ON)</sub>				32		
Rise Time	t <sub>r</sub>	$V_{GS}$ = 10 V, $V_{DD}$ = 75 V, $I_{D}$ = 97 A, $R_{G}$ = 4.7 $\Omega$			14		ns
Turn-Off Delay Time	t <sub>d(OFF)</sub>				45		
Fall Time	t <sub>f</sub>				9.0		
DRAIN-SOURCE DIODE CHARACTERISTIC	s						
Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 97 A	T <sub>J</sub> = 25°C		0.96	1.2	V
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, V <sub>DD</sub> = 75 V dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 97 A			92		ns
Reverse Recovery Charge	Q <sub>RR</sub>				189		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

#### **TYPICAL CHARACTERISTICS**

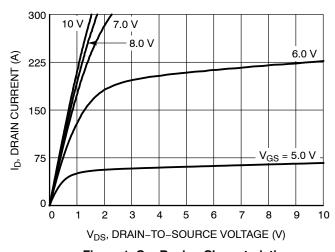


Figure 1. On-Region Characteristics

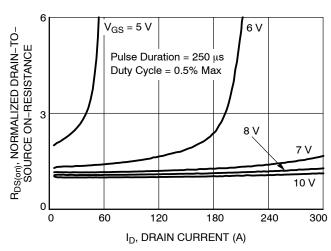


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

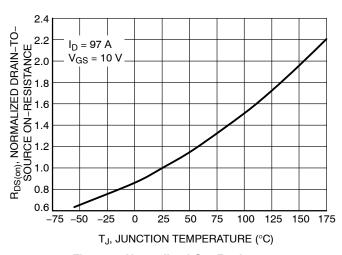


Figure 3. Normalized On–Resistance vs. Junction Temperature

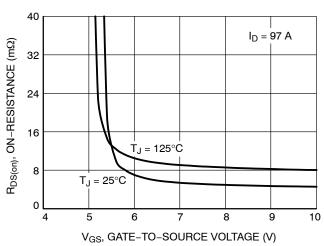


Figure 4. On-Resistance vs. Gate-to-Source Voltage

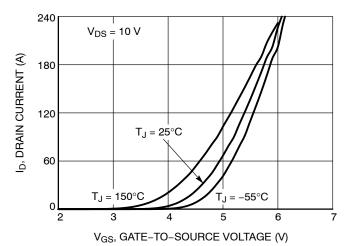


Figure 5. Transfer Characteristics

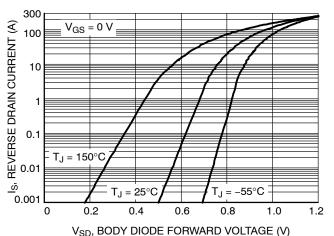


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

#### **TYPICAL CHARACTERISTICS**

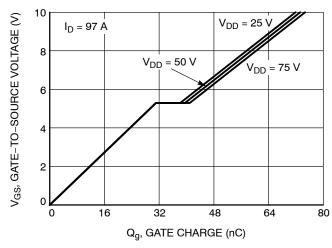


Figure 7. Gate Charge Characteristics

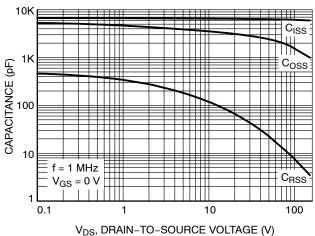


Figure 8. Capacitance vs. Drain-to-Source
Voltage

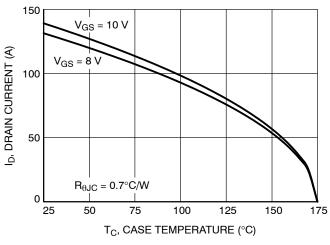


Figure 9. Drain Current vs. Case Temperature

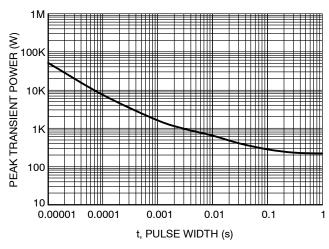


Figure 10. Peak Power

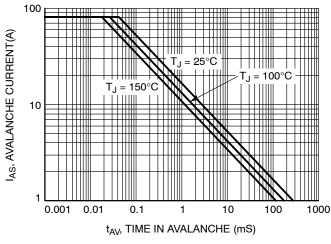


Figure 11. Unclamped Inductive Switching Capability

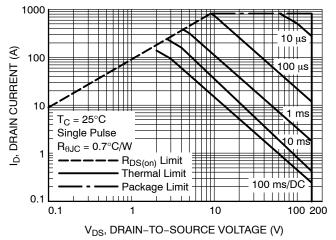


Figure 12. Forward Bias Safe Operating Area

## **TYPICAL CHARACTERISTICS**

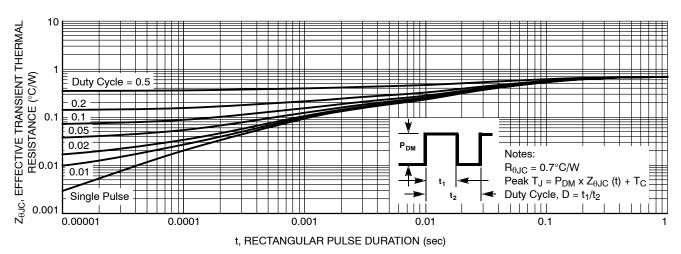
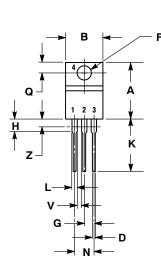
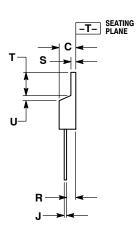


Figure 13. Transient Thermal Impedance

#### PACKAGE DIMENSIONS

TO-220 CASE 221A-09 **ISSUE AH** 





#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INC	HES	MILLIN	ETERS
DIM	MIN	MIN MAX		MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.415	9.66	10.53
С	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
7	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
٧	0.045		1.15	
Z		0.080		2.04

#### STYLE 5

- PIN 1. GATE
  - 2 DRAIN
  - SOURCE 3. DRAIN

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