Quad 2-Input Exclusive OR Gate

High-Performance Silicon-Gate CMOS

The MC74HC86A is identical in pinout to the LS86. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with JEDEC Standard No. 7 A Requirements
- Chip Complexity: 56 FETs or 14 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

LOGIC DIAGRAM

A1
$$\frac{1}{2}$$
 3 Y1

A2 $\frac{4}{5}$ 6 Y2

A3 $\frac{9}{10}$ 8 Y3

A4 $\frac{12}{13}$ 11 Y4

Y = A \oplus B PIN 14 = V_{CC}
= \overline{AB} + A \overline{B} PIN 7 = GND



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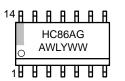


SOIC-14 NB D SUFFIX CASE 751A TSSOP-14 DT SUFFIX CASE 948G

PIN ASSIGNMENT

A1 [1●	14	v _{cc}
B1 [2	13	B4
Y1 [3	12	A4
A2 [4	11	Y4
B2 [5	10	Вз
Y2 [6	9	_ A3
GND [7	8	Y3

MARKING DIAGRAMS





SOIC-14 NB

TSSOP-14

A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

W, WW = Work Week
G or ■ = Pb–Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inp	Output	
Α	В	Υ
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} + 0.5	V
l _{in}	DC Input Current, per Pin	±20	mA
l _{out}	DC Output Current, per Pin	±25	mA
Icc	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: – 7mW/°C from 65° to 125°C TSSOP Package: –6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Paramet	er	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced	DC Input Voltage, Output Voltage (Referenced to GND)		V _{CC}	V
T _A	Operating Temperature, All Package Types		– 55	+ 125	°C
t _r , t _f	(Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Gu	aranteed Li	mit	
Symbol	Parameter	Test Conditions	V _{CC} V	–55 to 25°C	≤ 85°C	≤ 125°C	Unit
V _{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \le 20 \mu\text{A}$	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V _{IL}	Maximum Low–Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \le 20 \mu\text{A}$	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V _{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9 2.48	1.9 4.4 5.9 2.34	1.9 4.4 5.9	V
		$ \begin{aligned} V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}} & I_{\text{out}} \leq 2.4 \text{ mA} \\ I_{\text{out}} \leq 4.0 \text{ mA} \\ I_{\text{out}} \leq 5.2 \text{ mA} \end{aligned} $	3.0 4.5 6.0	2.48 3.98 5.48	3.84 5.34	2.20 3.70 5.20	
V _{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}} \qquad I_{\text{out}} \le 2.4 \text{ mA} \ I_{\text{out}} \le 4.0 \text{ mA} \ I_{\text{out}} \le 5.2 \text{ mA}$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
l _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μΑ
I _{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	1.0	10	40	μΑ

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input t, = $t_f = 6 \text{ ns}$)

			Guaranteed Limit			
Symbol	Parameter	V _{CC}	–55 to 25°C	≤ 85°C	≤ 125°C	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0	100 80	125 90	150 110	ns
PHL	(Figures Fana 2)	4.5 6.0	20 17	25 21	31 26	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0	75 30	95 40	110 55	ns
		4.5 6.0	15 13	19 16	22 19	
C _{in}	Maximum Input Capacitance	_	10	10	10	pF
			Typical	@ 25°C, V _C	_C = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Gate)*			33		pF

^{*} Used to determine the no–load dynamic power consumption: $P_D = C_{PD} \ V_{CC}^2 f + I_{CC} \ V_{CC}$.

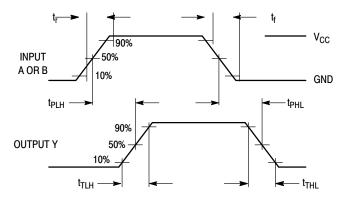
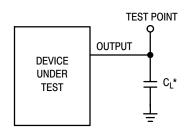


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

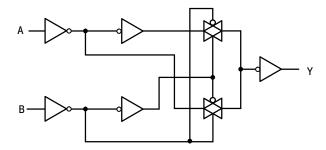


Figure 3. Expanded Logic Diagram (1/4 of Device)

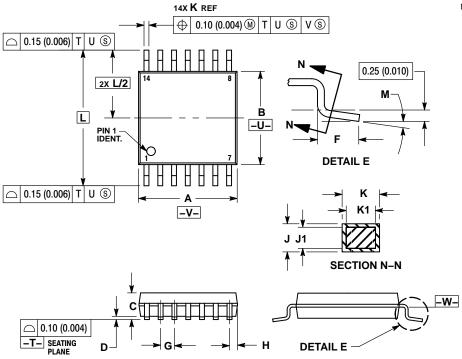
ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HC86ADG	SOIC-14 NB (Pb-Free)	55 Units / Rail
NLV74HC86ADG*	SOIC-14 NB (Pb-Free)	55 Units / Rail
MC74HC86ADR2G	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel
NLV74HC86ADR2G*	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel
MC74HC86ADTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NLV74HC86ADTR2G*	TSSOP-14 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP

PACKAGE DIMENSIONS

TSSOP-14 CASE 948G **ISSUE B**



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER

 - DIMENSIONING AND TOLERANCING FER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
 MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

 DIMENSION B DOES NOT INCLUDE.

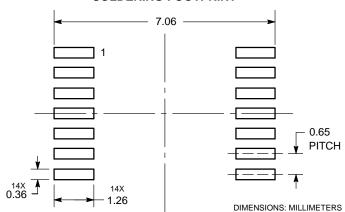
 - EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

 - REFERENCE ONLY.

 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

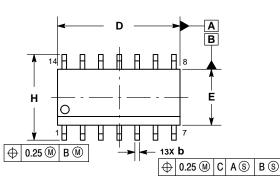
	MILLIMETERS		INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026	BSC	
Н	0.50	0.60	0.020	0.024	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40		0.252 BSC		
М	0 °	8 °	0 °	8 °	

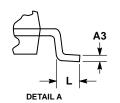
SOLDERING FOOTPRINT

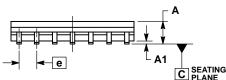


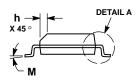
PACKAGE DIMENSIONS

SOIC-14 NB CASE 751A-03 ISSUE K









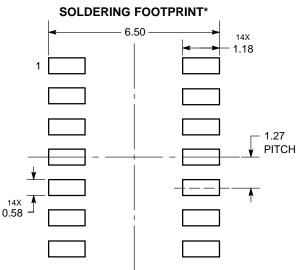
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- ASME 114.3M, 1994.

 2. CONTROLLING DIMENSION: MILLIMETERS.

 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT
- MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
- MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
А3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
Е	3.80	4.00	0.150	0.157
Φ	1.27	BSC	0.050 BSC	
Η	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
М	0°	7°	0 °	7°



DIMENSIONS: MILLIMETERS

*For additional information on our Pb—Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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