19-1868; Rev 1; 1/01

MAXIM

Low-Voltage SOT23 µP Supervisors with Manual Reset and Watchdog Timer

General Description

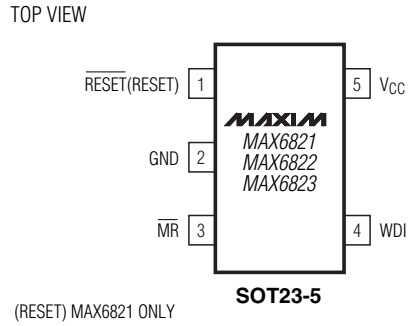
The MAX6821–MAX6825 are low-voltage microprocessor (µP) supervisory circuits that combine voltage monitoring, watchdog timer, and manual reset input functions in a 5-pin SOT23 package. Microprocessor supervisory circuits significantly improve system reliability and accuracy compared to separate ICs or discrete components. These devices assert a reset signal whenever the monitored voltage drops below its preset threshold, keeping it asserted for a minimum timeout period after V_{CC} rises above the threshold. In addition, a watchdog timer monitors against code execution errors. A debounced manual reset is also available. The MAX6821–MAX6825 monitor voltages from +1.8V to +5.0V. These outputs are guaranteed to be in the correct state for V_{CC} down to +1.0V.

Nine preprogrammed reset threshold voltages are available (see *Threshold Suffix Guide*). The MAX6821, MAX6822, and MAX6823 all have a manual reset input and a watchdog timer. The MAX6821 has push-pull RESET, the MAX6822 has open-drain $\overline{RESET}$, and the MAX6823 has push-pull $\overline{RESET}$. The MAX6824 has a watchdog timer and both push-pull $\overline{RESET}$ and push-pull RESET. The MAX6825 has a manual reset input and both push-pull $\overline{RESET}$ and push-pull RESET. The *Selector Guide* explains the functions offered in this series of parts.

Applications

Set-Top Boxes
Computers and Controllers
Embedded Controllers
Intelligent Instruments
Automotive Systems
Critical µP Monitoring
Portable/Battery-Powered Equipment

Pin Configurations



Pin Configurations continued at end of data sheet.

Typical Operating Circuit appears at end of data sheet.

Features

- **Monitors +1.8V, +2.5V, +3.0V, +3.3V, +5.0V Supplies**
- **140ms (min) Reset Timeout Delay**
- **1.6s Watchdog Timeout Period (MAX6821/MAX6822/MAX6823/MAX6824)**
- **Manual Reset Input (MAX6821/MAX6822/MAX6823/MAX6825)**
- **Three Reset Output Options**
  - **Push-Pull $\overline{RESET}$**
  - **Push-Pull RESET**
  - **Open-Drain $\overline{RESET}$**
- **Guaranteed Reset Valid to V_{CC} = +1.0V**
- **Immune to Short Negative V_{CC} Transients**
- **No External Components**
- **Small 5-Pin SOT23 Packages**

Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX6821_UK-T	-40°C to +125°C	5 SOT23-5
MAX6822_UK-T	-40°C to +125°C	5 SOT23-5
MAX6823_UK-T	-40°C to +125°C	5 SOT23-5
MAX6824_UK-T	-40°C to +125°C	5 SOT23-5
MAX6825_UK-T	-40°C to +125°C	5 SOT23-5

**Insert the desired suffix letter (from the table below) into the blank to complete the part number.*

Threshold Suffix Guide

SUFFIX	RESET THRESHOLD (V)
L	4.63
M	4.38
T	3.08
S	2.93
R	2.63
Z	2.32
Y	2.19
W	1.67
V	1.58

Note: *Bold indicates standard versions. Samples are typically available for standard versions only. All parts require a 2.5k minimum order increment. Contact factory for availability.*

Selector Guide appears at end of data sheet.

Low-Voltage SOT23 µP Supervisors with Manual Reset and Watchdog Timer

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6.0V
Open-Drain $\overline{RESET}$ .....-0.3V to +6.0V
Push-Pull $\overline{RESET}$, RESET, $\overline{MR}$, WDI .....-0.3V to (V_{CC} + 0.3V)
Input Current (V_{CC}) 20mA
Output Current ($\overline{RESET}$, RESET) 20mA
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.1mW/°C above +70°C).....571mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V for MAX682_L/M, V_{CC} = +2.7V to +3.6V for MAX682_T/S/R, V_{CC} = +2.1V to +2.75V for MAX682_Z/Y, V_{CC} = +1.53V to +2.0V for MAX682_W/V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	T_A = 0°C to +85°C		1.0		5.5	V
		T_A = -40°C to +125°C		1.2		5.5	
V_{CC} Supply Current ($\overline{MR}$ and WDI Unconnected)	I_{CC}	V_{CC} = +5.5V, no load	T_A = -40°C to +85°C		10	20	µA
			T_A = -40°C to +125°C			30	
		V_{CC} = +3.6V, no load	T_A = -40°C to +85°C		7	16	
			T_A = -40°C to +125°C			25	
		V_{CC} = +3.6V, no load (MAX6825 only)	T_A = -40°C to +85°C		5	12	
			T_A = -40°C to +125°C			20	
V_{CC} Reset Threshold (V_{CC} Falling)	V_{TH}	MAX682_L	T_A = -40°C to +85°C	4.50	4.63	4.75	V
			T_A = -40°C to +125°C	4.47	4.63	4.78	
		MAX682_M	T_A = -40°C to +85°C	4.25	4.38	4.50	
			T_A = -40°C to +125°C	4.22	4.38	4.53	
		MAX682_T	T_A = -40°C to +85°C	3.00	3.08	3.15	
			T_A = -40°C to +125°C	2.97	3.08	3.17	
		MAX682_S	T_A = -40°C to +85°C	2.85	2.93	3.00	
			T_A = -40°C to +125°C	2.83	2.93	3.02	
		MAX682_R	T_A = -40°C to +85°C	2.55	2.63	2.70	
			T_A = -40°C to +125°C	2.53	2.63	2.72	
		MAX682_Z	T_A = -40°C to +85°C	2.25	2.32	2.38	
			T_A = -40°C to +125°C	2.24	2.32	2.40	
		MAX682_Y	T_A = -40°C to +85°C	2.12	2.19	2.25	
			T_A = -40°C to +125°C	2.11	2.19	2.27	
		MAX682_W	T_A = -40°C to +85°C	1.62	1.67	1.71	
			T_A = -40°C to +125°C	1.61	1.67	1.72	
		MAX682_V	T_A = -40°C to +85°C	1.52	1.58	1.62	
Reset Threshold Temperature Coefficient					60		ppm/°C
Reset Threshold Hysteresis					$2 \times V_{TH}$		mV
V_{CC} to Reset Output Delay	t_{RD}	V_{CC} = V_{TH} to (V_{TH} - 100mV)			20		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.5V to +5.5V for MAX682_L/M, V_{CC} = +2.7V to +3.6V for MAX682_T/S/R, V_{CC} = +2.1V to +2.75V for MAX682_Z/Y, V_{CC} = +1.53V to +2.0V for MAX682_W/V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Timeout Period	t_{RP}	T_A = -40°C to +85°C	140	200	280	ms
		T_A = -40°C to +125°C	100		320	
$\overline{RESET}$ Output LOW (Push-Pull or Open-Drain)	V_{OL}	V_{CC} ≥ 1.0V, I_{SINK} = 50µA, reset asserted, T_A = 0°C to +85°C			0.3	V
		V_{CC} ≥ 1.2V, I_{SINK} = 100µA, reset asserted			0.3	
		V_{CC} ≥ 2.55V, I_{SINK} = 1.2mA, reset asserted			0.3	
		V_{CC} ≥ 4.25V, I_{SINK} = 3.2mA, reset asserted			0.4	
$\overline{RESET}$ Output HIGH (Push-Pull Only)	V_{OH}	V_{CC} ≥ 1.8V, I_{SOURCE} = 200µA, reset not asserted	0.8 × V_{CC}			V
		V_{CC} ≥ 3.15V, I_{SOURCE} = 500µA, reset not asserted	0.8 × V_{CC}			
		V_{CC} ≥ 4.75V, I_{SOURCE} = 800µA, reset not asserted	0.8 × V_{CC}			
Open-Drain $\overline{RESET}$ Output Leakage Current (Note 1)	I_{LKG}	V_{CC} > V_{TH}, $\overline{RESET}$ not asserted			1.0	µA
RESET Output HIGH (Push-Pull Only)	V_{OH}	V_{CC} ≥ 1.0V, I_{SOURCE} = 1µA, reset asserted, T_A = 0°C to +85°C	0.8 × V_{CC}			V
		V_{CC} ≥ 1.50V, I_{SOURCE} = 100µA, reset asserted	0.8 × VCC			
		V_{CC} ≥ 2.55V, I_{SOURCE} = 500µA, reset asserted	0.8 × VCC			
		V_{CC} ≥ 4.25V, I_{SOURCE} = 800µA, reset asserted	0.8 × VCC			
RESET Output LOW (Push-Pull Only)	VOL	V_{CC} ≥ 1.8V, I_{SINK} = 500µA, reset not asserted			0.3	V
		V_{CC} ≥ 3.15V, I_{SINK} = 1.2mA, reset not asserted			0.3	
		V_{CC} ≥ 4.75V, I_{SINK} = 3.2mA, reset not asserted			0.4	
MANUAL RESET INPUT (MAX6821/MAX6822/MAX6823/MAX6825)						
$\overline{MR}$ Input Voltage	V_{IL}				0.3 × V_{CC}	V
	V_{IH}		0.7 × V_{CC}			
$\overline{MR}$ Minimum Input Pulse			1			µs
$\overline{MR}$ Glitch Rejection				100		ns
$\overline{MR}$ to Reset Delay				200		ns
$\overline{MR}$ Pullup Resistance			25	50	75	kΩ
WATCHDOG INPUT (MAX6821/MAX6822/MAX6823/MAX6824)						
Watchdog Timeout Period	t_{WD}	T_A = -40°C to +85°C	1.12	1.60	2.40	s
		T_A = -40°C to +125°C	0.80		2.60	
WDI Pulse Width (Note 2)	t_{WDI}		50			ns
WDI Input Voltage	V_{IL}				0.3 × V_{CC}	V
	V_{IH}		0.7 × V_{CC}			
WDI Input Current	I_{WDI}	WDI = V_{CC}, time average		120	160	µA
		WDI = 0, time average	-20	-15		

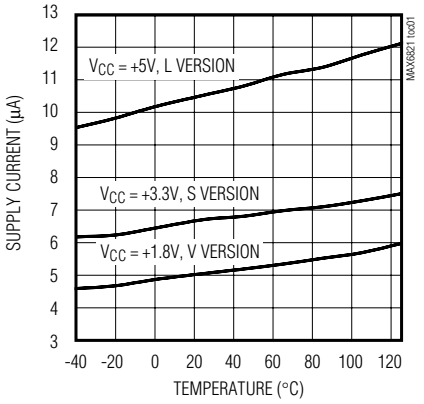
Note 1: Over-temperature limits are guaranteed by design and not production tested. Devices tested at T_A = +25°C.
Note 2: Guaranteed by design and not production tested.

Low-Voltage SOT23 µP Supervisors with Manual Reset and Watchdog Timer

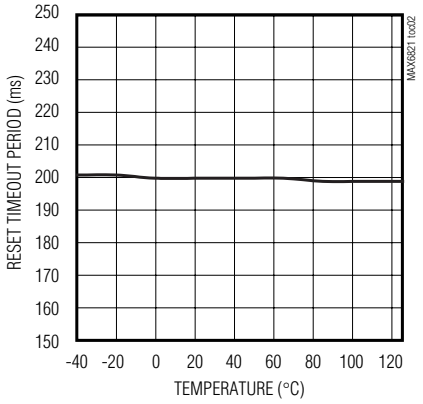
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

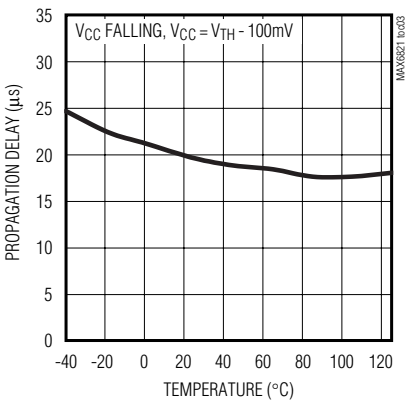
SUPPLY CURRENT vs. TEMPERATURE



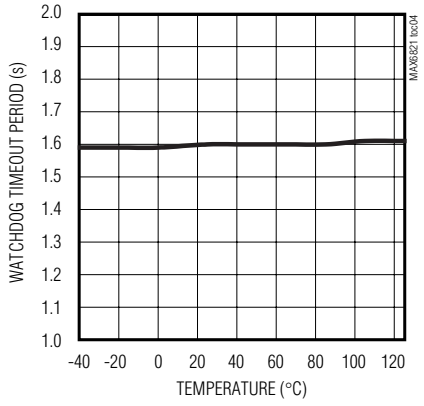
RESET TIMEOUT PERIOD vs. TEMPERATURE



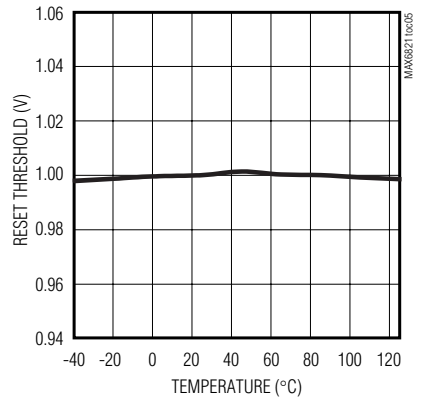
VCC TO RESET OUTPUT DELAY vs. TEMPERATURE



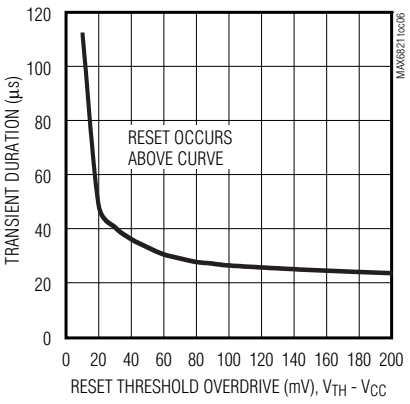
WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



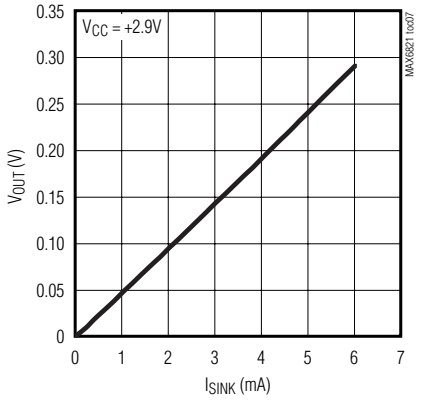
NORMALIZED RESET THRESHOLD DELAY vs. TEMPERATURE



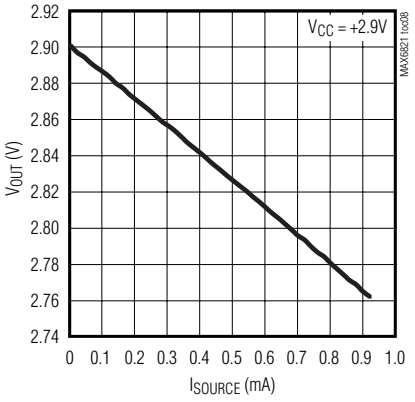
MAXIMUM VCC TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



VOLTAGE OUTPUT LOW vs. I_{SINK}



VOLTAGE OUTPUT HIGH vs. I_{SOURCE}



Pin Description

PIN NUMBERS					PIN NAME	FUNCTION
MAX6821	MAX6822	MAX6823	MAX6824	MAX6825		
	1	1	1	1	$\overline{RESET}$	Active-Low Open-Drain or Push-Pull Reset Output. $\overline{RESET}$ changes from high to low when the V_{CC} input drops below the selected reset threshold, $\overline{MR}$ is pulled low, or the watchdog triggers a reset. $\overline{RESET}$ remains low for the reset timeout period after V_{CC} exceeds the device reset threshold, $\overline{MR}$ goes low to high, or the watchdog triggers a reset.
1			3	3	RESET	Active-High Push-Pull Reset Output. RESET changes from low to high when the V_{CC} input drops below the selected reset threshold, $\overline{MR}$ is pulled low, or the watchdog triggers a reset. RESET remains high for the reset timeout period after V_{CC} exceeds the device reset threshold, $\overline{MR}$ goes low to high, or the watchdog triggers a reset.
2	2	2	2	2	GND	Ground
3	3	3		4	$\overline{MR}$	Active-Low Manual Reset Input. Internal 50kΩ pullup to V_{CC}. Pull low to force a reset. Reset remains active as long as $\overline{MR}$ is low and for the reset timeout period after $\overline{MR}$ goes high. Leave unconnected or connect to V_{CC} if unused.
4	4	4	4		WDI	Watchdog Input. If WDI remains high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and a reset is triggered for the reset timeout period. The internal watchdog timer clears whenever reset is asserted, the manual reset is asserted, or WDI sees a rising or falling edge. If WDI is left unconnected or is connected to a three-stated buffer output, the watchdog feature is disabled.
5	5	5	5	5	V_{CC}	Supply Voltage and Input for Reset Threshold Monitor

Detailed Description

$\overline{RESET}$/RESET Output

A µP's reset input starts the µP in a known state. The MAX6821–MAX6825 µP supervisory circuits assert a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. Whenever V_{CC} falls below the reset threshold, the reset output asserts low for $\overline{RESET}$ and high for RESET. Once V_{CC} exceeds the reset threshold, an internal timer keeps the reset output asserted for the specified reset timeout period (t_{RP}); after this interval, reset output returns to its original state (see Figure 2).

Manual Reset Input

Many µP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. On the MAX6821/MAX6822/MAX6823/MAX6825, a logic low on $\overline{MR}$ asserts a reset. Reset remains asserted while $\overline{MR}$ is low, and for the timeout period (140ms min) after it returns high. $\overline{MR}$ has an internal 50kΩ pullup resistor, so it can be left open if not used. This input can be driven with CMOS logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{MR}$ to GND to provide additional noise immunity.

Watchdog Input

In the MAX6821–MAX6824, the watchdog circuit monitors the µP's activity. If the µP does not toggle (low to high or high to low) the watchdog input (WDI) within the watchdog timeout period (1.6s nominal), reset asserts for the reset timoeout period. The internal 1.6s timer can be cleared by either a reset pulse or by toggling WDI. The WDI can detect pulses as short as 50ns. While reset is asserted, the timer remains cleared and does not count. As soon as reset is released, the timer starts counting (see Figure 3).

Low-Voltage SOT23 µP Supervisors with Manual Reset and Watchdog Timer

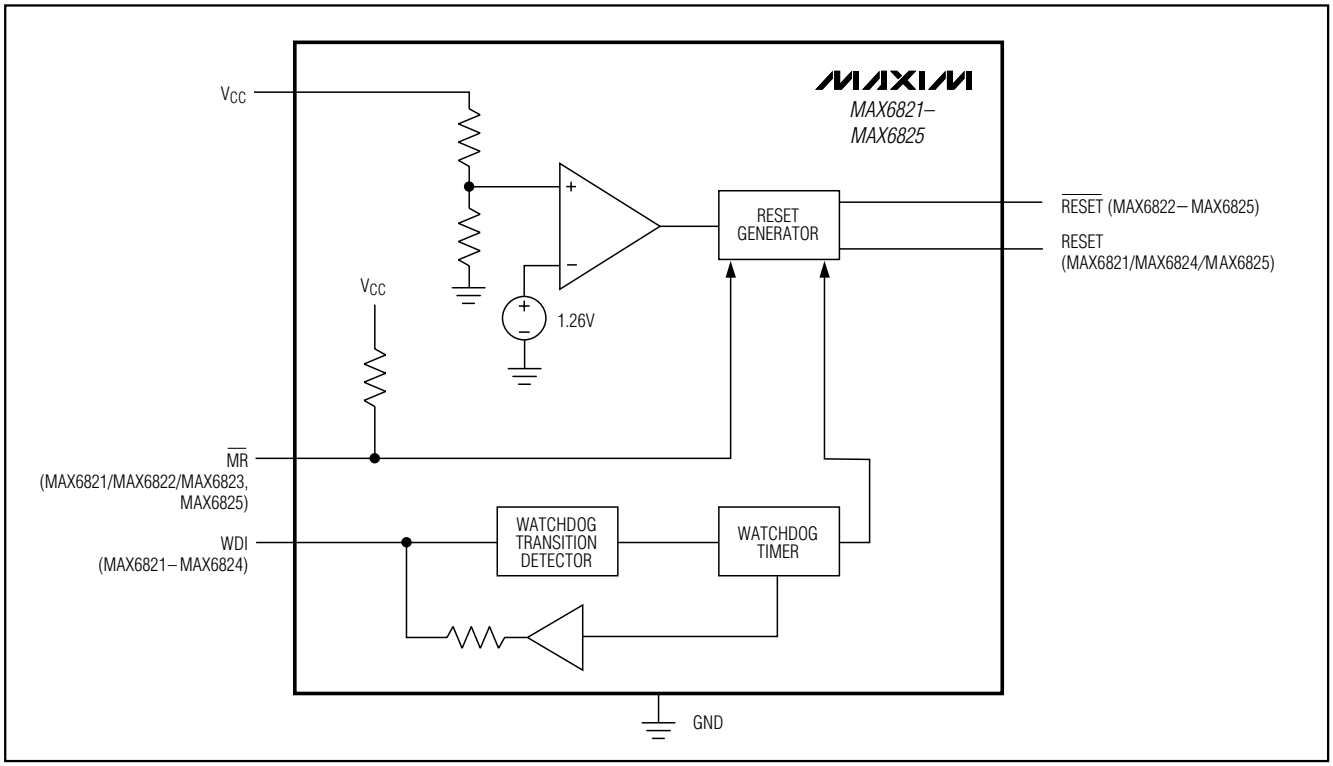


Figure 1. Functional Diagram

Disable the watchdog function by leaving WDI unconnected or by three-stating the driver connected to WDI. The watchdog input is internally driven low during the first 7/8 of the watchdog timeout period and high for the last 1/8 of the watchdog timeout period. When WDI is left unconnected, this internal driver clears the 1.6s timer every 1.4s. When WDI is three-stated or unconnected, the maximum allowable leakage current is 10µA and the maximum allowable load capacitance is 200pF.

Applications Information

Watchdog Input Current

The MAX6821/MAX6822/MAX6823/MAX6824 WDI inputs are internally driven through a buffer and series resistor from the watchdog timer (Figure 1). When WDI is left unconnected, the watchdog timer is serviced within the watchdog timeout period by a low-high-low pulse from the counter chain. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog timeout period, pulsing it low-high-low once within the first 7/8 of the watchdog timeout period to reset the watchdog timer. If WDI is externally driven high for the majority of the timeout period, up to 160µA can flow into WDI.

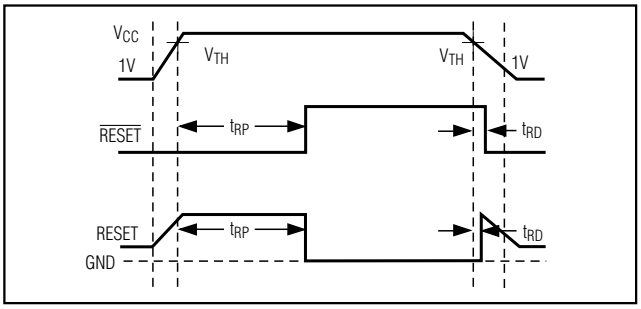


Figure 2. Reset Timing Diagram

Interfacing to µPs with Bidirectional Reset Pins

Since the RESET output on the MAX6822 is open drain, it interfaces easily with µPs that have bidirectional reset pins, such as the Motorola 68HC11. Connecting the µP supervisor's RESET output directly to the microcontroller's RESET pin with a single pullup resistor allows either device to assert reset (see Figure 4).

Negative-Going V_{CC} Transients

These supervisors are relatively immune to short-duration, negative-going V_{CC} transients (glitches), which usually do not require the entire system to shut down.

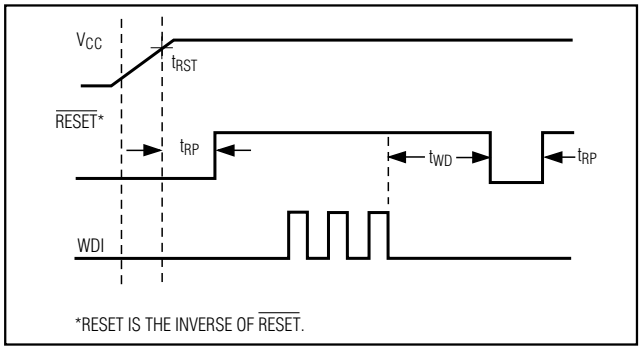


Figure 3. Watchdog Timing Relationship

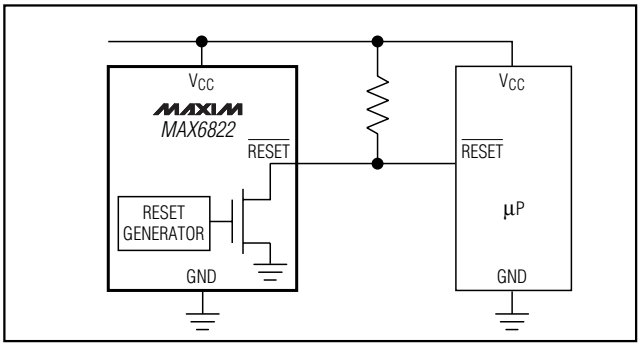


Figure 4. Interfacing Open-Drain RESET to µPs with Bidirectional Reset I/O

Resets are issued to the µP during power-up, power-down, and brownout conditions. The *Typical Operating Characteristics* show a graph of the MAX6821–MAX6825's Maximum V_{CC} Transient Duration vs. Reset Threshold Overdrive, for which reset pulses are not generated. The graph was produced using negative-going V_{CC} pulses, starting at the standard monitored voltage and ending below the reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a negative-going V_{CC} transient can typically have without triggering a reset pulse. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 20µs or less will not trigger a reset pulse.

Watchdog Software Considerations

One way to help the watchdog timer monitor software execution more closely is to set and reset the watchdog input at different points in the program, rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop, in which the watchdog timer would continue to be reset inside the loop, keeping the watchdog from timing out.

Figure 5 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should hang in any subroutine, the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued. As described in the *Watchdog Input Current* section, this scheme results in higher time average WDI input current than does leaving WDI low for the majority of the timeout period and periodically pulsing it low-high-low.

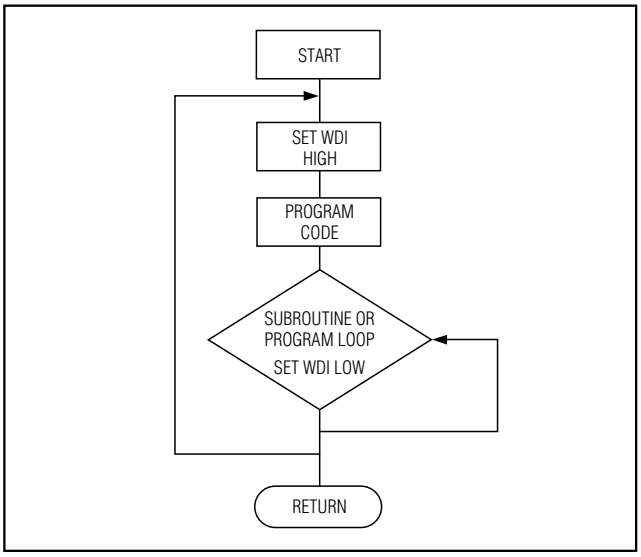
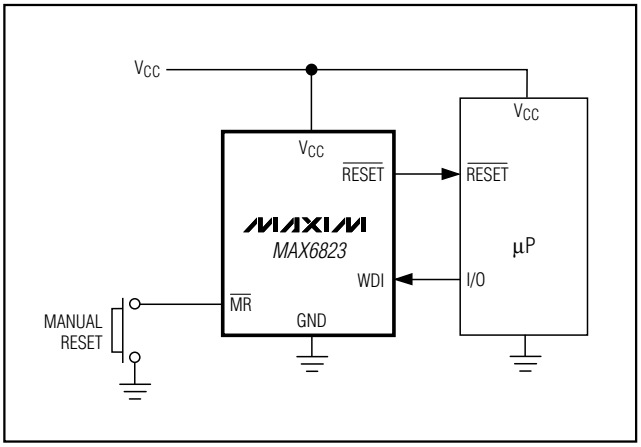


Figure 5. Watchdog Flow Diagram

Typical Operating Circuit



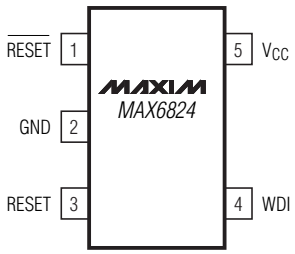
Low-Voltage SOT23 µP Supervisors with Manual Reset and Watchdog Timer

Selector Guide

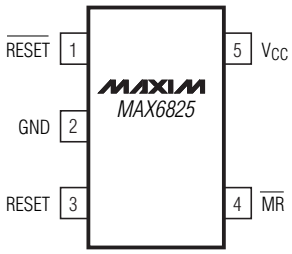
FUNCTION	ACTIVE-LOW $\overline{\text{RESET}}$	ACTIVE-HIGH RESET	OPEN-DRAIN $\overline{\text{RESET}}$	WATCHDOG INPUT	MANUAL RESET INPUT
MAX6821	—	✔	—	✔	✔
MAX6822	—	—	✔	✔	✔
MAX6823	✔	—	—	✔	✔
MAX6824	✔	✔	—	✔	—
MAX6825	✔	✔	—	—	✔

Pin Configurations (continued)

TOP VIEW



SOT23-5



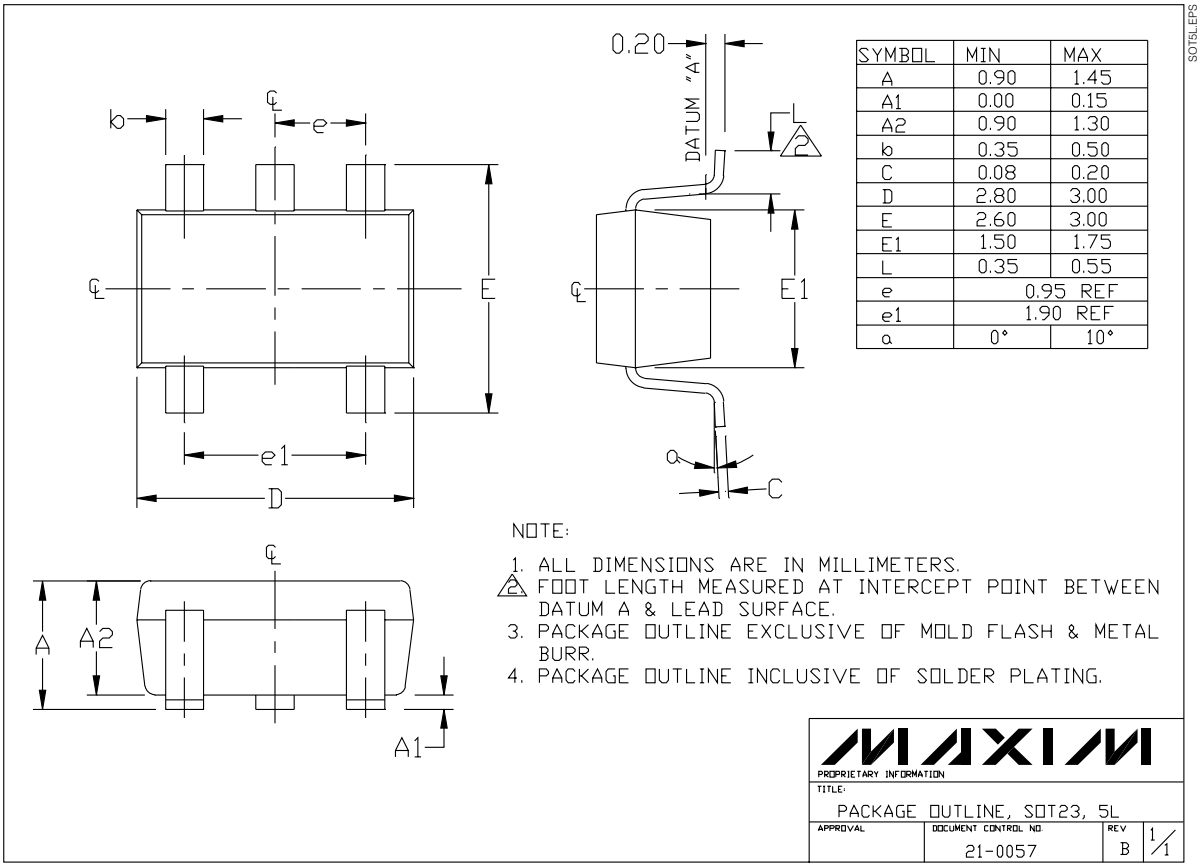
SOT23-5

Chip Information

TRANSISTOR COUNT: 750

PROCESS: BiCMOS

Package Information



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
e1	1.90 REF	
α	0°	10°