19-4754; Rev 0; 12/97

High-Speed, Single-Supply, Gain of +2, Closed-Loop, Rail-to-Rail Buffers with Enable

General Description

The MAX4214/MAX4215/MAX4217/MAX4219/MAX4222 are precision, closed-loop, gain of +2 (or -1) buffers featuring high slew rates, high output current drive, and low differential gain and phase error. They operate with a single +3.15V to +11V supply or with ±1.575V to ±5.5V dual supplies. The input common-mode voltage range extends 100mV beyond the negative power-supply rail, and the output swings Rail-to-Rail®.

These devices require only 5.5mA of quiescent supply current while achieving a 230MHz -3dB bandwidth and a 600V/µs slew rate. In addition, the MAX4215/MAX4219 have a disable feature that reduces the supply current to 400µA per buffer. Input voltage noise is only 10nV/$\sqrt{Hz}$, and input current noise is only 1.3pA/$\sqrt{Hz}$. This buffer family is ideal for low-power/low-voltage applications requiring wide bandwidth, such as video, communications, and instrumentation systems. For space-sensitive applications, the MAX4214 comes in a miniature 5-pin SOT23 package.

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4214EUK-T	-40°C to +85°C	5 SOT23-5	ABAH
MAX4215ESA	-40°C to +85°C	8 SO	—
MAX4215EUA	-40°C to +85°C	8 µMAX	—
MAX4217ESA	-40°C to +85°C	8 SO	—
MAX4217EUA	-40°C to +85°C	8 µMAX	—
MAX4219ESD	-40°C to +85°C	14 SO	—
MAX4219EEE	-40°C to +85°C	16 QSOP	—
MAX4222ESD	-40°C to +85°C	14 SO	—
MAX4222EEE	-40°C to +85°C	16 QSOP	—

Applications

Battery-Powered Instruments

Video Line Driver

Analog-to-Digital Converter Interface

CCD Imaging Systems

Video Routing and Switching Systems

Video Multiplexing Applications

Typical Application Circuit appears at end of data sheet.

Rail-to-Rail is a registered trademark of Nippon Motorola, Inc.

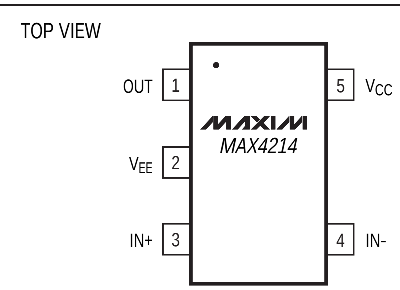
Features

- **Internal Precision Resistors for Closed-Loop Gains of +2V/V or -1V/V**
- **High Speed:**
  - **230MHz -3dB Bandwidth**
  - **90MHz 0.1dB Gain Flatness (MAX4219/22)**
  - **600V/µs Slew Rate**
- **Single 3.3V/5.0V Operation**
- **Outputs Swing Rail-to-Rail**
- **Input Common-Mode Range Extends Beyond V_{EE}**
- **Low Differential Gain/Phase Error: 0.03%/0.04°**
- **Low Distortion at 5MHz:**
  - **-72dBc SFDR**
  - **-71dB Total Harmonic Distortion**
- **High Output Drive: ±120mA**
- **Low 5.5mA Supply Current**
- **400µA Shutdown Supply Current (MAX4215/19)**
- **Space-Saving SOT23-5, µMAX, or QSOP Packages**

Selector Guide

PART	NO. OF AMPS	ENABLE	PIN-PACKAGE
MAX4214	1	No	5 SOT23
MAX4215	1	Yes	8 SO/µMAX
MAX4217	2	No	8 SO/µMAX
MAX4219	3	Yes	14 SO, 16 QSOP
MAX4222	4	No	14 SO, 16 QSOP

Pin Configurations



SOT23-5

Pin Configurations continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) 12V
IN_-, IN_+, OUT_, EN_ ....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Output Short-Circuit Duration to V_{CC} or V_{EE} ....Continuous
Continuous Power Dissipation (T_A = +70°C)
5-pin SOT23 (derate 7.1mW/°C above +70°C)....571mW
8-pin SO (derate 5.9mW/°C above +70°C)....471mW
8-pin µMAX (derate 4.1mW/°C above +70°C)....330mW
14-pin SO (derate 8.3mW/°C above +70°C)....667mW
16-pin QSOP (derate 8.3mW/°C above +70°C)....667mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = 0V, IN_- = 0V, EN_ = 5V, R_L = ∞ to 0V, V_{OUT} = V_{CC}/2, noninverting configuration, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range		V_{CC} to V_{EE}, guaranteed by PSRR tests		3.15		11.0	V
Input Voltage Range	V_{IN}	IN_+		V_{EE} - 0.1		V_{CC} - 2.25	V
		IN_-		V_{EE} - 0.1		V_{CC} + 0.1	
Input Offset Voltage	V_{OS}	R_L = 50Ω	SO, QSOP		4	10	mV
			SOT23-5, µMAX		4	15	
Input Offset Voltage Drift	TCV_{OS}				8		µV/°C
Input Offset Voltage Matching		Between any two channels for MAX4217/MAX4219/MAX4222			1		mV
Input Bias Current	I_B	IN_+			5.4	12	µA
Input Resistance	R_{IN}	IN_+, over input voltage range			3		MΩ
Voltage Gain	A_V	$R_L \geq 50Ω$, (V_{EE} + 0.5V) ≤ V_{OUT} ≤ (V_{CC} - 2.0V)		1.9	2	2.1	V/V
Power-Supply Rejection Ratio (Note 2)	PSRR	V_{CC} = 5V, V_{EE} = 0V, V_{OUT} = 2.0V		55	58		dB
		V_{CC} = 5V, V_{EE} = -5V, V_{OUT} = 0V		60	66		
		V_{CC} = 3.3V, V_{EE} = 0V, V_{OUT} = 0.90V			45		
Output Resistance	R_{OUT}	f = DC			25		mΩ
Output Current	I_{OUT}	R_L = 20Ω to V_{CC} or V_{EE}		±100	±120		mA
Short-Circuit Output Current	I_{SC}	Sinking or sourcing			±150		mA
Output Voltage Swing	V_{OUT}	R_L = 50Ω	V_{CC} - V_{OH}		1.60	1.90	V
			V_{OL} - V_{EE}		0.04	0.075	
		R_L = 150Ω	V_{CC} - V_{OH}		0.75	1.00	
			V_{OL} - V_{EE}		0.04	0.075	
		R_L = 2kΩ	V_{CC} - V_{OH}		0.06		
			V_{OL} - V_{EE}		0.06		
Disabled Output Resistance	$R_{OUT(OFF)}$	MAX4215/MAX4219, EN_ = 0V, 0V ≤ V_{OUT} ≤ 5V			1		kΩ
EN_ Logic Low Threshold	V_{IL}	MAX4215/MAX4219				V_{CC} - 2.6	V
EN_ Logic High Threshold	V_{IH}	MAX4215/MAX4219		V_{CC} - 1.6			V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = 0V, IN_- = 0V, EN_ = 5V, R_L = ∞ to 0V, V_{OUT} = V_{CC}/2, noninverting configuration, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN_ Logic Input Low Current	I_{IL}	MAX4215/MAX4219, (V_{EE} + 0.2V) ≤ EN_ ≤ V_{CC}		0.5		µA
		MAX4215/MAX4219, EN_ = V_{EE}		200	350	
EN_ Logic Input High Current	I_{IH}	MAX4215/MAX4219, EN_ = V_{CC}		0.5	10	µA
Quiescent Supply Current (per Buffer)	I_{CC}			5.5	7.0	mA
Shutdown Supply Current	I_{SD}	MAX4215/MAX4219, disabled (EN_ = V_{EE})		400	550	µA

Note 1: The MAX421_EU_ is 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.

Note 2: PSR for single +5V supply tested with V_{EE} = 0V, V_{CC} = +4.5V to +5.5V; for dual ±5V supply with V_{EE} = -4.5V to -5.5V, V_{CC} = +4.5V to +5.5V; and for single +3V supply with V_{EE} = 0V, V_{CC} = +3.15V to +3.45V.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = 0V, IN_- = 0V, EN_ = 5V, R_L = 100Ω to V_{CC}/2, noninverting configuration, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW_{-3dB}	V_{OUT} = 100mVp-p	MAX4214/MAX4215/MAX4217		230		MHz
			MAX4219/MAX4222		200		
Full-Power -3dB Bandwidth	FPBW	V_{OUT} = 2Vp-p	MAX4214/MAX4215/MAX4217		220		MHz
			MAX4219/MAX4222		200		
Bandwidth for 0.1dB Gain Flatness	$BW_{0.1dB}$	V_{OUT} = 100mVp-p	MAX4214/MAX4215/MAX4217		50		MHz
			MAX4219/MAX4222		90		
Slew Rate	SR	V_{OUT} = 2V step			600		V/µs
Settling Time to 0.1%	t_S	V_{OUT} = 2V step			45		ns
Rise/Fall Time	t_R, t_F	V_{OUT} = 100mVp-p			1		ns
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz, V_{OUT} = 2Vp-p			-72		dBc
Harmonic Distortion	HD	V_{OUT} = 2Vp-p, f_C = 5MHz	Second harmonic		-72		dBc
			Third harmonic		-77		
			Total harmonic distortion		-71		
Third-Order Intercept	IP3	f = 10MHz			35		dBm
Input 1dB Compression Point		f = 10MHz			11		dBm
Differential Phase Error	DP	NTSC, R_L = 150Ω			0.04		degrees
Differential Gain Error	DG	NTSC, R_L = 150Ω			0.03		%
Input Noise-Voltage Density	e_n	f = 10kHz			10		$nV/\sqrt{Hz}$
Input Noise-Current Density	i_n	f = 10kHz			1.3		$pA/\sqrt{Hz}$
Input Capacitance	C_{IN}				1		pF
Disabled Output Capacitance	$C_{OUT(OFF)}$	MAX4215/MAX4219, EN_ = 0V			2		pF

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = 0V, IN_- = 0V, EN_ = 5V, R_L = 100Ω to V_{CC}/2, noninverting configuration, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

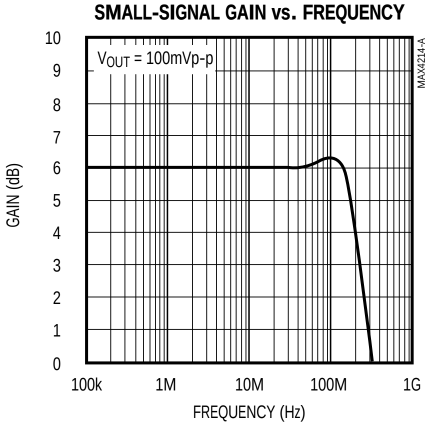
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	Z_{OUT}	f = 10MHz		200		mΩ
Buffer Enable Time	t_{ON}	MAX4215/MAX4219		100		ns
Buffer Disable Time	t_{OFF}	MAX4215/MAX4219		1		µs
Buffer Gain Matching		MAX4217/MAX4219/MAX4222, f = 10MHz, V_{OUT} = 100mVp-p		0.1		dB
All-Hostile Crosstalk	X_{TALK}	MAX4217/MAX4219/MAX4222, f = 10MHz, V_{OUT} = 2Vp-p		-95		dB

Note 2: PSR for single +5V supply tested with V_{EE} = 0V, V_{CC} = +4.5V to +5.5V; for dual ±5V supply with V_{EE} = -4.5V to -5.5V, V_{CC} = +4.5V to +5.5V; and for single +3V supply with V_{EE} = 0V, V_{CC} = +3.15V to +3.45V.

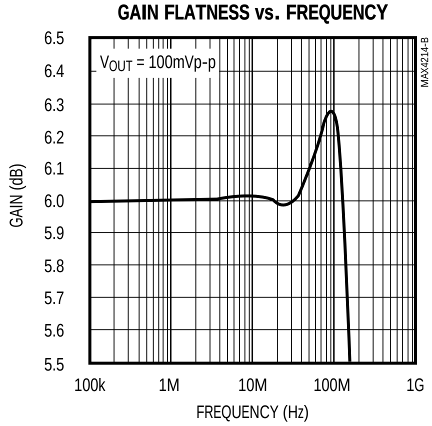
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = 0V, A_{VCL} = +2V/V, R_L = 100Ω to V_{CC}/2, T_A = +25°C, unless otherwise noted.)

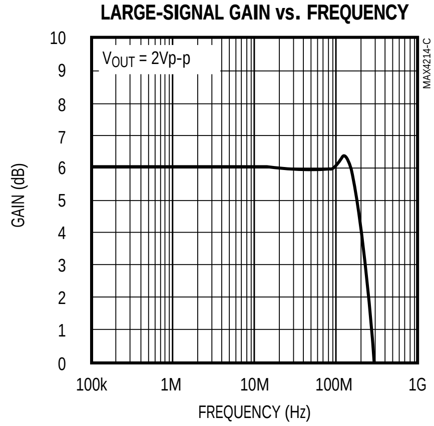
MAX4214/MAX4215/MAX4217 SMALL-SIGNAL GAIN vs. FREQUENCY



MAX4214/MAX4215/MAX4217 GAIN FLATNESS vs. FREQUENCY



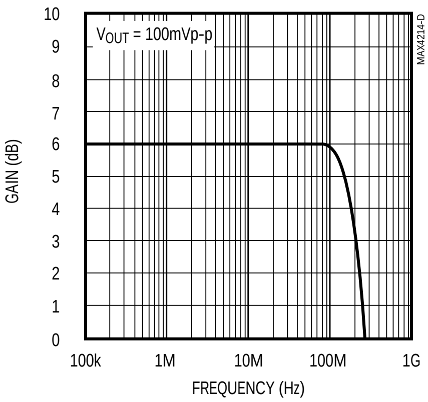
MAX4214/MAX4215/MAX4217 LARGE-SIGNAL GAIN vs. FREQUENCY



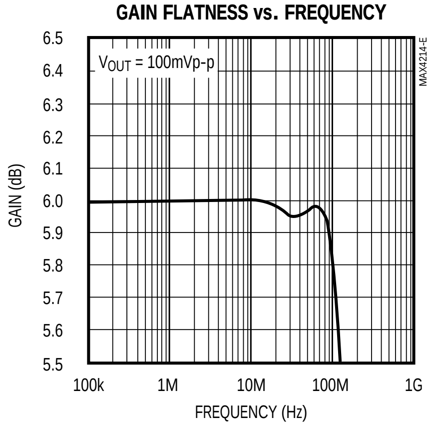
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, A_{VCL} = +2V/V, R_L = 100Ω to V_{CC}/2, T_A = +25°C, unless otherwise noted.)

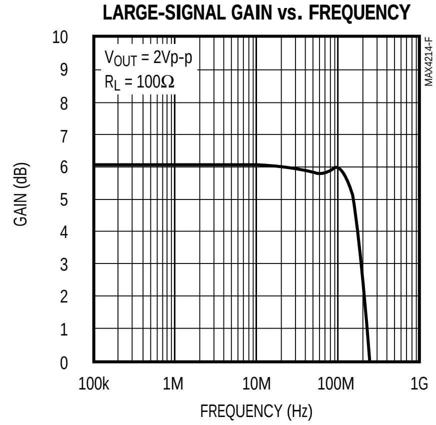
MAX4219/MAX4222
SMALL-SIGNAL GAIN vs. FREQUENCY



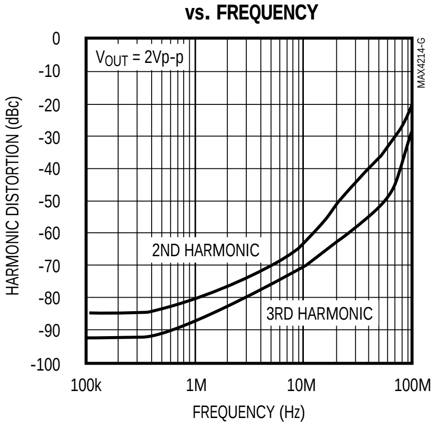
MAX4219/MAX4222
GAIN FLATNESS vs. FREQUENCY



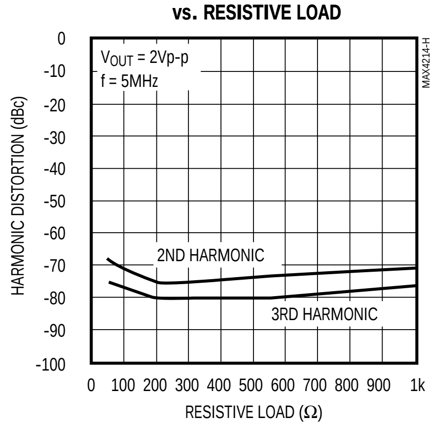
MAX4219/MAX4222
LARGE-SIGNAL GAIN vs. FREQUENCY



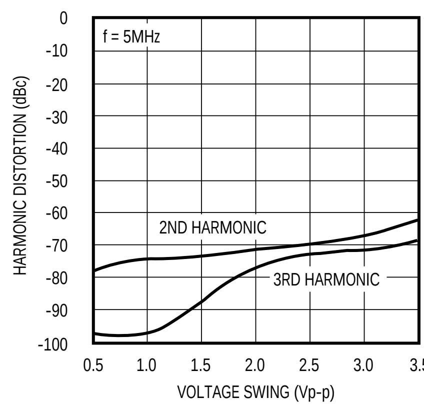
HARMONIC DISTORTION vs. FREQUENCY



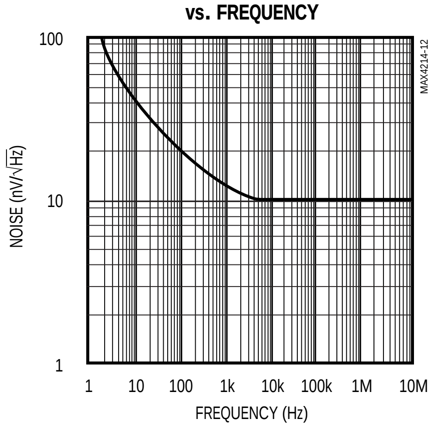
HARMONIC DISTORTION vs. RESISTIVE LOAD



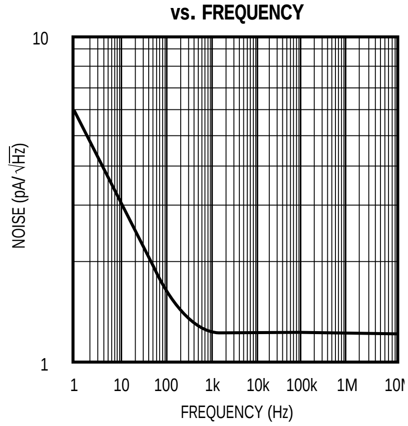
HARMONIC DISTORTION vs. VOLTAGE SWING



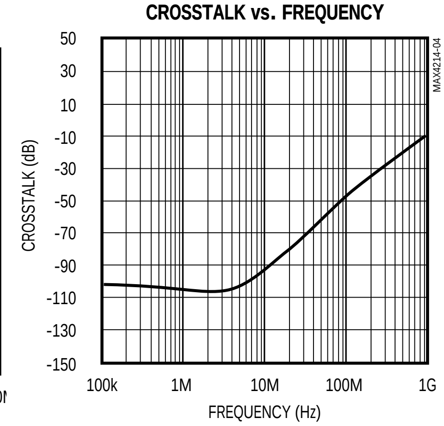
VOLTAGE-NOISE DENSITY vs. FREQUENCY



CURRENT-NOISE DENSITY vs. FREQUENCY



MAX4217/MAX4219/MAX4222
CROSSTALK vs. FREQUENCY

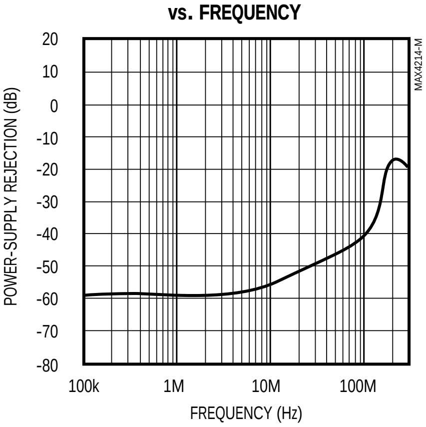


High-Speed, Single-Supply, Gain of +2, Closed-Loop, Rail-to-Rail Buffers with Enable

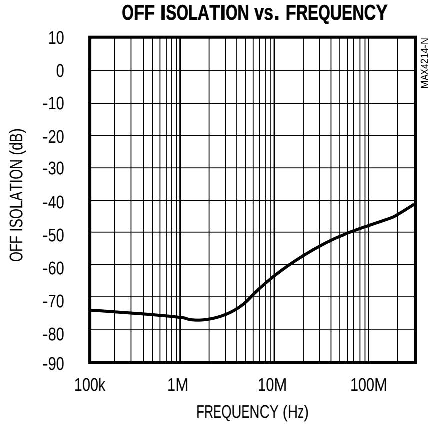
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, A_{VCL} = +2V/V, R_L = 100Ω to V_{CC}/2, T_A = +25°C, unless otherwise noted.)

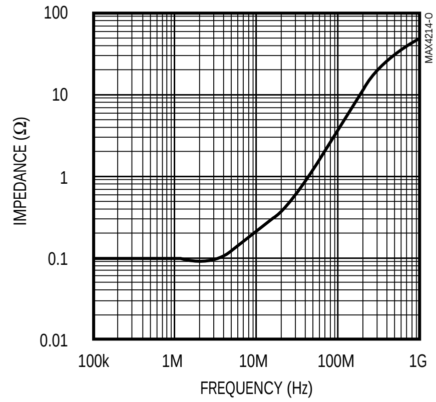
POWER-SUPPLY REJECTION vs. FREQUENCY



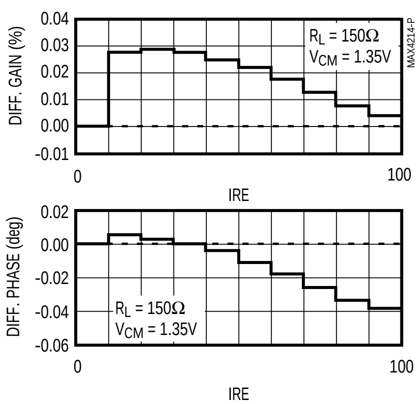
MAX4215/MAX4219 OFF ISOLATION vs. FREQUENCY



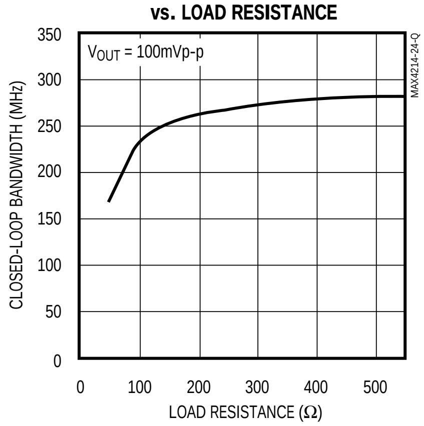
CLOSED-LOOP OUTPUT IMPEDANCE vs. FREQUENCY



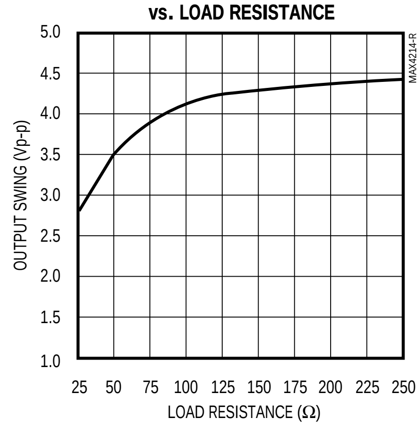
DIFFERENTIAL GAIN AND PHASE



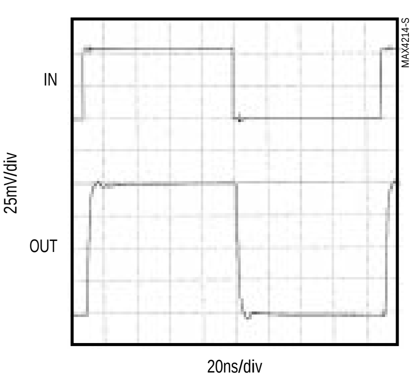
CLOSED-LOOP BANDWIDTH vs. LOAD RESISTANCE



OUTPUT SWING vs. LOAD RESISTANCE

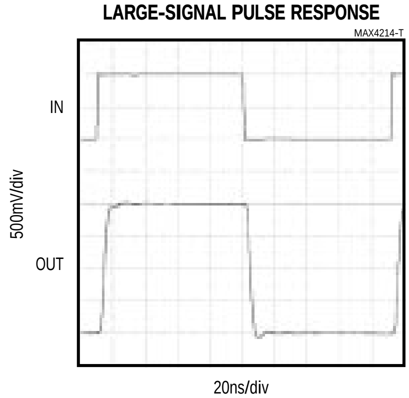


SMALL-SIGNAL PULSE RESPONSE



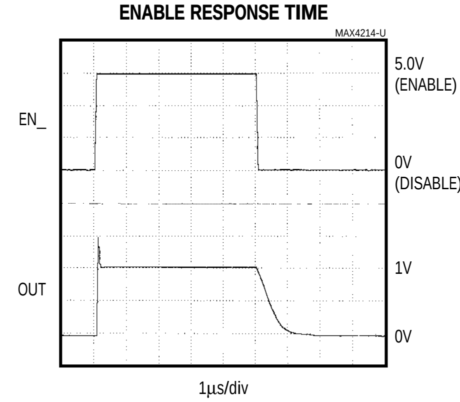
V_{CM} = 1.25V, R_L = 100Ω to GROUND

LARGE-SIGNAL PULSE RESPONSE



V_{CM} = 0.9V, R_L = 100Ω to GROUND

ENABLE RESPONSE TIME



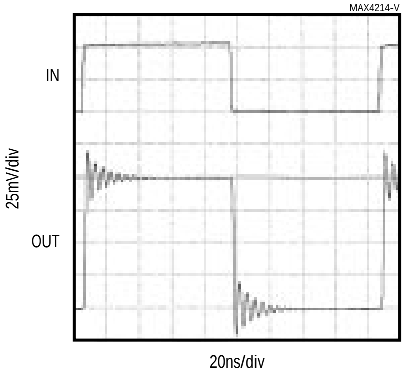
V_{IN} = 0.5V

High-Speed, Single-Supply, Gain of +2, Closed-Loop, Rail-to-Rail Buffers with Enable

Typical Operating Characteristics (continued)

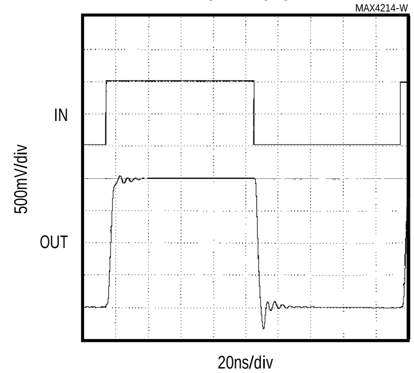
(V_{CC} = +5V, V_{EE} = 0V, A_{VCL} = +2V/V, R_L = 100Ω to V_{CC}/2, T_A = +25°C, unless otherwise noted.)

SMALL-SIGNAL PULSE RESPONSE (C_L = 5pF)



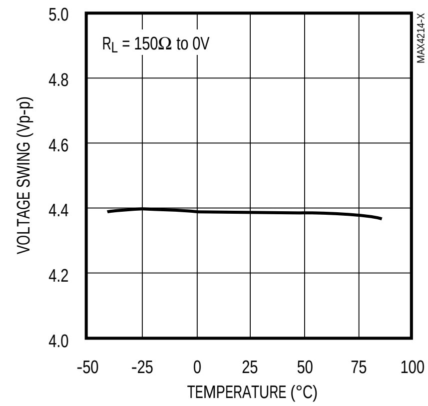
V_{CM} = 1.25V, R_L = 100Ω to 0V

LARGE-SIGNAL PULSE RESPONSE (C_L = 5pF)

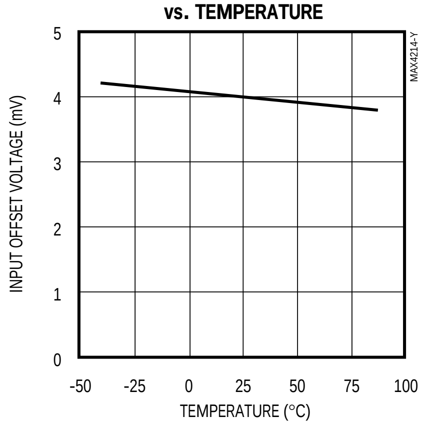


V_{CM} = 1.75V, R_L = 100Ω to 0V

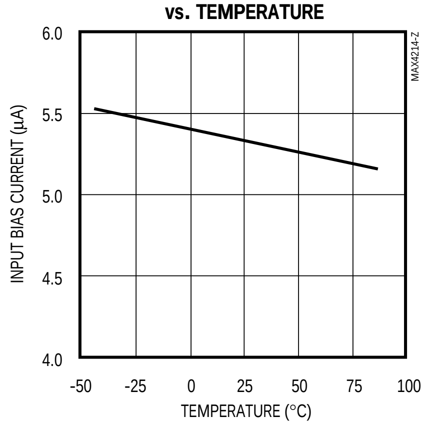
VOLTAGE SWING vs. TEMPERATURE



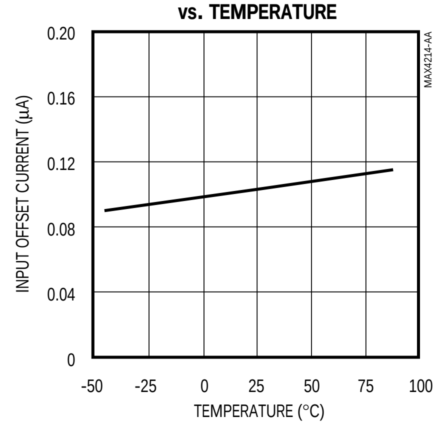
INPUT OFFSET VOLTAGE vs. TEMPERATURE



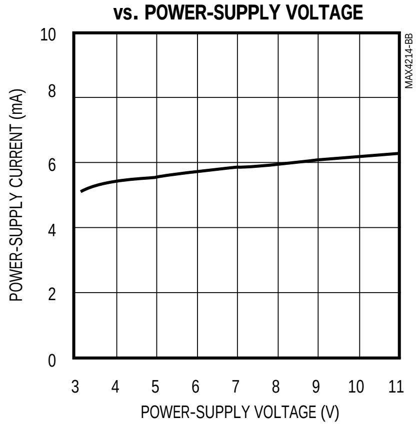
INPUT BIAS CURRENT vs. TEMPERATURE



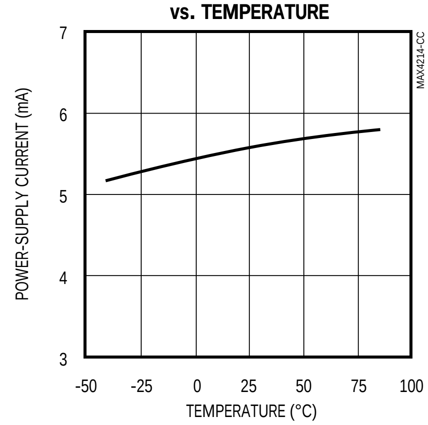
INPUT OFFSET CURRENT vs. TEMPERATURE



POWER-SUPPLY CURRENT (PER AMPLIFIER) vs. POWER-SUPPLY VOLTAGE



POWER-SUPPLY CURRENT (PER AMPLIFIER) vs. TEMPERATURE



High-Speed, Single-Supply, Gain of +2, Closed-Loop, Rail-to-Rail Buffers with Enable

Pin Description

PIN							NAME	FUNCTION
MAX4214	MAX4215	MAX4217	MAX4219		MAX4222			
SOT23-5	SO/μMAX	SO/μMAX	SO	QSOP	SO	QSOP		
—	1, 5	—	—	8, 9	—	8, 9	N.C.	No Connect. Not internally connected. Tie to ground or leave open.
1	6	—	—	—	—	—	OUT	Amplifier Output
2	4	4	11	13	11	13	V_{EE}	Negative Power Supply or Ground (in single-supply operation)
3	3	—	—	—	—	—	IN+	Noninverting Input
4	2	—	—	—	—	—	IN-	Inverting Input
5	7	8	4	4	4	4	V_{CC}	Positive Power Supply
—	8	—	—	—	—	—	EN	Enable Amplifier
—	—	—	1	1	—	—	ENA	Enable Amplifier A
—	—	—	3	3	—	—	ENB	Enable Amplifier B
—	—	—	2	2	—	—	ENC	Enable Amplifier C
—	—	1	7	7	1	1	OUTA	Amplifier A Output
—	—	2	6	6	2	2	INA-	Amplifier A Inverting Input
—	—	3	5	5	3	3	INA+	Amplifier A Noninverting Input
—	—	7	8	10	7	7	OUTB	Amplifier B Output
—	—	6	9	11	6	6	INB-	Amplifier B Inverting Input
—	—	5	10	12	5	5	INB+	Amplifier B Noninverting Input
—	—	—	14	16	8	10	OUTC	Amplifier C Output
—	—	—	13	15	9	11	INC-	Amplifier C Inverting Input
—	—	—	12	14	10	12	INC+	Amplifier C Noninverting Input
—	—	—	—	—	14	16	OUTD	Amplifier D Output
—	—	—	—	—	13	15	IND-	Amplifier D Inverting Input
—	—	—	—	—	12	14	IND+	Amplifier D Noninverting Input

Detailed Description

The MAX4214/MAX4215/MAX4217/MAX4219/MAX4222 are single-supply, rail-to-rail output, voltage-feedback, closed-loop buffers that employ current-feedback techniques to achieve 600V/µs slew rates and 230MHz bandwidths. These buffers use internal 500Ω resistors to provide a preset closed-loop gain of +2V/V in the noninverting configuration or -1V/V in the inverting configuration. Excellent harmonic distortion and differential gain/phase performance make them an ideal choice for a wide variety of video and RF signal-processing applications.

Local feedback around the buffer's output stage ensures low output impedance, which reduces gain sensitivity to load variations. This feedback also produces demand-driven current bias to the output transistors for ±120mA drive capability, while constraining total supply current to less than 7mA.

Applications Information

Power Supplies

These devices operate from a single +3.15V to +11V power supply or from dual supplies of ±1.575V to ±5.5V. For single-supply operation, bypass the V_{CC} pin to ground with a 0.1µF capacitor as close to the pin as possible. If operating with dual supplies, bypass each supply with a 0.1µF capacitor.

Selecting Gain Configuration

Each buffer in the MAX4214 family can be configured for a voltage gain of +2V/V or -1V/V. For a gain of +2V/V, ground the inverting terminal. Use the noninverting terminal as the signal input of the buffer (Figure 1a). Grounding the noninverting terminal and using the inverting terminal as the signal input configures the buffer for a gain of -1V/V (Figure 1b).

Since the inverting input exhibits a 500Ω input impedance, terminate the input with a 56Ω resistor when configured for an inverting gain in 50Ω applications (terminate with 88Ω in 75Ω applications). Terminate the input with a 49.9Ω resistor in the noninverting case. Output terminating resistors should directly match cable impedances in either configuration.

Layout Techniques

Maxim recommends using microstrip and stripline techniques to obtain full bandwidth. To ensure the PC board does not degrade the buffer's performance, design it for a frequency greater than 1GHz. Pay careful attention to inputs and outputs to avoid large parasitic capacitance. Whether or not you use a constant-impedance board, observe the following guidelines when designing the board:

- Don't use wire-wrapped boards. They are too inductive.
- Don't use IC sockets. They increase parasitic capacitance and inductance.
- Use surface-mount instead of through-hole components for better high-frequency performance.
- Use a PC board with at least two layers; it should be as free from voids as possible.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.

Input Voltage Range and Output Swing

The MAX4214 family's input range extends from (V_{EE} - 100mV) to (V_{CC} - 2.25V). Input ground sensing increases the dynamic range for single-supply applications. The outputs drive a 2kΩ load to within 60mV of the power-supply rails. With smaller resistive loads, the output swing is reduced as shown in the *Electrical Characteristics* and *Typical Operating Characteristics*.

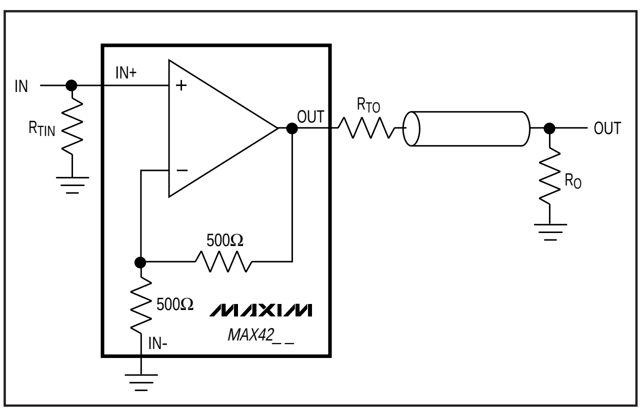


Figure 1a. Noninverting Gain Configuration (A_V = +2V/V)

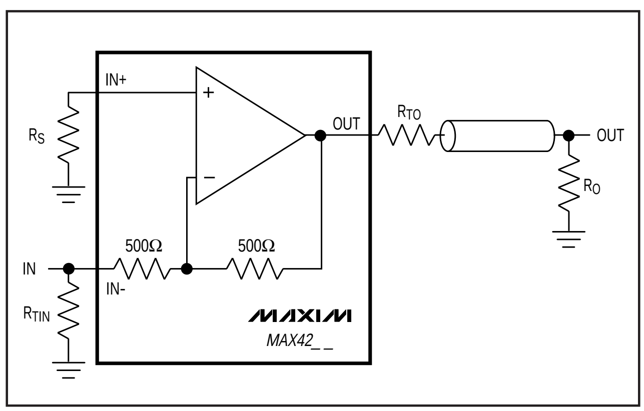


Figure 1b. Inverting Gain Configuration (A_V = -1V/V)

As the load resistance decreases, the useful input range is effectively limited by the output drive capability, since the buffers have a fixed voltage gain of +2V/V or -1V/V.

For example, a 50Ω load can typically be driven from 40mV above V_{EE} to 1.6V below V_{CC}, or 40mV to 3.4V when operating from a single +5V supply. If the buffer is operated in the noninverting, gain of +2V/V configuration with the inverting input grounded, the useful input voltage range becomes 20mV to 1.7V instead of the -100mV to 2.75V indicated by the *Electrical Characteristics*. Beyond the useful input range, the buffer output is a nonlinear function of the input, but it will not undergo phase reversal or latchup.

Enable

The MAX4215 and MAX4219 have an enable feature (EN_) that allows the buffer to be placed in a low-power state. When the buffers are disabled, the supply current is reduced to 400µA per buffer.

As the voltage at the EN_ pin approaches the negative supply rail, the EN_ input current rises. Figure 2 shows a graph of EN_ input current versus EN_ pin voltage. Figure 3 shows the addition of an optional resistor in series with the EN pin, to limit the magnitude of the current increase. Figure 4 displays the resulting EN pin input current to voltage relationship.

Disabled Output Resistance

The MAX4214/MAX4215/MAX4217/MAX4219/MAX4222 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages (Figure 5). This protection circuitry consists of five back-to-back Schottky diodes between IN_+ and IN_-. These diodes reduce the disabled output resistance from 1kΩ to 500Ω when the output voltage is 3V greater or less than the voltage at IN_+. Under these conditions, the input protection diodes will be forward biased, lowering the disabled output resistance to 500Ω.

Output Capacitive Loading and Stability

The MAX4214 family provides maximum AC performance with no load capacitance. This is the case when the load is a properly terminated transmission line. These devices are designed to drive up to 20pF of load capacitance without oscillating, but AC performance will be reduced under these conditions.

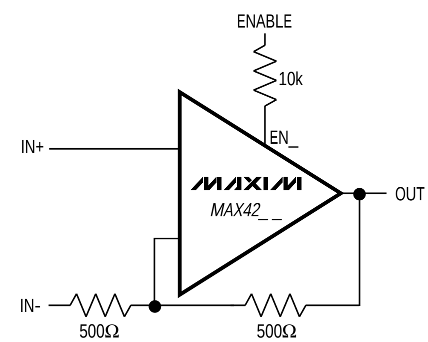


Figure 3. Circuit to Reduce Enable Logic-Low Input Current

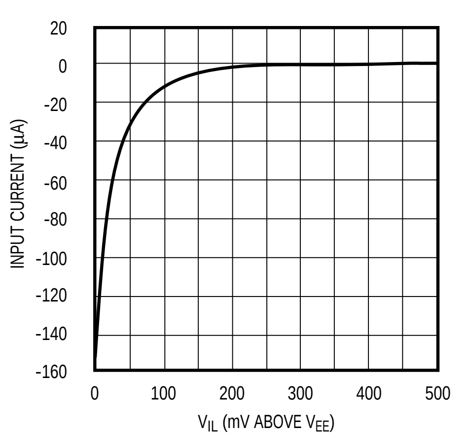


Figure 2. Enable Logic-Low Input Current vs. Enable Logic-Low Threshold

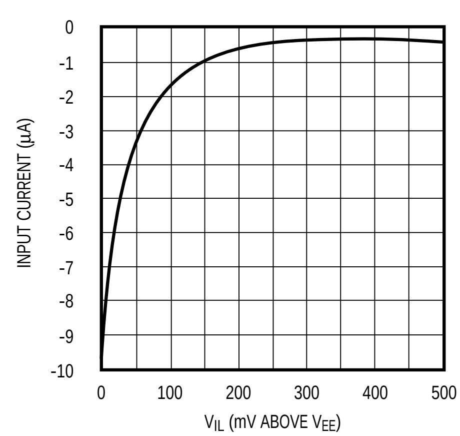


Figure 4. Enable Logic-Low Input Current vs. Enable Logic-Low Threshold with 10kΩ Series Resistor

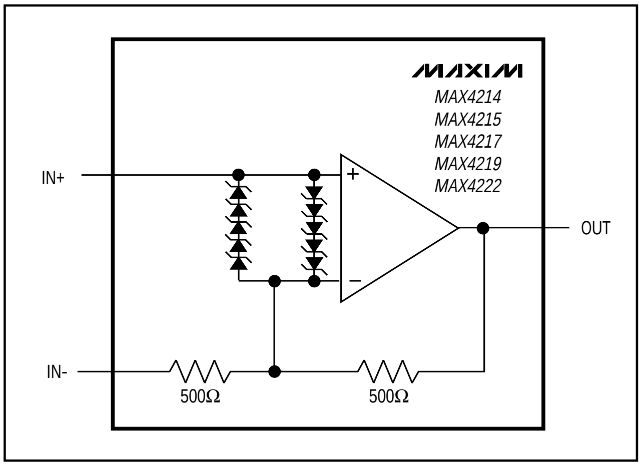


Figure 5. Input Protection Circuit

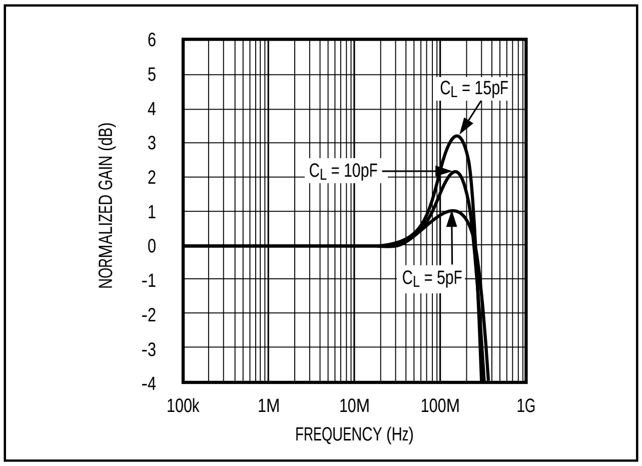


Figure 6. Small-Signal Gain vs. Frequency with Load Capacitance and No Isolation Resistor

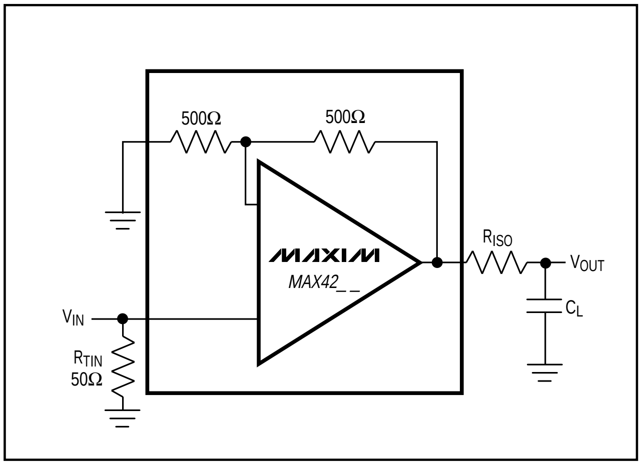


Figure 7. Driving a Capacitive Load Through an Isolation Resistor

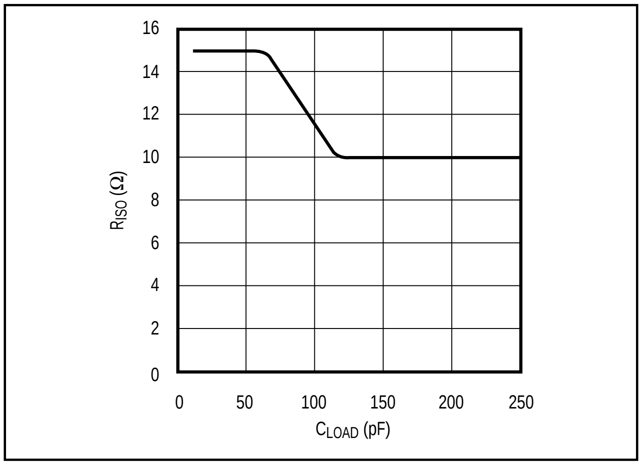


Figure 8. Isolation Resistance vs. Capacitive Load

Driving large capacitive loads increases the chance of oscillations occurring in most amplifier circuits. This is especially true for circuits with high loop gains, such as voltage followers. The buffer's output resistance and the load capacitor combine to add a pole and excess phase to the loop response. If the frequency of this pole is low enough to interfere with the loop response and degrade phase margin sufficiently, oscillations can occur.

A second problem when driving capacitive loads results from the amplifier's output impedance, which looks inductive at high frequencies. This inductance forms an L-C resonant circuit with the capacitive load, which causes peaking in the frequency response and degrades the amplifier's gain margin.

Figure 6 shows the devices' frequency response under different capacitive loads. To drive loads with greater than 20pF of capacitance or to settle out some of the peaking, the output requires an isolation resistor like the one shown in Figure 7. Figure 8 is a graph of the optimal isolation resistor versus load capacitance. Figure 9 shows the frequency response of the MAX4214/MAX4215/MAX4217/MAX4219/MAX4222 when driving capacitive loads with a 27Ω isolation resistor.

Coaxial cables and other transmission lines are easily driven when properly terminated at both ends with their characteristic impedance. Driving back-terminated transmission lines essentially eliminates the lines' capacitance.

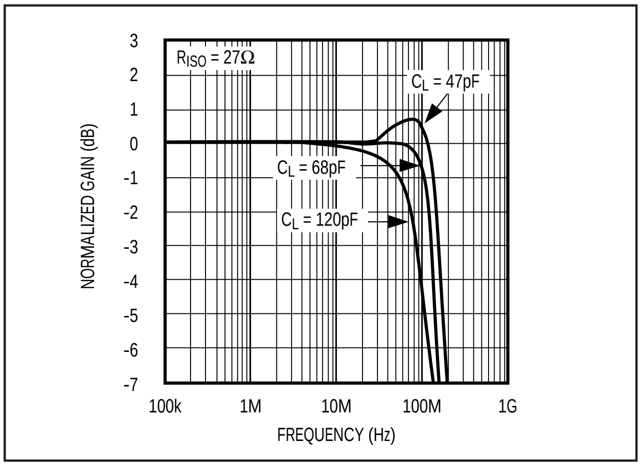
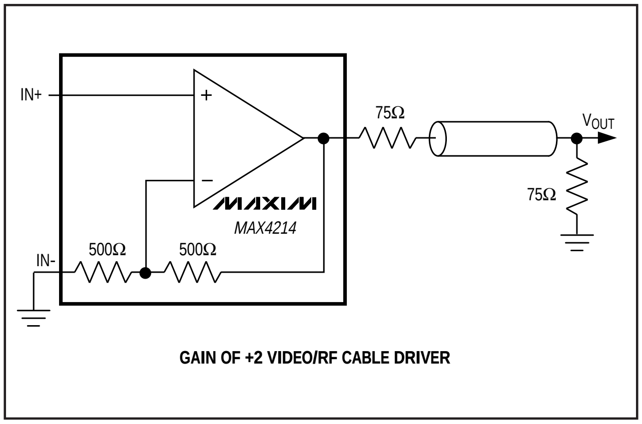


Figure 9. Small-Signal Gain vs. Frequency with Load Capacitance and 27Ω Isolation Resistor

Typical Application Circuit

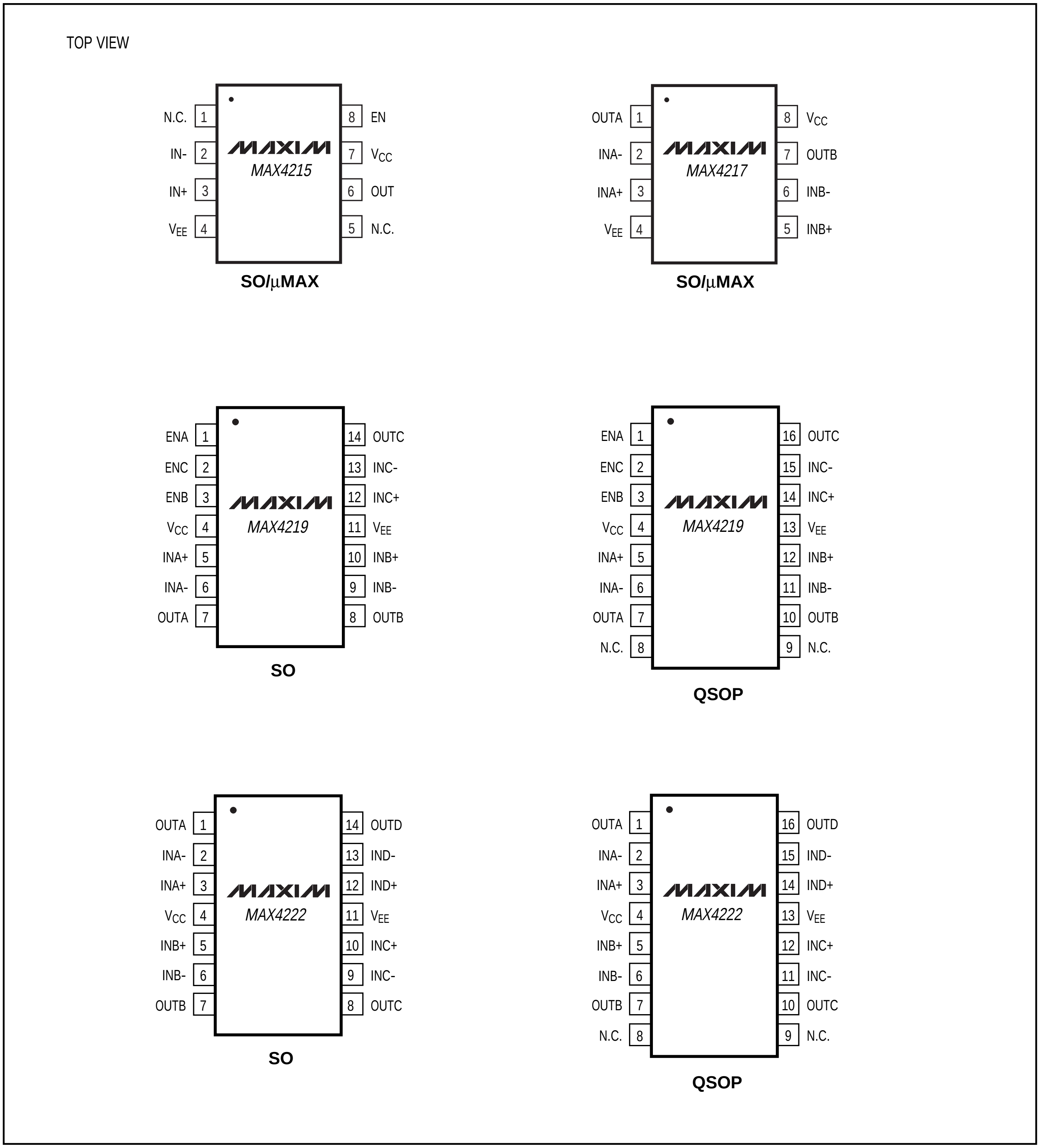


Chip Information

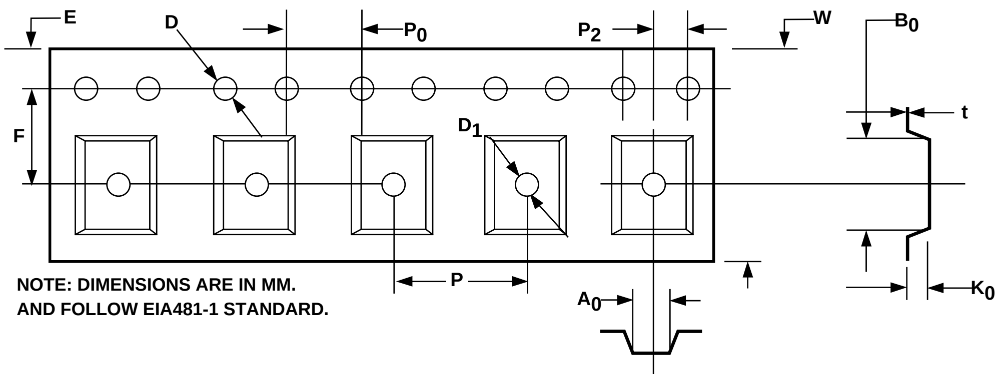
PART	NO. OF TRANSISTORS
MAX4214	95
MAX4215	95
MAX4217	190
MAX4219	299
MAX4222	362

SUBSTRATE CONNECTED TO V_{EE}

Pin Configurations (continued)



Tape-and-Reel Information



NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

A_0	3.200	±0.102
B_0	3.099	±0.102
D	1.499	+0.102 +0.000
D_1	0.991	+0.254 +0.000

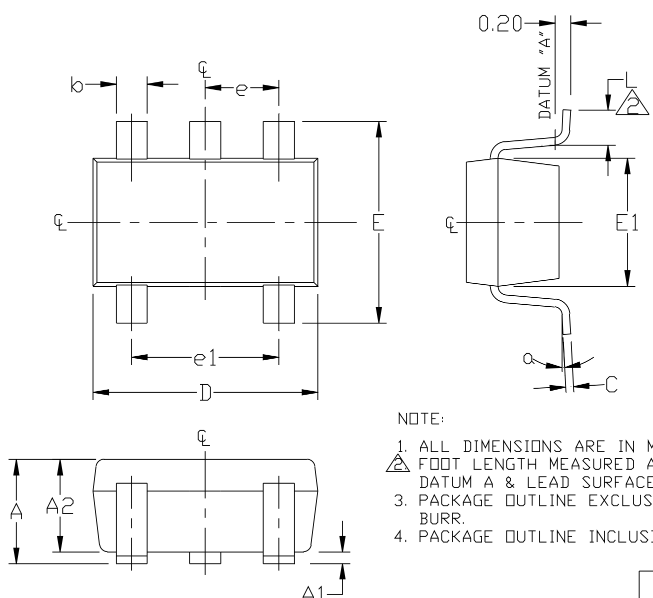
E	1.753	±0.102
F	3.505	±0.051
K_0	1.397	±0.102
P	3.988	±0.102

P_0	3.988	±0.102
$P_0$10	40.005	±0.203
P_2	2.007	±0.051
t	0.254	±0.127
W	8.001	+0.305 -0.102

5 SOT23-5

Package Information

SOT5L.EPS



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
e1	1.90 REF	
α	0°	10°

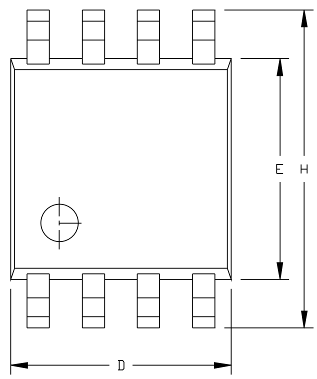
NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, SOT23, 5L

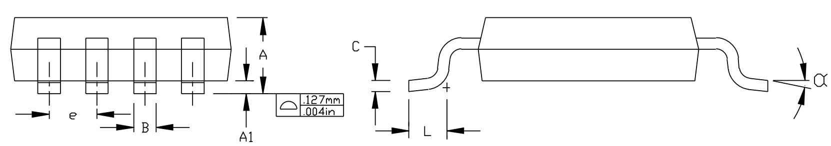
APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0057	B	1/1

Package Information (continued)

8LUMAXD.EPS



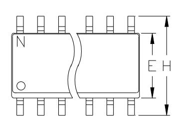
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256		0.65	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°

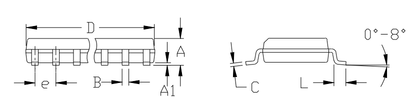


NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm(.006").
3. CONTROLLING DIMENSION: INCHES

MAXIM
PROPRIETARY INFORMATION
TITLE:
8LD uMAX PACKAGE OUTLINE DWG.
APPROVAL | DOCUMENT CONTROL NO. 21-0036 | REV D | 1/1

SOICN.EPS





	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

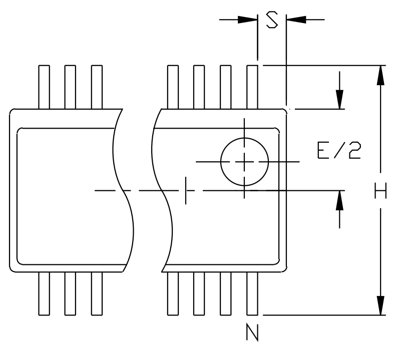
	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM PROPRIETARY INFORMATION | TITLE: PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | DOCUMENT CONTROL NUMBER 21-0041 REV A

High-Speed, Single-Supply, Gain of +2, Closed-Loop, Rail-to-Rail Buffers with Enable

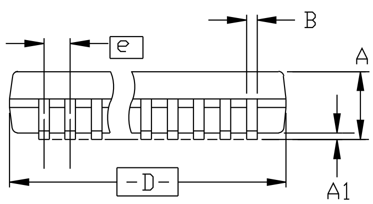
Package Information (continued)

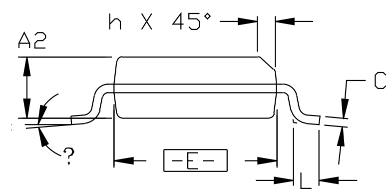


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.127	0.25
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.19	0.25
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
S	SEE VARIATIONS			
?	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.27	1.40		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.64	0.76		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.64	0.76		





NOTES:

1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006"
3. CONTROLLING DIMENSIONS: INCHES

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, QSOP, .150 INCH, .025" LEAD PITCH

APPROVAL | DOCUMENT CONTROL NO. 21-0055 | REV A | 1/1

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