1A, 0.9V to 10V, Very Low Dropout Linear Regulator

FEATURES

- **V_{IN} Range: 0.9V to 10V**
- **Dropout Voltage: 145mV Typical**
- **Output Current: 1A**
- **Adjustable Output (V_{REF} = $V_{OUT(MIN)}$ = 200mV)**
- Stable with Low ESR, Ceramic Output Capacitors (10µF Minimum)
- 0.05% Typical Load Regulation from 1mA to 1A
- Quiescent Current: 400µA Typical
- 7.5µA Typical Quiescent Current in Shutdown
- Current Limit Protection
- Reverse-Battery Protection with No Reverse Current
- Thermal Limiting with Hysteresis
- 16-Lead (5mm × 3mm) DFN and MSOP Packages

APPLICATIONS

- High Efficiency Linear Regulators
- Battery-Powered Systems
- Logic Supplies
- Post Regulator for Switching Supplies
- Wireless Modems
- FPGA Core Supplies

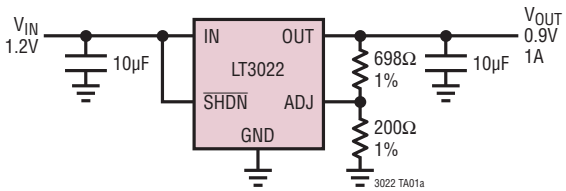
DESCRIPTION

The LT®3022 is a very low dropout voltage (VLDO™) linear regulator that operates from single input supplies down to 0.9V. The device supplies 1A output current with 145mV typical dropout voltage. The LT3022 is ideal for low input voltage to low output voltage applications, providing comparable electrical efficiency to a switching regulator. The regulator optimizes stability and transient response with low ESR ceramic output capacitors as small as 10µF. Other LT3022 features include 0.05% typical line regulation and 0.05% typical load regulation. In shutdown, quiescent current typically drops to 7.5µA. Internal protection circuitry includes reverse-battery protection, current limiting, thermal limiting with hysteresis and reverse-current protection.

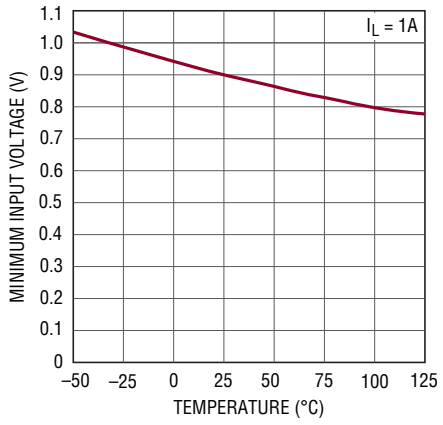
The LT3022 is available as an adjustable device with an output voltage range down to the 200mV reference. The LT3022 regulator is available in the thermally enhanced low profile (0.75mm) 16-lead (5mm × 3mm) DFN and MSOP packages.

TYPICAL APPLICATION

1.2V to 0.9V, 1A VLDO Regulator



Minimum Input Voltage

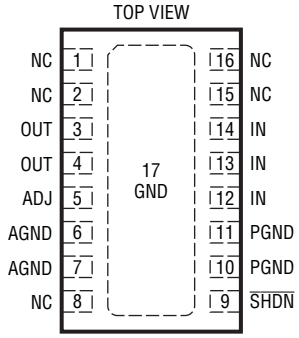


ABSOLUTE MAXIMUM RATINGS (Note 1)

IN Pin Voltage ..... ±10V
OUT Pin Voltage ..... ±10V
Input-to-Output Differential Voltage ..... ±10V
ADJ Pin Voltage ..... ±10V
$\overline{SHDN}$ Pin Voltage ..... ±10V
Output Short-Circuit Duration ..... Indefinite

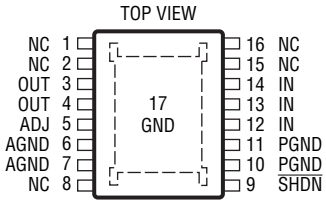
Operating Junction Temperature Range
E-, I-Grades (Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP Package ..... 300°C

PIN CONFIGURATION



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 38°C/W*, θ_{JC} = 4°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB
*SEE THE APPLICATIONS INFORMATION SECTION



MSE PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 38°C/W*, θ_{JC} = 5°C/W TO 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB
*SEE THE APPLICATIONS INFORMATION SECTION

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3022EDHC#PBF	LT3022EDHC#TRPBF	3022	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LT3022IDHC#PBF	LT3022IDHC#TRPBF	3022	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LT3022EMSE#PBF	LT3022EMSE#TRPBF	3022	16-Lead Plastic MSOP	–40°C to 125°C
LT3022IMSE#PBF	LT3022IMSE#TRPBF	3022	16-Lead Plastic MSOP	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT3022EDHC	LT3022EDHC#TR	3022	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LT3022IDHC	LT3022IDHC#TR	3022	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LT3022EMSE	LT3022EMSE#TR	3022	16-Lead Plastic MSOP	–40°C to 125°C
LT3022IMSE	LT3022IMSE#TR	3022	16-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage (Notes 4, 6)	I_{LOAD} = 1A, T_A > 0°C I_{LOAD} = 1A, T_A ≤ 0°C			0.9 0.9	1.05 1.10	V V
ADJ Pin Voltage (Notes 5, 6)	V_{IN} = 1.5V, I_{LOAD} = 1mA 1.15V < V_{IN} < 10V, 1mA < I_{LOAD} < 1A	 ●	196 194	200 200	204 206	mV mV
Line Regulation (Note 7)	ΔV_{IN} = 1.15V to 10V, I_{LOAD} = 1mA	●	–1.5	–0.1	0.5	mV
Load Regulation (Note 7)	V_{IN} = 1.15V, ΔI_{LOAD} = 1mA to 1A	 ●	–0.5 –1.0	0.1	0.5 1.0	mV mV
Dropout Voltage (Notes 8, 9)	I_{LOAD} = 10mA	 ●		45	75 135	mV mV
	I_{LOAD} = 100mA	 ●		55	90 175	mV mV
	I_{LOAD} = 500mA	 ●		110	150 235	mV mV
	I_{LOAD} = 1A	 ●		145	185 285	mV mV
GND Pin Current, V_{IN} = $V_{OUT(NOMINAL)}$ + 0.4V (Notes 9, 10)	I_{LOAD} = 0mA I_{LOAD} = 1mA I_{LOAD} = 100mA I_{LOAD} = 500mA I_{LOAD} = 1A	 ● ● ● ●		400 1.2 3.4 8.3 18	 2.5 8.5 20 36	µA mA mA mA mA
Output Voltage Noise	C_{OUT} = 10µF, I_{LOAD} = 1A, BW = 10Hz to 100kHz, V_{OUT} = 1.2V			165		μV_{RMS}
ADJ Pin Bias Current (Notes 7, 11)	V_{ADJ} = 0.2V, V_{IN} = 1.5V			30	100	nA
Shutdown Threshold	V_{OUT} = Off to On V_{OUT} = On to Off	● ●	 0.25	0.64 0.64	0.9 	V V
$\overline{SHDN}$ Pin Current (Note 12)	$V_{\overline{SHDN}}$ = 0V, V_{IN} = 10V $V_{\overline{SHDN}}$ = 10V, V_{IN} = 10V	● ●		 3	±1 9.5	µA µA
Quiescent Current in Shutdown	V_{IN} = 6V, $V_{\overline{SHDN}}$ = 0V			7.5	15	µA
Ripple Rejection (Note 13)	V_{IN} – V_{OUT} = 1V, V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 1A		55	70		dB
Current Limit (Note 9)	V_{IN} = 10V, V_{OUT} = 0V V_{IN} = $V_{OUT(NOMINAL)}$ + 0.5V, ΔV_{OUT} ≤ –5%	 ●	 1.1	2.6 1.7	 	A A
Input Reverse Leakage Current (Note 14)	V_{IN} = –10V, V_{OUT} = 0V			4	20	µA
Reverse Output Current (Notes 15, 16)	V_{OUT} = 1.2V, V_{IN} = 0V			0.1	5	µA
Minimum Required Output Current	V_{IN} = 1.6V, V_{OUT} = 1.2V	●	1			mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3022 regulator is tested and specified under pulse load conditions such that $T_J \approx T_A$. The LT3022 is 100% tested at T_A = 25°C. Performance of the LT3022E over the full –40°C and 125°C operating junction temperature range is assured by design, characterization and correlation with statistical process controls. The LT3022I regulators are guaranteed over the full –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetime. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Minimum input voltage is the voltage required by the LT3022 to regulate the output voltage and supply the rated 1A output current. This specification is tested at V_{OUT} = 0.2V. For higher output voltages, the minimum input voltage required for regulation equals the regulated output voltage V_{OUT} plus the dropout voltage or 1.1V, whichever is greater.

Note 5: Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. Limit the output current range if operating at maximum input voltage. Limit the input-to-output voltage differential range if operating at maximum output current.

ELECTRICAL CHARACTERISTICS

Note 6: The LT3022 typically supplies 1A output current with a 0.9V input supply. The guaranteed minimum input voltage for 1A output current is 1.10V, especially if cold temperature operation is required.

Note 7: The LT3022 is tested and specified for these conditions with ADJ tied to OUT.

Note 8: Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout the output voltage equals: ($V_{IN} – V_{DROPOUT}$).

Note 9: The LT3022 is tested and specified for these conditions with an external resistor divider (3.92k and 19.6k) setting V_{OUT} to 1.2V. The external resistor divider adds 50µA of load current.

Note 10: GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)} + 0.4V$ and a current source load. GND pin current increases in dropout. See GND pin current curves in the Typical Performance Characteristics section.

Note 11: Adjust pin bias current flows out of the ADJ pin.

Note 12: Shutdown pin current flows into the $\overline{SHDN}$ pin.

Note 13: The LT3022 is tested and specified for this condition with an external resistor divider (3.92k and 5.9k) setting V_{OUT} to 0.5V. The external resistor divider adds 50µA of load current. The specification refers to the change in the 0.2V reference voltage, not the 0.5V output voltage.

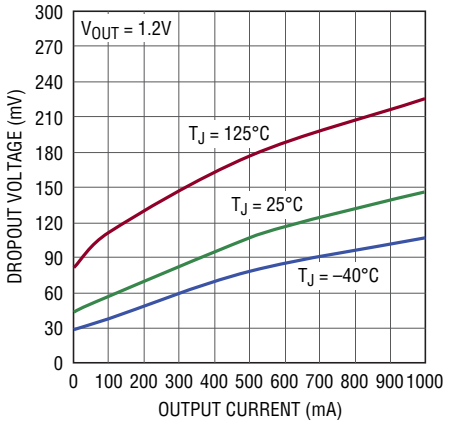
Note 14: Input reverse leakage current flows out of the IN pin.

Note 15: Reverse output current is tested with IN grounded and OUT forced to the rated output voltage. This current flows into the OUT pin and out of the GND pin.

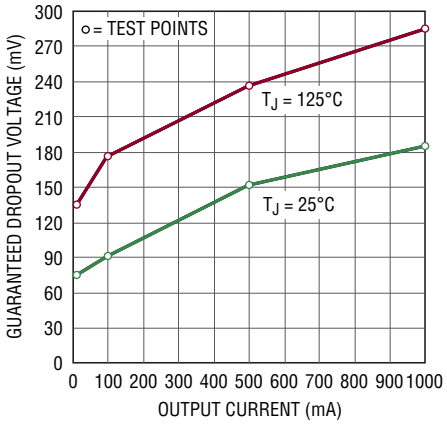
Note 16: Reverse current is higher for the case of (rated_output) < V_{OUT} < V_{IN}, because the no-load recovery circuitry is active in this region and is trying to restore the output voltage to its nominal value.

TYPICAL PERFORMANCE CHARACTERISTICS

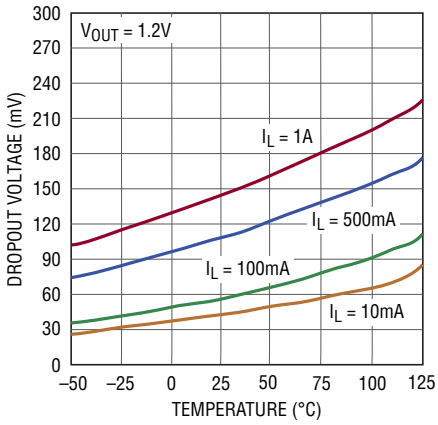
Dropout Voltage



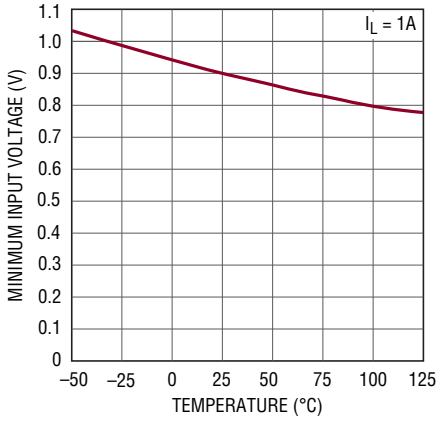
Guaranteed Dropout Voltage



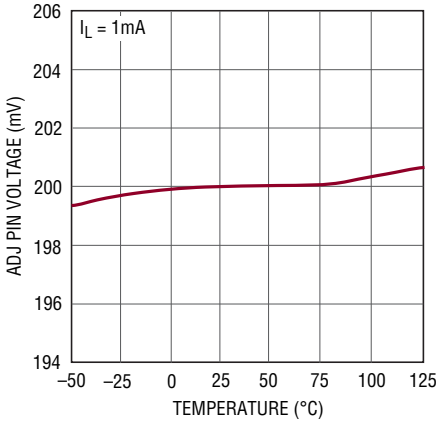
Dropout Voltage



Minimum Input Voltage

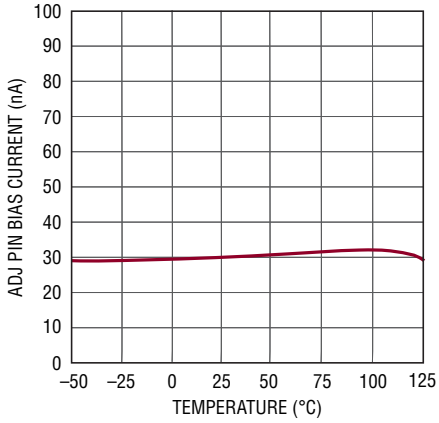


ADJ Pin Voltage

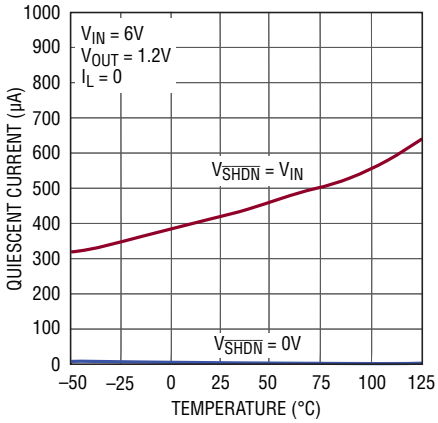


TYPICAL PERFORMANCE CHARACTERISTICS

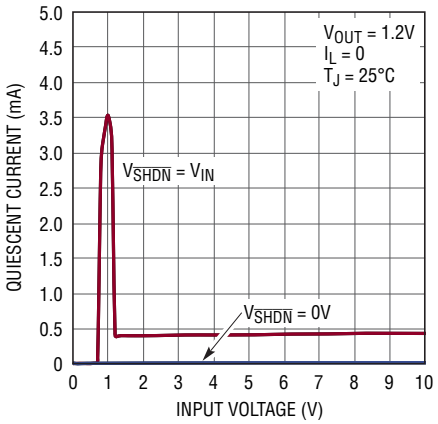
ADJ Pin Bias Current



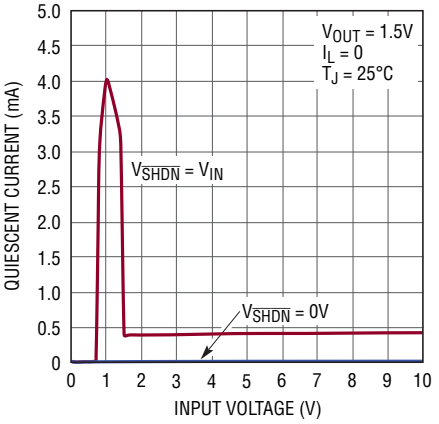
Quiescent Current



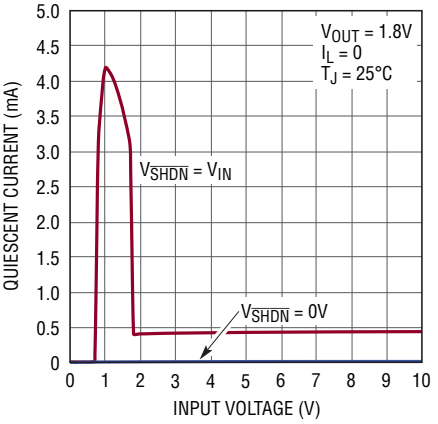
Quiescent Current



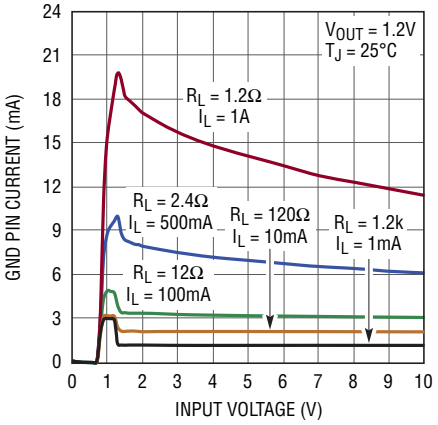
Quiescent Current



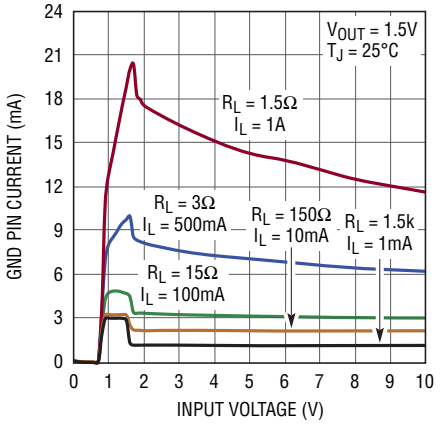
Quiescent Current



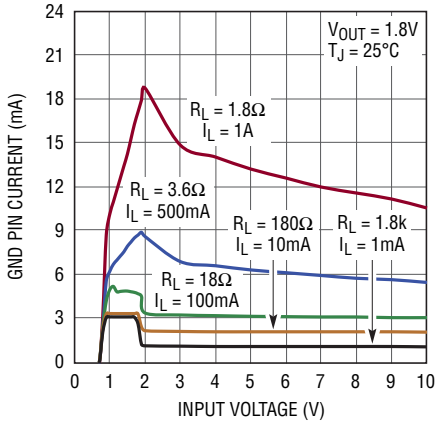
GND Pin Current



GND Pin Current

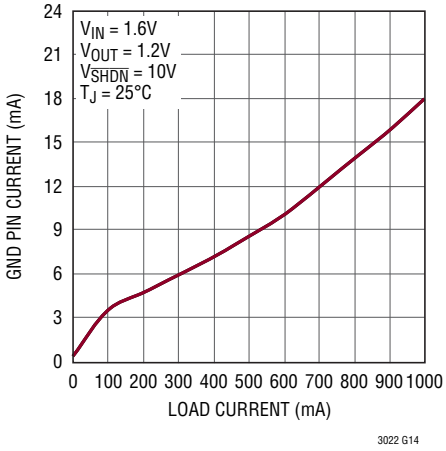


GND Pin Current



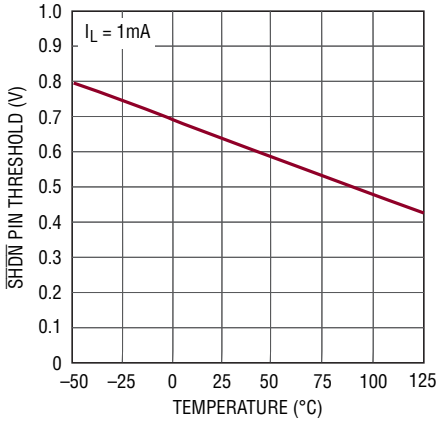
TYPICAL PERFORMANCE CHARACTERISTICS

GND Pin Current vs I_{LOAD}



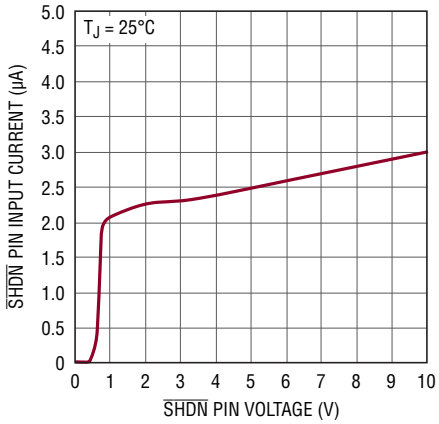
3022 G14

$\overline{SHDN}$ Pin Threshold



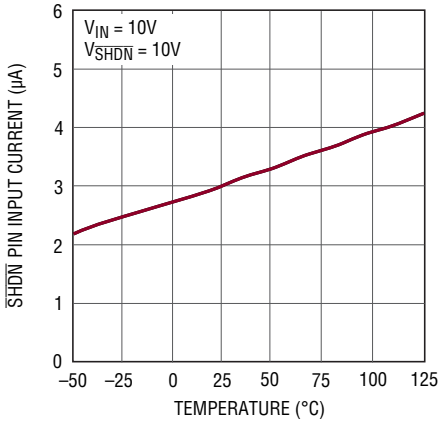
3022 G15

$\overline{SHDN}$ Pin Input Current



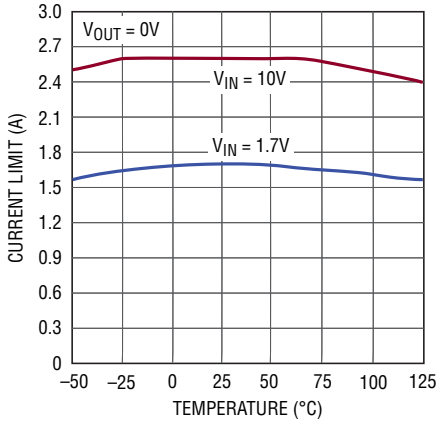
3022 G16

$\overline{SHDN}$ Pin Input Current



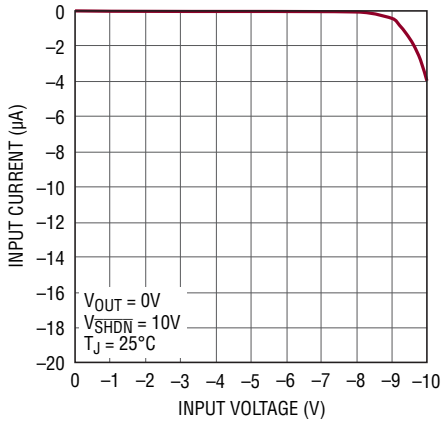
3022 G17

Current Limit



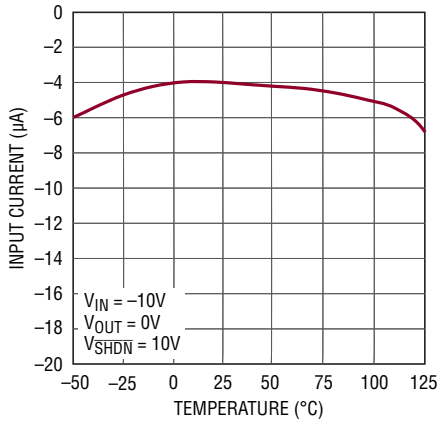
3022 G18

Reverse Input Leakage Current



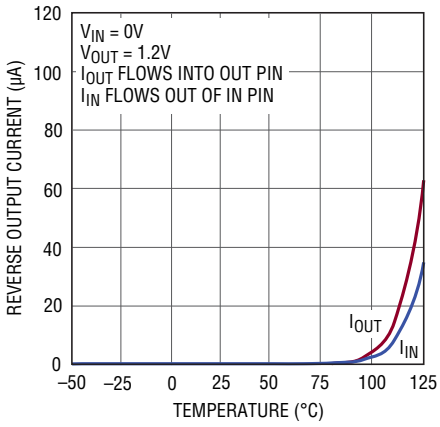
3022 G19

Reverse Input Leakage Current



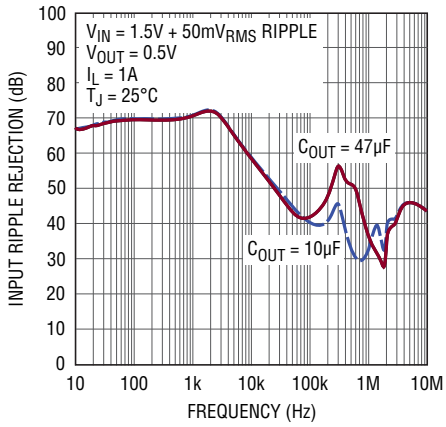
3022 G20

Reverse Output Current



3022 G21

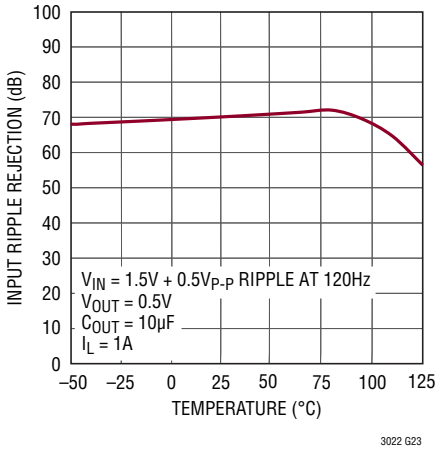
Input Ripple Rejection



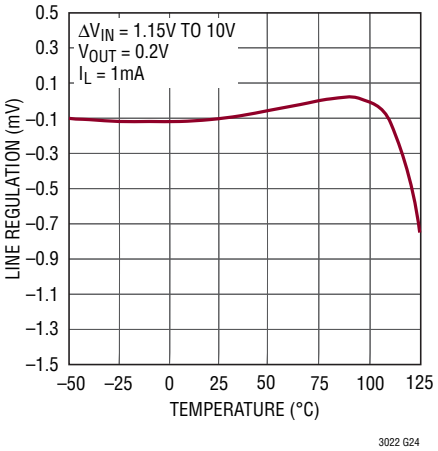
3022 G22

TYPICAL PERFORMANCE CHARACTERISTICS

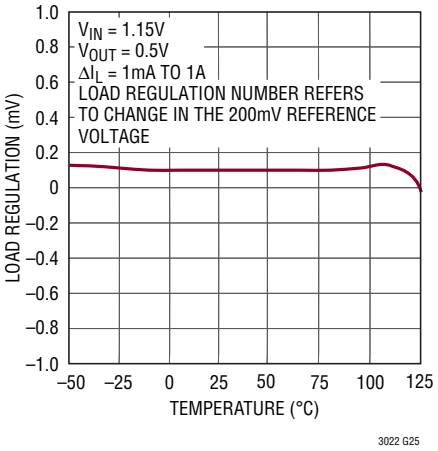
Input Ripple Rejection



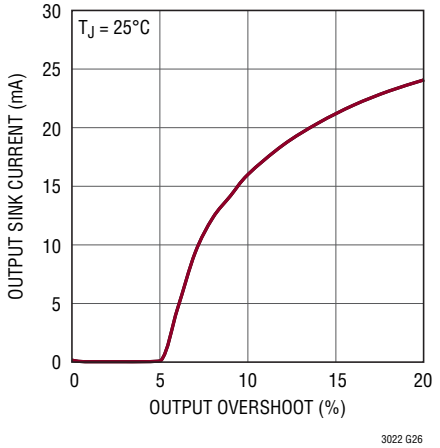
Line Regulation



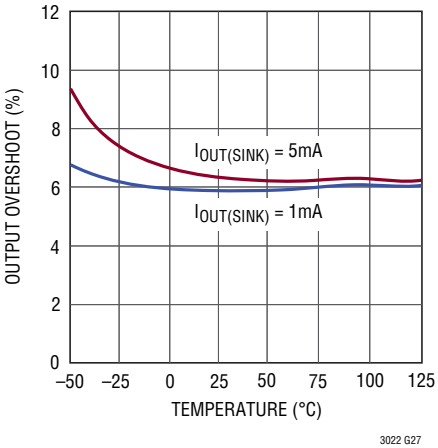
Load Regulation



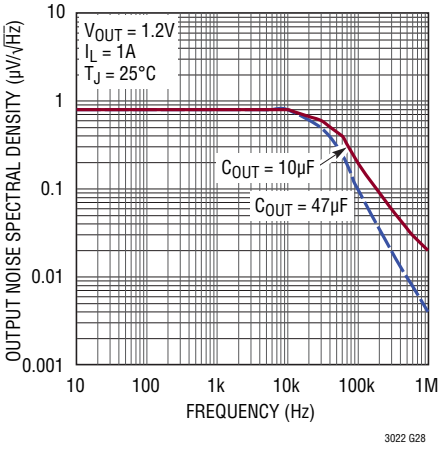
No-Load Recovery Threshold



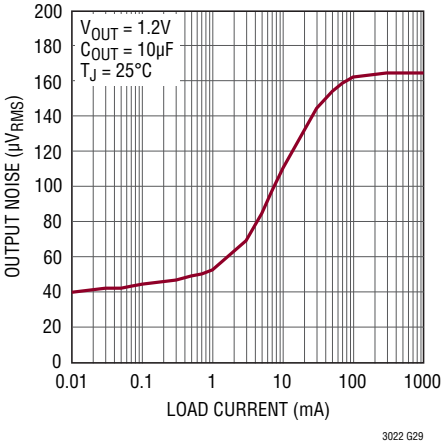
No-Load Recovery Threshold



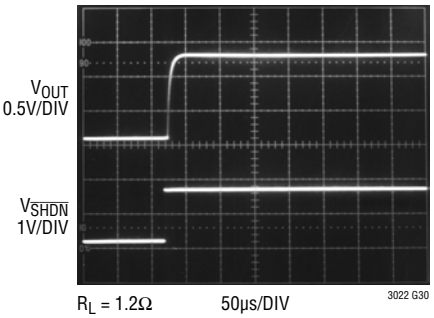
Output Noise Spectral Density



RMS Output Noise vs Load Current (10Hz to 100kHz)

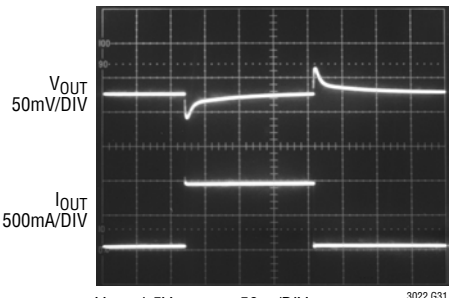


Start-Up from Shutdown



RL = 1.2Ω
VIN = 1.5V
VOUT = 1.2V
COUT = 10µF
50µs/DIV

Transient Response



VIN = 1.5V
VOUT = 1.2V
IOUT = 100mA to 1A
COUT = 22µF
tRISE = tFALL = 100ns
50µs/DIV

PIN FUNCTIONS

NC (Pins 1, 2, 8, 15, 16): No Connect Pins. These pins have no connection to internal circuitry. These pins may be floated, tied to V_{IN} or tied to GND for improved thermal performance.

OUT (Pins 3, 4): These pins supply power to the load. Use a minimum output capacitor of 10µF to prevent oscillations. Large load transient applications require larger output capacitors to limit peak voltage transients. See the Applications Information section for more information on output capacitance and reverse-output characteristics. The LT3022 requires a 1mA minimum load current to ensure proper regulation and stability.

ADJ (Pin 5): This pin is the error amplifier inverting terminal. Its 30nA typical input bias current flows out of the pin (see curve of ADJ Pin Bias Current vs Temperature in the Typical Performance Characteristics). The ADJ pin reference voltage is 200mV (referred to AGND).

AGND (Pins 6, 7): Analog Ground. Tie these pins directly to PGND (Pins 10, 11) and the exposed backside GND (Pin 17). Connect the bottom of the external resistor divider, setting output voltage, directly to AGND for optimum regulation.

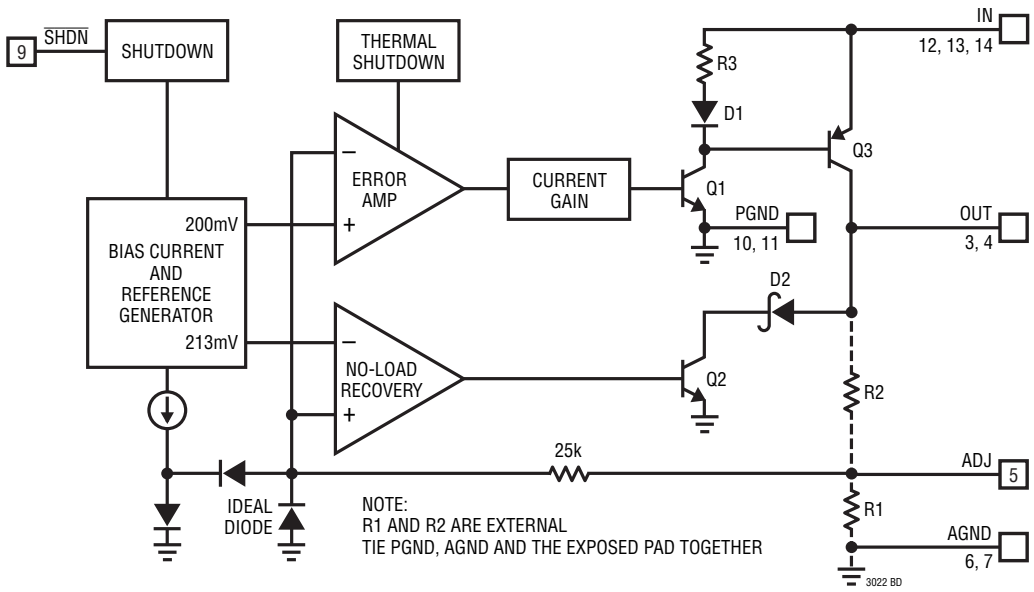
$\overline{\text{SHDN}}$ (Pin 9): Pulling the $\overline{\text{SHDN}}$ pin low puts the LT3022 into a low power state and turns the output off. Drive the $\overline{\text{SHDN}}$ pin with either logic or an open-collector/drain device with a pull-up resistor. The resistor supplies the pull-up current to the open collector/drain logic, normally several microamperes, and the $\overline{\text{SHDN}}$ pin current, typically 3µA. If unused, connect the $\overline{\text{SHDN}}$ pin to V_{IN}. The LT3022 does not function if the $\overline{\text{SHDN}}$ pin is not connected.

PGND (Pins 10, 11): Power Ground. The majority of ground pin current flows out of PGND. Tie these pins directly to AGND (Pins 6, 7) and the exposed backside GND (Pin 17).

IN (Pins 12, 13,14): These pins supply power to the device. The LT3022 requires a bypass capacitor at IN if located more than six inches from the main input filter capacitor. Include a bypass capacitor in battery-powered circuits as a battery's output impedance rises with frequency. A minimum bypass capacitor of 10µF suffices. The LT3022 withstands reverse voltages on the IN pin with respect to ground and the OUT pin. In the case of a reversed input, which occurs if a battery is plugged in backwards, the LT3022 behaves as if a diode is in series with its input. No reverse current flows into the LT3022 and no reverse voltage appears at the load. The device protects itself and the load.

GND (Pin 17): Exposed Pad. Tie this pin directly to AGND (Pins 6, 7), PGND (Pins 10, 11) and the PCB ground. This pin provides enhanced thermal performance with its connection to the PCB ground. See the Applications Information section for thermal considerations and calculating junction temperature.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

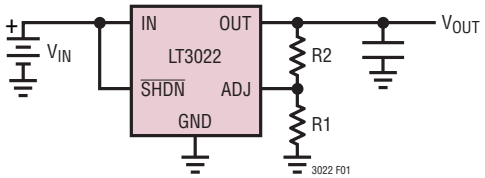
The LT3022 very low dropout linear regulator is capable of 0.9V input supply operation. It supplies 1A output current and dropout voltage is typically 145mV. Quiescent current is typically 400µA and drops to 7.5µA in shutdown. The LT3022 incorporates several protection features, making it ideal for use in battery-powered systems. The device protects itself against reverse-input and reverse-output voltages. If the output is held up by a backup battery when the input is pulled to ground in a battery backup application, the LT3022 behaves as if a diode is in series with its output, preventing reverse current flow. In dual supply applications where the regulator load is returned to a negative supply, pulling the output below ground by as much as 10V does not affect start-up or normal operation.

Adjustable Operation

The LT3022's output voltage range is 0.2V to 9.5V. Figure 1 shows that the external resistor ratio sets output voltage. The device regulates the output to maintain ADJ at 200mV referred to ground. R1's current equals 200mV/R1. R2's current is R1's current minus the ADJ pin bias current. The 30nA ADJ pin bias current flows out of the pin. Use Figure 1's formula to calculate output voltage. Given the LT3022's 1mA minimum load current requirement, Linear Technology recommends choosing resistor divider values to satisfy this requirement. A 200Ω R1 value sets a 1mA resistor divider current. In shutdown, the output is off and the divider current is zero. Curves of ADJ Pin Voltage vs Temperature and ADJ Pin Bias Current vs Temperature appear in the Typical Performance Characteristics section.

Specifications for output voltages greater than 200mV are proportional to the ratio of desired output voltage to 200mV (V_{OUT}/200mV). For example, load regulation for an output current change of 1mA to 1A is typically 0.1mV at V_{ADJ} = 200mV. At V_{OUT} = 1.5V, load regulation is:

$$\frac{1.5V}{200mV} \bullet 0.1mV = 750\,\mu V$$



V_{OUT}: 200mV • (1 + R2/R1) – (I_{ADJ} • R2)
V_{ADJ}: 200mV
I_{ADJ}: 30nA AT 25°C
OUTPUT RANGE: 0.2V TO 9.5V

Figure 1. Adjustable Operation

APPLICATIONS INFORMATION

Table 1 shows 1% resistor divider values for some common output voltages with a resistor divider current equaling or about 1mA.

Table 1

V_{OUT} (V)	R1 (Ω)	R2 (Ω)
0.9	200	698
1.0	187	750
1.2	200	1000
1.5	200	1300
1.8	187	1500
2.5	187	2150
3.3	200	3090

Output Capacitance and Transient Response

The LT3022's design is stable with a wide range of output capacitors, but is optimized for low ESR ceramic capacitors. The output capacitor's ESR affects stability, most notably with small value capacitors. Use a minimum output capacitor of 10µF with an ESR of less than 0.1Ω to prevent oscillations. The LT3022 is a low voltage device and output load transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for large load current changes.

Ceramic capacitors require extra consideration. Manufacturers make ceramic capacitors with a variety of dielectrics; each with a different behavior across temperature and applied voltage. The most common dielectrics are Z5U, Y5V, X5R and X7R. Z5U and Y5V dielectrics provide high C-V products in a small package at low cost, but exhibit strong voltage and temperature coefficients. X5R and X7R dielectrics yield highly stable characteristics and are more suitable for use as the output capacitor at fractionally increased cost. X5R and X7R dielectrics both exhibit excellent voltage coefficient characteristics. X7R works over a larger temperature range and exhibits better temperature stability whereas X5R is less expensive and is available in higher values. Figures 2 and 3 show voltage coefficient and temperature coefficient comparisons between Y5V and X5R material.

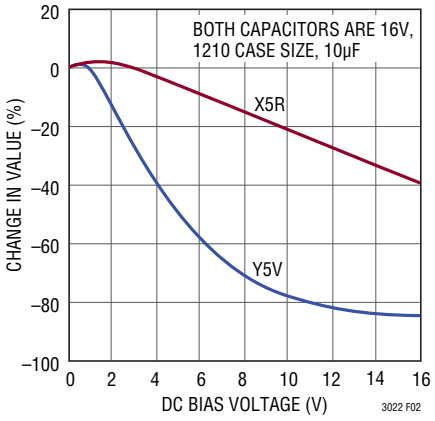


Figure 2. Ceramic Capacitor DC Bias Characteristics

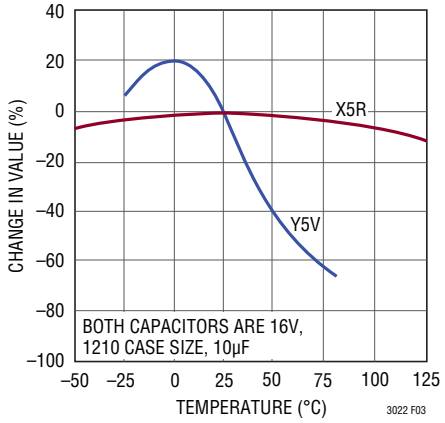


Figure 3. Ceramic Capacitor Temperature Characteristics

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients. The resulting voltages produced can cause appreciable amounts of noise. A ceramic capacitor produced Figure 4's trace in response to light tapping from a pencil. Similar vibration induced behavior can masquerade as increased output voltage noise.

APPLICATIONS INFORMATION

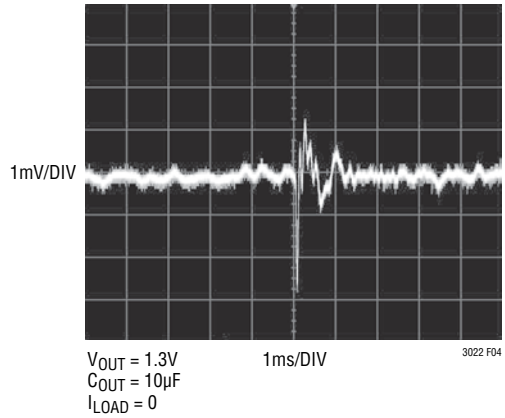


Figure 4. Noise Resulting from Tapping on a Ceramic Capacitor

No-Load/Light-Load Recovery

A possible transient load step that occurs is where the output current changes from its maximum level to zero current or a very small load current. The output voltage responds by overshooting until the regulator lowers the amount of current it delivers to the new level. The regulator loop response time and the amount of output capacitance control the amount of overshoot. Once the regulator has decreased its output current, the current provided by the resistor divider (which sets V_{OUT}) is the only current remaining to discharge the output capacitor from the level to which it overshot. The amount of time it takes for the output voltage to recover easily extends to milliseconds with minimum divider current and many microfarads of output capacitance.

To eliminate this problem, the LT3022 incorporates a no-load or light load recovery circuit. This circuit is a voltage-controlled current sink that significantly improves the light load transient response time by discharging the output capacitor quickly and then turning off. The current sink turns on when the output voltage exceeds 6.5% of the nominal output voltage. The current sink level is then proportional to the overdrive above the threshold up to a maximum of about 24mA. Consult the curve in the Typical Performance Characteristics for the No-Load Recovery Threshold.

If external circuitry forces the output above the no-load recovery circuit's threshold, the current sink turns on in an attempt to restore the output voltage to nominal. The current sink remains on until the external circuitry releases the output. However, if the external circuitry pulls the output voltage above the input voltage or the input falls below the output, the LT3022 turns the current sink off and shuts down the bias current/reference generator circuitry.

Thermal Considerations

The LT3022's maximum rated junction temperature of 125°C limits its power handling capability. Two components comprise the power dissipation of the device:

1. Output current multiplied by the input-to-output voltage differential:

   $(I_{LOAD}) \bullet (V_{IN} – V_{OUT})$ and

2. GND pin current multiplied by the input voltage:

   $(I_{GND}) \bullet (V_{IN})$

GND pin current is found by examining the GND pin current curves in the Typical Performance Characteristics. Power dissipation equals the sum of the two components listed. The LT3022's internal thermal limiting (with hysteresis) protects the device during overload conditions. For normal continuous conditions, do not exceed the maximum junction temperature rating of 125°C. Carefully consider all sources of thermal resistance from junction to ambient including other heat sources mounted in proximity to the LT3022.

The underside of the LT3022 DHC and MSE packages has exposed metal from the lead frame to the die attachment. Heat transfers directly from the die junction to the printed circuit board metal, allowing maximum junction temperature control. The dual-in-line pin arrangement allows metal to extend beyond the ends of the package on the topside (component side) of a PCB. Connect this metal to GND on the PCB. The multiple IN and OUT pins of the LT3022 also assist in spreading heat to the PCB. Copper board stiffeners and plated throughholes can also be used to spread the heat generated by power devices.

APPLICATIONS INFORMATION

The following tables list thermal resistance as a function of copper area in a fixed board size. All measurements are taken in still air on a 4-layer FR-4 board with 1oz solid internal planes, and 2oz external trace planes with a total board thickness of 1.6mm. For more information on thermal resistance and high thermal conductivity test boards, refer to JEDEC standard JESD51, notably JESD51-12 and JESD51-7. Achieving low thermal resistance necessitates attention to detail and careful PCB layout.

Table 2. Measured Thermal Resistance for DHC Package

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	35°C/W
1000mm^2	2500mm^2	2500mm^2	37°C/W
225mm^2	2500mm^2	2500mm^2	38°C/W
100mm^2	2500mm^2	2500mm^2	40°C/W

*Device is mounted on topside

Table 3. Measured Thermal Resistance for MSE Package

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	35°C/W
1000mm^2	2500mm^2	2500mm^2	37°C/W
225mm^2	2500mm^2	2500mm^2	38°C/W
100mm^2	2500mm^2	2500mm^2	40°C/W

*Device is mounted on topside.

Calculating Junction Temperature

Example: Given an output voltage of 1.5V, an input voltage range of 1.7V to 1.9V, an output load current range of 1mA to 1A and a maximum ambient temperature of 85°C, what is the maximum junction temperature for an application using the DHC package?

The power dissipated by the device equals:

$$I_{LOAD(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) + I_{GND} \bullet (V_{IN(MAX)})$$

where:

$I_{LOAD(MAX)} = 1A$

$V_{IN(MAX)} = 1.9V$

I_{GND} at (I_{LOAD} = 1A, V_{IN} = 1.9V) = 18mA

so:

$$P = 1A \bullet (1.9V - 1.5V) + 18mA \bullet (1.9V) = 0.434W$$

The thermal resistance is about 38°C/W depending on the copper area. So the junction temperature rise above ambient is approximately equal to:

$$0.434W \bullet (38°C/W) = 16.5°C$$

The maximum junction temperature equals the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$$T_{JMAX} = 85°C + 16.5°C = 101.5°C$$

Protection Features

The LT3022 incorporates several protection features that make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device also protects against reverse-input voltages, reverse-output voltages and reverse output-to-input voltages.

Current limit protection and thermal overload protection protect the device against current overload conditions at its output. For normal operation, do not exceed 125°C junction temperature. The typical thermal shutdown temperature is 165°C and the thermal shutdown circuit incorporates about 7°C of hysteresis.

The IN pins withstand reverse voltages of 10V. The LT3022 limits current flow to less than 1µA and no negative voltage appears at OUT. The device protects both itself and the load against batteries that are plugged in backwards.

The LT3022 incurs no damage if OUT is pulled below ground. If IN is left open-circuited or grounded, OUT can be pulled below ground by 10V. No current flows from the pass transistor connected to OUT. However, current flows in (but is limited by) the resistor divider that sets the output voltage. Current flows from the bottom resistor in the divider and from the ADJ pin's internal clamp through the top resistor in the divider to the external circuitry pulling OUT below ground. If IN is powered by a voltage source, OUT sources current equal to its current limit capability and the LT3022 protects itself by thermal limiting. In this case, grounding $\overline{SHDN}$ turns off the LT3022 and stops OUT from sourcing current.

APPLICATIONS INFORMATION

The LT3022 incurs no damage if the ADJ pin is pulled above or below ground by 10V. If IN is left open-circuited or grounded and ADJ is pulled above ground, ADJ acts like a 25k resistor in series with two diodes. ADJ acts like a 25k resistor if pulled below ground. If IN is powered by a voltage source and ADJ is pulled below its reference voltage, the LT3022 attempts to source its current limit capability at OUT. The output voltage increases to $V_{IN} – V_{DROPOUT}$ with $V_{DROPOUT}$ set by whatever load current the LT3022 supports. This condition can potentially damage external circuitry powered by the LT3022 if the output voltage increases to an unregulated high voltage. If IN is powered by a voltage source and ADJ is pulled above its reference voltage, two situations can occur. If ADJ is pulled slightly above its reference voltage, the LT3022 turns off the pass transistor, no output current is sourced and the output voltage decreases to either the voltage at ADJ or less. If ADJ is pulled above its no-load recovery threshold, the no-load recovery circuitry turns on and attempts to sink current. OUT is actively pulled low and the output voltage clamps at a Schottky diode above ground. Please note that the behavior described above applies to the LT3022 only. If a resistor divider is connected under the same conditions, there will be additional V/R current.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage or is left open circuit. In the case where the input is grounded, there is less than 1µA of reverse output current. If the LT3022 IN pin is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current drops to less than 10µA typically. This occurs if the LT3022 input is connected to a discharged (low voltage) battery and either a backup battery or a second regulator circuit holds up the output. The state of the $\overline{SHDN}$ pin has no effect on the reverse output current if OUT is pulled above IN.

Input Capacitance and Stability

The LT3022 design is stable with a minimum of 10µF capacitor placed at the IN pin. Very low ESR ceramic capacitors may be used. However, in cases where long wires connect the power supply to the LT3022's input and ground, use of low value input capacitors combined with an output load current of greater than 20mA may result in instability. The resonant LC tank circuit formed by the wire inductance and the input capacitor is the cause and not a result of LT3022 instability.

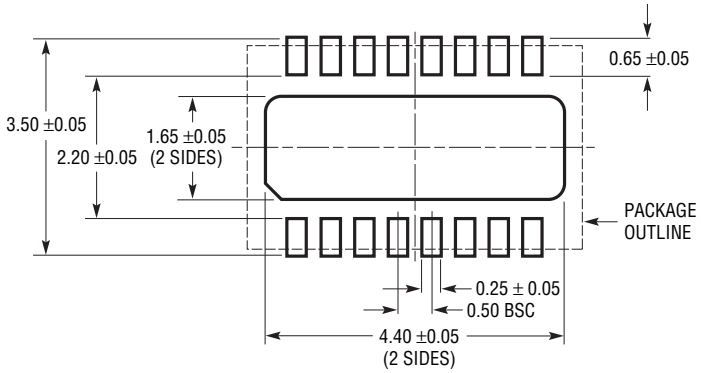
The self-inductance, or isolated inductance, of a wire is directly proportional to its length. However, the wire diameter has less influence on its self inductance. For example, the self-inductance of a 2-AWG isolated wire with a diameter of 0.26" is about half the inductance of a 30-AWG wire with a diameter of 0.01". One foot of 30-AWG wire has 465nH of self-inductance.

Several methods exist to reduce a wire's self-inductance. One method divides the current flowing towards the LT3022 between two parallel conductors. In this case, placing the wires further apart reduces the inductance; up to a 50% reduction when placed only a few inches apart. Splitting the wires connects two equal inductors in parallel. However, when placed in close proximity to each other, mutual inductance adds to the overall self inductance of the wires. The most effective technique to reducing overall inductance is to place the forward and return current conductors (the input wire and the ground wire) in close proximity. Two 30-AWG wires separated by 0.02" reduce the overall self-inductance to about one-fifth of a single wire.

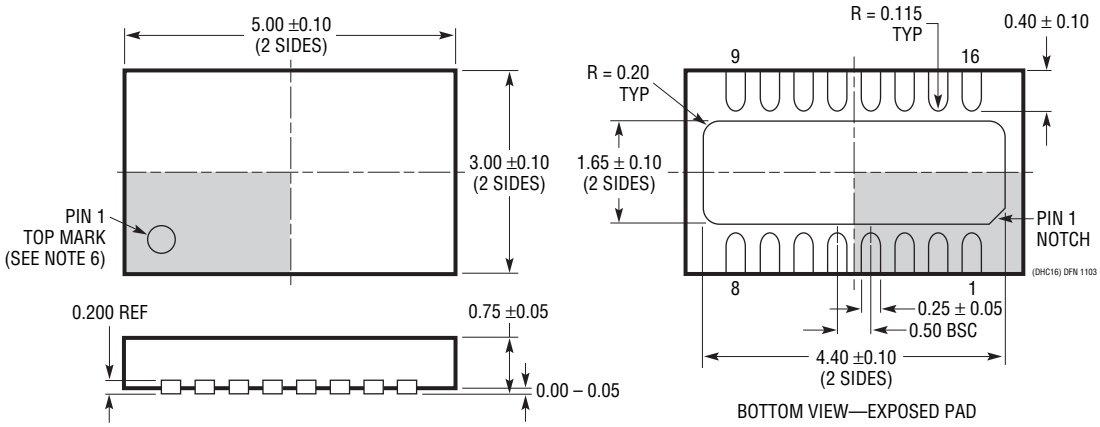
If a battery, mounted in close proximity, powers the LT3022, a 10µF input capacitor suffices for stability. However, if a distantly located supply powers the LT3022, use a larger value input capacitor. Use a rough guideline of 1µF (in addition to the 10µF minimum) per 8 inches of wire length. The minimum input capacitance needed to stabilize the application also varies with power supply output impedance variations. Placing additional capacitance on the LT3022's output also helps. However, this requires an order of magnitude more capacitance in comparison with additional LT3022 input bypassing. Series resistance between the supply and the LT3022 input also helps stabilize the application; as little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at the expense of dropout voltage. A better alternative is to use higher ESR tantalum or electrolytic capacitors at the LT3022 input in place of ceramic capacitors.

PACKAGE DESCRIPTION

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

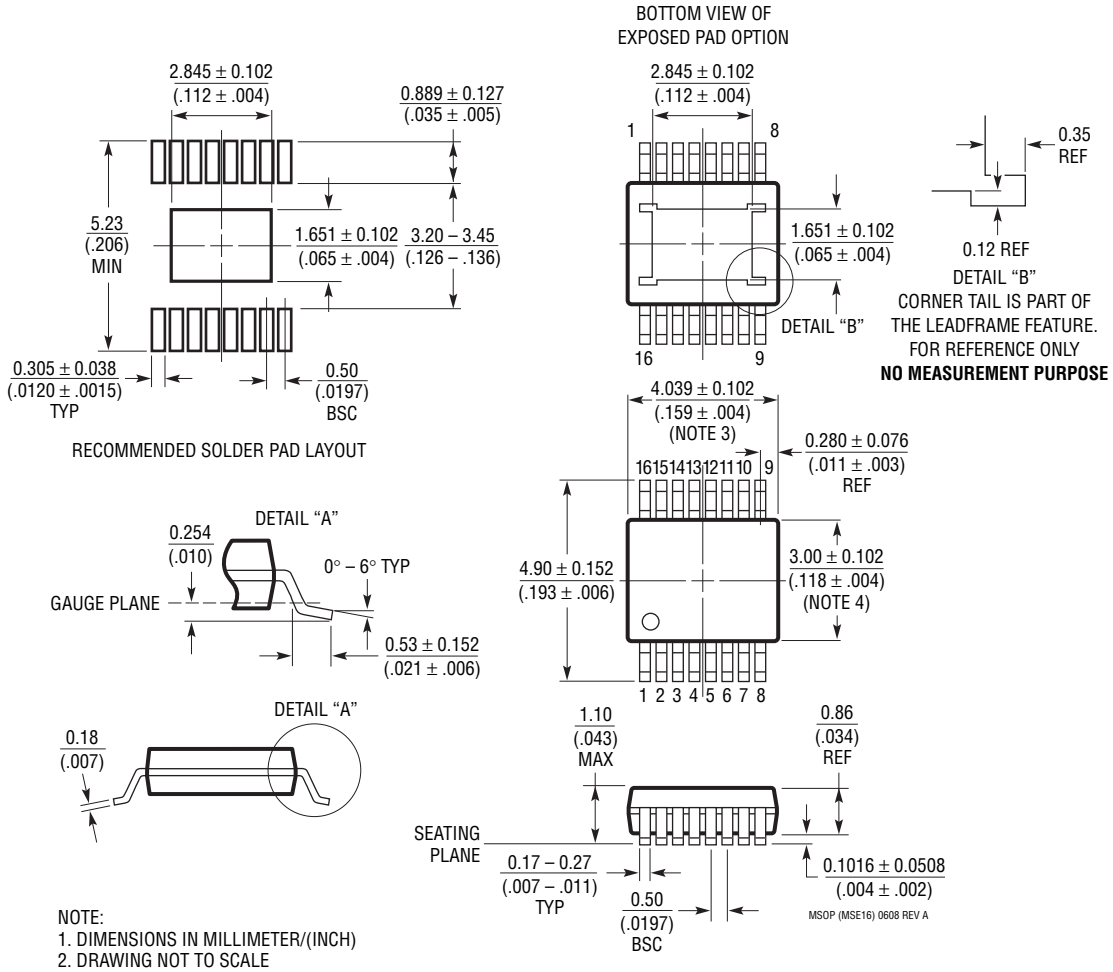


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

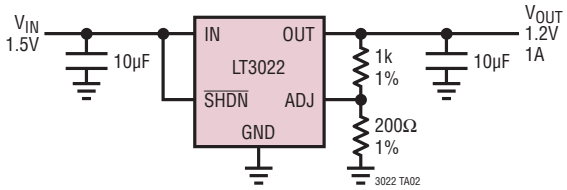
MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev A)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

1.5V to 1.2V, 1A VLDO Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3020	100mA, Low Voltage VLDO Linear Regulator	V_{IN}: 0.9V to 10V, V_{OUT}: 0.2V to 9.5V, V_{DO} = 0.15V, I_Q = 120µA, Noise: <250µV_{RMS}, Stable with 2.2µF Ceramic Capacitors, DFN-8, MS8 Packages
LT3021	500mA, Low Voltage, VLDO Linear Regulator	V_{IN}: 0.9V to 10V, Dropout Voltage: 160mV Typical, Adjustable Output (V_{REF} = $V_{OUT(MIN)}$ = 200mV), Fixed Output Voltages: 1.2V, 1.5V, 1.8V, Stable with Low ESR, Ceramic Output Capacitors, 16-Pin DFN (5mm × 5mm) and 8-Lead SO Packages
LTC®3025	300mA Micropower VLDO Linear Regulator	V_{IN} = 0.9V to 5.5V, Dropout Voltage: 45mV, Low Noise 80µV_{RMS}, Low I_Q: 54µA, 2mm × 2mm 6-Lead DFN Package
LTC3025-1/LTC3025-2/ LTC3025-3/LTC3025-4	500mA Micropower VLDO Linear Regulator in 2mm × 2mm DFN	V_{IN} = 0.9V to 5.5V, Dropout Voltage: 75mV, Low Noise 80µV_{RMS}, Low I_Q: 54µA, Fixed Output: 1.2V (LTC3025-2), 1.5V (LTC3025-3), 1.8V (LTC3025-4); Adjustable Output Range: 0.4V to 3.6V (LTC3025-1), 2mm × 2mm 6-Lead DFN Package
LTC3026	1.5A, Low Input Voltage VLDO Linear Regulator	V_{IN}: 1.14V to 3.5V (Boost Enabled), 1.14V to 5.5V (with External 5V), V_{DO} = 0.1V, I_Q = 950µA, Stable with 10µF Ceramic Capacitors, 10-Lead MSOP and DFN-10 Packages
LT3029	Dual 500mA/500mA, Low Dropout, Low Noise, Micropower Linear Regulator	Output Current: 500mA per Channel, Low Dropout Voltage: 300mV Low Noise: 20µV_{RMS} (10Hz to 100kHz), Low Quiescent Current: 55µA per Channel, Wide Input Voltage Range: 1.8V to 20V (Common or Independent Input Supply), Adjustable Output: 1.215V Reference, Very Low Quiescent Current in Shutdown: <1µA per Channel Stable with 3.3µF Minimum Output Capacitor, Stable with Ceramic, Tantalum or Aluminum Electrolytic Capacitors, Reverse-Battery, Reverse-Output and Reverse Output-to-Input Protection, Thermally Enhanced 16-Lead MSOP and 16-Lead (4mm × 3mm) DFN Packages
LTC3035	300mA VLDO Linear Regulator with Charge Pump Bias Generator	V_{IN} = 1.7V to 5.5V, V_{OUT}: 0.4V to 3.6V, Dropout Voltage: 45mV, I_Q: 100µA, 3mm × 2mm DFN-8
LT3080/LT3080-1	1.1A, Parallelable, Low Noise, Low Dropout Linear Regulator	300mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set; Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors, TO-220, SOT-223, MSOP-8 and 3mm × 3mm DFN-8 Packages; LT3080-1 Has Integrated Internal Ballast Resistor
LT3085	500mA, Parallelable, Low Noise, Low Dropout Linear Regulator	275mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set; Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors, MSOP-8 and 2mm × 3mm DFN-6 packages

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