1.5A, Low Noise, Negative Linear Regulator with Precision Current Limit

FEATURES

- **Output Current: 1.5A**
- **Dropout Voltage: 310mV**
- **Precision Current Limit with Foldback**
- **Low Output Noise: 60μV_{RMS} (10Hz to 100kHz)**
- **Low Quiescent Current: 1.1mA**
- **Precision Positive or Negative Shutdown Logic**
- **Fast Transient Response**
- Wide Input Voltage Range: –1.8V to –30V
- Adjustable Output Voltage Range: –1.22V to –29.5V
- Controlled Quiescent Current in Dropout
- < 1μA Quiescent Current in Shutdown
- Stable with 10μF Output Capacitor
- Stable with Ceramic, Tantalum or Aluminum Capacitors
- Thermal Limit with Hysteresis
- Reverse Output Protection
- 5-Lead TO-220 and DD-Pak, Thermally Enhanced 12-Lead MSOP and 8-Lead 3mm × 3mm × 0.75mm DFN Packages

APPLICATIONS

- Post-Regulator for Switching Supplies
- Negative Logic Supplies
- Low Noise Instrumentation
- Industrial Supplies
- Negative Complement to the LT1963A

DESCRIPTION

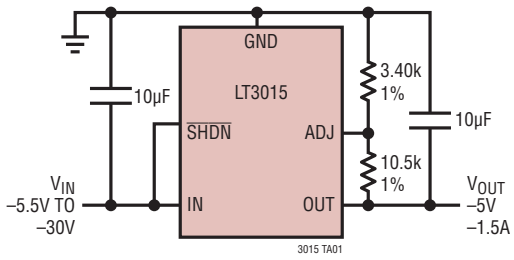
The LT®3015 is a low noise, low dropout, negative linear regulator with fast transient response. The device supplies up to 1.5A of output current at a typical dropout voltage of 310mV. Operating quiescent current is typically 1.1mA and drops to < 1μA in shutdown. Quiescent current is also well controlled in dropout. In addition to fast transient response, the LT3015 exhibits very low output noise, making it ideal for noise sensitive applications.

The LT3015 regulator is stable with a minimum 10μF output capacitor. Moreover, the regulator can use small ceramic capacitors without the necessary addition of ESR as is common with other regulators. Internal protection circuitry includes reverse output protection, precision current limit with foldback and thermal limit with hysteresis.

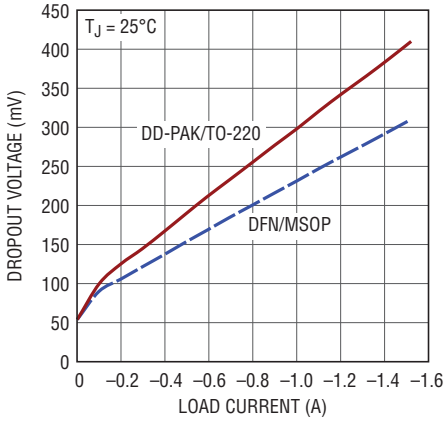
The LT3015 is available as an adjustable device with a –1.22V reference voltage. Packages include the 5-lead TO-220 and DD-Pak, a thermally enhanced 12-lead MSOP and the low profile (0.75 mm) 8-lead 3mm × 3mm DFN.

TYPICAL APPLICATION

–5V, –1.5A, Low-Noise Regulator



Dropout Voltage



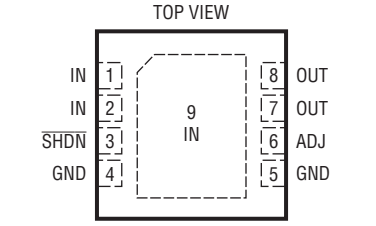
ABSOLUTE MAXIMUM RATINGS

(Note 1)

IN Pin Voltage ..... ±33V
OUT Pin Voltage (Note 10) ..... ±33V
OUT to IN Differential Voltage (Note 10) ..... –0.3V, 33V
ADJ Pin Voltage
(with Respect to IN Pin) (Note 10) ..... –0.3V, 33V
$\overline{SHDN}$ Pin Voltage
(with Respect to IN Pin) (Note 10) ..... –0.3V, 55V
$\overline{SHDN}$ Pin Voltage
(with Respect to GND Pin) ..... –33V, 22V

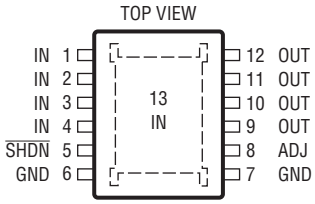
Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range (Note 9)
E-, I-Grade ..... –40°C to 125°C
MP-Grade ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10Sec)
MS12E Package ..... 300°C
Q, T Packages ..... 250°C

PIN CONFIGURATION



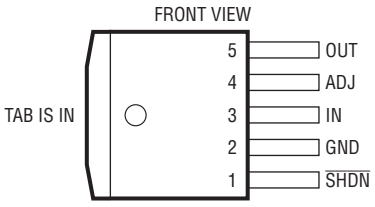
DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 40°C/W, θ_{JC} = 7.5°C/W
EXPOSED PAD (PIN 9) IS IN, MUST BE SOLDERED TO PCB



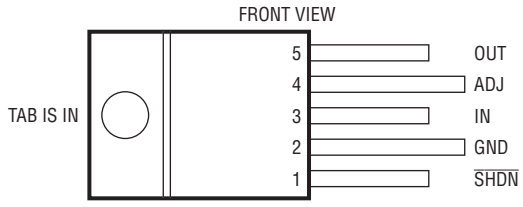
MSE PACKAGE
12-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 37°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 13) IS IN, MUST BE SOLDERED TO PCB



Q PACKAGE
5-LEAD PLASTIC DD-PAK

T_{JMAX} = 125°C, θ_{JA} = 14°C/W, θ_{JC} = 3°C/W



T PACKAGE
5-LEAD PLASTIC TO-220

T_{JMAX} = 125°C, θ_{JA} = 50°C/W, θ_{JC} = 3°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3015EDD#PBF	LT3015EDD#TRPBF	LFXS	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3015IDD#PBF	LT3015IDD#TRPBF	LFXS	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3015EMSE#PBF	LT3015EMSE#TRPBF	3015	12-Lead Plastic MSOP	–40°C to 125°C
LT3015IMSE#PBF	LT3015IMSE#TRPBF	3015	12-Lead Plastic MSOP	–40°C to 125°C
LT3015MPMSE#PBF	LT3015MPMSE#TRPBF	3015	12-Lead Plastic MSOP	–55°C to 125°C
LT3015EQ#PBF	LT3015EQ#TRPBF	LT3015Q	5-Lead Plastic DD-Pak	–40°C to 125°C
LT3015IQ#PBF	LT3015IQ#TRPBF	LT3015Q	5-Lead Plastic DD-Pak	–40°C to 125°C
LT3015MPQ#PBF	LT3015MPQ#TRPBF	LT3015Q	5-Lead Plastic DD-Pak	–55°C to 125°C
LT3015ET#PBF	LT3015ET#TRPBF	LT3015T	5-Lead Plastic TO-220	–40°C to 125°C
LT3015IT#PBF	LT3015IT#TRPBF	LT3015T	5-Lead Plastic TO-220	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT3015EDD	LT3015EDD#TR	LFXS	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3015IDD	LT3015IDD#TR	LFXS	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3015EMSE	LT3015EMSE#TR	3015	12-Lead Plastic MSOP	–40°C to 125°C
LT3015IMSE	LT3015IMSE#TR	3015	12-Lead Plastic MSOP	–40°C to 125°C
LT3015MPMSE	LT3015MPMSE#TR	3015	12-Lead Plastic MSOP	–55°C to 125°C
LT3015EQ	LT3015EQ#TR	LT3015Q	5-Lead Plastic DD-Pak	–40°C to 125°C
LT3015IQ	LT3015IQ#TR	LT3015Q	5-Lead Plastic DD-Pak	–40°C to 125°C
LT3015MPQ	LT3015MPQ#TR	LT3015Q	5-Lead Plastic DD-Pak	–55°C to 125°C
LT3015ET	LT3015ET#TR	LT3015T	5-Lead Plastic TO-220	–40°C to 125°C
LT3015IT	LT3015IT#TR	LT3015T	5-Lead Plastic TO-220	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum IN Pin Voltage (Note 11)	I_{LOAD} = –0.5A I_{LOAD} = –1.5A	 ●		–1.75 –1.8	 –2.3	V
ADJ Pin Voltage (Notes 2, 3)	V_{IN} = –2.3V, I_{LOAD}= –1mA –30V < V_{IN} < –2.3V, –1.5A < I_{LOAD} < –1mA	 ●	–1.208 –1.196	–1.22 –1.22	–1.232 –1.244	V V
Line Regulation (Note 2)	ΔV_{IN} = –2.3V to –30V, I_{LOAD} = –1mA	●		2.5	6	mV
Load Regulation (Note 2)	V_{IN} = –2.3V, ΔI_{LOAD} = –1mA to –1.5A V_{IN} = –2.3V, ΔI_{LOAD} = –1mA to –1.5A	 ●		2	3.8 9	mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Dropout Voltage $V_{IN} = V_{OUT(NOMINAL)}$ (Notes 4, 5)	I_{LOAD} = –1mA			0.055	0.095	V
	I_{LOAD} = –1mA	●			0.16	V
	I_{LOAD} = –100mA			0.1	0.16	V
	I_{LOAD} = –100mA	●			0.24	V
	I_{LOAD} = –500mA (DFN/MSOP)			0.17	0.23	V
	I_{LOAD} = –500mA (DFN/MSOP)	●			0.32	V
	I_{LOAD} = –500mA (DD-PAK/TO-220)			0.2	0.27	V
	I_{LOAD} = –500mA (DD-PAK/TO-220)	●			0.39	V
	I_{LOAD} = –1.5A (DFN/MSOP)			0.31	0.39	V
	I_{LOAD} = –1.5A (DFN/MSOP)	●			0.5	V
	I_{LOAD} = –1.5A (DD-PAK/TO-220)			0.41	0.51	V
	I_{LOAD} = –1.5A (DD-PAK/TO-220)	●			0.68	V
GND Pin Current $V_{IN} = V_{OUT(NOMINAL)}$ (Notes 4, 6)	I_{LOAD} = 0mA	●		1.1	2.4	mA
	I_{LOAD} = –1mA	●		1.15	2.5	mA
	I_{LOAD} = –100mA	●		2.9	7.0	mA
	I_{LOAD} = –500mA	●		9.5	23	mA
	I_{LOAD} = –1.5A	●		35	70	mA
Output Voltage Noise	C_{OUT} = 10µF, I_{LOAD} = –1.5A, BW = 10Hz to 100kHz			60		μV_{RMS}
ADJ Pin Bias Current (Notes 2, 7)	V_{IN} = –2.3V		–200	30	200	nA
Shutdown Threshold (Note 11)	V_{OUT} = Off-to-On (Positive)	●	1.07	1.21	1.35	V
	V_{OUT} = Off-to-On (Negative)	●	–1.34	–1.20	–1.06	V
	V_{OUT} = On-to-Off (Positive)	●	0.5	0.73		V
	V_{OUT} = On-to-Off (Negative)	●		–0.73	–0.5	V
$\overline{SHDN}$ Pin Current (Note 8)	$V_{\overline{SHDN}}$ = 0V	●	–1.0	0	10	µA
	$V_{\overline{SHDN}}$ = 15V	●		17	27	µA
	$V_{\overline{SHDN}}$ = –15V	●		–2.8	–4.5	µA
Quiescent Current in Shutdown	V_{IN} = –6V, $\overline{SHDN}$ = 0V	●		0.01	6	µA
Ripple Rejection	V_{IN} - V_{OUT} = –1.5V (Avg), V_{RIPPLE} = 0.5V_{P-P} f_{RIPPLE} = 120Hz, I_{LOAD} = –1.5A		55	65		dB
Current Limit	V_{IN} = –2.3V, V_{OUT} = 0V	●	1.8	2.0	2.2	A
	V_{IN} = –2.3V, ΔV_{OUT} = 0.1V	●	1.75	1.95	2.15	A
Input Reverse Leakage Current	V_{IN} = 30V, V_{OUT}, V_{ADJ}, $V_{\overline{SHDN}}$ = Open Circuit	●		1.55	1.7	mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. The LT3015 is tested and specified for these conditions with the ADJ pin connected to the OUT pin.

Note 3. Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. If operating at maximum output current, limit the input voltage range. If operating at maximum input voltage, limit the output current range.

Note 4. To satisfy minimum input voltage requirements, the LT3015 is tested and specified for these conditions with an external resistor divider (54.9k top, 49.9k bottom) for an output voltage of –2.56V. The external resistor adds 25µA of DC load on the output.

Note 5. Dropout voltage is the minimum input-to-output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is: $V_{IN} + V_{DROPOUT}$.

Note 6. GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)}$ and a current source load. Therefore, the device is tested while operating in dropout. This is the worst-case GND pin current. GND pin current decreases slightly at higher input voltages.

Note 7. Positive ADJ pin bias current flows into the ADJ pin.

Note 8. Positive $\overline{SHDN}$ pin current flows into the $\overline{SHDN}$ pin.

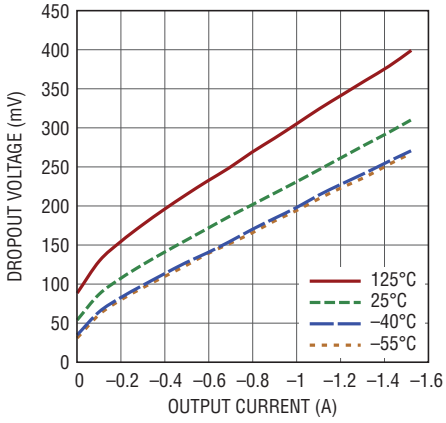
Note 9. The LT3015 is tested and specified under pulsed load conditions such that $T_J \cong T_A$. The LT3015E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LT3015I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3015MP is 100% tested and guaranteed over the full –55°C to 125°C operating junction temperature range.

Note 10. Parasitic diodes exist internally between the OUT, ADJ, $\overline{SHDN}$ pins and the IN pin. Do not drive the OUT, ADJ, and $\overline{SHDN}$ pins more that 0.3V below the IN pin during fault conditions, and these pins must remain at a voltage more positive than IN during normal operation.

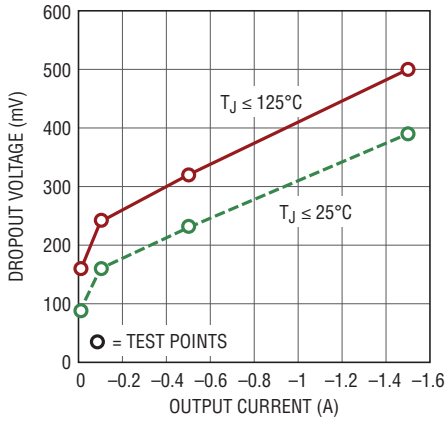
Note 11. The $\overline{SHDN}$ threshold must be met to ensure device operation.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

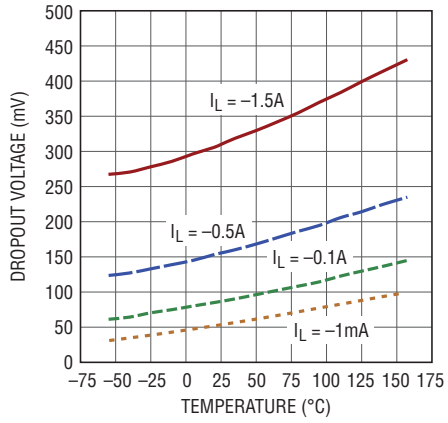
Typical Dropout Voltage (DFN/MSOP)



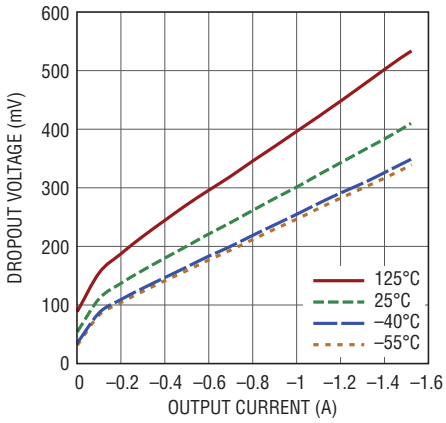
Guaranteed Dropout Voltage (DFN/MSOP)



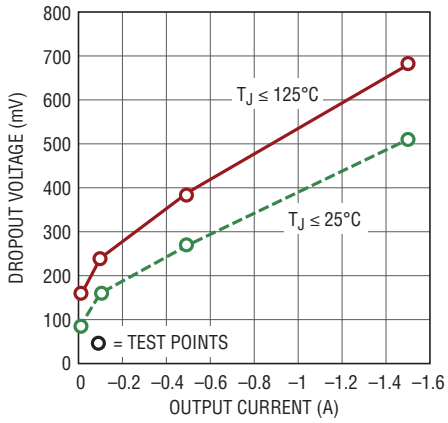
Dropout Voltage (DFN/MSOP)



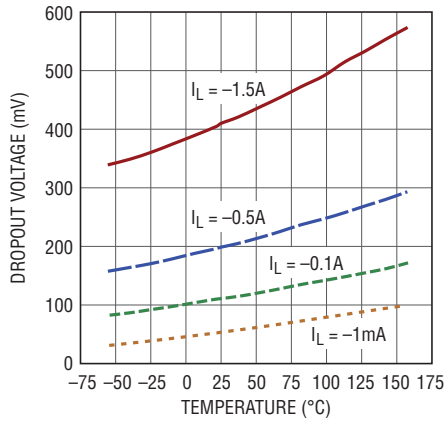
Typical Dropout Voltage (DD-PAK/TO-220)



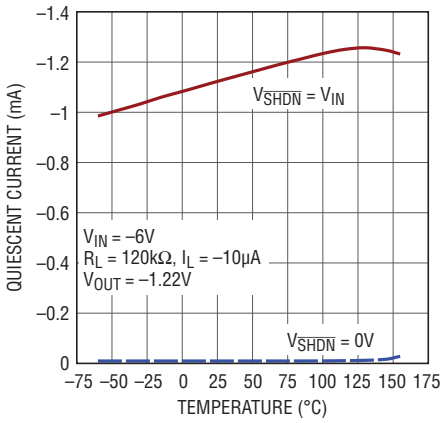
Guaranteed Dropout Voltage (DD-PAK/TO-220)



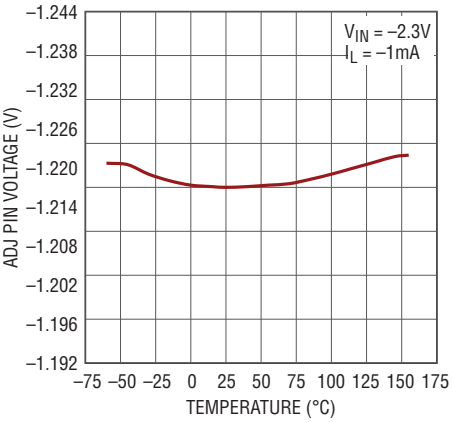
Dropout Voltage (DD-PAK/TO-220)



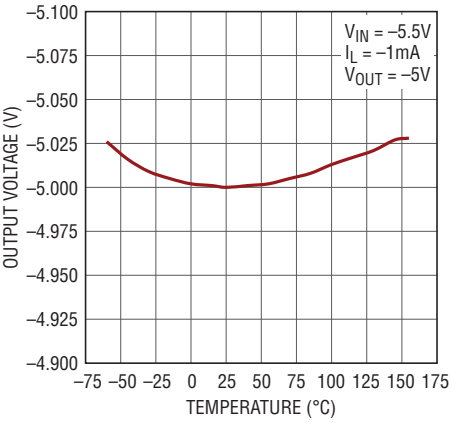
Quiescent Current



LT3015 ADJ Pin Voltage

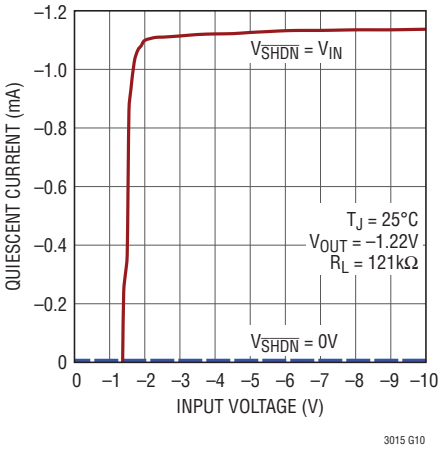


LT3015 Output Voltage

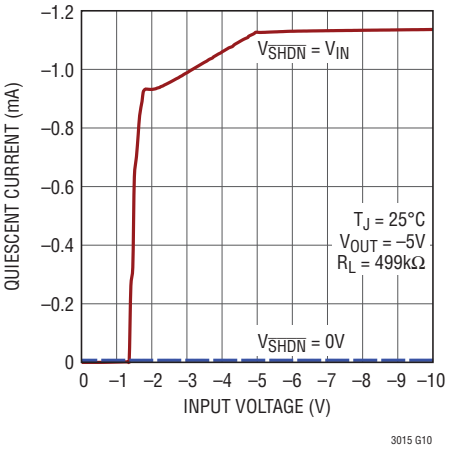


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

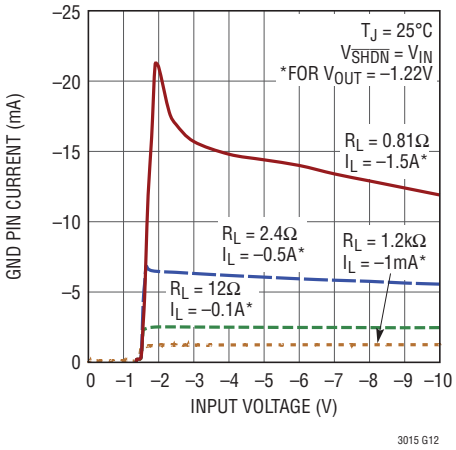
LT3015 Quiescent Current



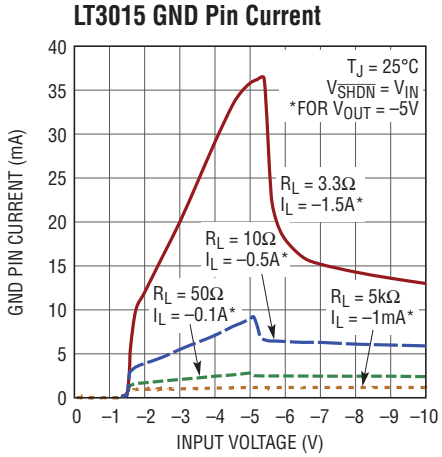
LT3015 Quiescent Current



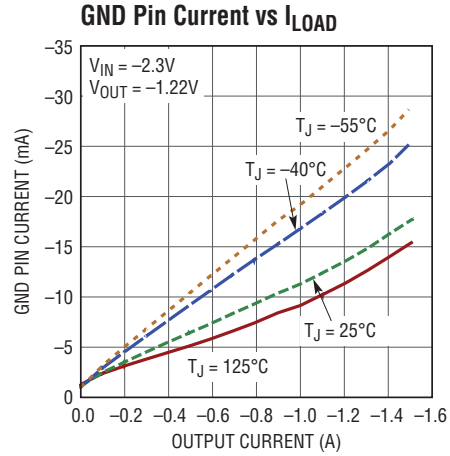
LT3015 GND Pin Current



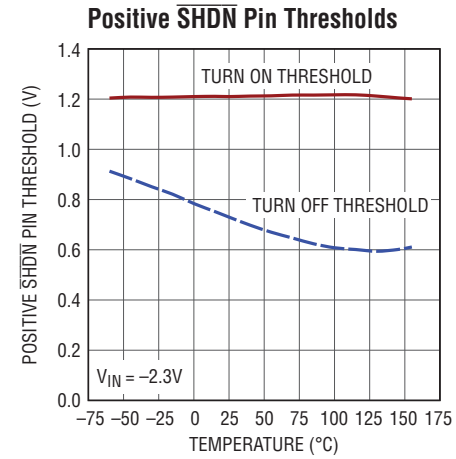
LT3015 GND Pin Current



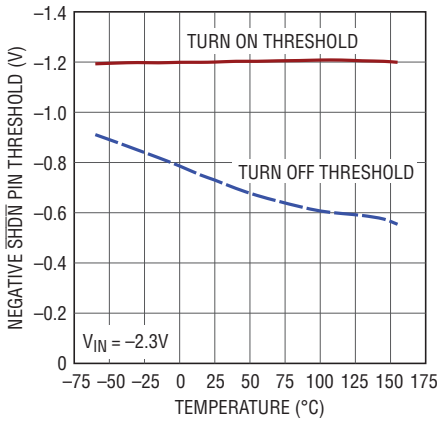
GND Pin Current vs I_{LOAD}



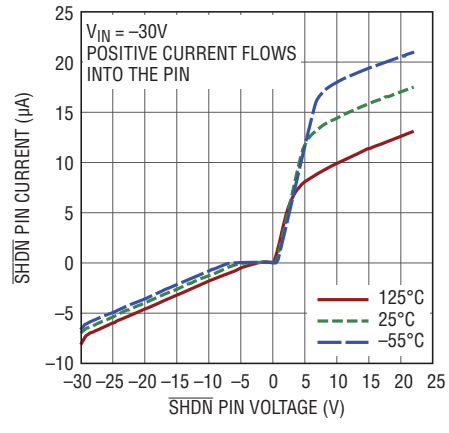
Positive $\overline{SHDN}$ Pin Thresholds



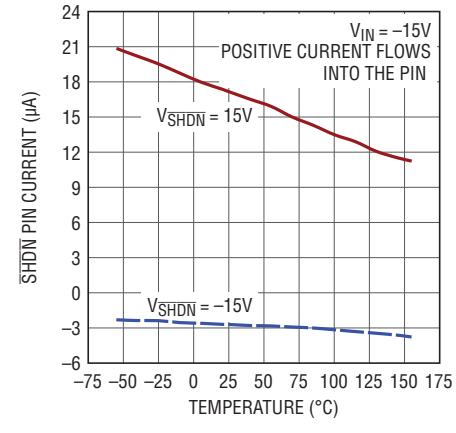
Negative $\overline{SHDN}$ Pin Thresholds



$\overline{SHDN}$ Pin Input Current

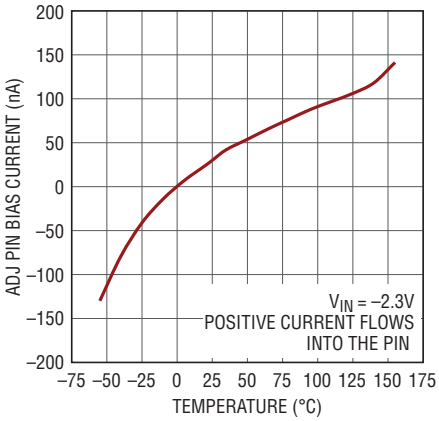


$\overline{SHDN}$ Pin Input Current



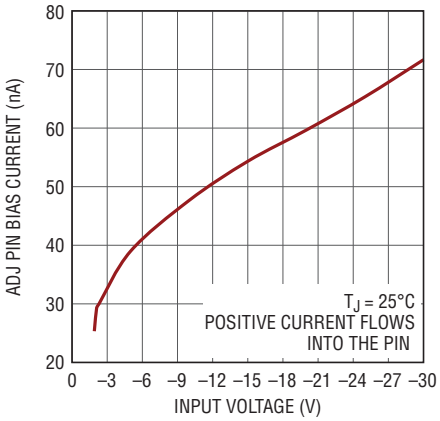
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

ADJ Pin Bias Current



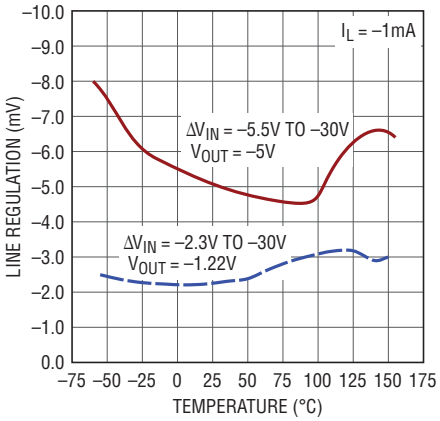
3015 G19

ADJ Pin Bias Current



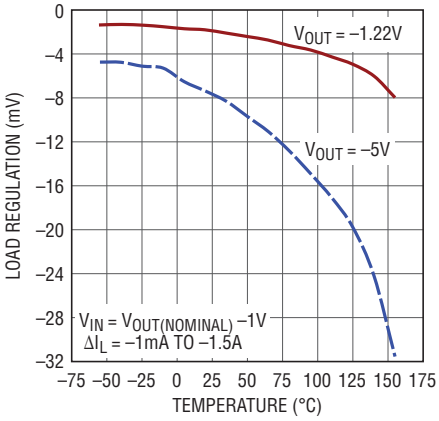
3015 G20

Line Regulation



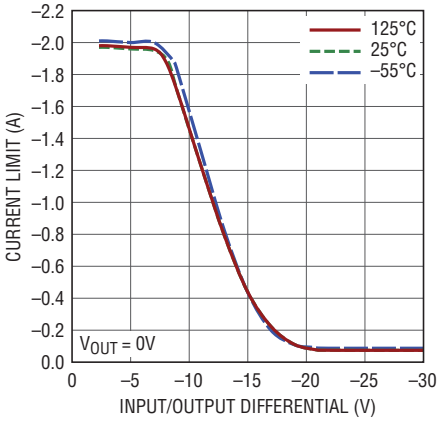
3015 G21

Load Regulation



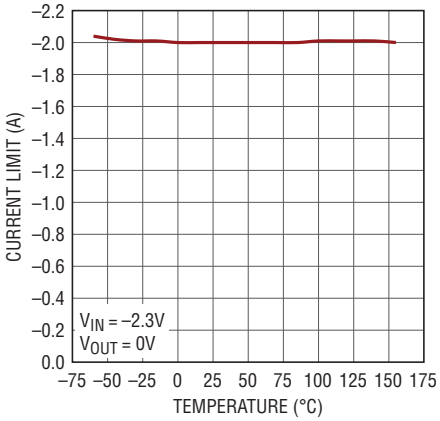
3015 G22

Current Limit vs V_{IN} –V_{OUT}



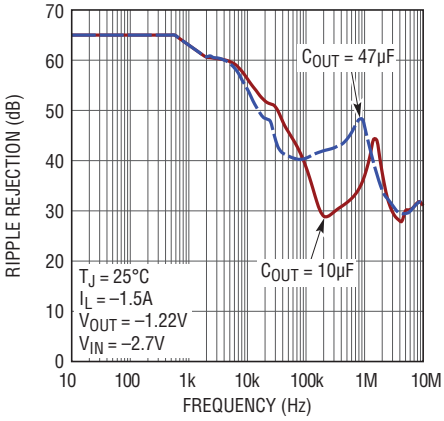
3015 G26

Current Limit vs Temperature



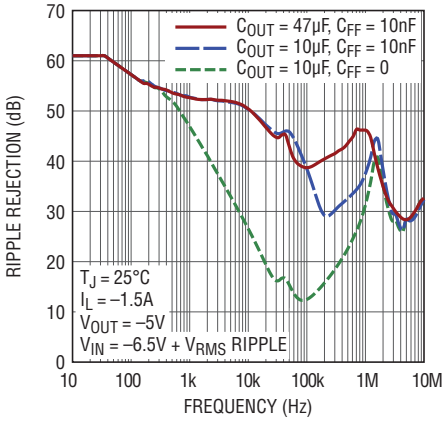
3015 G27

LT3015 Input Ripple Rejection



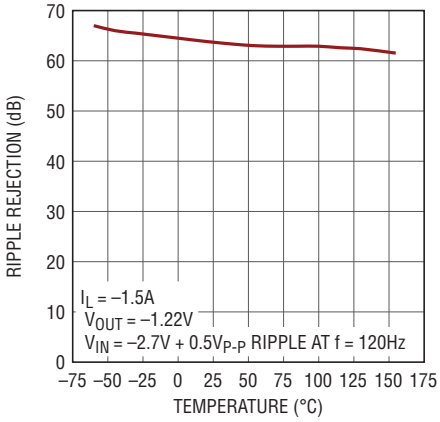
3015 G28

LT3015 Input Ripple Rejection



3015 G29

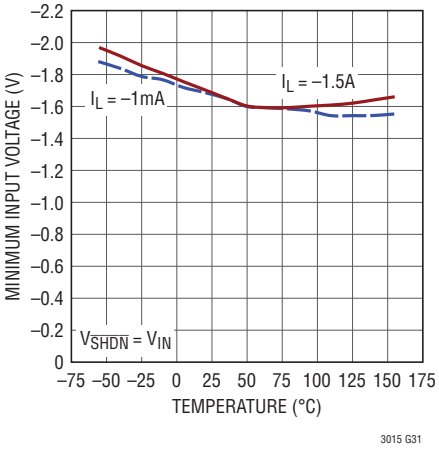
Ripple Rejection vs Temperature



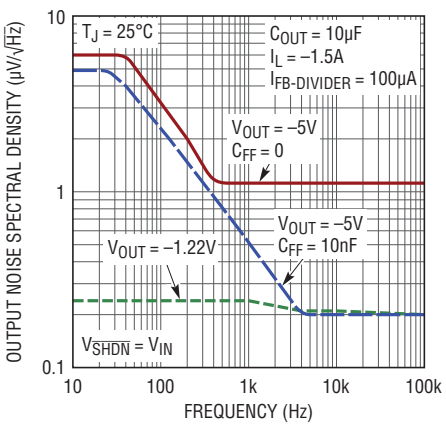
3015 G30

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

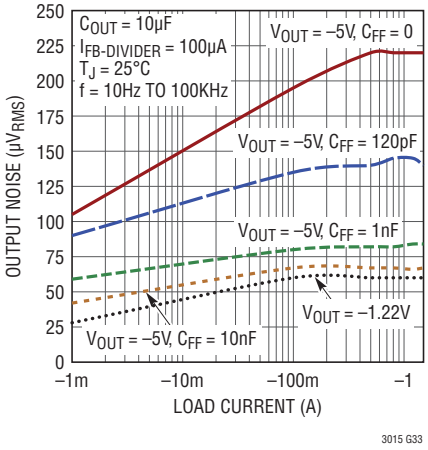
Minimum Input Voltage



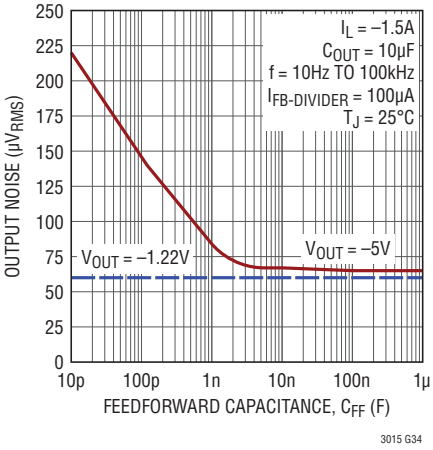
Output Noise Spectral Density



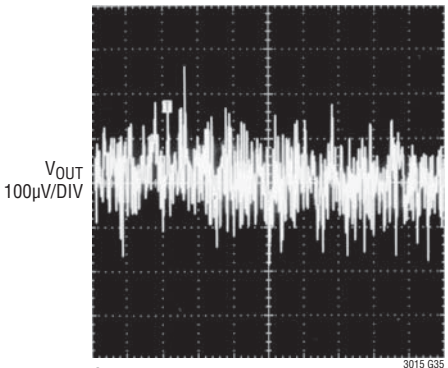
RMS Output Noise vs Load Current



RMS Output Noise vs Feedforward Capacitor (C_{FF})

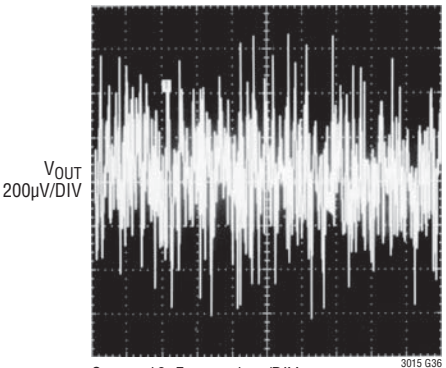


LT3015 10Hz to 100kHz Output Noise



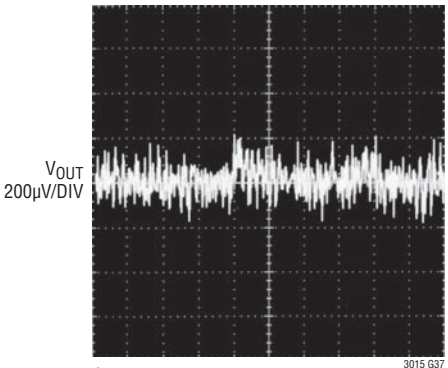
C_{OUT} = 10μF 1ms/DIV
V_{OUT} = –1.22V
I_L = –1.5A

LT3015 10Hz to 100kHz Output Noise, C_{FF} = 0



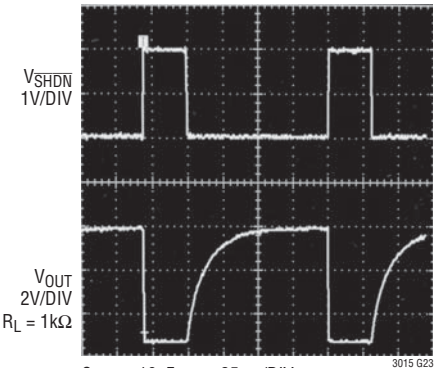
C_{OUT} = 10μF 1ms/DIV
V_{OUT} = –5V
I_L = –1.5A
C_{FF} = 0

LT3015 10Hz to 100kHz Output Noise, C_{FF} = 10nF



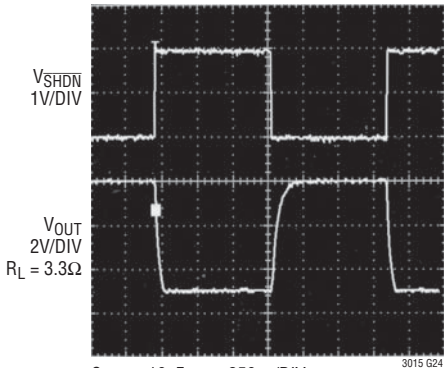
C_{OUT} = 10μF 1ms/DIV
V_{OUT} = –5V
I_L = –1.5A
C_{FF} = 10nF

$\overline{SHDN}$ Transient Response, I_L = –5mA, C_{FF} = 0



C_{OUT} = 10μF 25ms/DIV
V_{OUT} = –5V
C_{FF} = 0

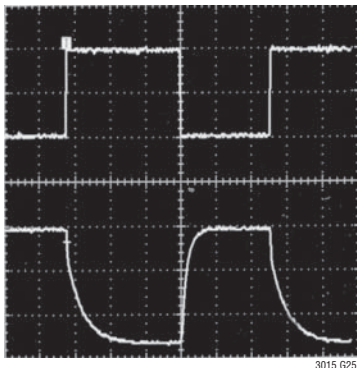
$\overline{SHDN}$ Transient Response, I_L = –1.5A, C_{FF} = 0



C_{OUT} = 10μF 250μs/DIV
V_{OUT} = –5V
C_{FF} = 0

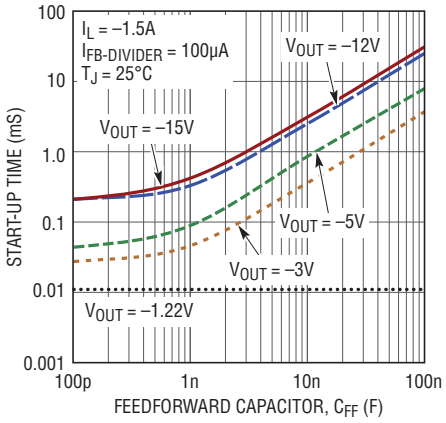
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

$\overline{SHDN}$ Transient Response, I_L = –1.5A, C_{FF} = 10nF

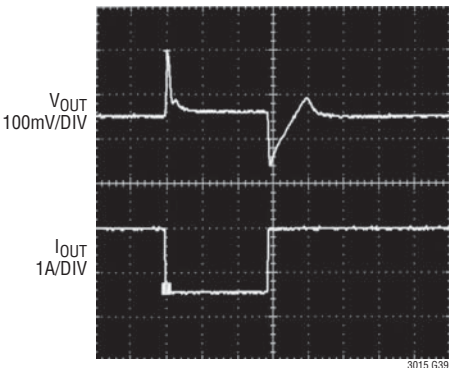


C_{OUT} = 10µF 250µs/DIV
V_{OUT} = –5V
C_{FF} = 10nF

Start-Up Time vs C_{FF}

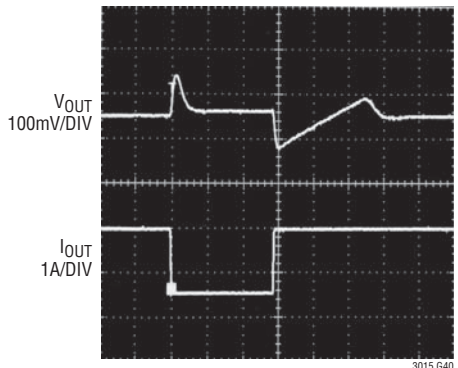


LT3015 Transient Response, C_{OUT} = 10µF



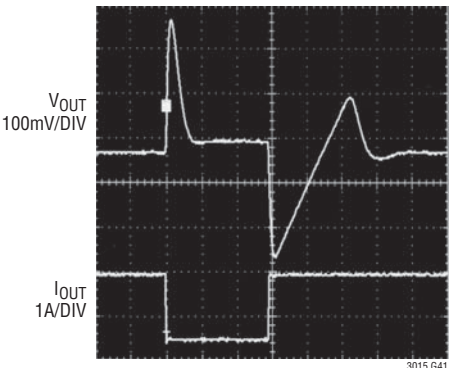
C_{OUT} = 10µF 25µs/DIV
V_{OUT} = –1.22V
ΔI_{OUT} = –50mA TO –1.5A

LT3015 Transient Response, C_{OUT} = 47µF



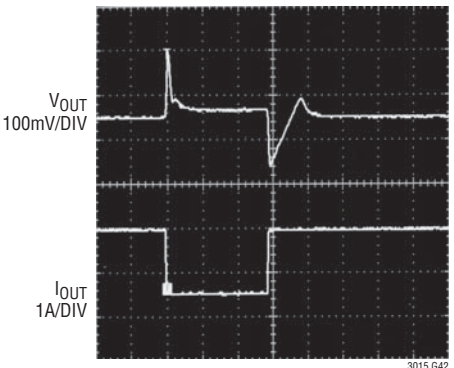
C_{OUT} = 47µF 25µs/DIV
V_{OUT} = –1.22V
ΔI_{OUT} = –50mA TO –1.5A

LT3015 Transient Response, C_{FF} = 0, C_{OUT} = 10µF



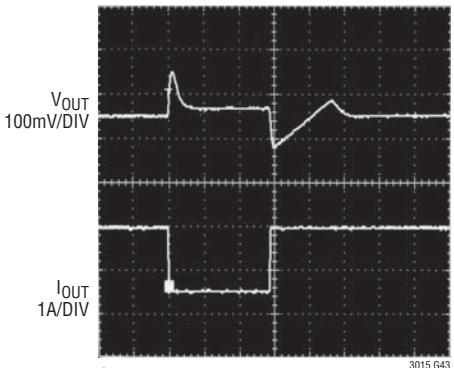
C_{OUT} = 10µF 25µs/DIV
V_{OUT} = –5V
C_{FF} = 0
$I_{FB-DIVIDER}$ = 100µA
ΔI_{OUT} = –50mA TO –1.5A

LT3015 Transient Response, C_{FF} = 10nF, C_{OUT} = 10µF



C_{OUT} = 10µF 25µs/DIV
V_{OUT} = –5V
C_{FF} = 10nF
$I_{FB-DIVIDER}$ = 100µA
ΔI_{OUT} = –50mA TO –1.5A

LT3015 Transient Response, C_{FF} = 10nF, C_{OUT} = 47µF



C_{OUT} = 47µF 25µs/DIV
V_{OUT} = –5V
C_{FF} = 10nF
$I_{FB-DIVIDER}$ = 100µA
ΔI_{OUT} = –50mA TO –1.5A

PIN FUNCTIONS (DFN/MSOP/Q/T)

IN (Pins 1, 2, Exposed Pad Pin 9 / 1, 2, 3, 4, Exposed Pad Pin 13 / 3, Tab / 3, Tab): Input. These pins supply power to the regulator. The Tab of the DD-Pak, TO-220 and the exposed backside pad of the DFN and MSOP packages is an electrical connection to IN and to the device's substrate. For proper electrical and thermal performance, tie all IN pins together and tie IN to the exposed backside or Tab of the relevant package on the PCB. See the Applications Information Section for thermal considerations and calculating junction temperature. The LT3015 requires a bypass capacitor at IN. In general, a battery's output impedance rises with frequency, so include a bypass capacitor in battery powered applications. An input bypass capacitor in the range of 1µF to 10µF generally suffices, but applications with large load transients may require higher input capacitance to prevent input supply droop and prevent the regulator from entering dropout.

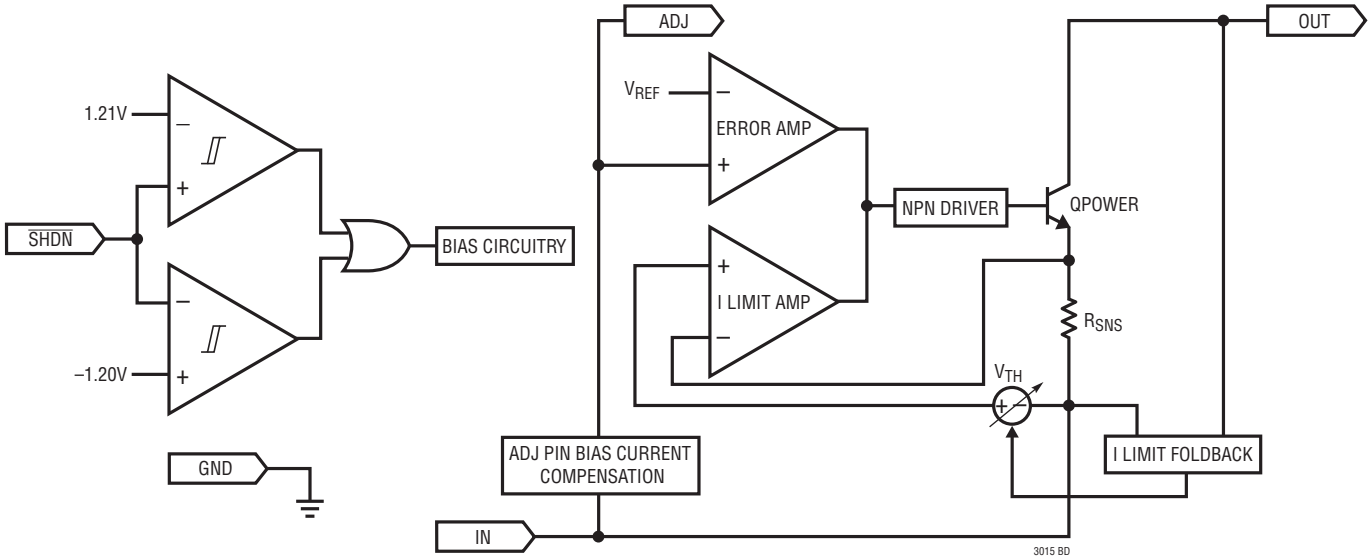
$\overline{\text{SHDN}}$ (Pin 3 / 5 / 1 / 1): Shutdown. Use the $\overline{\text{SHDN}}$ pin to put the LT3015 into a micropower shutdown state. The $\overline{\text{SHDN}}$ function is bi-directional, allowing use of either positive or negative logic. The $\overline{\text{SHDN}}$ pin threshold voltages are referenced to GND. The output of the LT3015 is OFF if the $\overline{\text{SHDN}}$ pin is pulled within ±0.73V of GND. Driving the $\overline{\text{SHDN}}$ pin more than ±1.21V turns the LT3015 ON. Drive the $\overline{\text{SHDN}}$ pin with either a logic gate or with open collector/drain logic using a pull-up resistor. The resistor supplies the pull-up current of the open collector/drain gate, typically several microamperes. The typical $\overline{\text{SHDN}}$ pin current is 2.8µA out of the pin (for negative logic) or 17µA into the pin (for positive logic). If the $\overline{\text{SHDN}}$ function is unused, connect the $\overline{\text{SHDN}}$ pin to V_{IN} to turn the device ON. If the $\overline{\text{SHDN}}$ pin is floated, then the LT3015 is OFF. A parasitic diode exists between $\overline{\text{SHDN}}$ and IN of the LT3015. Therefore, do not drive the $\overline{\text{SHDN}}$ pin more than 0.3V below IN during normal operation or during a fault condition. The $\overline{\text{SHDN}}$ pin can also be used to set a programmable undervoltage lockout (UVLO) threshold for the regulator input supply.

GND (Pins 4, 5 / 6, 7 / 2 / 2): Ground. Tie all GND pin(s) together and tie the bottom of the output voltage setting resistor divider directly to the GND pin(s) for optimum load regulation performance.

ADJ (Pin 6 / 8 / 4 / 4): Adjust. This pin is the error amplifier's non-inverting input. It has a typical bias current of 30nA that flows into the pin. The ADJ pin reference voltage is –1.22V referred to GND, and the output voltage range is –1.22V to –29.5V. A parasitic substrate diode exists between ADJ and IN of the LT3015. Therefore, do not drive ADJ more than 0.3V below IN during normal operation or during a fault condition.

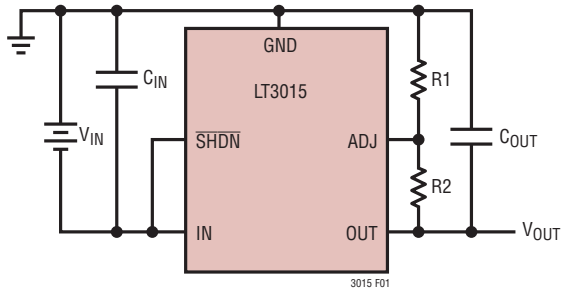
OUT (Pins 7, 8 / 9, 10, 11, 12 / 5 / 5): Output. These pins supply power to the load. Tie all OUT pins together for best performance. Use a minimum output capacitor of 10µF to prevent oscillations. Large load transient applications require larger output capacitors to limit peak voltage transients. See the Applications Information section for more information on output capacitance. A parasitic substrate diode exists between OUT and IN of the LT3015. Therefore, do not drive OUT more than 0.3V below IN during normal operation or during a fault condition.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LT3015 regulator is a 1.5A negative low dropout linear regulator featuring precision current limit and precision bi-directional shutdown. The device supplies up to 1.5A of output load current at a typical dropout voltage of 310mV. Moreover, the low 1.1mA operating quiescent current drops to less than 1µA in shutdown. In addition to low quiescent current, the LT3015 incorporates several protection features that make it ideal for battery powered applications. In dual supply applications where the regulator's load is returned to a positive supply, OUT can be pulled above GND by 30V and still allow the LT3015 to start up and operate.



$V_{OUT} = -1.22V\left(1+\frac{R2}{R1}\right)+(I_{ADJ})(R2)$

$V_{ADJ} = -1.22V$ AND $I_{ADJ} = 30nA$ AT 25°C

OUTPUT RANGE = –1.22 TO –29.5V

Figure 1. Adjustable Operation

Adjustable Operation

The LT3015 regulator has an output voltage range of –1.22V to –29.5V. Output voltage is set by the ratio of two external resistors as shown in Figure 1. The device regulates the output to maintain the ADJ pin voltage to –1.22V referred to ground. The current in R1 equals –1.22V/R1 and the current in R2 equals the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 30nA at 25°C, flows into the ADJ pin. Calculate the output voltage using the formula shown in Figure 1. The value of R1 should be less than 50k to minimize errors in the output voltage created by the ADJ pin bias current. Note that in shutdown, the output is off and the divider current is zero. Curves of ADJ Pin Voltage vs Temperature, ADJ Pin Bias Current vs Temperature and ADJ Pin Bias Current vs Input Voltage appear in the Typical Performance Characteristics section.

The adjustable device is tested and specified with the ADJ pin tied to the OUT pin for a –1.22V output voltage. Specifications for output voltages greater than –1.22V are proportional to the ratio of the desired V_{OUT} to –1.22V (V_{OUT}/–1.22V). For example, load regulation for an output current change of –1mA to –1.5A is typically 2mV at V_{OUT} = –1.22V. At V_{OUT} = –5V, load regulation equals:

(–5V/–1.22V) • (2mV) = 8.2mV

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Table 1 shows 1% resistor divider values for some common output voltages with a resistor divider current of approximately 100µA.

Table 1. Output Voltage Resistor Divider Values

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
–2.5	12.1	12.7
–3.0	12.1	17.8
–3.3	12.1	20.5
–5.0	12.1	37.4
–12.0	12.1	107
–15.0	12.4	140

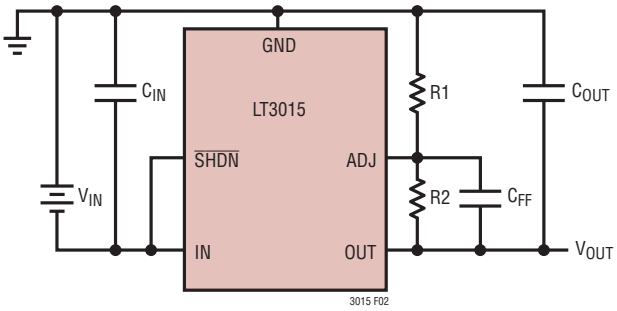
Feedforward Capacitance: Output Voltage Noise, Transient Performance, and PSRR

The LT3015 regulators provide low output voltage noise over the 10Hz to 100kHz bandwidth while operating at full load current. Output voltage noise is approximately 240nV/$\sqrt{Hz}$ over this frequency while operating in unity-gain configuration. For higher output voltages (using a resistor divider), the output voltage noise gains up accordingly. To lower the output voltage noise for higher output voltages, include a feedforward capacitor (C_{FF}) from V_{OUT} to V_{ADJ}. A good quality, low leakage, capacitor is recommended. This capacitor bypasses the resistor divider network at high frequencies; and hence, reduces the output noise. With the use of a 10nF feedforward capacitor, the output noise decreases from 220µV_{RMS} to 70µV_{RMS} when the output voltage is set to –5V by a 100µA feedback resistor divider.

Higher values of output voltage noise are often measured if care is not exercised with regard to circuit layout and testing. Crosstalk from nearby traces induces unwanted noise onto the LT3015's output. Moreover, power supply ripple rejection (PSRR) must also be considered, as the LT3015 does not exhibit unlimited PSRR; and thus, a small portion of the input noise propagates to the output.

Using a feedforward capacitor (C_{FF}) from V_{OUT} to V_{ADJ} has the added benefit of improving transient response and PSRR for output voltages greater than –1.22V. With no feedforward capacitor, the response and settling times will increase as the output voltage is raised above –1.22V. Use the equation in Figure 2 to determine the minimum value of C_{FF} to achieve a transient (and noise) performance that is similar to –1.22V output voltage performance regardless of the chosen output voltage (see Transient Response and Output Noise in the Typical Performance Characteristics section).

It is important to note that the start-up time is affected by the use of a feedforward capacitor. Start-up time is directly proportional to the size of the feedforward capacitor and the output voltage, and is inversely proportional to the feedback resistor divider current. In particular, it slows to 860µs with a 10nF feedforward capacitor and a 10µF output capacitor for an output voltage set to –5V by a 100µA feedback resistor divider current.



$C_{FF} \geq 10nF/100\mu A \bullet I_{FB\text{-}DIVIDER}$
$I_{FB\text{-}DIVIDER} = V_{OUT}/(R1+R2)$

Figure 2. Feedforward Capacitor for Fast Transient Response, Low Noise, and High PSRR

Output Capacitance and Transient Performance

The LT3015 regulator is stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. Use a minimum output capacitor of 10µF with an ESR of 500mΩ or less to prevent oscillations. The LT3015's load transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R, and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients as shown in Figures 3 and 4. When used with a 5V regulator, a 16V 10µF Y5V capacitor

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can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified in situ for all applications.

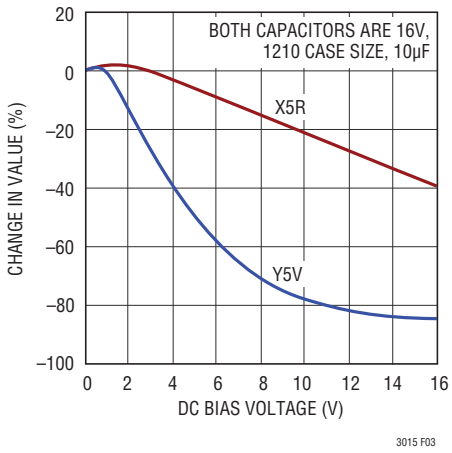

Figure 3. Ceramic Capacitor DC Bias Characteristics

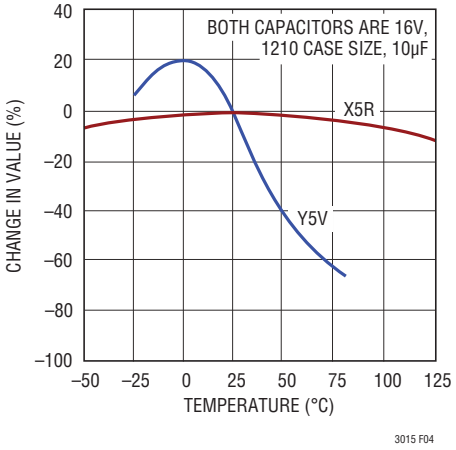

Figure 4. Ceramic Capacitor Temperature Characteristics

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients. The resulting voltages produced can cause appreciable amounts of noise. A ceramic capacitor produced the trace in Figure 5 in response to light tapping from a pencil. Similar vibration induced behavior can masquerade as increased output voltage noise.

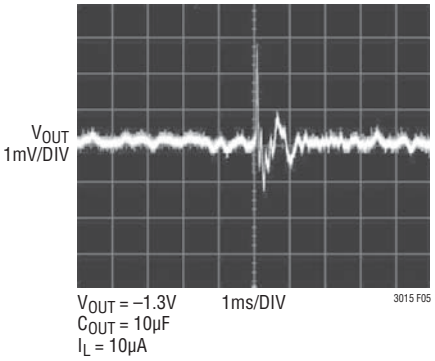

Figure 5. Noise Resulting from Tapping on a Ceramic Capacitor

Overload Recovery

Like many IC power regulators, the LT3015 has safe operating area protection. The safe operating area protection activates at IN-to-OUT differential voltages greater than 8V. The safe area protection decreases current limit as the IN-to-OUT differential voltage increases and keeps the power transistor inside a safe operating region for all values of forward input-to-output voltage up to the LT3015's Absolute Maximum Ratings.

When power is first applied and input voltage rises, the output follows the input and keeps the IN-to-OUT differential voltage small, allowing the regulator to supply large output currents and start-up into high current loads. With a high input voltage, a problem can occur wherein removal of an output short does not allow the output voltage to fully recover. Other LTC negative linear regulators such as the LT1175 and LT1964 also exhibit this phenomenon, so it is not unique to the LT3015.

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The problem occurs with a heavy output load when input voltage is high and output voltage is low. Such situations occur easily after the removal of a short-circuit or if the shutdown pin is pulled high after the input voltage has already been turned on. The load line for such a load intersects the output current curve at two points. If this happens, the regulator has two stable output operating points. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

Shutdown/UVLO

The $\overline{SHDN}$ pin is used to put the LT3015 into a micropower shutdown state. The LT3015 has an accurate –1.20V threshold (during turn-on) on the $\overline{SHDN}$ pin. This threshold can be used in conjunction with a resistor divider from the system input supply to define an accurate undervoltage lockout (UVLO) threshold for the regulator. The $\overline{SHDN}$ pin current (at the threshold) needs to be considered when determining the resistor divider network.

Thermal Considerations

The LT3015's maximum rated junction temperature of 125°C limits its power handling capability. Two components comprise the power dissipated by the device:

1. Output current multiplied by the input-to-output differential voltage: $I_{OUT} \bullet (V_{IN} - V_{OUT})$ and
2. GND pin current multiplied by the input voltage: $I_{GND} \bullet V_{IN}$

Determine GND pin current using the GND Pin Current curves in the Typical Performance Characteristics section. Total power dissipation is the sum of the above two components.

The LT3015 regulator incorporates a thermal shutdown circuit designed to protect the device during overload conditions. The typical thermal shutdown temperature is 165°C and the circuit incorporates about 8°C of hysteresis. For continuous normal conditions, do not exceed the maximum junction temperature rating of 125°C. Carefully consider all sources of thermal resistance from junction to ambient, including other heat sources mounted in close proximity to the LT3015.

The undersides of the DFN and MSOP packages have exposed metal from the lead frame to the die attachment. Both packages allow heat to directly transfer from the die junction to the printed circuit board metal to control maximum operating junction temperature. The dual-in-line pin arrangement allows metal to extend beyond the ends of the package on the topside (component side) of the PCB. Connect this metal to IN on the PCB. The multiple IN and OUT pins of the LT3015 also assist in spreading heat to the PCB.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

Tables 2-4 list thermal resistance as a function of copper area in a fixed board size. All measurements were taken in still air on a 4 layer FR-4 board with 1oz solid internal planes and 2oz top/bottom external trace planes with a total board thickness of 1.6mm. The four layers were electrically isolated with no thermal vias present. PCB layers, copper weight, board layout and thermal vias will affect the resultant thermal resistance. For more information on thermal resistance and high thermal conductivity test boards, refer to JEDEC standard JESD51, notably JESD51-12 and JESD51-7. Achieving low thermal resistance necessitates attention to detail and careful PCB layout.

APPLICATIONS INFORMATION

Table 2. Measured Thermal Resistance for DFN Package

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOP SIDE*	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	40°C/W
1000mm^2	2500mm^2	2500mm^2	40°C/W
225mm^2	2500mm^2	2500mm^2	41°C/W
100mm^2	2500mm^2	2500mm^2	42°C/W

*Device is mounted on topside

Table 3. Measured Thermal Resistance for MSOP Package

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOP SIDE*	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	37°C/W
1000mm^2	2500mm^2	2500mm^2	37°C/W
225mm^2	2500mm^2	2500mm^2	38°C/W
100mm^2	2500mm^2	2500mm^2	40°C/W

*Device is mounted on topside

Table 4. Measured Thermal Resistance for DD-Pak Package

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOP SIDE*	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	14°C/W
1000mm^2	2500mm^2	2500mm^2	16°C/W
225mm^2	2500mm^2	2500mm^2	19°C/W

*Device is mounted on topside

T Package, 5-Lead TO-220

Thermal Resistance (Junction-to-Case) = 3°C/W

Calculating Junction Temperature

Example: Given an output voltage of –2.5V, an input voltage range of –3.3V ± 5%, an output current range of 1mA to 500mA, and a maximum ambient temperature of 85°C, what is the maximum junction temperature?

The power dissipated by the LT3015 equals:

$$I_{OUT(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) + I_{GND} \bullet (V_{IN(MAX)})$$

where:

$I_{OUT(MAX)} = –500mA$

$V_{IN(MAX)} = –3.465V$

I_{GND} at ($I_{OUT} = –500mA$, $V_{IN} = –3.465V$) = –6.5mA

Thus:

$$P = –500mA(–3.465V + 2.5V) + –6.5mA \bullet (–3.465V) = 0.505W$$

Using a DFN package, the thermal resistance is in the range of 40°C/W to 42°C/W depending on the copper area. Therefore, the junction temperature rise above ambient approximately equals:

$$0.505W \bullet 41°C/W = 20.7°C$$

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient or:

$$T_{JMAX} = 85°C + 20.7°C = 105.7°C$$

Protection Features

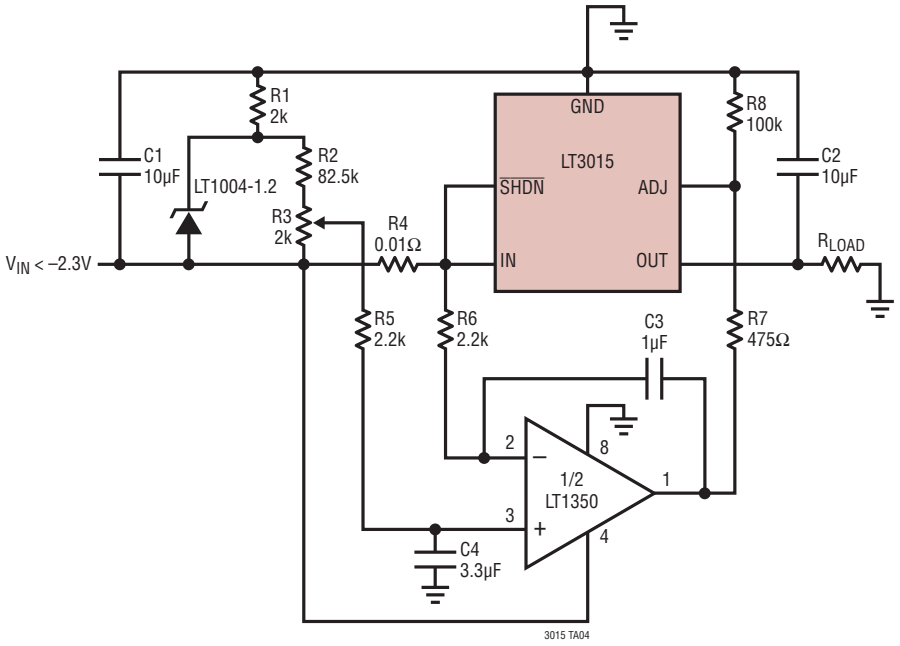
The LT3015 incorporates several protection features that make it ideal for use in battery-powered applications. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device protects itself against reverse input voltages and reverse output voltages.

Precision current limit and thermal overload protections are intended to protect the LT3015 against current overload conditions at the output of the device. For normal operation, do not allow the the junction temperature to exceed 125°C.

Pulling the LT3015's output above ground induces no damage to the part. If IN is left open circuit or grounded, OUT can be pulled above GND by 30V. In addition, OUT acts like an open circuit, i.e. no current flows into the pin. If IN is powered by a voltage source, OUT sinks the LT3105's short-circuit current and protects itself by thermal limiting. In this case, grounding the $\overline{SHDN}$ pin turns off the device and stops OUT from sinking the short-circuit current.

TYPICAL APPLICATIONS

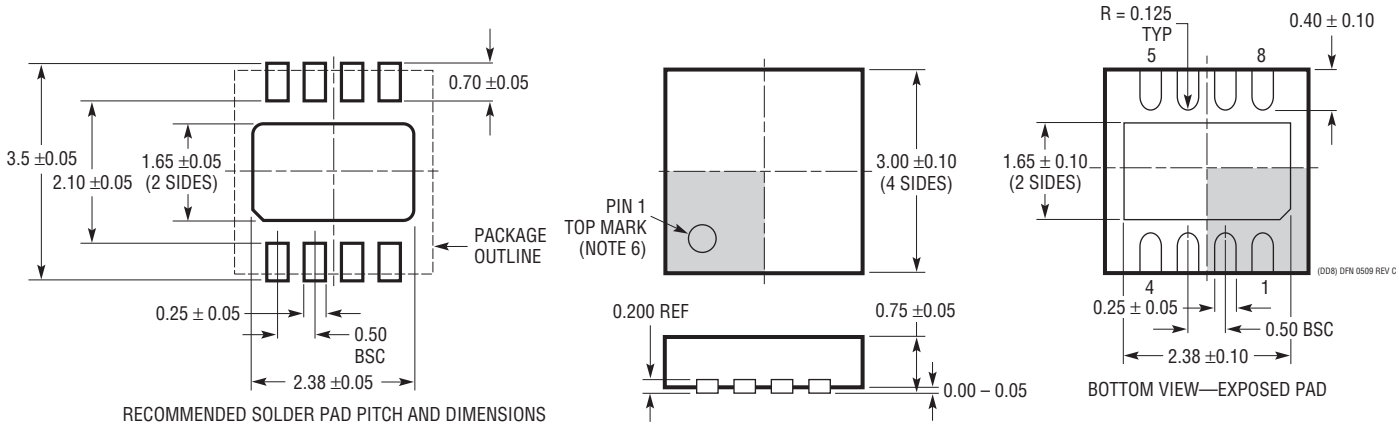
Adjustable Current Sink



NOTE: ADJUST R3 FOR 0 TO –1.5A CONSTANT CURRENT

PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



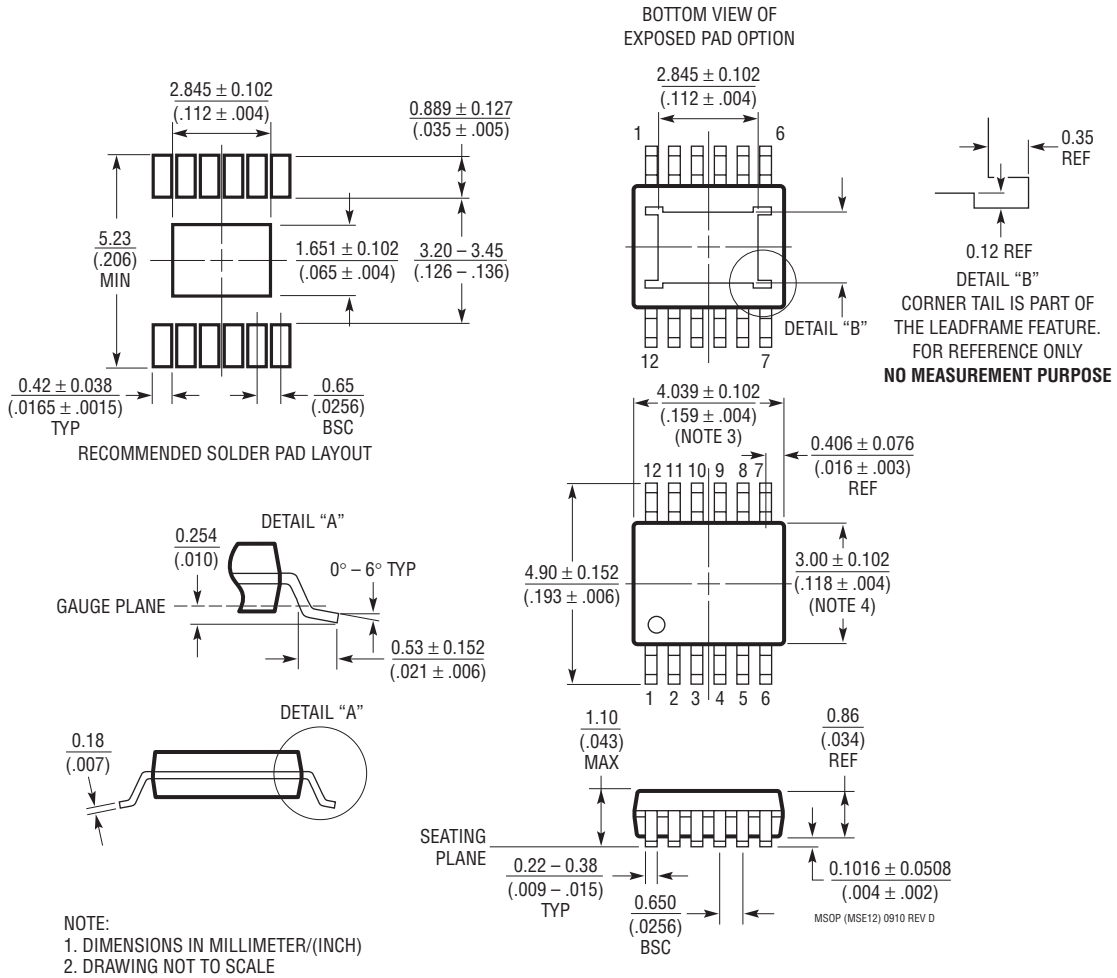
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

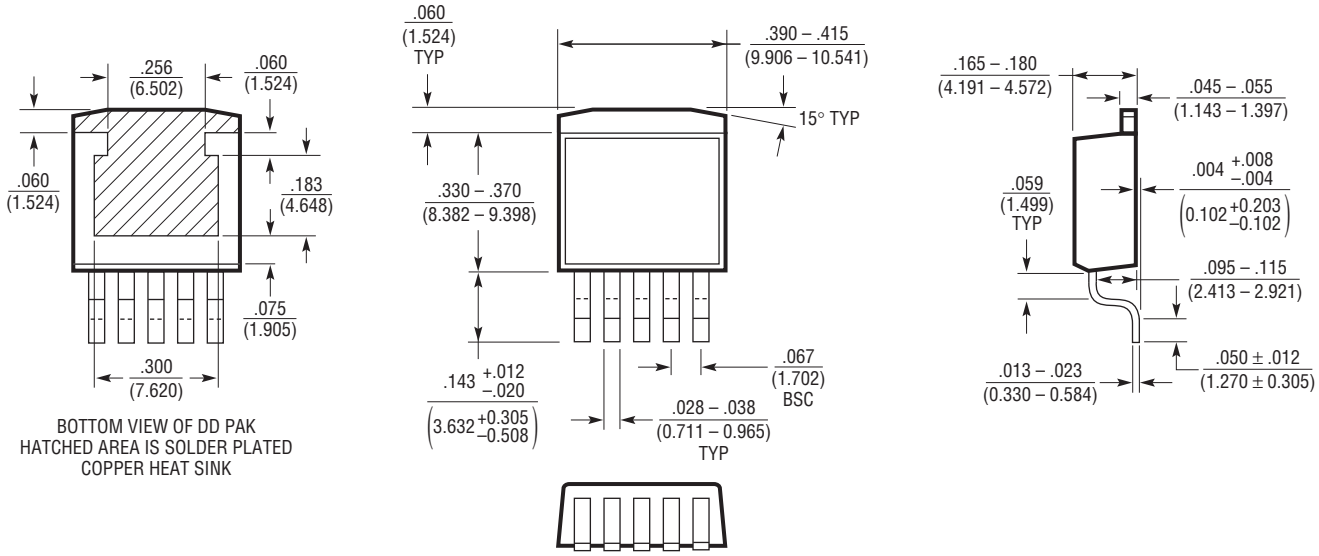
MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev D)



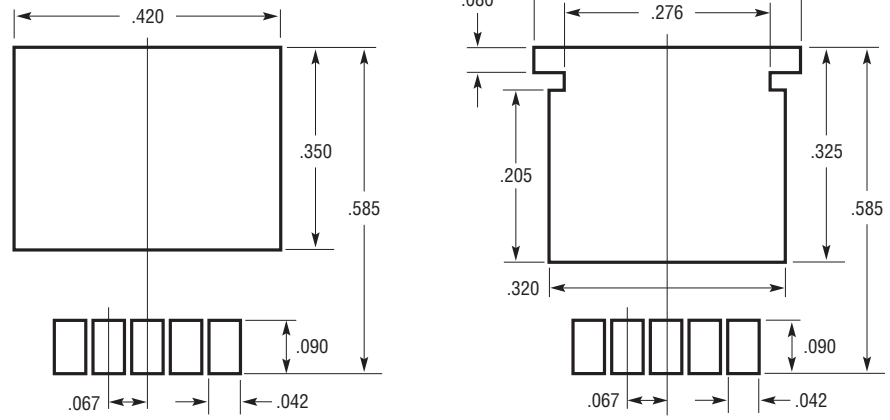
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Q Package
5-Lead Plastic DD Pak
(Reference LTC DWG # 05-08-1461 Rev E)



BOTTOM VIEW OF DD PAK
HATCHED AREA IS SOLDER PLATED
COPPER HEAT SINK



RECOMMENDED SOLDER PAD LAYOUT

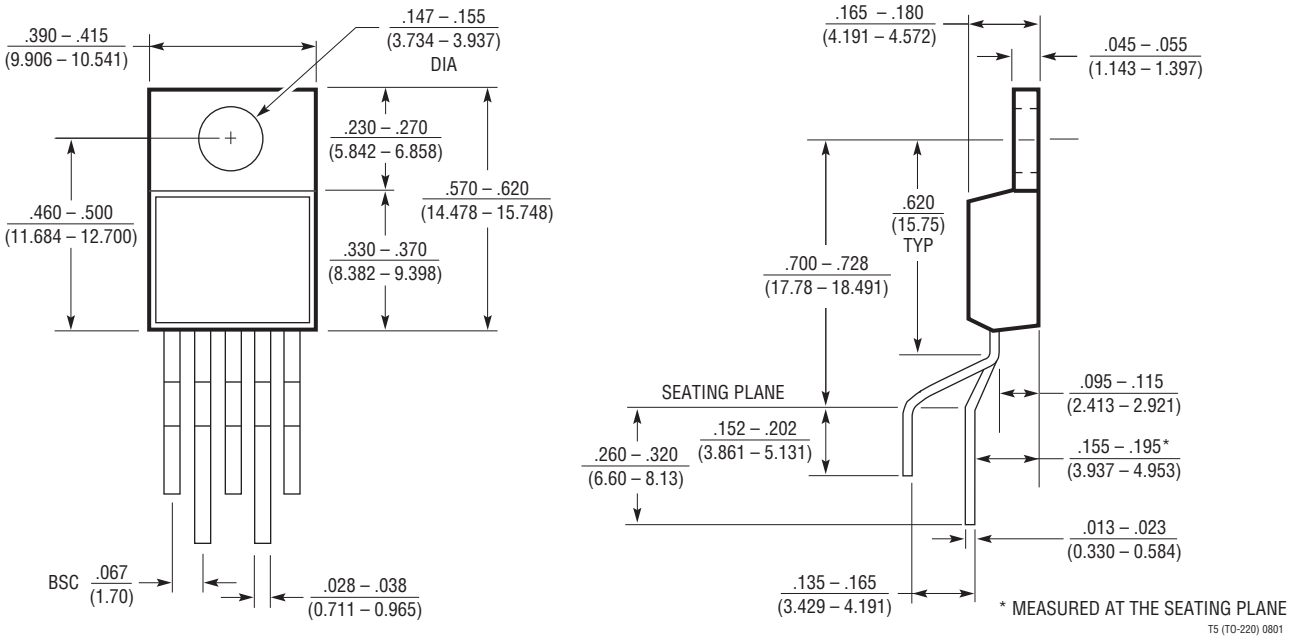
NOTE:
1. DIMENSIONS IN INCH/(MILLIMETER)
2. DRAWING NOT TO SCALE

RECOMMENDED SOLDER PAD LAYOUT
FOR THICKER SOLDER PASTE APPLICATIONS

Q(DD5) 0610 REV E

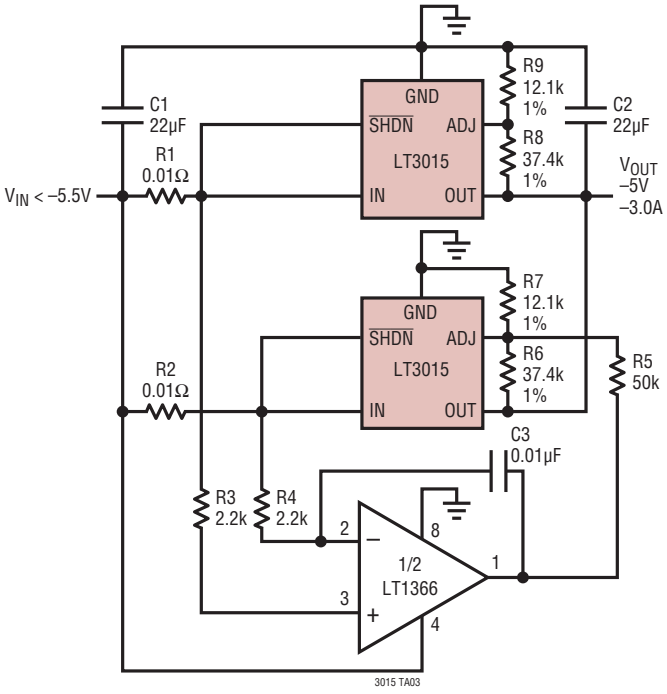
PACKAGE DESCRIPTION

T Package
5-Lead Plastic TO-220 (Standard)
(Reference LTC DWG # 05-08-1421)



TYPICAL APPLICATION

Paralleling Regulators For Higher Output Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1185	3A, Negative Linear Regulator	670mV Dropout Voltage, V_{IN} = –4.3V to –35V, DD-Pak and TO-220 Packages
LT1175	500mA, Negative Low Dropout Micropower Regulator	500mV Dropout Voltage, V_{IN} = –4.5V to –20V, S8, N8, SOT-223, DD-Pak and TO-220 Packages
LT1964	200mA, Negative Low Noise Low Dropout Regulator	340mV Dropout Voltage, Low Noise: 30µV_{RMS}, V_{IN} = –1.9V to –20V, 3mm × 3mm DFN and ThinSOT Packages
LT1764A	3A, Fast Transient Response, Low Noise LDO Regulator	340mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN} = 2.7V to 20V, TO-220 and DD-Pak Packages, "A" Version Stable also with Ceramic Caps
LT1763	500mA, Low Noise, LDO Regulator	300mV Dropout Voltage, Low Noise : 20µV_{RMS}, V_{IN} = 1.6V to 20V, Stable with 3.3µF Output Capacitors, S8 and 3mm × 4mm DFN Packages
LT1963A	1.5A Low Noise, Fast Transient Response LDO Regulator	340mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN} = 2.5V to 20V, "A" Version Stable with Ceramic Caps, TO-220, DD-Pak, SOT-223 and SO-8 Packages
LT1965	1.1A, Low Noise, LDO Regulator	310mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN}: 1.8V to 20V, V_{OUT}: 1.2V to 19.5V, Stable with Ceramic Caps, TO-220, DD-Pak, MSOP-8E and 3mm × 3mm DFN Packages
LT3022	1A, Low Voltage, Very Low Dropout V_{LDO} Linear Regulator	V_{IN} = 0.9V to 10V, Dropout Voltage: 145mV Typical, Adjustable Output (V_{REF} = $V_{OUT(MIN)}$ = 200mV), Fixed Output Voltages: 1.2V, 1.5V, 1.8V, Stable with Low ESR, Ceramic Output Capacitors 16-Pin 3mm × 5mm DFN and MSOP-16E Packages
LT3080/LT3080-1	1.1A, Parallelable, Low Noise, Low Dropout Linear Regulator	300mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} set; Directly Parallelable (no op amp required), Stable with Ceramic Caps, TO-220, DD-Pak, SOT-223, MSOP-8E and 3mm × 3mm DFN Packages; "–1" Version has Integrated Internal Ballast Resistor
LT3085	500mA, Parallelable, Low Noise, Low Dropout Linear Regulator	275mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} set; Directly Parallelable (no op amp required), Stable with Ceramic Caps, MSOP-8E and 2mm × 3mm DFN Packages

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