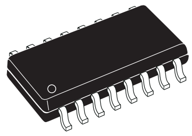
L6566A

Multi-mode controller for SMPS with PFC front-end

Features

- Selectable multi-mode operation: fixed frequency or quasi-resonant
- On-board 700 V high-voltage start-up
- Advanced light load management
- Low quiescent current (< 3 mA)
- Adaptive UVLO
- Line feedforward for constant power capability vs mains voltage
- Pulse-by-pulse OCP, shutdown on overload (latched or autorestart)
- Transformer saturation detection
- Switched supply rail for PFC controller
- Latched or autorestart OVP
- Brownout protection
- -600/+800 mA totem pole gate driver with active pull-down during UVLO
- SO16N package

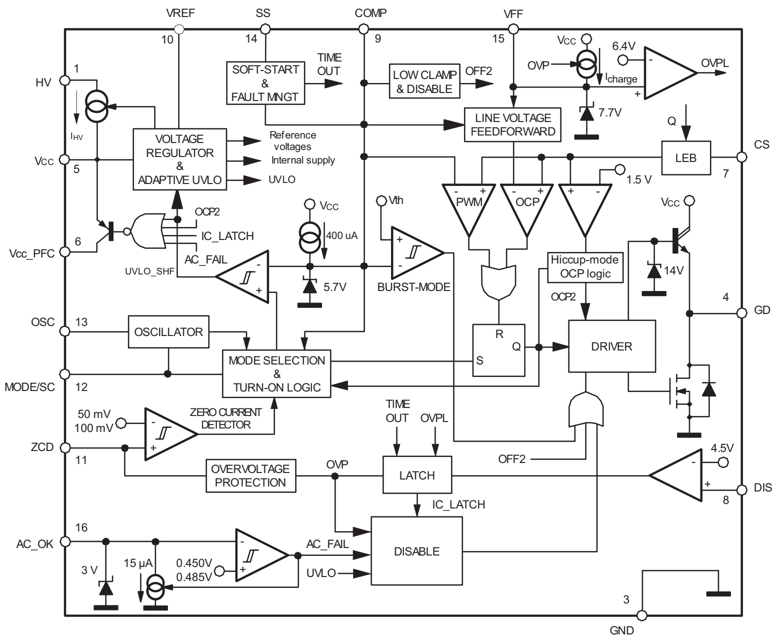


SO16N

Applications

- Notebook, TV and LCD monitors adapters
- High power chargers
- PDP/LCD TV
- Consumer appliances, like DVD, VCR, set-top box
- IT equipment, games, aux. power supplies
- Power supplies in excess of 150 W

Figure 1. Block diagram



Contents

List of tables

List of figures

1 Description

The L6566A is an extremely versatile current-mode primary controller IC specifically designed for high-performance offline flyback converters operated from front-end power factor correction (PFC) stages in applications supposed to comply with EN61000-3-2 or JEITA-MITI regulations.

Both fixed-frequency (FF) and quasi-resonant (QR) operation are supported. The user can pick either of the two depending on application needs.

The device features an externally programmable oscillator: it defines converter's switching frequency in FF mode and the maximum allowed switching frequency in QR mode.

When FF operation is selected, the IC works like a standard current-mode controller with a maximum duty cycle limited at 70 % min.

QR operation, when selected, occurs and is achieved through a transformer demagnetization sensing input that triggers MOSFET's turn-on. Under some conditions, ZVS (zero-voltage switching) can be achieved. Converter's power capability rise with the input voltage is compensated by line voltage feedforward. At medium and light load, as the QR operating frequency equals the oscillator frequency, a function (valley skipping) is activated to prevent further frequency rise and keep the operation as close to ZVS as possible.

With either FF or QR operation, at very light load the IC enters a controlled burst-mode operation that, along with the built-in non-dissipative high-voltage start-up circuit and a reduced quiescent current, helps keep low the consumption from the mains and meet energy saving recommendations.

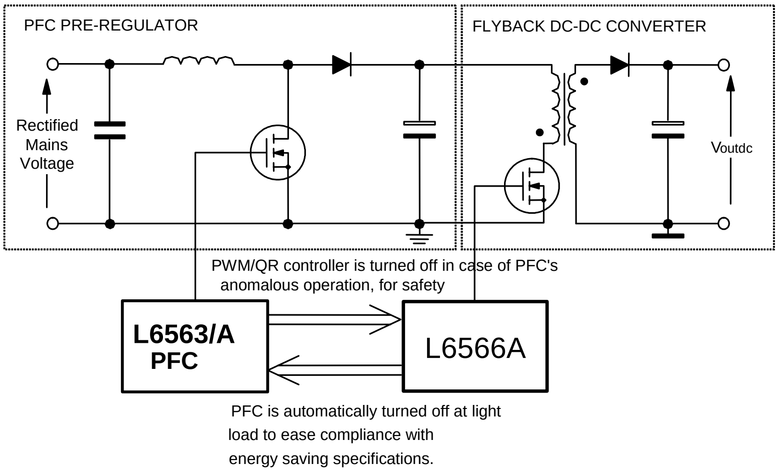
To allow meeting them in two-stage power-factor-corrected systems as well, the L6566A provides an interface with the PFC controller that enables to turn off the pre-regulator at light load.

An innovative adaptive UVLO helps minimize the issues related to the fluctuations of the self-supply voltage due to transformer's parasites.

The protection functions included in this device are: not-latched input undervoltage (brownout), output OVP (auto-restart or latch-mode selectable), a first-level OCP with delayed shutdown to protect the system during overload or short circuit conditions (auto-restart or latch-mode selectable) and a second-level OCP that is invoked when the transformer saturates or the secondary diode fails short. A latched disable input allows easy implementation of OTP with an external NTC, while an internal thermal shutdown prevents IC overheating.

Programmable soft-start, leading-edge blanking on the current sense input for greater noise immunity, slope compensation (in FF mode only), and a shutdown function for externally controlled burst-mode operation or remote ON/OFF control complete the equipment of this device.

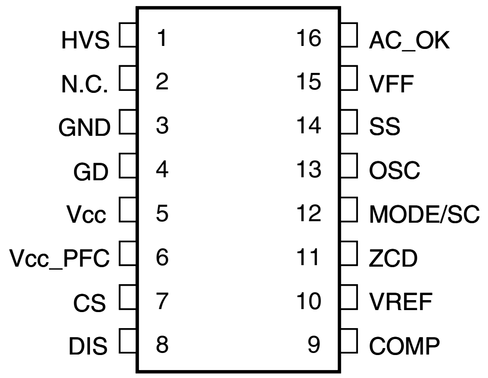
Figure 2. Typical system block diagram



2 Pin settings

2.1 Connections

Figure 3. Pin connection (through top view)



2.2 Pin description

Table 1. Pin functions

N°	Pin	Function
1	HVS	High-voltage start-up. The pin, able to withstand 700 V, is to be tied directly to the rectified mains voltage. A 1 mA internal current source charges the capacitor connected between Vcc pin (5) and GND pin (3) until the voltage on the Vcc pin reaches the turn-on threshold, then it is shut down. Normally, the generator is re-enabled when the Vcc voltage falls below 5 V to ensure a low power throughput during short circuit. Otherwise, when a latched protection is tripped the generator is re-enabled 0.5 V below the turn-on threshold, to keep the latch supplied; or, when the IC is turned off by pin COMP (9) pulled low the generator is active just below the UVLO threshold to allow a faster restart.
2	N.C.	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
3	GND	Ground. Current return for both the signal part of the IC and the gate drive. All of the ground connections of the bias components should be tied to a track going to this pin and kept separate from any pulsed current return.
4	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current capability of 800 mA source/sink.

Table 1. Pin functions (continued)

N°	Pin	Function
5	Vcc	Supply voltage of both the signal part of the IC and the gate driver. The internal high voltage generator charges an electrolytic capacitor connected between this pin and GND (pin 3) as long as the voltage on the pin is below the turn-on threshold of the IC, after that it is disabled and the chip is turned on. The IC is disabled as the voltage on the pin falls below the UVLO threshold. This threshold is reduced at light load to counteract the natural reduction of the self-supply voltage. Sometimes a small bypass capacitor (0.1 µF typ.) to GND might be useful to get a clean bias voltage for the signal part of the IC.
6	Vcc_PFC	Supply pin output. This pin is intended for supplying the PFC controller IC in systems comprising a PFC pre-regulator or other compatible circuitry. It is internally connected to the Vcc pin (5) via a controlled switch. The switch is closed as the IC starts up and opens when the voltage at pin COMP is lower than a threshold (light load), whenever the IC is shut down (either latched or not) and during UVLO. If not used, the pin will be left floating.
7	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal reference to determine MOSFET's turn-off. The pin is equipped with 150 ns min. blanking time after the gate-drive output goes high for improved noise immunity. A second comparison level located at 1.5 V latches the device off and reduces its consumption in case of transformer saturation or secondary diode short circuit. The information is latched until the voltage on the Vcc pin (5) goes below the UVLO threshold, hence resulting in intermittent operation. A logic circuit improves sensitivity to temporary disturbances.
8	DIS	IC's latched disable input. Internally the pin connects a comparator that, when the voltage on the pin exceeds 4.5 V, latches off the IC and brings its consumption to a lower value. The latch is cleared as the voltage on the Vcc pin (5) goes below the UVLO threshold, but the HV generator keeps the Vcc voltage high (see pin 1 description). It is then necessary to recycle the input power to restart the IC. For a quick restart pull pin 16 (AC_OK) below the disable threshold (see pin 16 description). Bypass the pin with a capacitor to GND (pin 3) to reduce noise pick-up. Ground the pin if the function is not used.
9	COMP	Control input for loop regulation. The pin will be driven by the phototransistor (emitter-grounded) of an optocoupler to modulate its voltage by modulating the current sunk. A capacitor placed between the pin and GND (3), as close to the IC as possible to reduce noise pick-up, sets a pole in the output-to-control transfer function. The dynamics of the pin is in the 2.5 to 5 V range. A voltage below an internally defined threshold activates burst-mode operation. The voltage at the pin is bottom-clamped at about 2 V. If the clamp is externally overridden and the voltage is pulled below 1.4 V the IC will shut down.
10	VREF	An internal generator furnishes an accurate voltage reference (5 V ± 2 %) that can be used to supply few mA to an external circuit. A small film capacitor (0.1 µF typ.), connected between this pin and GND (3), is recommended to ensure the stability of the generator and to prevent noise from affecting the reference. This reference is internally monitored by a separate auxiliary reference and any failure or drift will cause the IC to latch off.

Table 1. Pin functions (continued)

N°	Pin	Function
11	ZCD	Transformer demagnetization sensing input for quasi-resonant operation and OVP input. The pin is externally connected to the transformer's auxiliary winding through a resistor divider. A negative-going edge triggers MOSFET's turn-on if QR mode is selected. A voltage exceeding 5 V shuts the IC down and brings its consumption to a lower value (OVP). Latch-off or auto-restart mode is selectable externally. This function is strobed and digitally filtered to increase noise immunity.
12	MODE/SC	Operating mode selection. If the pin is connected to the VREF pin (7) quasi-resonant operation is selected and the oscillator (pin 13, OSC) determines the maximum allowed operating frequency. Fixed-frequency operation is selected if the pin is not tied to VREF, in which case the oscillator determines the actual operating frequency, the maximum allowed duty cycle is set at 70 % min. and the pin delivers a voltage ramp synchronized to the oscillator when the gate-drive output is high; the voltage delivered is zero while the gate-drive output is low. The pin is to be connected to pin CS (7) via a resistor for slope compensation.
13	OSC	Oscillator pin. The pin is an accurate 1 V voltage source, and a resistor connected from the pin to GND (pin 3) defines a current. This current is internally used to set the oscillator frequency that defines the maximum allowed switching frequency of the L6566A, if working in QR mode, or the operating switching frequency if working in FF mode.
14	SS	Soft-start current source. At start-up a capacitor Css between this pin and GND (pin 3) is charged with an internal current generator. During the ramp, the internal reference clamp on the current sense pin (7, CS) rises linearly starting from zero to its final value, thus causing the duty cycle to increase progressively starting from zero as well. During soft-start the adaptive UVLO function and all functions monitoring pin COMP are disabled. The soft-start capacitor is discharged whenever the supply voltage of the IC falls below the UVLO threshold. The same capacitor is used to delay IC's shutdown (latch-off or auto-restart mode selectable) after detecting an overload condition (OLP).
15	VFF	Line voltage feedforward input. The information on the converter's input voltage is fed into the pin through a resistor divider and is used to change the setpoint of the pulse-by-pulse current limitation (the higher the voltage, the lower the setpoint). The linear dynamics of the pin ranges from 0 to 3 V. A voltage higher than 3 V makes the IC stop switching. If feedforward is not desired, tie the pin to GND (pin 3) directly if a latch-mode OVP is not required (see pin 11, ZCD) or through a resistor if a latch-mode OVP is required. Bypass the pin with a capacitor to GND (pin 3) to reduce noise pick-up.
16	AC_OK	Brownout protection input. A voltage below 0.45 V shuts down (not latched) the IC, lowers its consumption, opens the Vcc_PFC pin (6), and clears the latch set by latched protections (DIS > 4.5 V, SS > 6.4 V, VFF > 6.4 V). IC's operation is re-enabled as the voltage exceeds 0.45 V. The comparator is provided with current hysteresis: an internal 15 µA current generator is ON as long as the voltage on the pin is below 0.45V and is OFF if this value is exceeded. Bypass the pin with a capacitor to GND (pin 3) to reduce noise pick-up. Tie to Vcc with a 220 to 680 kΩ resistor if the function is not used.

3 Electrical data

3.1 Maximum rating

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{HVS}	1	Voltage range (referred to ground)	-0.3 to 700	V
I_{HVS}	1	Start-up current	Self-limited	
V_{CC}	5	IC supply voltage (Icc = 20 mA)	Self-limited	
V_{Vcc_PFC}	6	Voltage range	-0.3 to Vcc	V
I_{Vcc_PFC}	6	Max. source current (continuous)	30	mA
V_{max}	7, 8, 10, 14	Analog inputs and outputs	-0.3 to 7	V
V_{max}	9, 15, 16	Maximum pin voltage (Ipin ≤ 1 mA)	Self-limited	
I_{ZCD}	11	Zero current detector max. current	±5	mA
$V_{MODE/SC}$	12	Voltage range	-0.3 to 5.3	V
V_{OSC}	13	Voltage range	-0.3 to 3.3	V
P_{TOT}		Power dissipation @T_A = 50 °C	0.75	W
T_{STG}		Storage temperature	-55 to 150	°C
T_J		Junction operating temperature range	-40 to 150	°C

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	120	°C/W

4 Electrical characteristics

(T_J = -25 to 125 °C, V_{CC} = 12 V, C_O = 1 nF; MODE/SC = V_{REF}, R_T = 20 kΩ from OSC to GND, unless otherwise specified).

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Supply voltage						
Vcc	Operating range after turn-on	$V_{COMP} > V_{COMPL}$	10.6		23	V
		$V_{COMP} = V_{COMPO}$	8		23	
Vcc_{On}	Turn-on threshold	(1)	13	14	15	V
Vcc_{Off}	Turn-off threshold	(1) $V_{COMP} > V_{COMPL}$	9.4	10	10.6	V
		(1) $V_{COMP} = V_{COMPO}$	7.2	7.6	8.0	
Hys	Hysteresis	$V_{COMP} > V_{COMPL}$		4		V
V_Z	Zener voltage	Icc = 20 mA, IC disabled	23	25	27	V
Supply current						
$I_{start-up}$	Start-up current	Before turn-on, Vcc = 13 V		200	250	µA
I_q	Quiescent current	After turn-on, $V_{ZCD} = V_{CS}$ = 1 V		2.6	2.8	mA
Icc	Operating supply current	MODE/SC open		4	4.6	mA
I_{qdis}	Quiescent current	IC disabled (2)	330		2500	µA
		IC latched off		440	500	
High-voltage start-up generator						
V_{HV}	Breakdown voltage	I_{HV} < 100 µA	700			V
$V_{HVstart}$	Start voltage	I_{Vcc} < 100 µA	65	80	100	V
I_{charge}	Vcc charge current	$V_{HV} > V_{Hvstart}$, Vcc > 3 V	0.55	0.85	1	mA
$I_{HV, ON}$	ON-state current	$V_{HV} > V_{Hvstart}$, Vcc > 3 V			1.6	mA
		$V_{HV} > V_{Hvstart}$, Vcc = 0			0.8	
$I_{HV, OFF}$	OFF-state leakage current	V_{HV} = 400 V			40	µA
$V_{CCrestart}$	Vcc restart voltage	Vcc falling	4.4	5	5.6	V
		(1) IC latched off	12.5	13.5	14.5	
		(1) Disabled by $V_{COMP} < V_{COMPOFF}$	9.4	10	10.6	

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Reference voltage						
V_{REF}	Output voltage	[(1)] T_J = 25 °C; I_{REF} = 1 mA	4.95	5	5.05	V
V_{REF}	Total variation	I_{REF} = 1 to 5 mA, Vcc = 10.6 to 23 V	4.9		5.1	V
I_{REF}	Short circuit current	V_{REF} = 0	10		30	mA
	Sink capability in UVLO	Vcc = 6 V; Isink = 0.5 mA		0.2	0.5	V
V_{OV}	Overvoltage threshold		5.3	5.7		V
Internal oscillator						
f_{sw}	Oscillation frequency	Operating range	10		300	kHz
		T_J = 25 °C, V_{ZCD} = 0, MODE/SC = Open	95	100	105	
		Vcc=12 to 23 V, V_{ZCD} = 0, MODE/SC = Open	93	100	107	
V_{OSC}	Voltage reference	[(3)]	0.97	1	1.03	V
D_{max}	Maximum duty cycle	MODE/SC = Open, V_{COMP} = 5 V	70		75	%
Brownout protection						
Vth	Threshold voltage	Voltage falling (turn-off)	0.432	0.450	0.468	V
		Voltage rising (turn-on)	0.452	0.458	0.518	V
I_{Hys}	Current hysteresis	Vcc > 5 V, V_{VFF} = 0.3 V	12	15	18	µA
$V_{AC\_OK\_CL}$	Clamp level	[(1)] I_{AC_OK} = 100 µA	3	3.15	3.3	V
Line voltage feedforward						
I_{VFF}	Input bias current	V_{VFF} = 0 to 3 V, $V_{ZCD} < V_{ZCDth}$			-1	µA
		$V_{ZCD} > V_{ZCDth}$	-0.7	-1		mA
V_{VFF}	Linear operation range			0 to 3		V
V_{OFF}	IC disable voltage		3	3.15	3.3	V
$V_{VFFlatch}$	Latch-off/clamp level	$V_{ZCD} > V_{ZCDth}$		6.4		V
Kc	Control voltage gain [(3)]	V_{VFF} = 1 V, V_{COMP} = 4 V		0.4		V/V
K_{FF}	Feedforward gain [(3)]	V_{VFF} = 1 V, V_{COMP} = 4 V		0.04		V/V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Current sense comparator						
I_{CS}	Input bias current	$V_{CS} = 0$			-1	µA
t_{LEB}	Leading edge blanking		150	250	300	ns
$td_{(H-L)}$	Delay to output				100	ns
V_{CSx}	Overcurrent setpoint	$V_{COMP} = V_{COMPHI}$, $V_{VFF} = 0$ V	0.92	1	1.08	V
		$V_{COMP} = V_{COMPHI}$, $V_{VFF} = 1.5$ V	0.45	0.5	0.55	
		$V_{COMP} = V_{COMPHI}$, $V_{VFF} = 3.0$ V		0	0.1	
V_{CSdis}	Hiccup-mode OCP level	(1)	1.4	1.5	1.6	V
PWM control						
V_{COMPHI}	Upper clamp voltage	$I_{COMP} = 0$		5.7		V
V_{COMPLO}	Lower clamp voltage	$I_{SOURCE} = -1$ mA		2.0		V
V_{COMPSH}	Linear dynamics upper limit	(1) $V_{VFF} = 0$ V	4.8	5	5.2	V
I_{COMP}	Max. source current	$V_{COMP} = 3.3$ V	320	400	480	µA
R_{COMP}	Dynamic resistance	$V_{COMP} = 2.6$ to 4.8 V		25		kΩ
V_{COMPBM}	Burst-mode threshold	(1)	2.52	2.65	2.78	V
		(1) MODE/SC = Open	2.7	2.85	3	
Hys	Burst-mode hysteresis			20		mV
I_{CLAMPL}	Lower clamp capability	$V_{COMP} = 2$ V	-3.5		-1.5	mA
$V_{COMPOFF}$	Disable threshold	Voltage falling		1.4		V
Zero current detector/ overvoltage protection						
V_{ZCDH}	Upper clamp voltage	$I_{ZCD} = 3$ mA	5.4	5.7	6	V
V_{ZCDL}	Lower clamp voltage	$I_{ZCD} = -3$ mA		-0.4		V
V_{ZCDA}	Arming voltage	(1) positive-going edge	85	100	115	mV
V_{ZCDT}	Triggering voltage	(1) negative-going edge	30	50	70	mV
I_{ZCD}	Internal pull-up	$V_{COMP} < V_{COMPSH}$			-1	µA
		VZCD < 2 V, $V_{COMP} = V_{COMPHI}$	-130	-100	-70	
I_{ZCDsrc}	Source current capability	$V_{ZCD} = V_{ZCDL}$	-3			mA
I_{ZCDsnk}	Sink current capability	$V_{ZCD} = V_{ZCDH}$	3			mA
T_{BLANK1}	Turn-on inhibit time	After gate-drive going low		2.5		µs
V_{ZCDth}	OVP threshold		4.85	5	5.15	V
T_{BLANK2}	OVP strobe delay	After gate-drive going low		2		µs

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Latched shutdown function						
I_{OTP}	Input bias current	V_{DIS} = 0 to V_{OTP}			-1	µA
V_{OTP}	Disable threshold	(1)	4.32	4.5	4.68	V
Thermal shutdown						
Vth	Shutdown threshold			180		°C
Hys	Hysteresis			40		°C
V_{CC}_PFC function						
I_{leak}	OFF-state leakage current	V_{COMP} = 2.5 V, V_{Vcc_PFC} = 0			1	µA
V_{Vcc} - V_{Vcc_PFC}	ON-state voltage dropout	V_{COMP} = 4 V, I_{VCC_PFC} = 10 mA		0.15	0.3	V
V_{COMPO}	Level for pin 6 open and lower UVLO off threshold (COMP voltage falling)	(3)	2.61	2.75	2.89	V
		(3) MODE/SC = Open	3.02	3.15	3.28	
V_{COMPL}	Level for pin 6 closed and higher UVLO off threshold (COMP voltage rising)	(3)	2.9	3.05	3.2	V
		(3) MODE/SC = Open	3.41	3.55	3.69	
T_{delay}	Pin 6 change of state delay	Closed-to-open		10		ms
Mode selection / slope compensation						
$MODE_{th}$	Threshold for QR operation			3		V
SC_{pk}	Ramp peak (MODE/SC = Open)	$R_{S\text{-}COMP}$ = 3 kΩ to GND, GD pin high, V_{COMP} = 5 V		1.7		V
SC_{vy}	Ramp starting value (MODE/SC = Open)	$R_{S\text{-}COMP}$ = 3 kΩ to GND, GD pin high		0.3		V
	Ramp voltage (MODE/SC = Open)	GD pin low		0		V
	Source capability (MODE/SC = Open)	$V_{S\text{-}COMP} = V_{S\text{-}COMPpk}$	0.8			mA
Soft-start						
I_{SS1}	Charge current	T_J = 25 °C, V_{SS} < 2 V, V_{COMP} = 4 V	14	20	26	µA
I_{SS2}		T_J = 25 °C, V_{SS} > 2 V, $V_{COMP} = V_{COMPHi}$	3.5	5	6.5	
I_{SSdis}	Discharge current	V_{SS} > 2 V	3.5	5	6.5	µA
$V_{SSclamp}$	High saturation voltage	V_{COMP} = 4 V		2		V
V_{SSDIS}	Disable level	(1) $V_{COMP} = V_{COMPHi}$	4.85	5	5.15	V
V_{SSLAT}	Latch-off level	$V_{COMP} = V_{COMPHi}$		6.4		V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Gate driver						
V_{GDH}	Output high voltage	$I_{GDsource}$ = 5 mA, Vcc = 12V	9.8	11		V
V_{GDL}	Output low voltage	I_{GDsink} = 100 mA		0.75		V
$I_{sourcepk}$	Output source peak current		-0.6			A
I_{sinkpk}	Output sink peak current		0.8			A
t_f	Fall time			40		ns
t_r	Rise time			50		ns
$V_{GDclamp}$	Output clamp voltage	$I_{GDsource}$ = 5 mA; Vcc = 20 V	10	11.3	15	V
	UVLO saturation	Vcc = 0 to Vccon, Isink = 1 mA		0.9	1.1	V

1. Parameters tracking one another.
2. See *Table 6 on page 41* and *Table 7 on page 42*
3. The voltage feedforward block output is given by: $V_{cs} = Kc\left(V_{COMP} - 2.5\right) - K_{FF} V_{VFF}$

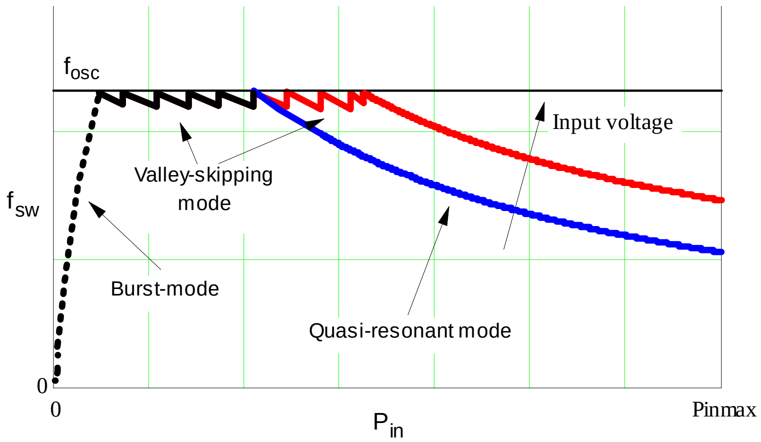
5 Application information

The L6566A is a versatile peak-current-mode PWM controller specific for offline flyback converters. The device allows either fixed-frequency (FF) or quasi-resonant (QR) operation, selectable with the pin MODE/SC (12): forcing the voltage on the pin over 3 V (e.g. by tying it to the 5 V reference externally available at pin VREF, 10) will activate QR operation, otherwise the device will be FF-operated.

Irrespective of the operating option selected by pin 12, the device is able to work in different modes, depending on the converter's load conditions. If QR operation is selected (see *Figure 4*):

1. QR mode at heavy load. Quasi-resonant operation lies in synchronizing MOSFET's turn-on to the transformer's demagnetization by detecting the resulting negative-going edge of the voltage across any winding of the transformer. Then the system works close to the boundary between discontinuous (DCM) and continuous conduction (CCM) of the transformer. As a result, the switching frequency will be different for different line/load conditions (see the hyperbolic-like portion of the curves in *Figure 4*). Minimum turn-on losses, low EMI emission and safe behavior in short circuit are the main benefits of this kind of operation.
2. Valley-skipping mode at medium/ light load. The externally programmable oscillator of the L6566A, synchronized to MOSFET's turn-on, enables the designer to define the maximum operating frequency of the converter. As the load is reduced MOSFET's turn-on will not any more occur on the first valley but on the second one, the third one and so on. In this way the switching frequency will no longer increase (piecewise linear portion in *Figure 4*).
3. Burst-mode with no or very light load. When the load is extremely light or disconnected, the converter will enter a controlled on/off operation with constant peak current. Decreasing the load will then result in frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations or recommendations. Being the peak current very low, no issue of audible noise arises.

Figure 4. Multi-mode operation with QR option active



If FF operation is selected:

1. FF mode from heavy to light load. The system operates exactly like a standard current mode, at a frequency f_{sw} determined by the externally programmable oscillator: both DCM and CCM transformer operation are possible, depending on whether the power that it processes is greater or less than:

Equation 1

$$Pin_T = \frac{\left(\frac{Vin\ V_R}{Vin + V_R}\right)^2}{2\, f_{sw}\, Lp}$$

where Vin is the input voltage to the converter, V_R the reflected voltage (i.e. the regulated output voltage times the primary-to-secondary turn ratio) and Lp the inductance of the primary winding. Pin_T is the power level that marks the transition from continuous to discontinuous operation mode of the transformer.

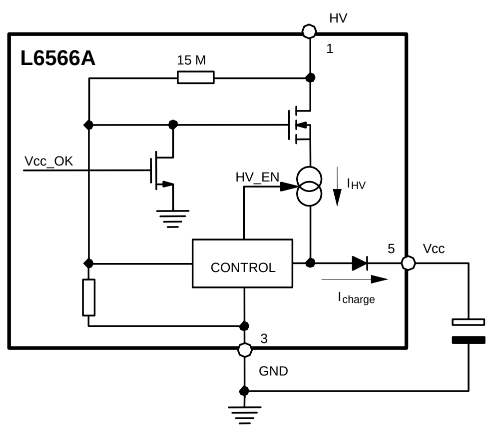
2. Burst-mode with no or very light load. This kind of operation is activated in the same way and results in the same behavior as previously described for QR operation.

The L6566A is specifically designed for flyback converters operated from front-end power factor correction (PFC) stages in applications supposed to comply with EN61000-3-2 or JEITA-MITI regulations. Pin 6 (Vcc_PFC) provides the supply voltage to the PFC control IC.

5.1 High-voltage start-up generator

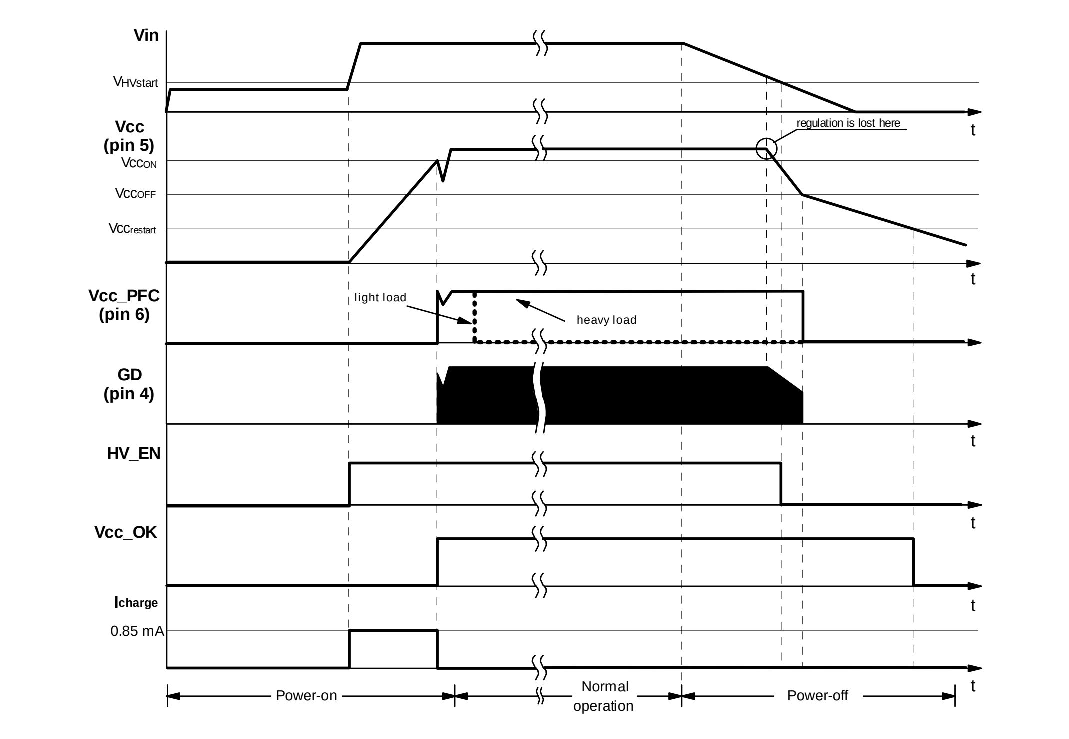
Figure 5 shows the internal schematic of the high-voltage start-up generator (HV generator). It is made up of a high-voltage N-channel FET, whose gate is biased by a 15 MΩ resistor, with a temperature-compensated current generator connected to its source.

Figure 5. High-voltage start-up generator: internal schematic



With reference to the timing diagram of *Figure 6*, when power is first applied to the converter the voltage on the bulk capacitor (Vin) builds up and, at about 80 V, the HV generator is enabled to operate (HV_EN is pulled high) so that it draws about 1 mA. This current, minus the device's consumption, charges the bypass capacitor connected from pin Vcc (5) to ground and makes its voltage rise almost linearly.

Figure 6. Timing diagram: normal power-up and power-down sequences



As the Vcc voltage reaches the start-up threshold (14 V typ.) the low-voltage chip starts operating and the HV generator is cut off by the Vcc_OK signal asserted high. The device is powered by the energy stored in the Vcc capacitor until the self-supply circuit (typically an auxiliary winding of the transformer and a steering diode) develops a voltage high enough to sustain the operation. The residual consumption of this circuit is just the one on the 15 MΩ resistor (≈10 mW at 400 Vdc), typically 50-70 times lower, under the same conditions, as compared to a standard start-up circuit made with external dropping resistors.

At converter power-down the system will lose regulation as soon as the input voltage is so low that either peak current or maximum duty cycle limitation is tripped. Vcc will then drop and stop IC activity as it falls below the UVLO threshold (10 V typ.). The Vcc_OK signal is de-asserted as the Vcc voltage goes below a threshold $Vcc_{restart}$ located at about 5 V. The HV generator can now restart. However, if $Vin < Vin_{start}$, as illustrated in *Figure 6*, HV_EN is de-asserted too and the HV generator is disabled. This prevents converter's restart attempts and ensures monotonic output voltage decay at power-down in systems where brownout protection (see the relevant section) is not used.

The low restart threshold $Vcc_{restart}$ ensures that, during short circuits, the restart attempts of the device will have a very low repetition rate, as shown in the timing diagram of *Figure 7 on page 20*, and that the converter will work safely with extremely low power throughput.

Figure 7. Timing diagram showing short-circuit behavior (SS pin clamped at 5 V)

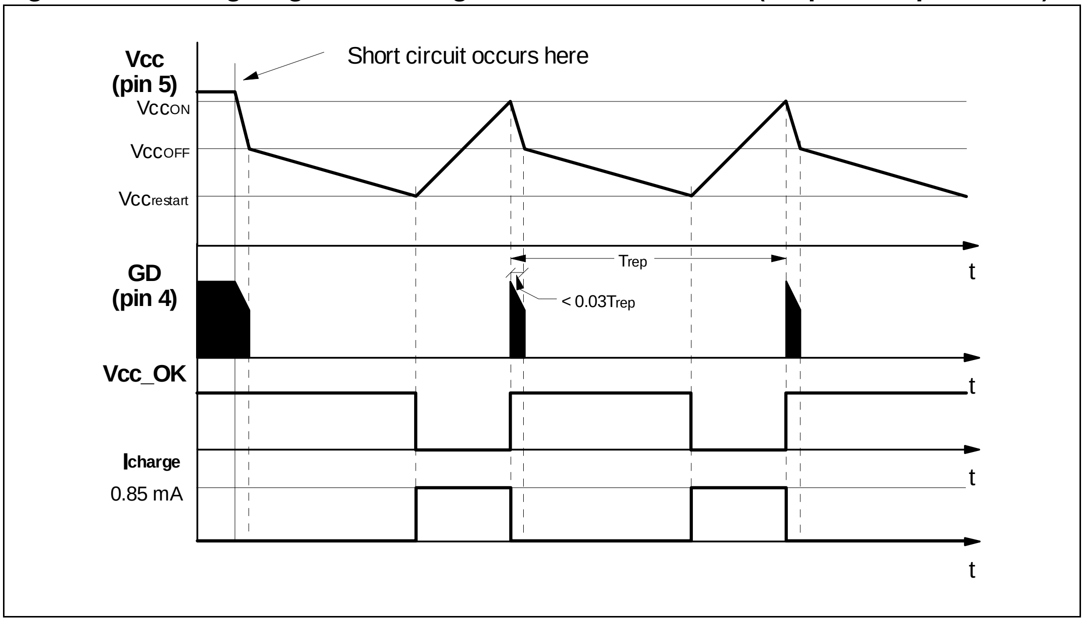
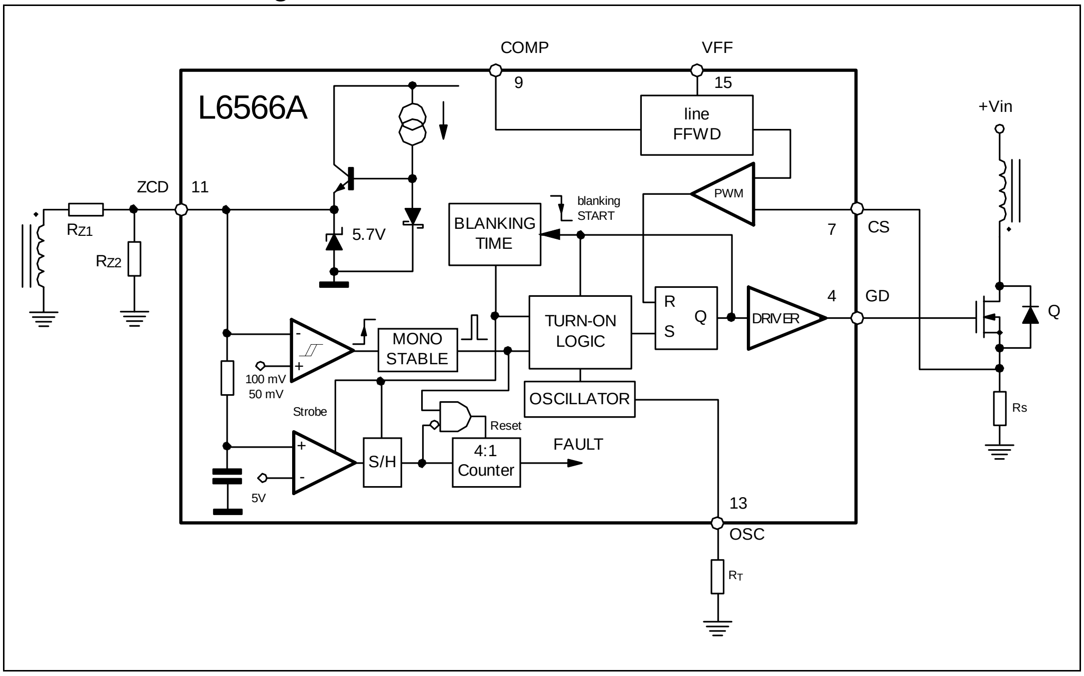


Figure 8. Zero current detection block, triggering block, oscillator block and related logic



5.2 Zero current detection and triggering block; oscillator block

The zero current detection (ZCD) and Triggering blocks switch on the external MOSFET if a negative-going edge falling below 50 mV is applied to the input (pin 11, ZCD). To do so the triggering block must be previously armed by a positive-going edge exceeding 100 mV.

This feature is typically used to detect transformer demagnetization for QR operation, where the signal for the ZCD input is obtained from the transformer's auxiliary winding used also to supply the L6566A. The triggering block is blanked for T_{BLANK} = 2.5 µs after MOSFET's turn-off to prevent any negative-going edge that follows leakage inductance demagnetization from triggering the ZCD circuit erroneously.

The voltage at the pin is both top and bottom limited by a double clamp, as illustrated in the internal diagram of the ZCD block of *Figure 8 on page 20*. The upper clamp is typically located at 5.7 V, while the lower clamp is located at -0.4 V. The interface between the pin and the auxiliary winding will be a resistor divider. Its resistance ratio will be properly chosen (see "*Section 5.11: OVP block on page 35*") and the individual resistance values (R_{Z1}, R_{Z2}) will be such that the current sourced and sunk by the pin be within the rated capability of the internal clamps (±3 mA).

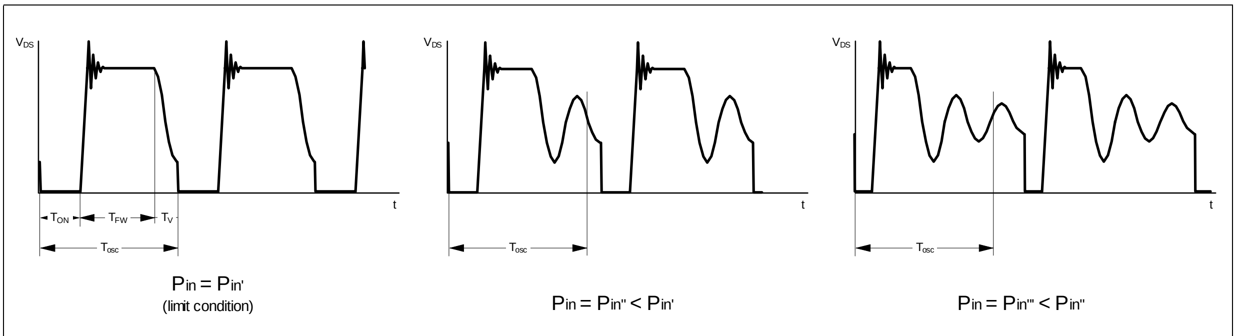
At converter power-up, when no signal is coming from the ZCD pin, the oscillator starts up the system. The oscillator is programmed externally by means of a resistor (R_T) connected from pin OSC (13) to ground. With good approximation the oscillation frequency f_{osc} will be:

Equation 2

$$f_{osc} \approx \frac{2 \cdot 10^3}{R_T}$$

(with f_{osc} in kHz and R_T in kW). As the device is turned on, the oscillator starts immediately; at the end of the first oscillator cycle, being zero the voltage on the ZCD pin, the MOSFET will be turned on, thus starting the first switching cycle right at the beginning of the second oscillator cycle. At any switching cycle, the MOSFET is turned off as the voltage on the current sense pin (CS, 7) hits an internal reference set by the line feedforward block, and the transformer starts demagnetization. If this completes (hence a negative-going edge appears on the ZCD pin) after a time exceeding one oscillation period T_{osc}=1/f_{osc} from the previous turn-on, the MOSFET will be turned on again - with some delay to ensure minimum voltage at turn-on – and the oscillator ramp will be reset. If, instead, the negative-going edge appears before T_{osc} has elapsed, it will be ignored and only the first negative-going edge after T_{osc} will turn-on the MOSFET and synchronize the oscillator. In this way one or more drain ringing cycles will be skipped ("valley-skipping mode", *Figure 9*) and the switching frequency will be prevented from exceeding f_{osc}.

Figure 9. Drain ringing cycle skipping as the load is gradually reduced



Note: When the system operates in valley skipping-mode, uneven switching cycles may be observed under some line/load conditions, due to the fact that the OFF-time of the MOSFET is allowed to change with discrete steps of one ringing cycle, while the OFF-time needed for cycle-by-cycle energy balance may fall in between. Thus one or more longer switching cycles will be compensated by one or more shorter cycles and vice versa. However, this mechanism is absolutely normal and there is no appreciable effect on the performance of the converter or on its output voltage.

If the MOSFET is enabled to turn on but the amplitude of the signal on the ZCD pin is smaller than the arming threshold for some reason (e.g. a heavy damping of drain oscillations, like in some single-stage PFC topologies, or when a turn-off snubber is used), MOSFET's turn-on cannot be triggered. This case is identical to what happens at start-up: at the end of the next oscillator cycle the MOSFET will be turned on, and a new switching cycle will take place after skipping no more than one oscillator cycle.

The operation described so far does not consider the blanking time T_{BLANK} after MOSFET's turn off, and actually T_{BLANK} does not come into play as long as the following condition is met:

Equation 3

$$D \leq 1 - \frac{T_{BLANK}}{T_{osc}}$$

where D is the MOSFET duty cycle. If this condition is not met, things do not change substantially: the time during which MOSFET's turn-on is inhibited is extended beyond T_{osc} by a fraction of T_{BLANK}. As a consequence, the maximum switching frequency will be a little lower than the programmed value f_{osc} and valley-skipping mode may take place slightly earlier than expected. However this is quite unusual: setting f_{osc} = 150 kHz, the phenomenon can be observed at duty cycles higher than 60 %. See *Section 5.11: OVP block on page 35* for further implications of T_{BLANK}.

If the voltage on the COMP pin (9) saturates high, which reveals an open control loop, an internal pull-up keeps the ZCD pin close to 2 V during MOSFET's OFF-time to prevent noise from false triggering the detection block. When this pull-up is active, the ZCD pin might not be able to go below the triggering threshold, which would stop the converter. To allow auto-restart operation, however ensuring minimum operating frequency in these conditions, the oscillator frequency that retriggers MOSFET's turn-on is that of the external oscillator divided by 128. Additionally, to prevent malfunction at converter's start-up, the pull-up is disabled during the initial soft-start (see the relevant section). However, to ensure a correct start-up, at the end of the soft-start phase the output voltage of the converter must meet the condition:

Equation 4

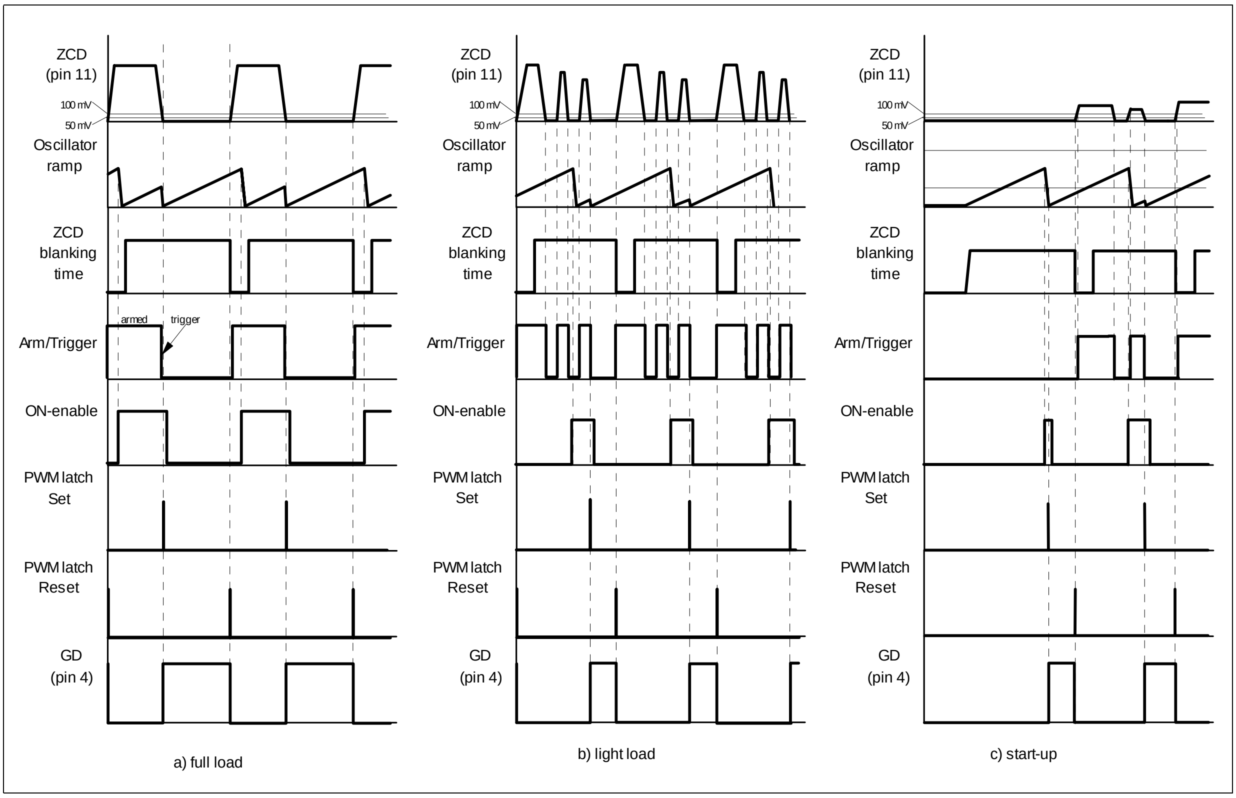
$$Vout > \frac{Ns}{Naux} R_{Z1} I_{ZCD}$$

where Ns is the turn number of the secondary winding, Naux the turn number of the auxiliary winding and I_{ZCD} the maximum pull-up current (130 µA).

The operation described so far under different operating conditions for the converter is illustrated in the timing diagrams of *Figure 10*.

If the FF option is selected the operation will be exactly equal to that of a standard current-mode PWM controller. It will work at a frequency fsw = fosc; both DCM and CCM transformer's operation are possible, depending on the operating conditions (input voltage and output load) and on the design of the power stage. The MOSFET is turned on at the beginning of each oscillator cycle and is turned off as the voltage on the current sense pin reaches an internal reference set by the Line Feedforward block. The maximum duty cycle is limited at 70 % minimum. The signal on the ZCD pin in this case is used only for detecting feedback loop failures (see *Section 5.11: OVP block on page 35*).

Figure 10. Operation of ZCD, triggering and oscillator blocks (QR option active)



5.3 Burst-mode operation at no load or very light load

When the voltage at the COMP pin (9) falls 20 mV below a threshold fixed internally at a value, V_{COMPBM}, depending on the selected operating mode, the L6566A is disabled with the MOSFET kept in OFF state and its consumption reduced at a lower value to minimize Vcc capacitor discharge.

The control voltage now will increase as a result of the feedback reaction to the energy delivery stop (the output voltage will be slowly decaying), the threshold will be exceeded and the device will restart switching again. In this way the converter will work in burst-mode with a nearly constant peak current defined by the internal disable level. A load decrease will then cause a frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations. This kind of operation, shown in the timing diagrams of *Figure 11* along with the others previously described, is noise-free since the peak current is low.

If it is necessary to decrease the intervention threshold of the burst-mode operation, this can be done by adding a small DC offset on the current sense pin as shown in *Figure 12 on page 25*.

Note: The offset reduces the available dynamics of the current signal; thereby, the value of the sense resistor must be determined taking this offset into account.

Figure 11. Load-dependent operating modes: timing diagrams

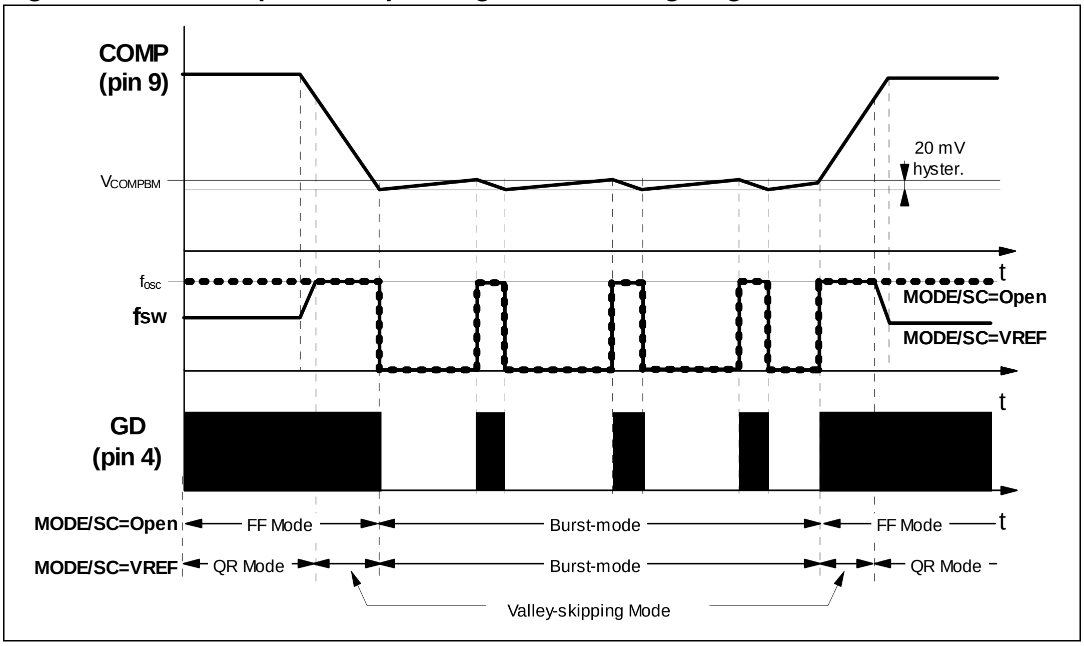
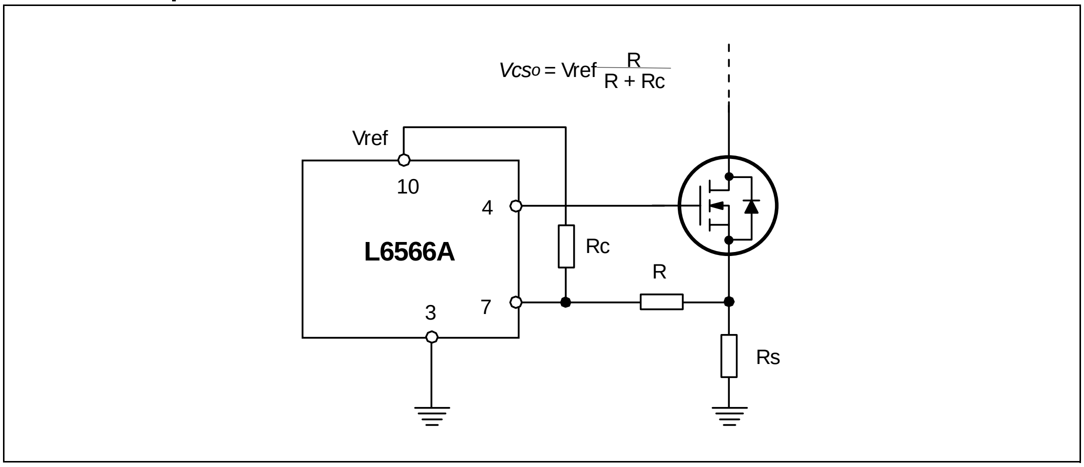


Figure 12. Addition of an offset to the current sense lowers the burst-mode operation threshold

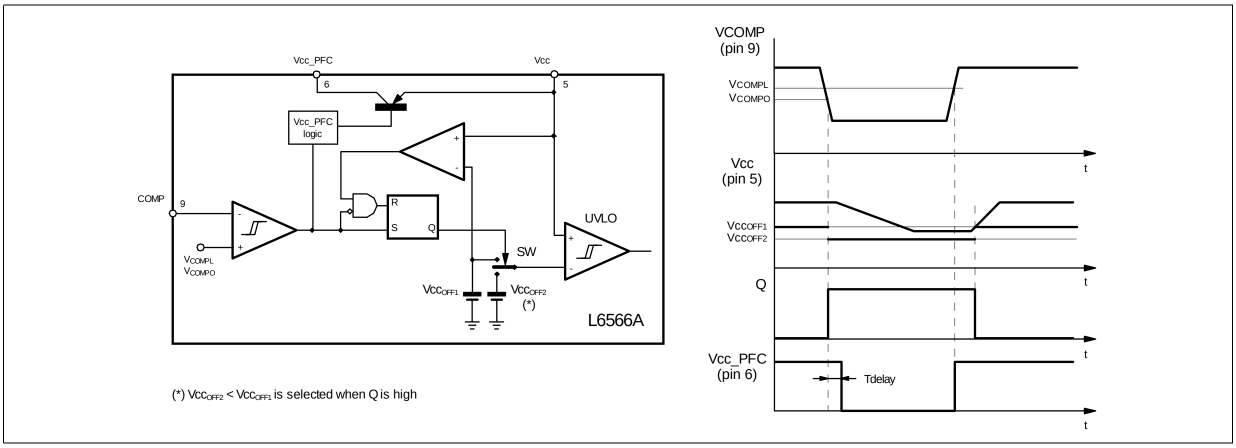


5.4 Adaptive UVLO

A major problem when optimizing a converter for minimum no-load consumption is that the voltage generated by the auxiliary winding under these conditions falls considerably as compared even to a few mA load. This very often causes the supply voltage Vcc of the control IC to drop and go below the UVLO threshold so that the operation becomes intermittent, which is undesired. Furthermore, this must be traded off against the need of generating a voltage not exceeding the maximum allowed by the control IC at full load.

To help the designer overcome this problem, the device, besides reducing its own consumption during burst-mode operation, also features a proprietary adaptive UVLO function. It consists of shifting the UVLO threshold downwards at light load, namely when the voltage at pin COMP falls below a threshold V_{COMPO} internally fixed (see "PFC Interface"), so as to have more headroom. To prevent any malfunction during transients from minimum to maximum load the normal (higher) UVLO threshold is re-established when the voltage at pin COMP exceeds V_{COMPL} (see "*Chapter 5.8: PFC interface on page 31*") and Vcc has exceeded the normal UVLO threshold (see *Figure 13*). The normal UVLO threshold ensures that at full load the MOSFET will be driven with a proper gate-to-source voltage.

Figure 13. Adaptive UVLO block



5.5 PWM control block

The device is specific for secondary feedback. Typically, there is a TL431 on the secondary side and an optocoupler that transfers output voltage information to the PWM control on the primary side, crossing the isolation barrier. The PWM control input (pin 9, COMP) is driven directly by the phototransistor's collector (the emitter is grounded to GND) to modulate the duty cycle (*Figure 14*, left-hand side circuit).

In applications where a tight output regulation is not required, it is possible to use a primary-sensing feedback technique. In this approach the voltage generated by the self-supply winding is sensed and regulated. This solution, shown in *Figure 14*, right-hand side circuit, is cheaper because no optocoupler or secondary reference is needed, but output voltage regulation, especially as a result of load changes, is quite poor. Ideally, the voltage generated by the self-supply winding and the output voltage should be related by the Naux/Ns turn ratio only. Actually, numerous non-idealities, mainly transformer's parasitics, cause the actual ratio to deviate from the ideal one. Line regulation is quite good, in the range of ± 2 %, whereas load regulation is about ±5 % and output voltage tolerance is in the range of ±10 %.

The dynamics of the pin is in the 2.5 to 5 V range. The voltage at the pin is clamped downwards at about 2 V. If the clamp is externally overridden and the voltage on the pin is pulled below 1.4 V the L6566A will shut down. This condition is latched as long as the device is supplied. While the device is disabled, however, no energy is coming from the self-supply circuit, thus the voltage on the Vcc capacitor will decay and cross the UVLO threshold after some time, which clears the latch and lets the HV generator restart. This function is intended for an externally controlled burst-mode operation at light load with a reduced output voltage, a technique typically used in multi-output SMPS, such as those for CRT TVs or monitors (see the timing diagram *Figure 15 on page 27*).

Figure 14. Possible feedback configurations that can be used with the L6566A

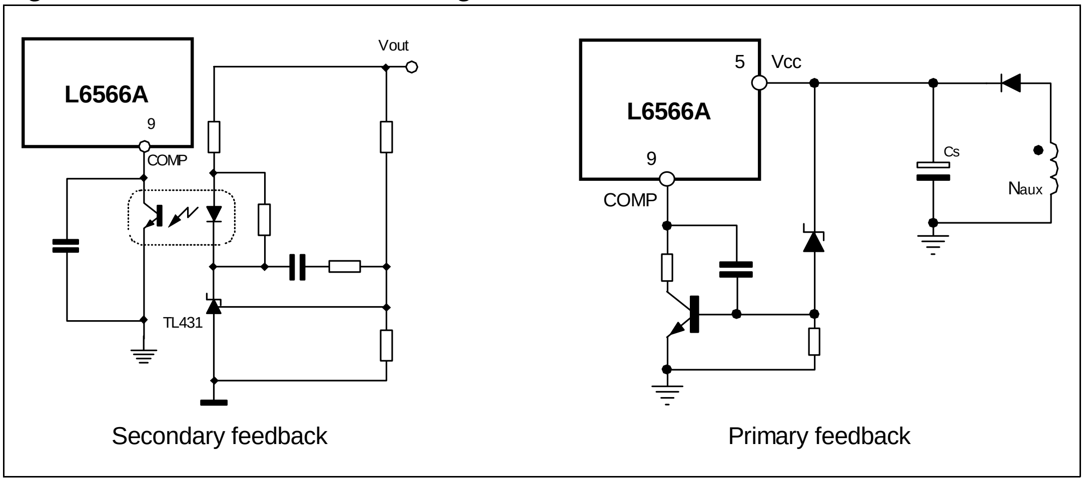
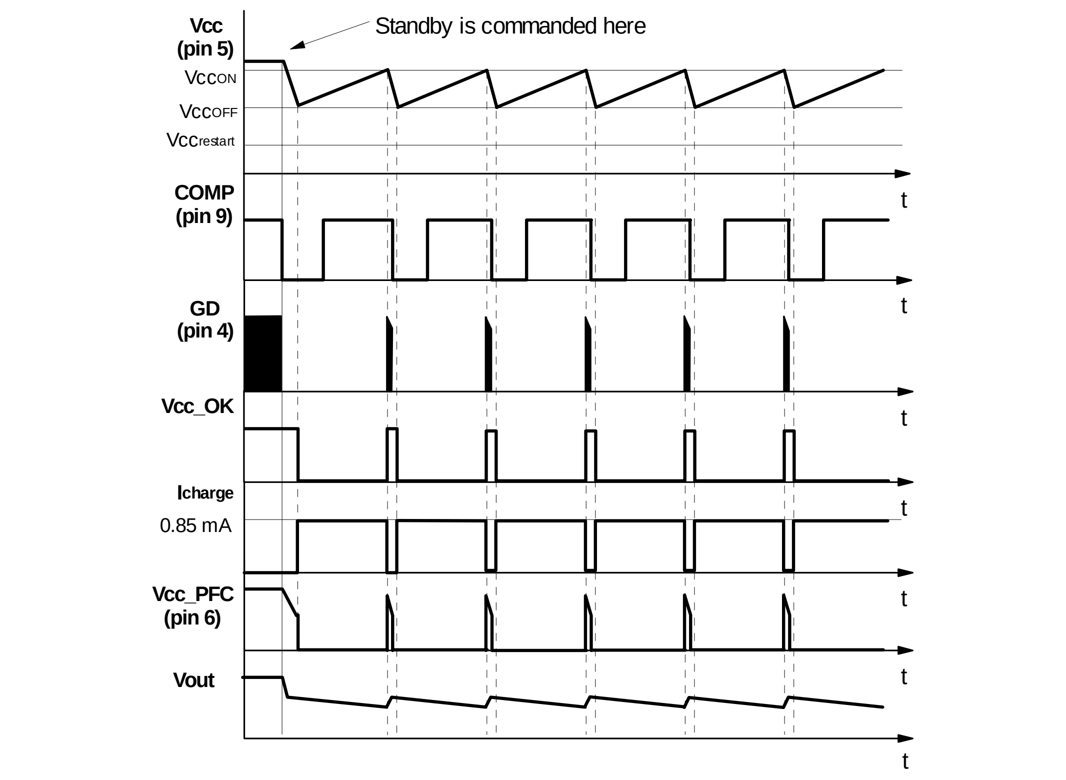


Figure 15. Externally controlled burst-mode operation by driving pin COMP: timing diagram



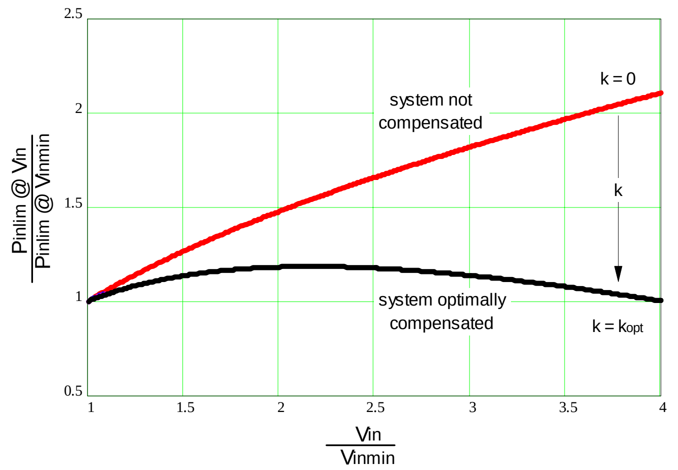
5.6 PWM comparator, PWM latch and voltage feedforward blocks

The PWM comparator senses the voltage across the current sense resistor Rs and, by comparing it to the programming signal delivered by the feedforward block, determines the exact time when the external MOSFET is to be switched off. Its output resets the PWM latch, previously set by the oscillator or the ZCD triggering block, which will assert the gate driver output low. The use of PWM latch avoids spurious switching of the MOSFET that might result from the noise generated ("double-pulse suppression").

Cycle-by-cycle current limitation is realized with a second comparator (OCP comparator) that senses the voltage across the current sense resistor Rs as well and compares this voltage to a reference value V_{CSX}. Its output is or-ed with that of the PWM comparator (see the circuit schematic in *Figure 17 on page 29*). In this way, if the programming signal delivered by the feedforward block and sent to the PWM comparator exceeds V_{CSX}, it will be the OCP comparator to reset first the PWM latch instead of the PWM comparator. The value of Vcsx, thereby, determines the overcurrent setpoint along with the sense resistor Rs.

The power that QR flyback converters with a fixed overcurrent setpoint (like fixed-frequency systems) are able to deliver changes with the input voltage considerably. Obviously, this is not a problem if the flyback converter runs off a fixed voltage bus generated by the PFC pre-regulator; however, with a tracking boost PFC (a "boost follower" PFC), the regulated output voltage at maximum mains voltage can be even twice the value at minimum mains voltage. In this case the issue is still there, although not as big as without PFC and wide-range mains. With a 1:2 voltage change, the maximum transferable power at maximum line can be 50 % higher than at minimum line, as shown by the upper curve in the diagram of *Figure 16*. The L6566A has the line feedforward function available to solve this issue.

Figure 16. Typical power capability change vs input voltage in QR flyback converters



It acts on the overcurrent setpoint V_{csx}, so that it is a function of the converter's input voltage Vin (output of the PFC pre-regulator) sensed through a dedicated pin (15, VFF): the higher the input voltage, the lower the setpoint. This is illustrated in the diagram on the left-hand side of *Figure 17 on page 29*: it shows the relationship between the voltage on the pin VFF and V_{csx} (with the error amplifier saturated high in the attempt of keeping output voltage regulation):

Equation 5

$$V_{csx} = 1 - \frac{V_{VFF}}{3} = 1 - \frac{k}{3} Vin$$

Note: If the voltage on the pin exceeds 3 V switching ceases but the soft-start capacitor is not discharged. The schematic in Figure 17 on page 29 shows also how the function is included in the control loop.

With a proper selection of the external divider R1-R2, i.e. of the ratio k = R2 / (R1+R2), it is possible to achieve the optimum compensation described by the lower curve in the diagram of *Figure 16*.

The optimum value of k, k_{opt}, which minimizes the power capability variation over the input voltage range, is the one that provides equal power capability at the extremes of the range. The exact calculation is complex, and non-idealities shift the real-world optimum value from the theoretical one. It is therefore more practical to provide a first cut value, simple to be calculated, and then to fine tune experimentally.

Assuming that the system operates exactly at the boundary between DCM and CCM, and neglecting propagation delays, the following expression for k_{opt} can be found:

Equation 6

$$k_{opt} = 3 \cdot \frac{V_R}{V_{inmin} \cdot V_{inmax} + (V_{inmin} + V_{inmax}) \cdot V_R}$$

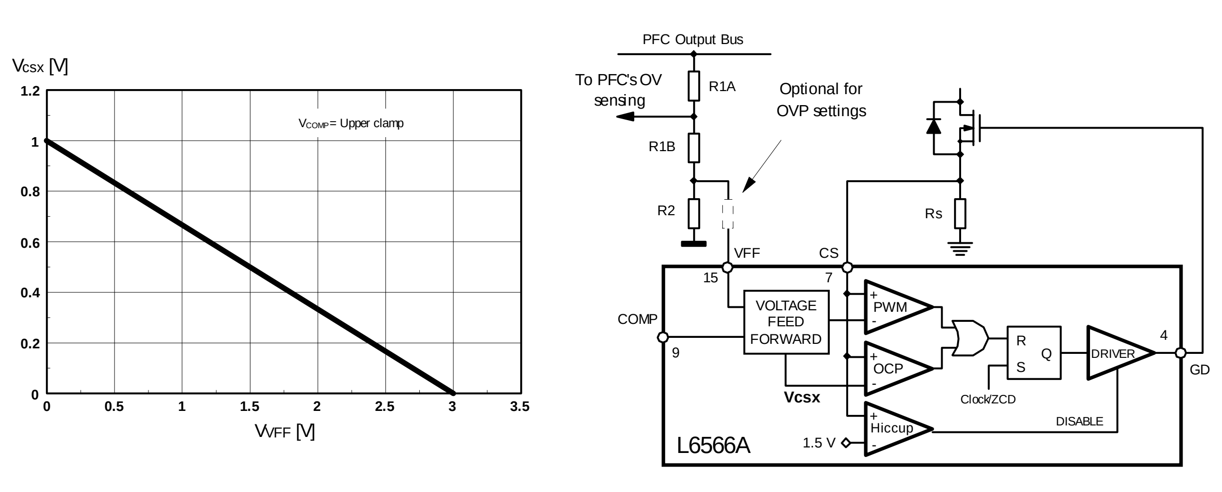
Experience shows that this value is typically lower than the real one. Once the maximum peak primary current, I_{PKpmax}, occurring at minimum input voltage Vinmin has been found, the value of Rs can be determined from (2):

Equation 7

$$Rs = \frac{1 - \frac{k_{opt}}{3} V_{in\,min}}{I_{PKp\,max}}$$

The converter is then tested on the bench to find the output power level $Pout_{lim}$ where regulation is lost (because overcurrent is being tripped) both at Vin = Vin_{min} and Vin = Vin_{max}.

Figure 17. Left: overcurrent setpoint vs VFF voltage; right: line feedforward function block



If $Pout_{lim}$ @ Vin_{max} > $Pout_{lim}$ @ Vin_{min} the system is still undercompensated and k needs increasing; if $Pout_{lim}$ @ Vin_{max} < $Pout_{lim}$ @ Vin_{min} the system is overcompensated and k needs decreasing. This will go on until the difference between the two values is acceptably low. Once found the true k_{opt} in this way, it is possible that $Pout_{lim}$ turns out slightly different from the target; to correct this, the sense resistor Rs needs adjusting and the above tuning process will be repeated with the new Rs value. Typically a satisfactory setting is achieved in no more than a couple of iterations.

In applications where this function is not wanted, e.g. because the PFC stage regulates at a fixed voltage, the VFF pin can be simply grounded, directly or through a resistor (see "*Chapter 5.11: OVP block on page 35*"). The overcurrent setpoint will be then fixed at the maximum value of 1 V. If a lower setpoint is desired to reduce the power dissipation on Rs, the pin can be also biased at a fixed voltage using a divider from VREF (pin 10).

If the FF option is selected the Line Feedforward function can be still used to compensate for the total propagation delay Td of the current sense chain (internal propagation delay $td_{(H-L)}$ plus the turn-off delay of the external MOSFET), which in standard current mode PWM controllers is done by adding an offset on the current sense pin proportional to the input voltage. In that case the divider ratio k, which will be much smaller as compared to that used with the QR option selected, can be calculated with the following equation:

Equation 8

$$k_{opt} = 3\frac{Td}{Rs\,Lp}$$

where Lp is the inductance of the primary winding. In case a constant maximum power capability vs. the input voltage is not required, the VFF pin can be grounded, directly or through a resistor (see *Section 5.11: OVP block on page 35*), hence fixing the overcurrent setpoint at 1 V, or biased at a fixed voltage through a divider from VREF to get a lower setpoint.

It is possible to bypass the pin to ground with a small film capacitor (e.g. 1-10 nF) to ensure a clean operation of the IC even in a noisy environment.

The pin is internally forced to ground during UVLO, after activating any latched protection and when pin COMP is pulled below its low clamp voltage (see *Section 5.5: PWM control block on page 26*).

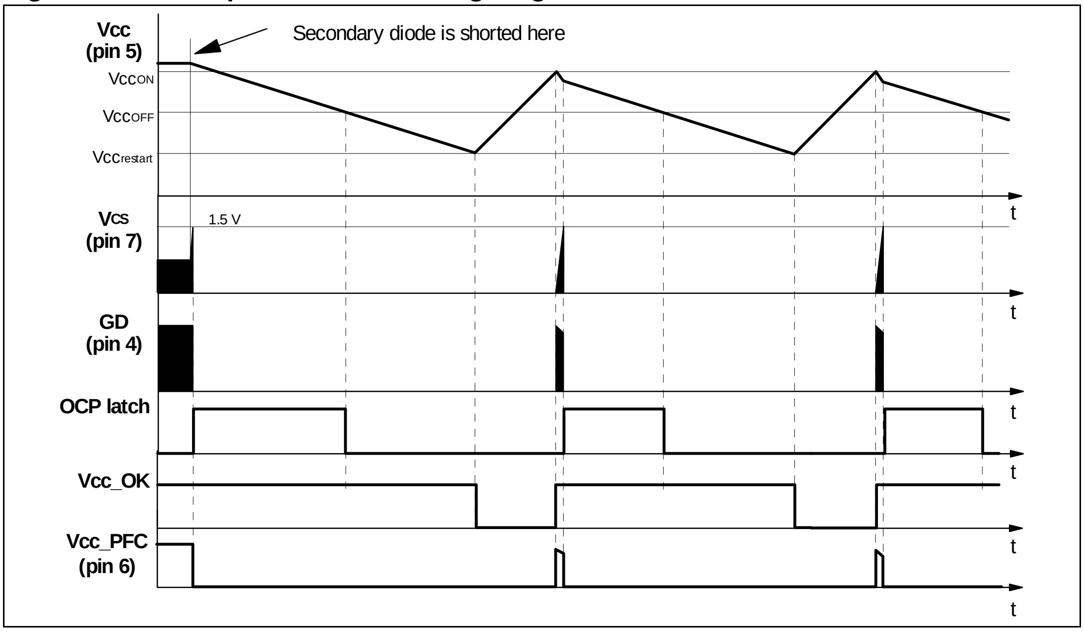
5.7 Hiccup-mode OCP

A third comparator senses the voltage on the current sense input and shuts down the device if the voltage on the pin exceeds 1.5 V, a level well above that of the maximum overcurrent setpoint (1 V). Such an anomalous condition is typically generated by either a short circuit of the secondary rectifier or a shorted secondary winding or a hard-saturated flyback transformer.

To distinguish an actual malfunction from a disturbance (e.g. induced during ESD tests), the first time the comparator is tripped the protection circuit enters a “warning state”. If in the next switching cycle the comparator is not tripped, a temporary disturbance is assumed and the protection logic will be reset in its idle state; if the comparator will be tripped again a real malfunction is assumed and the L6566A will be stopped. Depending on the time relationship between the detected event and the oscillator, occasionally the device could stop after the third detection.

This condition is latched as long as the device is supplied. While it is disabled, however, no energy is coming from the self-supply circuit; hence the voltage on the Vcc capacitor will decay and cross the UVLO threshold after some time, which clears the latch. The internal start-up generator is still off, then the Vcc voltage still needs to go below its restart voltage before the Vcc capacitor is charged again and the device restarted. Ultimately, this will result in a low-frequency intermittent operation (Hiccup-mode operation), with very low stress on the power circuit. This special condition is illustrated in the timing diagram of *Figure 18*.

Figure 18. Hiccup-mode OCP: timing diagram



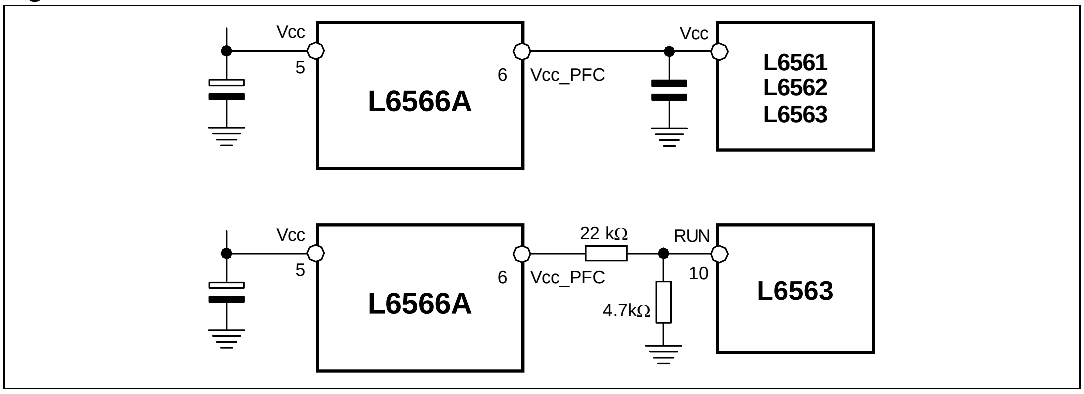
5.8 PFC interface

The device is specifically designed to minimize converter's losses under light or no-load conditions, and a special function has been provided to help the designer meet energy saving requirements even in power-factor-corrected systems where a PFC pre-regulator precedes the isolated DC-DC converter.

Actually EMC regulations require compliance with low-frequency harmonic emission limits at nominal load; no limit is envisaged when the converter operates with a light load. Then the PFC pre-regulator can be turned off, thus saving the no-load consumption of this stage (0.5÷1 W).

To do so, the L6566A provides the Vcc_PFC pin (6): this pin is internally connected to the Vcc pin (5) via a PNP transistor, normally closed, that opens when the voltage V_{COMP} falls below V_{COMPO}, a threshold internally set at a value depending on whether QR operation or FF operation is selected. This pin is intended for supplying the PFC controller of the pre-regulator as shown in *Figure 16 on page 28*. The switch is thermally protected, so that the IC will stop if an external failure causes the pin to be overloaded for too long time or shorted to ground.

Figure 19. Possible interfaces between the L6566A and a PFC controller



To prevent intermittent operation of the PFC stage, some hysteresis is provided: if the internal switch is open, it will be closed (which will re-enable the PFC pre-regulator) when V_{COMP} exceeds $V_{COMPL} > V_{COMPO}$. Additionally, to reject V_{COMP} undershoots during transients V_{COMP} must stay below V_{COMPO} for more than 1024 oscillator cycles in order for the Vcc_PFC pin to open. Entering burst-mode ($V_{COMP} < V_{COMPBM}$) will open Vcc_PFC immediately.

Besides pin 6 going open, when V_{COMP} falls below V_{COMPO} the UVLO threshold is set 2.4 V below to compensate for the drop of the voltage delivered by the self-supply circuit that occurs at light load (see *Section 5.4: Adaptive UVLO on page 25*).

5.9 Latched disable function

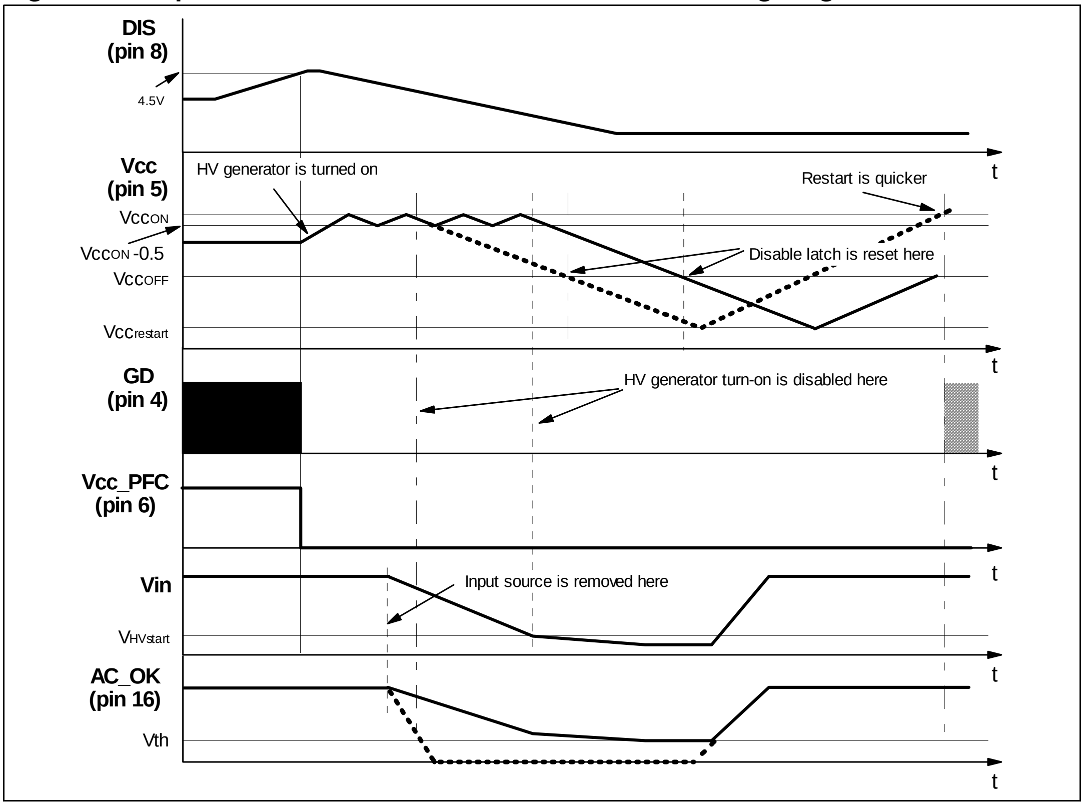
The device is equipped with a comparator having the non-inverting input externally available at the pin DIS (8) and with the inverting input internally referenced to 4.5 V. As the voltage on the pin exceeds the internal threshold, the device is immediately shut down and its consumption reduced to a low value.

The information is latched and it is necessary to let the voltage on the Vcc pin go below the UVLO threshold to reset the latch and restart the device. To keep the latch supplied as long as the converter is connected to the input source, the HV generator is activated periodically so that Vcc oscillates between the start-up threshold V_{ccON} and V_{ccON} - 0.5 V. Activating the HV generator in this way cuts its power dissipation approximately by three (as compared to the case of continuous conduction) and keeps peak silicon temperature close to the average value.

To let the L6566A restart it is then necessary to disconnect the converter from the input source. Pulling pin 16 (AC_OK) below the disable threshold (see *Section 5.12: Brownout protection on page 38*) will stop the HV generator until Vcc falls below $Vcc_{restart}$, so that the latch can be cleared and a quicker restart is allowed as the input source is removed. This operation is shown in the timing diagram of *Figure 20*.

This function is useful to implement a latched overtemperature protection very easily by biasing the pin with a divider from VREF, where the upper resistor is an NTC physically located close to a heating element like the MOSFET, or the transformer. The DIS pin is a high impedance input, thus it is prone to pick up noise, which might give origin to undesired latch-off of the device. It is possible to bypass the pin to ground with a small film capacitor (e.g. 1-10 nF) to prevent any malfunctioning of this kind.

Figure 20. Operation after latched disable activation: timing diagram



5.10 Soft-start and delayed latched shutdown upon overcurrent

At device start-up, a capacitor (Css) connected between the SS pin (14) and ground is charged by an internal current generator, I_{SS1}, from zero up to about 2 V where it is clamped. During this ramp, the overcurrent setpoint progressively rises from zero to the value imposed by the voltage on the VFF pin 15, (see "*Section 5.6: PWM comparator, PWM latch and voltage feedforward blocks on page 27*"); MOSFET's conduction time increases gradually, hence controlling the start-up inrush current. The time needed for the overcurrent setpoint to reach its steady state value, referred to as soft-start time, is approximately:

Equation 9

$$T_{SS} = \frac{Css}{I_{SS1}} V_{csx}(V_{VFF}) = \frac{Css}{I_{SS1}}\left(1 - \frac{V_{VFF}}{3}\right)$$

During the ramp (i.e. until $V_{SS} = 2$ V) all the functions that monitor the voltage on pin COMP are disabled.

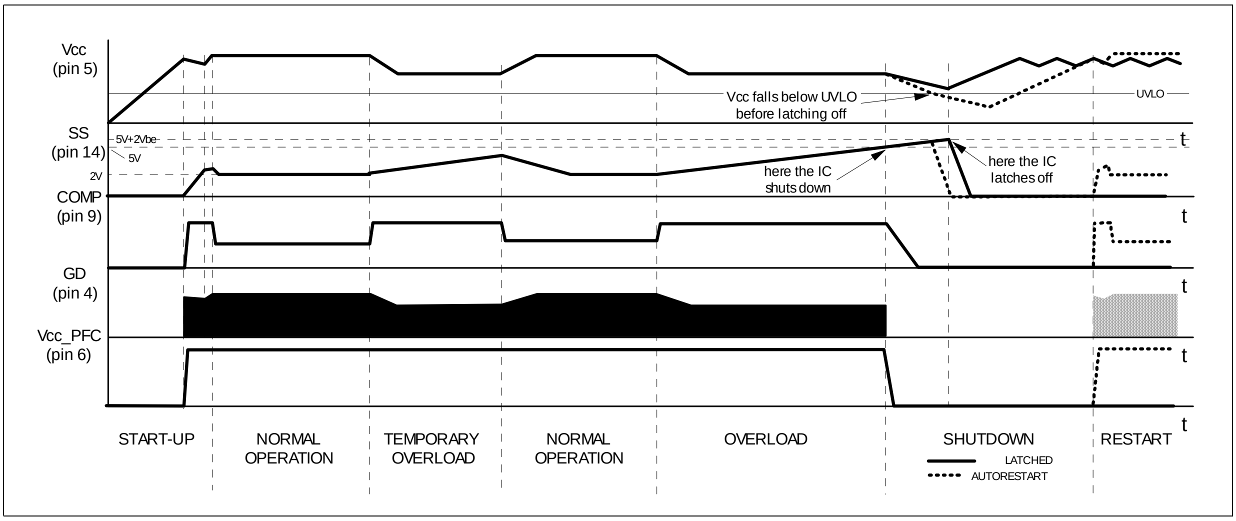
The soft-start pin is also invoked whenever the control voltage (COMP) saturates high, which reveals an open-loop condition for the feedback system. This condition very often occurs at start-up, but may be also caused by either a control loop failure or a converter overload/short circuit. A control loop failure results in an output overvoltage that is handled by the OVP function of the L6566A (see next section). In case of QR operation, a short circuit causes the converter to run at a very low frequency, then with very low power capability. This makes the self-supply system that powers the device unable to keep it operating, so that the converter will work intermittently, which is very safe. In case of overload the system has a power capability lower than that at nominal load but the output current may be quite high and overstress the output rectifier. In case of FF operation the capability is almost unchanged and both short circuit and overload conditions are more critical to handle.

The L6566A, regardless of the operating option selected, makes it easier to handle such conditions: the 2 V clamp on the SS pin is removed and a second internal current generator $I_{SS2} = I_{SS1}$ /4 keeps on charging Css. As the voltage reaches 5 V the device is disabled, if it is allowed to reach 2 V_{BE} over 5 V, the device will be latched off. In the former case the resulting behavior will be identical to that under short circuit illustrated in *Figure 6 on page 19*; in the latter case the result will be identical to that of *Figure 20 on page 33*. See *Section 5.9: Latched disable function on page 32* for additional details.

A diode, with the anode to the SS pin and the cathode connected to the VREF pin (10) is the simplest way to select either auto-restart mode or latch-mode behavior upon overcurrent. If the overload disappears before the Css voltage reaches 5 V the I_{SS2} generator will be turned off and the voltage gradually brought back down to 2 V. Refer to the *Section 6: Application examples and ideas on page 44* section (*Figure 7 on page 45*) for additional hints.

If latch-mode behavior is desired also for converter's short circuit, make sure that the supply voltage of the device does not fall below the UVLO threshold before activating the latch. *Figure 21* shows soft-start pin behavior under different operating conditions and with different settings (latch-mode or autorestart).

Figure 21. Soft-start pin operation under different operating conditions and settings



Note: Unlike other PWM controllers provided with a soft-start pin, in the L6566A grounding the SS pin does not guarantee that the gate driver is disabled.

5.11 OVP block

The OVP function of the L6566A monitors the voltage on the ZCD pin (11) in MOSFET's OFF-time, during which the voltage generated by the auxiliary winding tracks converter's output voltage. If the voltage on the pin exceeds an internal 5 V reference, a comparator is triggered, an overvoltage condition is assumed and the device is shut down. An internal current generator is activated that sources 1 mA out of the VFF pin (15). If the VFF voltage is allowed to reach 2 Vbe over 5 V, the L6566A will be latched off. See *Section 5.9: Latched disable function on page 32* for more details on IC's behavior under these conditions. If the impedance externally connected to pin 15 is so low that the 5+2 V_{BE} threshold cannot be reached or if some means is provided to prevent that, the device will be able to restart after the Vcc has dropped below 5 V. Refer to the "Application examples and Ideas" section (*Table 7 on page 45*) for additional hints.

Figure 22. OVP Function: internal block diagram

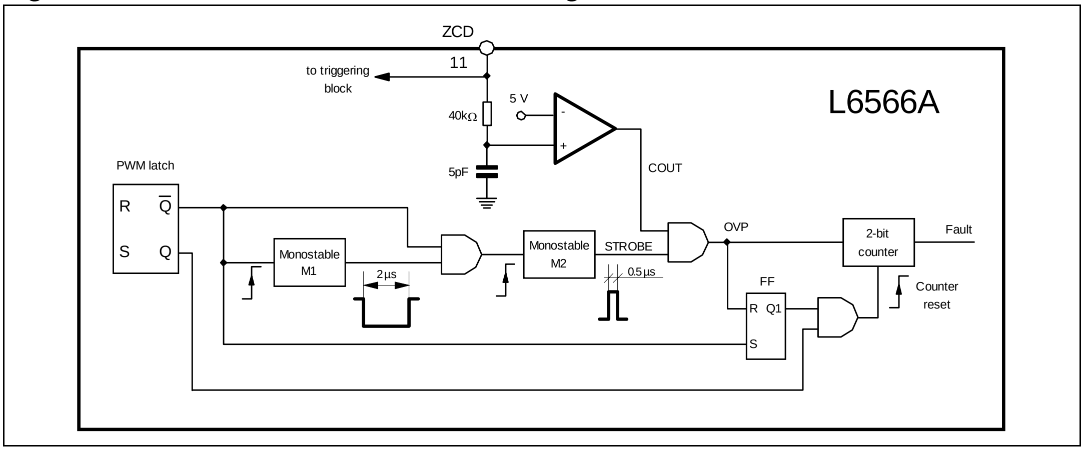
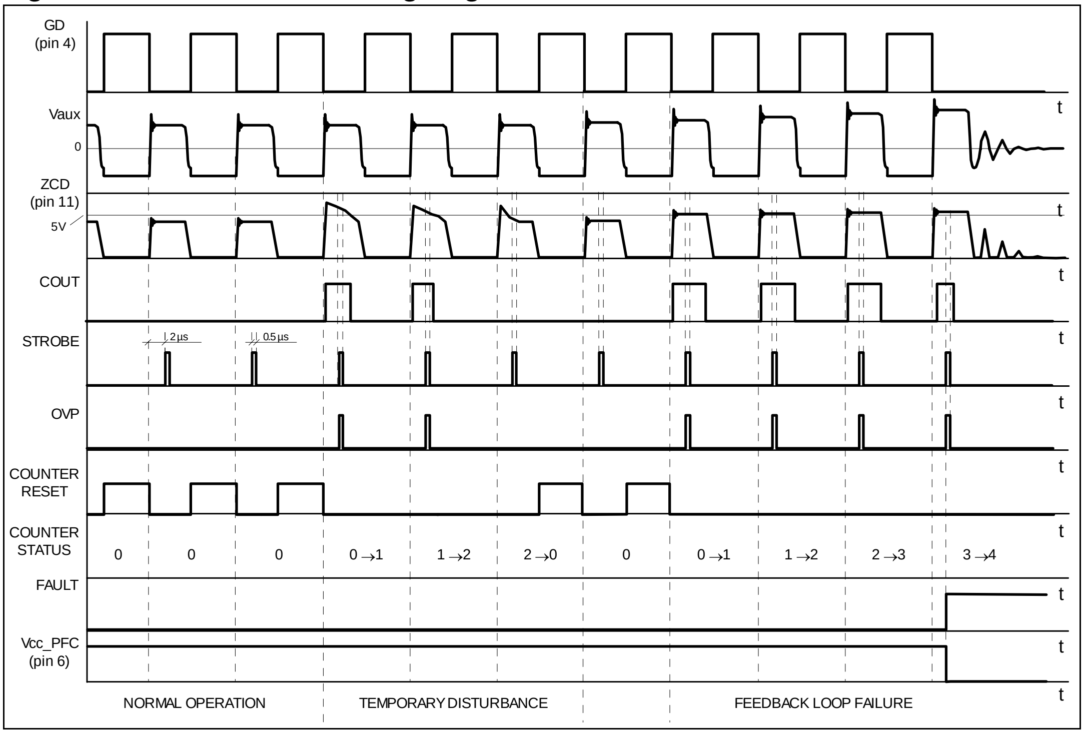


Figure 23. OVP function: timing diagram



The ZCD pin will be connected to the auxiliary winding through a resistor divider R_{Z1}, R_{Z2} (see *Figure 8 on page 20*). The divider ratio $k_{OVP} = R_{Z2} / (R_{Z1} + R_{Z2})$ will be chosen equal to:

Equation 10

$$k_{OVP} = \frac{5}{Vout_{OVP}} \frac{Ns}{Naux}$$

where $Vout_{OVP}$ is the output voltage value that is to activate the protection, Ns the turn number of the secondary winding and Naux the turn number of the auxiliary winding. The value of R_{Z1} will be such that the current sourced by the ZCD pin be within the rated capability of the internal clamp:

Equation 11

$$R_{Z1} \geq \frac{1}{3 \cdot 10^{-3}} \frac{Naux}{Np} Vin_{max}$$

where Vin_{max} is the maximum dc input voltage and Ns the turn number of the primary winding. See *Section 5.2: Zero current detection and triggering block; oscillator block on page 21* for additional details.

To reduce sensitivity to noise and prevent the latch from being erroneously activated, first the OVP comparator is active only for a small time window (typically, 0.5 µs) starting 2 µs after MOSFET's turn-off, to reject the voltage spike associated to the positive-going edges of the voltage across the auxiliary winding Vaux; second, to stop the L6566A the OVP comparator must be triggered for four consecutive switching cycles. A counter, which is reset every time the OVP comparator is not triggered in one switching cycle, is provided to this purpose.

Figure 22 on page 35 shows the internal block diagram, while the timing diagrams in *Figure 23 on page 36* illustrate the operation.

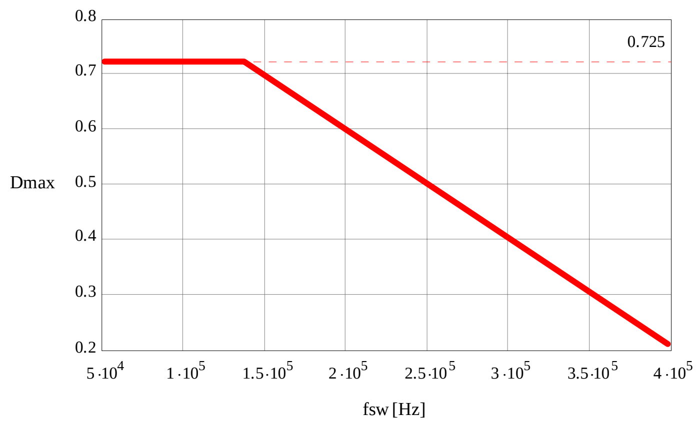
Note: To use the OVP function effectively, i.e. to ensure that the OVP comparator will be always interrogated during MOSFET's OFF-time, the duty cycle D under open-loop conditions must fulfill the following inequality:

Equation 12

$$D + T_{BLANK2}\, f_{sw} \le 1$$

where T_{BLANK2} = 2 µs; this is also illustrated in the diagram of *Figure 24*.

Figure 24. Maximum allowed duty cycle vs switching frequency for correct OVP detection



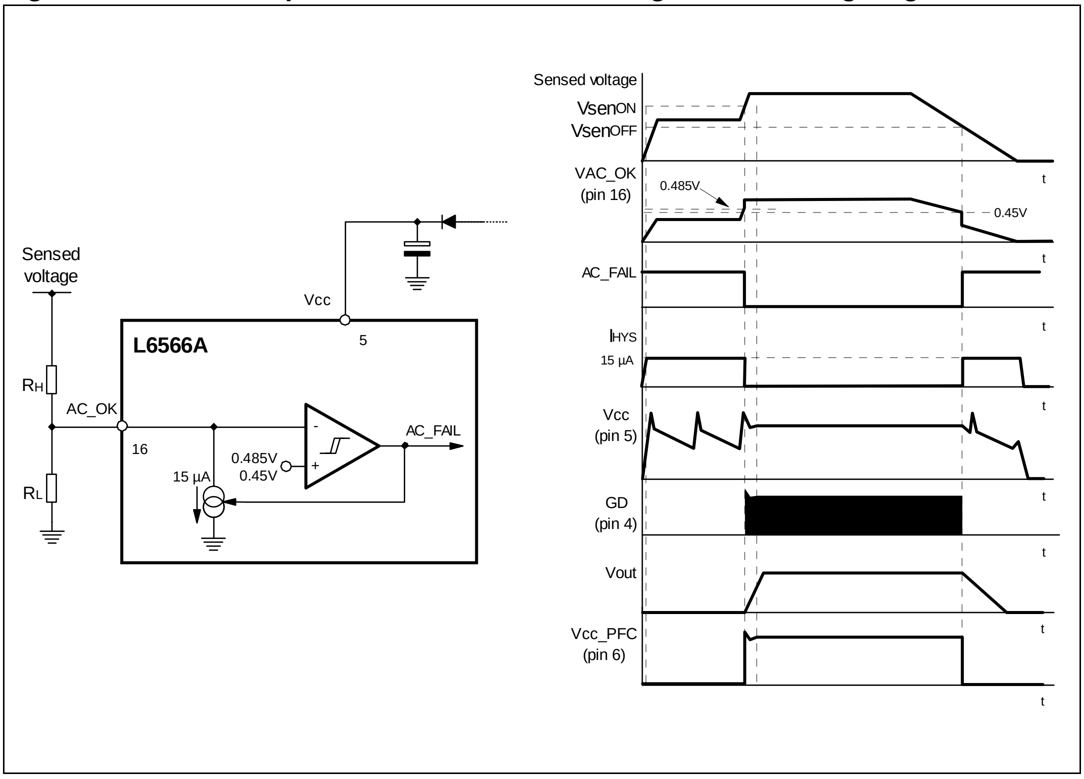
5.12 Brownout protection

Brownout protection is basically a not-latched device shutdown function activated when a condition of mains undervoltage is detected. There are several reasons why it may be desirable to shut down a converter during a brownout condition, which occurs when the mains voltage falls below the minimum specification of normal operation.

Firstly, a brownout condition may cause overheating of the PFC front-end due to an excess of RMS current. Secondly, brownout can also cause the PFC pre-regulator to work open loop. This could be dangerous to the PFC itself and the downstream converter, should the input voltage return abruptly to its rated value, given the slow response of PFC to transient events. Finally, spurious restarts may occur during converter power down, hence causing the output voltage not to decay to zero monotonically.

L6566A shutdown upon brownout is accomplished by means of an internal comparator, as shown in the block diagram of *Figure 25*, which shows the basic circuit usage. The inverting input of the comparator, available on the AC_OK pin (16), is supposed to sense a voltage proportional to either the RMS or the peak mains voltage; the non-inverting input is internally referenced to 0.485 V with 35 mV hysteresis. If the voltage applied on the AC_OK pin before the device starts operating does not exceed 0.485 V or if it falls below 0.45 V while the device is running, The AC_OK signal goes high, the pin Vcc_PFC is open and the device shuts down, with the soft-start capacitor discharged and the gate-drive output low. Additionally, in case the device has been latched off by some protection function (in which case Vcc is oscillating between V_{ccON} and V_{ccON} - 0.5 V) the AC_OK voltage falling below 0.45 V will clear the latch. This feature can be used to allow a quicker restart as the input source is removed.

Figure 25. Brownout protection: internal block diagram and timing diagram



While the brownout protection is active the start-up generator keeps on working but, being there no PWM activity, the Vcc voltage continuously oscillates between the start-up and the HV generator restart thresholds, as shown in the timing diagram of *Figure 25 on page 38*.

The brownout comparator is provided with current hysteresis in addition to voltage hysteresis: an internal 15 µA current sink is ON as long as the voltage applied on the AC_OK pin is such that the AC_FAIL signal is high. This approach provides an additional degree of freedom: it is possible to set the ON threshold and the OFF threshold separately by properly choosing the resistors of the external divider (see below). With just voltage hysteresis, instead, fixing one threshold automatically fixes the other one depending on the built-in hysteresis of the comparator.

With reference to *Figure 25 on page 38*, the following relationships can be established for the ON ($Vsen_{ON}$) and OFF ($Vsen_{OFF}$) thresholds of the sensed voltage:

Equation 13

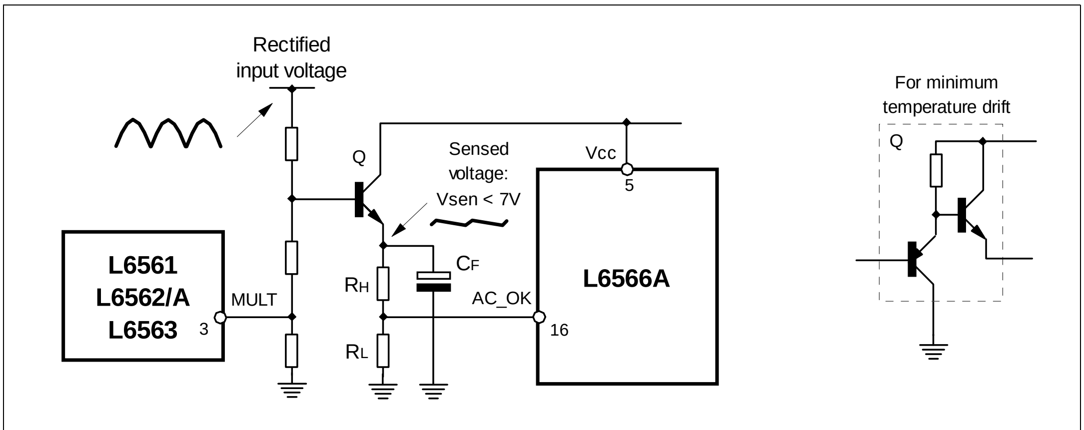
$$\frac{Vsen_{ON} - 0.485}{R_H} = 15 \cdot 10^{-6} + \frac{0.485}{R_L} \qquad \frac{Vsen_{OFF} - 0.45}{R_H} = \frac{0.45}{R_L}$$

which, solved for R_H and R_L, yield:

Equation 14

$$R_H = \frac{Vsen_{ON} - 1.078 \cdot Vsen_{OFF}}{15 \cdot 10^{-6}}; \qquad R_L = R_H \frac{0.45}{Vsen_{OFF} - 0.45}$$

Figure 26. AC voltage sensing with the L6566A



It is typically convenient not to use additional dividers connected to high-voltage rails because this could make it difficult to meet no-load consumption targets envisaged by energy-saving regulations. *Figure 26* shows a simple voltage sensing technique that makes use of the divider already used by the PFC control chip to sense the ac mains voltage with just the addition of an extra tap.

The small-signal NPN Q and the capacitor C_F make a peak detector, so that the information of the rms mains voltage can be found across C_F. Tap's position determines the dc voltage to be sensed by the AC_OK pin. It is convenient to use a level as high as possible to minimize the effect of V_{BE} changes with temperature. However, it could be necessary to limit the maximum sensed voltage below 7 V to prevent Q's emitter reverse breakdown; it would not be destructive because the reverse current would be quite small (the resistors seen by the base terminal are several ten kW) but this could distort the signal on the MULT pin of the PFC chip and adversely affect the operation of the pre-regulator. C_F needs to be quite a big capacitor (in the µF) to have small residual ripple superimposed on the dc level; as a rule-of-thumb, use a time constant $(R_L + R_H) \cdot C_F$ at least 4-5 times the maximum line cycle period, then fine tune if needed, considering also transient conditions such as mains missing cycles.

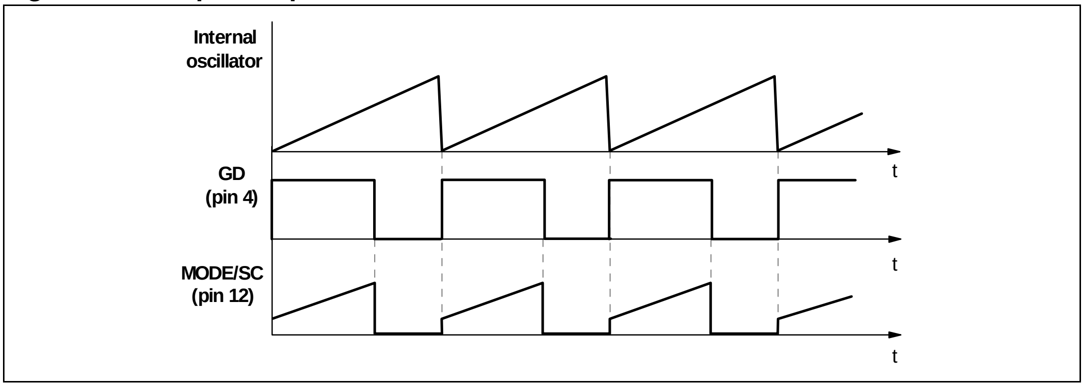
If temperature effects are critical, the NPN Q can be replaced by a PNP-NPN pair arranged as shown in *Figure 26 on page 39* on the right-hand side; other sensing techniques can be adopted anyway.

The voltage on the pin is clamped upwards at about 3.15 V; then, if the function is not used the pin has to be connected to Vcc through a resistor (220 to 680 kΩ).

5.13 Slope compensation

The pin MODE/SC (12), when not connected to VREF, provides a voltage ramp during MOSFET's ON-time synchronous to that of the internal oscillator sawtooth, with 0.8 mA minimum current capability. This ramp is intended for implementing additive slope compensation on current sense. This is needed to avoid the sub-harmonic oscillation that arises in all peak-current-mode-controlled converters working at fixed frequency in continuous conduction mode with a duty cycle close to or exceeding 50 %.

Figure 27. Slope compensation waveforms



The compensation will be realized by connecting a programming resistor between this pin and the current sense input (pin 7, CS). The CS pin has to be connected to the sense resistor with another resistor to make a summing node on the pin. Since no ramp is delivered during MOSFET OFF-time (see *Figure 27*), no external component other than the programming resistor is needed to ensure a clean operation at light loads.

Note: The addition of the slope compensation ramp will reduce the available dynamics of the current signal; thereby, the value of the sense resistor must be determined taking this into account. Note also that the burst-mode threshold (in terms of power) will be slightly changed.

If slope compensation is not required with FF operation, the pin shall be left floating.

5.14 Summary of L6566A power management functions

It has been seen that the device is provided with a number of power management functions: multiple operating mode upon loading conditions, protection functions, as well as interaction with the PFC pre-regulator. To help the designer familiarize with these functions, in the following tables all of theme are summarized with their respective activation mechanism and the resulting status of the most important pins. This can be useful not only for a correct use of the IC but also for diagnostic purposes: especially at prototyping/debugging stage, it is quite common to bump into unwanted activation of some function, and these tables can be used as a sort of quick troubleshooting guide.

Table 5. L6566A light load management features

Feature	Description	Caused by	IC behavior	Vcc_restart (V)	Consump. (Iqdis,mA)	V_{REF} (V)	SS	V_{COMP} (V)	OSC (V)	FMOD
Burst mode	Controlled ON-OFF operation for low power consumption at light load	$V_{COMP} < V_{COMPBM}$ - Hys	Pulse skipping operation	N.A.	1.34mA	5	unchanged	$V_{COMPBM-HYS}$ to V_{COMPBM}	0/1	0
PFC manage ment	PFC off at light load, on at heavy load	$V_{COMP} < V_{COMPO}$	$V_{CC\_PFC} =$ 0	N.A.		5	unchanged	unchanged	1	0
		$V_{COMP} < V_{COMPL}$	$V_{CC\_PFC} = V_{CC}$							V_{CC}

Table 6. L6566A protections

Protection	Description	Caused by	IC behavior	Vcc restart (V)	IC Iq (mA)	VREF (V)	SS	VCOMP (V)	OSC (V)	FMOD	VFF
OVP	Output overvoltage protection	V_{ZCD}>V_{ZCDth} for 4 consecutive switching cycles	Auto restart(1)	5	2.2	5(6)	unchanged (6)	0	0	0	unchanged
		VFF > VFFlatch	Latched	13.5	0.33	0	0	0	0	0	0
OLP	Output overload protection	V_{COMP} =V_{COMPHi} V_{SS} > V_{SSDIS}	Auto restart(2)	5	1.46	5(6)	V_{SS} <V_{SSLAT}(3)	V_{COMPHi} (6)	0	0	unchanged
		V_{COMP} =V_{COMPHi} V_{SS} > V_{SSLAT}	Latched	13.5	0.33	0	0	0	0	0	0
Short circuit protection	Output short circuit protection	V_{COMP} =V_{COMPHi} V_{SS} > V_{SSDIS}(4)	Auto restart	5	1.46	0	V_{SS} <V_{SSLAT}(6)	V_{COMPHi} (5)		0	unchanged
		V_{COMP} =V_{COMPHi} V_{SS} > V_{SSLAT}(6)	Latched	13.5	0.33	0	0	0	0	0	0
2nd OCP	Transformer saturation or shorted secondary diode protection	V_{CS} > V_{CSDIS} for 2-3 consecutive switching cycles	Latched	5	0.33	0	0	0	0	0	0
OTP	Externally settable overtemperature protection	V_{DIS}>V_{OTP}	Latched	13.5	0.33	0	0	0	0	0	0
	Internal thermal shutdown	T_j > 160°C	Auto restart(5)	5	0.33	0	0	0	0	0	0
Brownout	Mains undervoltage protection	V_{AC_OK} < V_{th}	Auto restart	5	0.33	0	0	0	0	0	unchanged
Reference drift	V_{REF} drift protection	V_{REF} > V_{ov}	Latched	13.5	0.33	0	0	0	0	0	0
Shutdown1	Gate driver disable	V_{FF} > V_{off}	Auto restart	5	2.5	5	unchanged	unchanged	1	unchanged	unchanged
Shutdown2	Shutdown by V_{COMP} low	V_{COMP} < $V_{COMPOFF}$	Latched	10	0.33	0	0	0	0	0	0

Table 6. L6566A protections (continued)

Protection	Description	Caused by	IC behavior	Vcc restart (V)	IC Iq (mA)	VREF (V)	SS	VCOMP (V)	OSC (V)	FMOD	VFF
ADAPTIVE UVLO	Shutdown by V_{cc} going below V_{ccoff} (lowering of V_{ccoff} threshold at light load)	V_{cc} < 9.4V (VCOMP > V_{COMPL}) V_{cc} < 7.2V (VCOMP > V_{COMPO})	Auto restart	5V	0.18 mA	0	0	0	0	0	0

1. Use One external diode from V_{FF} (#15) to AC_OK (#16), cathode to AC_OK
2. Use one external diode from SS (#14) to V_{REF} (#10), cathode to V_{REF}
3. If C_{ss} and the V_{cc} capacitor are such that V_{cc} falls below UVLO before latch tripping (*Figure 21 on page 34*)
4. If C_{SS} and the Vcc capacitor are such that the latch is tripped before V_{cc} falls below UVLO (*Figure 21 on page 34*)
5. When T_J < 110 °C
6. Discharged to zero by V_{cc} going below UVLO

It is worth reminding that “auto-restart” means that the device will work intermittently as long as the condition that is activating the function is not removed; “latched” means that the device is stopped as long as the unit is connected to the input power source and the unit must be disconnected for some time from the source in order for the device (and the unit) to restart. Optionally, a restart can be forced by pulling the voltage of pin 16 (AC_OK) below 0.45 V.

6 Application examples and ideas

Figure 28. Typical low-cost application schematic

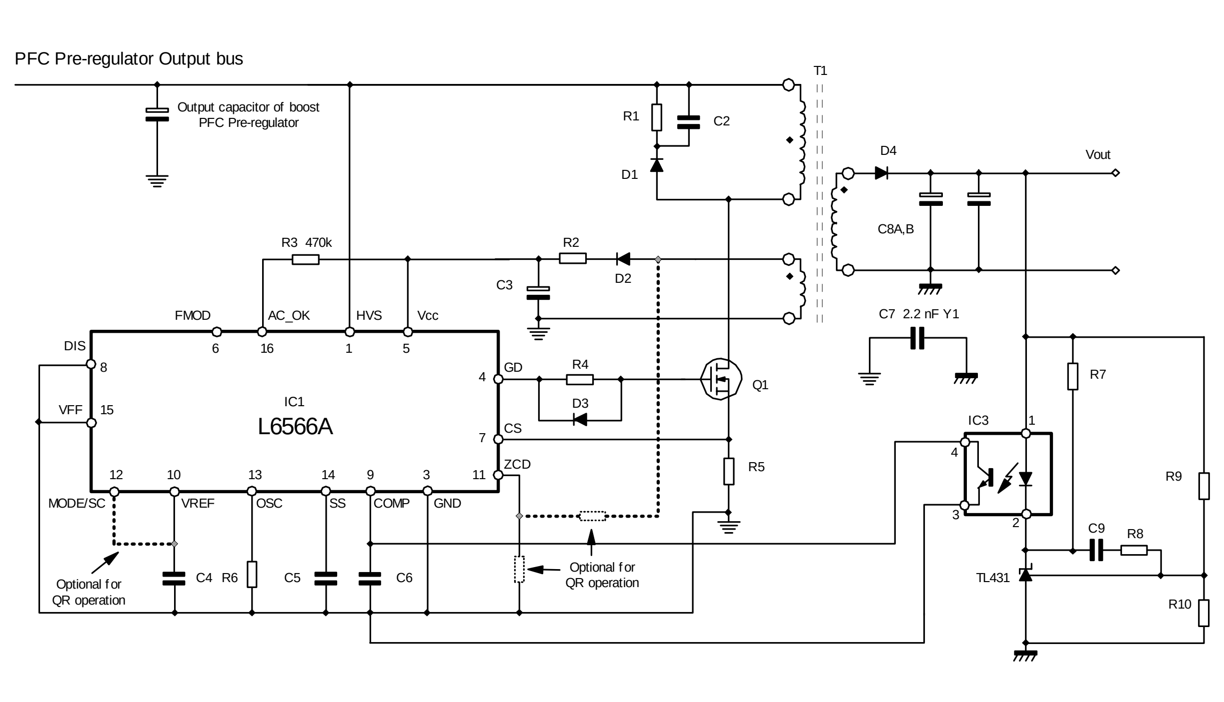


Figure 29. Typical full-feature application schematic (QR operation)

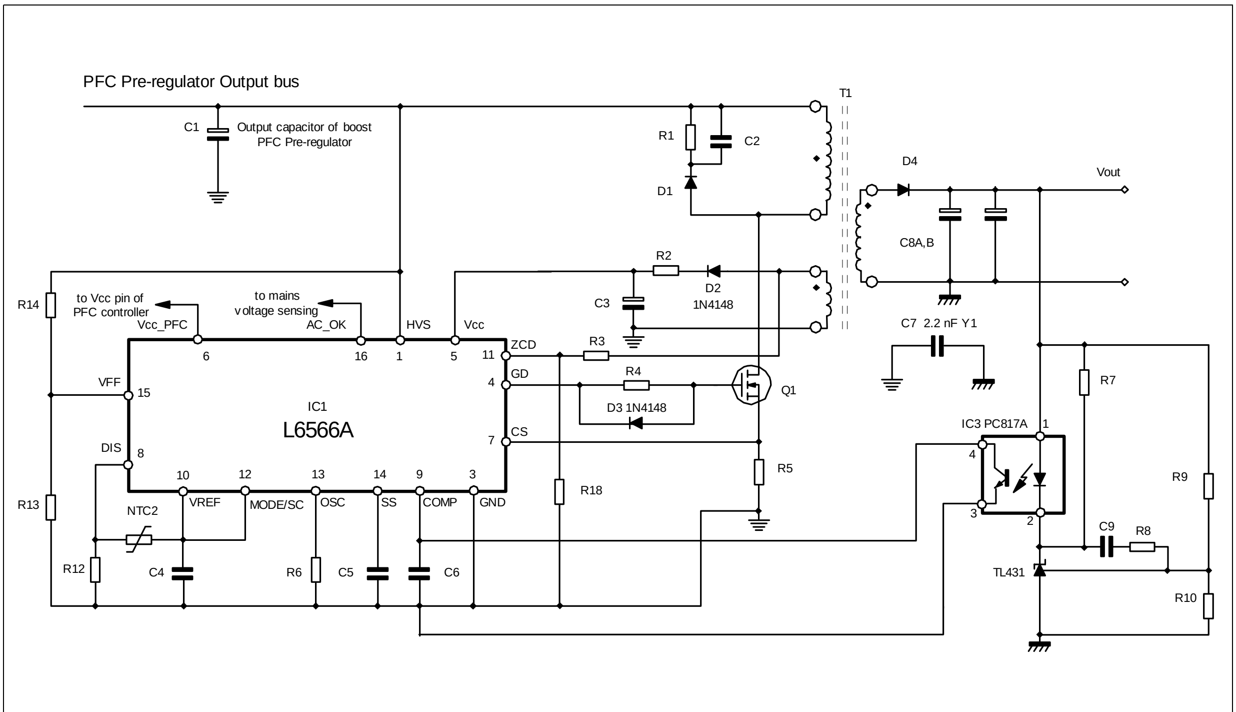


Figure 30. Typical full-feature application schematic (FF operation)

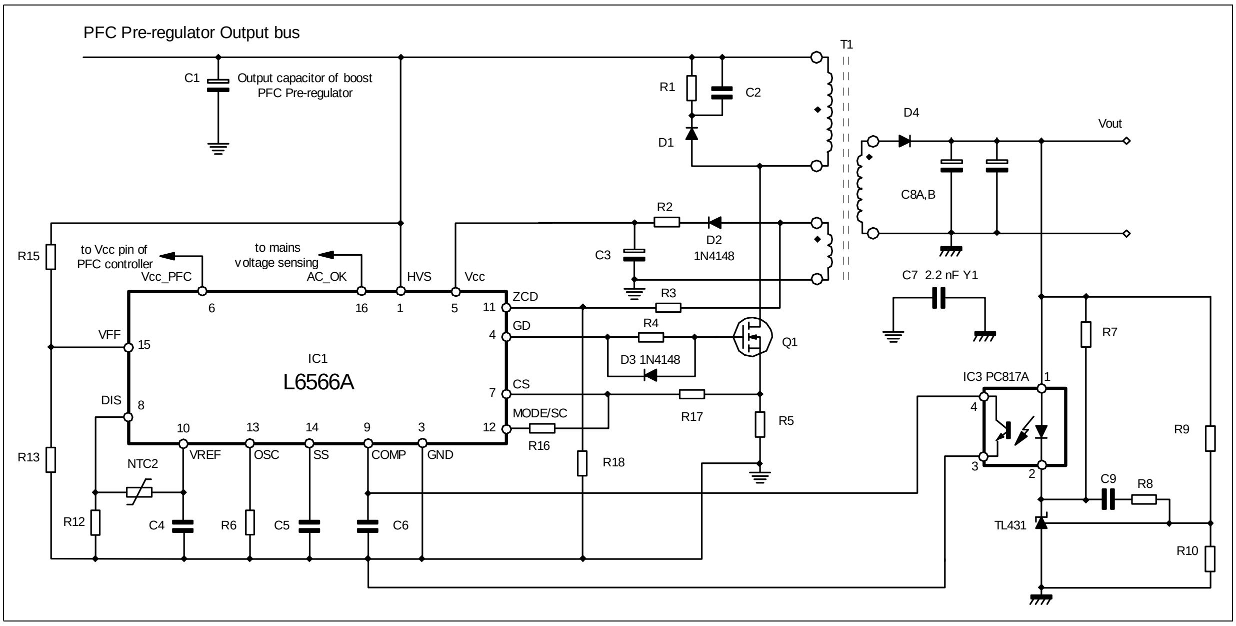
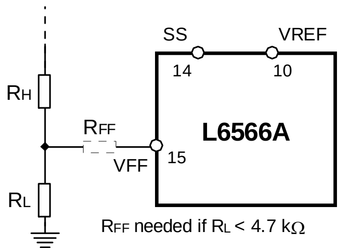


Table 7. External circuits that determine IC behavior upon OVP and OCP

<table>
<tr><th></th><th>OVP latched</th><th>OVP auto-restart</th></tr>
<tr><td>OCP latched</td><td>


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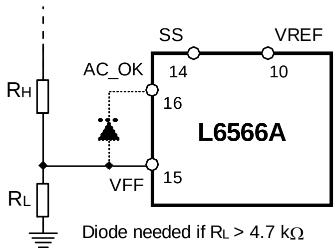

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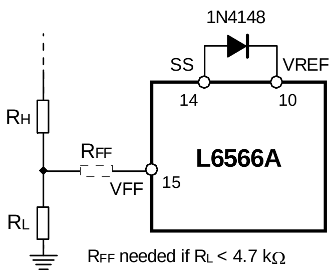
<tr><td>OCP auto-restart</td><td>


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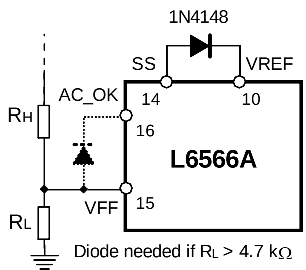

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Figure 31. Frequency foldback at light load (FF operation)

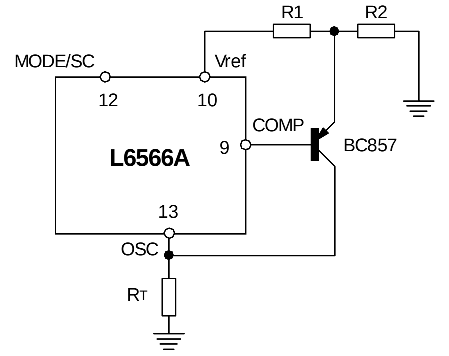
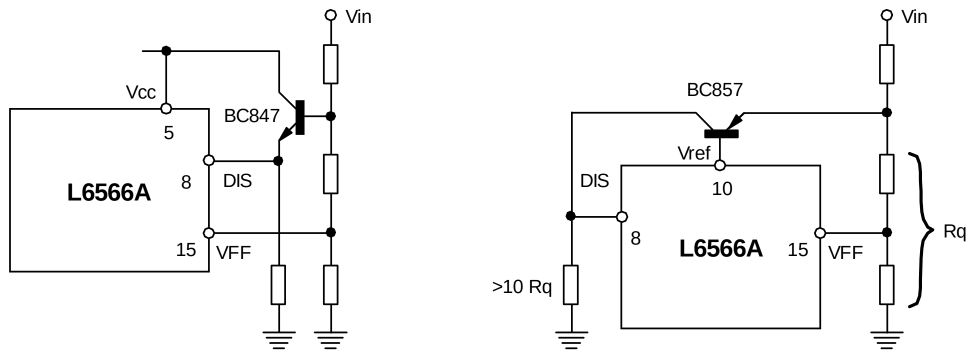


Figure 32. Latched shutdown upon mains overvoltage



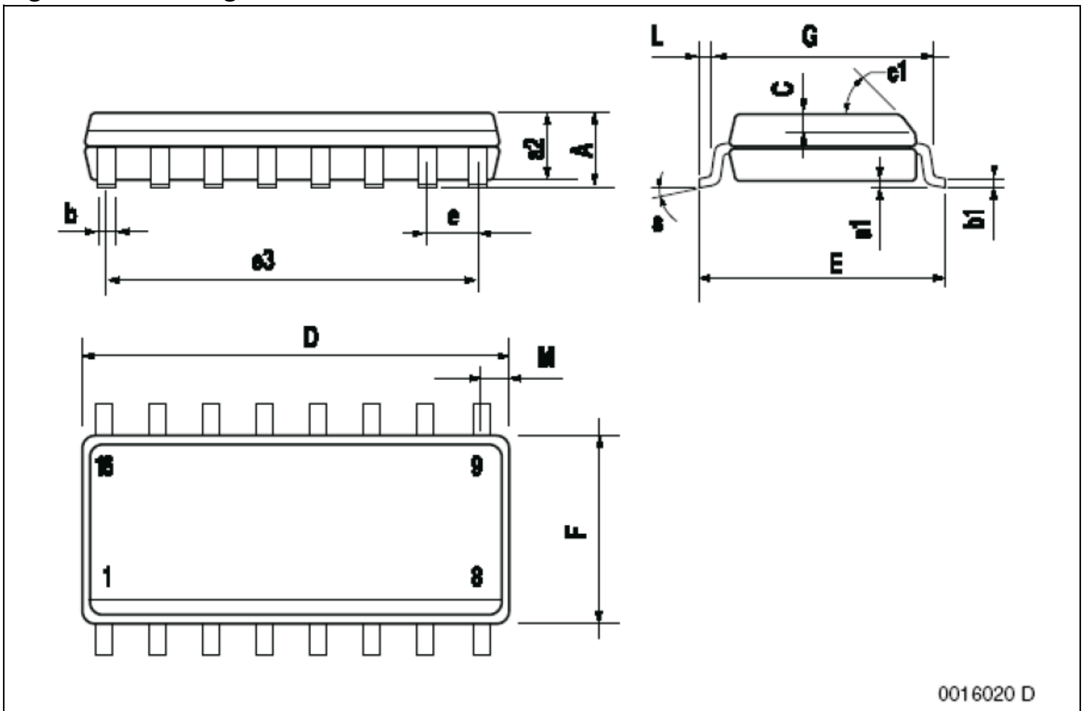
7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 8. SO16N mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1			45°	(typ.)		
D(1)	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F(1)	3.8		4.0	0.150		0.157
G	4.60		5.30	0.181		0.208
L	0.4		1.27	0.150		0.050
M			0.62			0.024
S	8°(max.)					

Figure 33. Package dimensions



8 Order codes

Table 9. Order codes

Order codes	Package	Packaging
L6566A	SO16N	Tube
L6566ATR	SO16N	Tape and reel

9 Revision history

Table 10. Document revision history

Date	Revision	Changes
20-Aug-2007	1	First release
29-May-2008	2	Updated $V_{MODE/SC}$ value *Table 2 on page 11*