L6229

DMOS DRIVER FOR THREE-PHASE BRUSHLESS DC MOTOR

1 FEATURES

- OPERATING SUPPLY VOLTAGE FROM 8 TO 52V
- 2.8A OUTPUT PEAK CURRENT (1.4A DC)
- $R_{DS(ON)}$ 0.73Ω TYP. VALUE @ T_j = 25 °C
- OPERATING FREQUENCY UP TO 100KHz
- NON DISSIPATIVE OVERCURRENT DETECTION AND PROTECTION
- DIAGNOSTIC OUTPUT
- CONSTANT t_{OFF} PWM CURRENT CONTROLLER
- SLOW DECAY SYNCHR. RECTIFICATION
- 60° & 120° HALL EFFECT DECODING LOGIC
- BRAKE FUNCTION
- TACHO OUTPUT FOR SPEED LOOP
- CROSS CONDUCTION PROTECTION
- THERMAL SHUTDOWN
- UNDERVOLTAGE LOCKOUT
- INTEGRATED FAST FREEWEELING DIODES

2 DESCRIPTION

The L6229 is a DMOS Fully Integrated Three-Phase Motor Driver with Overcurrent Protection.

Realized in MultiPower-BCD technology, the device combines isolated DMOS Power Transistors with CMOS and bipolar circuits on the same chip.

The device includes all the circuitry needed to drive a three-phase BLDC motor including: a three-phase DMOS Bridge, a constant off time PWM Current Controller and the decoding logic for single ended hall sensors that generates the required sequence for the power stage.

Available in PowerDIP24 (20+2+2), PowerSO36 and SO24 (20+2+2) packages, the L6229 features a non-dissipative overcurrent protection on the high side Power MOSFETs and thermal shutdown.

Figure 1. Package

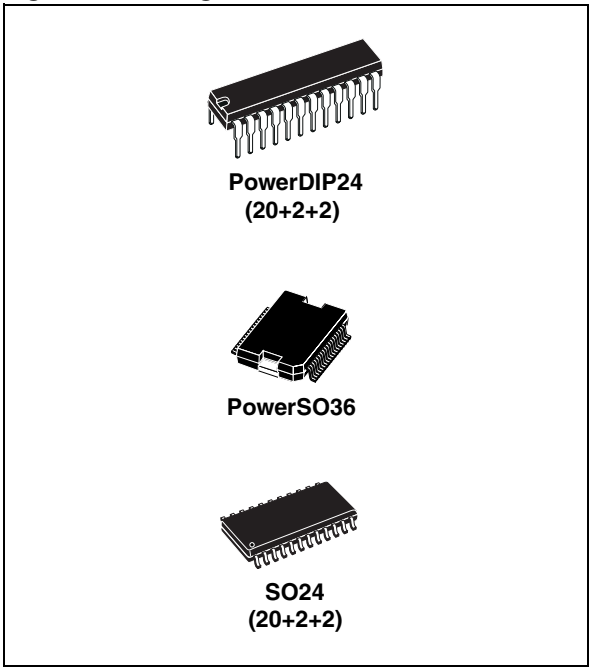


Table 1. Order Codes

Part Number	Package
L6229N	PowerDIP24
L6229PD	PowerSO36
L6229PDTR	PowerSO36 in Tape & Reel
L6229D	SO24
L6229DTR	SO24 in Tape & Reel

Figure 2. Block Diagram

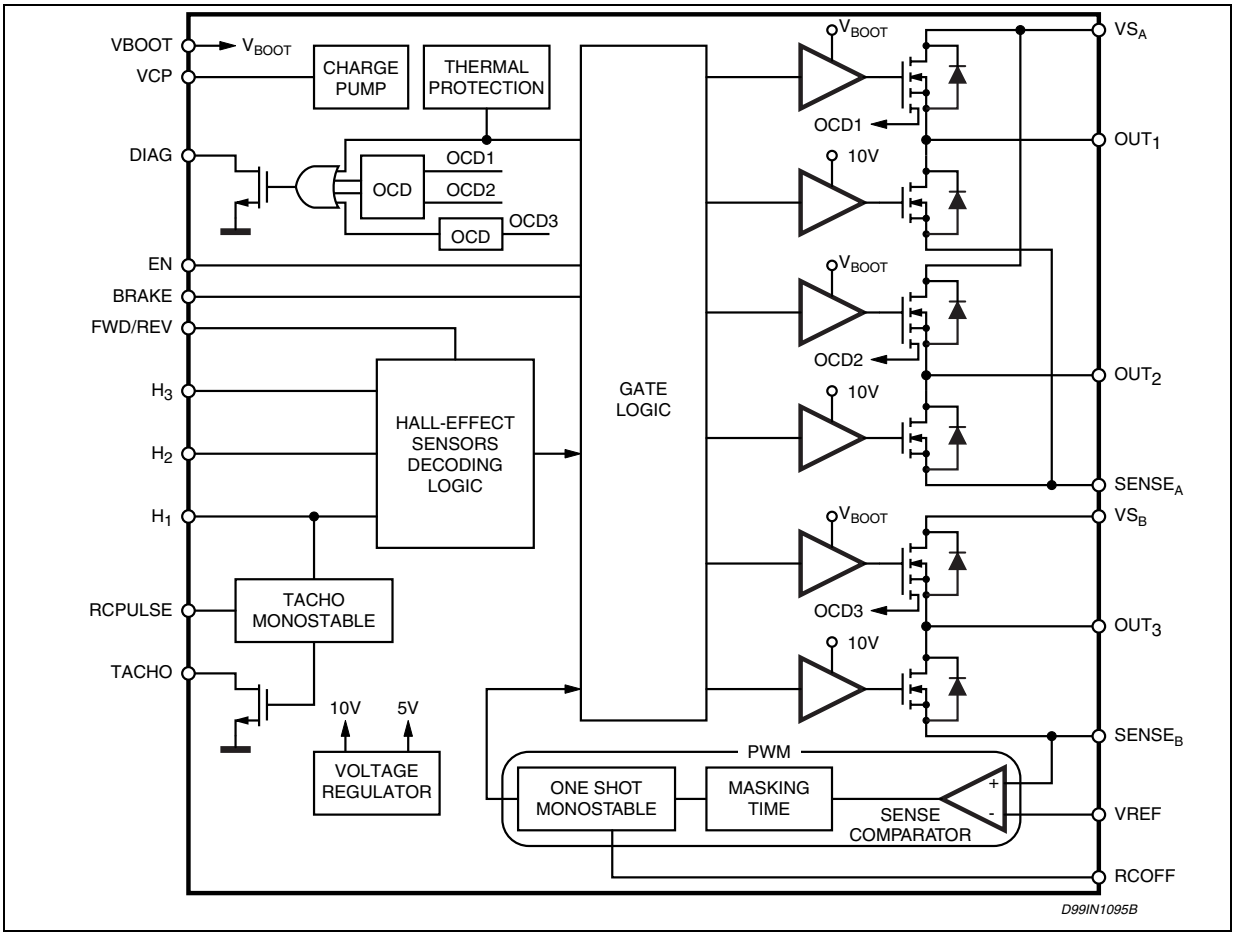


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Test conditions	Value	Unit
V_S	Supply Voltage	$V_{SA} = V_{SB} = V_S$	60	V
V_{OD}	Differential Voltage between: VS_A, OUT_1, OUT_2, $SENSE_A$ and VS_B, OUT_3, $SENSE_B$	$V_{SA} = V_{SB} = V_S$ = 60V; $V_{SENSEA} = V_{SENSEB}$ = GND	60	V
V_{BOOT}	Bootstrap Peak Voltage	$V_{SA} = V_{SB} = V_S$	V_S + 10	V
V_{IN}, V_{EN}	Logic Inputs Voltage Range		-0.3 to 7	V
V_{REF}	Voltage Range at pin VREF		-0.3 to 7	V
V_{RCOFF}	Voltage Range at pin RCOFF		-0.3 to 7	V
$V_{RCPULSE}$	Voltage Range at pin RCPULSE		-0.3 to 7	V
V_{SENSE}	Voltage Range at pins $SENSE_A$ and $SENSE_B$		-1 to 4	V
$I_{S(peak)}$	Pulsed Supply Current (for each VS_A and VS_B pin)	$V_{SA} = V_{SB} = V_S$; T_{PULSE} < 1ms	3.55	A
I_S	DC Supply Current (for each VS_A and VS_B pin)	$V_{SA} = V_{SB} = V_S$	1.4	A
T_{stg}, T_{OP}	Storage and Operating Temperature Range		-40 to 150	°C

Table 3. Recommended Operating Condition

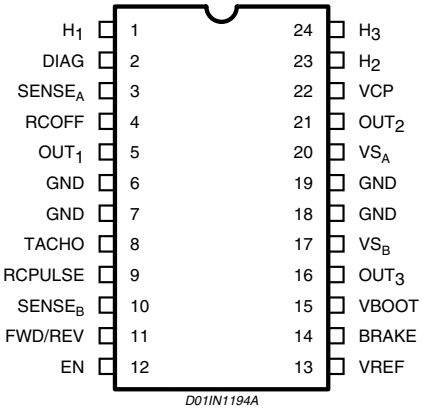
Symbol	Parameter	Test Conditions	MIN	MAX	Unit
V_S	Supply Voltage	$V_{SA} = V_{SB} = V_S$	12	52	V
V_{OD}	Differential Voltage between: VS_A, OUT_1, OUT_2, $SENSE_A$ and VS_B, OUT_3, $SENSE_B$	$V_{SA} = V_{SB} = V_S$; $V_{SENSEA} = V_{SENSEB}$		52	V
V_{REF}	Voltage Range at pin VREF		-0.1	5	V
V_{SENSE}	Voltage Range at pins $SENSE_A$ and $SENSE_B$	(pulsed $t_W < t_{rr}$) (DC)	-6 -1	6 1	V V
I_{OUT}	DC Output Current	$V_{SA} = V_{SB} = V_S$		1.4	A
T_J	Operating Junction Temperature		-25	125	°C
f_{SW}	Switching Frequency			100	KHz

Table 4. Thermal Data

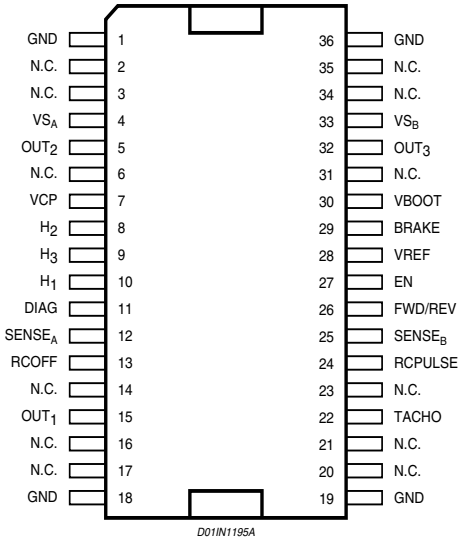
Symbol	Description	PDIP24	SO24	PowerSO36	Unit
$R_{th(j\text{-}pins)}$	Maximum Thermal Resistance Junction-Pins	19	15		°C/W
$R_{th(j\text{-}case)}$	Maximum Thermal Resistance Junction-Case			2	°C/W
$R_{th(j\text{-}amb)1}$	MaximumThermal Resistance Junction-Ambient (1)	44	55	-	°C/W
$R_{th(j\text{-}amb)1}$	Maximum Thermal Resistance Junction-Ambient (2)	-	-	36	°C/W
$R_{th(j\text{-}amb)1}$	MaximumThermal Resistance Junction-Ambient (3)	-	-	16	°C/W
$R_{th(j\text{-}amb)2}$	Maximum Thermal Resistance Junction-Ambient (4)	59	78	63	°C/W

(1) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the bottom side of 6 cm^2 (with a thickness of 35 µm).
(2) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm).
(3) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm), 16 via holes and a ground layer.
(4) Mounted on a multi-layer FR4 PCB without any heat-sinking surface on the board.

Figure 3. Pin Connections (Top view)



PowerDIP24/SO24



PowerSO36 (5)

(5) The slug is internally connected to pins 1, 18, 19 and 36 (GND pins).

Table 5. Pin Description

PACKAGE		Name	Type	Function
SO24/ PowerDIP24	PowerSO36			
PIN #	PIN #			
1	10	H_1	Sensor Input	Single Ended Hall Effect Sensor Input 1.
2	11	DIAG	Open Drain Output	Overcurrent Detection and Thermal Protection pin. An internal open drain transistor pulls to GND when an overcurrent on one of the High Side MOSFETs is detected or during Thermal Protection.
3	12	$SENSE_A$	Power Supply	Half Bridge 1 and Half Bridge 2 Source Pin. This pin must be connected together with pin $SENSE_B$ to Power Ground through a sensing power resistor.
4	13	RCOFF	RC Pin	RC Network Pin. A parallel RC network connected between this pin and ground sets the Current Controller OFF-Time.
5	15	OUT_1	Power Output	Output 1
6, 7, 18, 19	1, 18, 19, 36	GND	GND	Ground terminals. On PowerDIP24 and SO24 packages, these pins are also used for heat dissipation toward the PCB. On PowerSO36 package the slug is connected on these pins.
8	22	TACHO	Open Drain Output	Frequency-to-Voltage open drain output. Every pulse from pin H_1 is shaped as a fixed and adjustable length pulse.
9	24	RCPULSE	RC Pin	RC Network Pin. A parallel RC network connected between this pin and ground sets the duration of the Monostable Pulse used for the Frequency-to-Voltage converter.

Table 5. Pin Description (continued)

PACKAGE		Name	Type	Function
SO24/ PowerDIP24	PowerSO36			
PIN #	PIN #			
10	25	$SENSE_B$	Power Supply	Half Bridge 3 Source Pin. This pin must be connected together with pin $SENSE_A$ to Power Ground through a sensing power resistor. At this pin also the Inverting Input of the Sense Comparator is connected.
11	26	FWD/REV	Logic Input	Selects the direction of the rotation. HIGH logic level sets Forward Operation, whereas LOW logic level sets Reverse Operation. If not used, it has to be connected to GND or +5V..
12	27	EN	Logic Input	Chip Enable. LOW logic level switches OFF all Power MOSFETs. If not used, it has to be connected to +5V.
13	28	VREF	Logic Input	Current Controller Reference Voltage. Do not leave this pin open or connect to GND.
14	29	BRAKE	Logic Input	Brake Input pin. LOW logic level switches ON all High Side Power MOSFETs, implementing the Brake Function. If not used, it has to be connected to +5V.
15	30	VBOOT	Supply Voltage	Bootstrap Voltage needed for driving the upper Power MOSFETs.
16	32	OUT_3	Power Output	Output 3.
17	33	VS_B	Power Supply	Half Bridge 3 Power Supply Voltage. It must be connected to the supply voltage together with pin VS_A.
20	4	VS_A	Power Supply	Half Bridge 1 and Half Bridge 2 Power Supply Voltage. It must be connected to the supply voltage together with pin VS_B.
21	5	OUT_2	Power Output	Output 2.
22	7	VCP	Output	Charge Pump Oscillator Output.
23	8	H_2	Sensor Input	Single Ended Hall Effect Sensor Input 2.
24	9	H_3	Sensor Input	Single Ended Hall Effect Sensor Input 3.

Table 6. Electrical Characteristics

(V_S = 48V , T_{amb} = 25 °C , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{Sth(ON)}$	Turn ON threshold		5.8	6.3	6.8	V
$V_{Sth(OFF)}$	Turn OFF threshold		5	5.5	6	V
I_S	Quiescent Supply Current	All Bridges OFF; Tj = -25 to 125°C (6)		5	10	mA
$T_{J(OFF)}$	Thermal Shutdown Temperature			165		°C
Output DMOS Transistors						
$R_{DS(ON)}$	High-Side + Low-Side Switch ON Resistance	T_j = 25 °C		1.47	1.69	Ω
		T_j =125 °C (7)		2.35	2.70	Ω
I_{DSS}	Leakage Current	EN = Low; OUT = V_{CC}			2	mA
		EN = Low; OUT = GND	-0.3			mA

Table 6. Electrical Characteristics (continued)
(V_S = 48V , T_{amb} = 25 °C , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Source Drain Diodes						
V_{SD}	Forward ON Voltage	I_{SD} = 1.4A, EN = LOW		1.15	1.3	V
t_{rr}	Reverse Recovery Time	I_f = 1.4A		300		ns
t_{fr}	Forward Recovery Time			200		ns
Logic Input (H1, H2, H3, EN, FWD/REV, BRAKE)						
V_{IL}	Low level logic input voltage		-0.3		0.8	V
V_{IH}	High level logic input voltage		2		7	V
I_{IL}	Low level logic input current	GND Logic Input Voltage	-10			µA
I_{IH}	High level logic input current	7V Logic Input Voltage			10	µA
$V_{th(ON)}$	Turn-ON Input Threshold			1.8	2.0	V
$V_{th(OFF)}$	Turn-OFF Input Threshold		0.8	1.3		V
V_{thHYS}	Input Thresholds Hysteresys		0.25	0.5		V
Switching Characteristics						
$t_{D(on)EN}$	Enable to out turn-ON delay time (7)	I_{LOAD} = 1.4 A, Resistive Load	500	650	800	ns
$t_{D(off)EN}$	Enable to out turn-OFF delay time (7)	I_{LOAD} = 1.4 A, Resistive Load	500		1000	ns
$t_{D(on)IN}$	Other Logic Inputs to Output Turn-ON delay Time	I_{LOAD} = 1.4 A, Resistive Load		1.6		µs
$t_{D(off)IN}$	Other Logic Inputs to out Turn-OFF delay Time	I_{LOAD} = 1.4 A, Resistive Load		800		ns
t_{RISE}	Output Rise Time (7)	I_{LOAD} = 1.4 A, Resistive Load	40		250	ns
t_{FALL}	Output Fall Time (7)	I_{LOAD} = 1.4 A, Resistive Load	40		250	ns
t_{DT}	Dead Time		0.5	1		µs
f_{CP}	Charge Pump Frequency	Tj = -25 to 125°C (6)		0.6	1	MHz
PWM Comparator and Monostable						
I_{RCOFF}	Source current at pin RC_{OFF}	V_{RCOFF} = 2.5 V	3.5	5.5		mA
V_{OFFSET}	Offset Voltage on Sense Comparator	V_{ref} = 0.5 V		±5		mV
t_{prop}	Turn OFF Propagation delay (8)	V_{ref} = 0.5 V		500		ns
t_{blank}	Internal Blanking Time on Sense Comparator			1		µs
$t_{ON(min)}$	Minimum on Time			2.5	3	µs
t_{OFF}	PWM RecirculationTime	R_{OFF}= 20kΩ ; C_{OFF} =1nF		13		µs
		R_{OFF}= 100kΩ ; C_{OFF} =1nF		61		µs
I_{BIAS}	Input Bias Current at pin VREF				10	µA
Tacho Monostable						
$I_{RCPULSE}$	Source Current at pin RCPULSE	$V_{RCPULSE}$ = 2.5V	3.5	5.5		mA

Table 6. Electrical Characteristics (continued)
(V_S = 48V , T_{amb} = 25 °C , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PULSE}	Monostable of Time	R_{PUL} = 20kΩ ; C_{PUL} =1nF		12		µs
		R_{PUL} = 100kΩ ; C_{PUL} =1nF		60		µs
R_{TACHO}	Open Drain ON Resistance			40	60	Ω
Over Current Detection & Protection						
I_{SOVER}	Supply Overcurrent Protection Threshold	T_J = -25 to 125°C (6)	2	2.8	3.55	A
R_{OPDR}	Open Drain ON Resistance	I_{DIAG} = 4mA		40	60	Ω
I_{OH}	OCD high level leakage current	V_{DIAG} = 5V		1		µA
$t_{OCD(ON)}$	OCD Turn-ON Delay Time (9)	I_{DIAG} = 4mA; C_{DIAG} < 100pF		200		ns
$t_{OCD(OFF)}$	OCD Turn-OFF Delay Time (9)	I_{DIAG} = 4mA; C_{DIAG} < 100pF		100		ns

(6) Tested at 25°C in a restricted range and guaranteed by characterization.
(7) See Fig. 4.
(8) Measured applying a voltage of 1V to pin SENSE and a voltage drop from 2V to 0V to pin VREF.
(9) See Fig. 5.

Figure 4. Switching Characteristic Definition

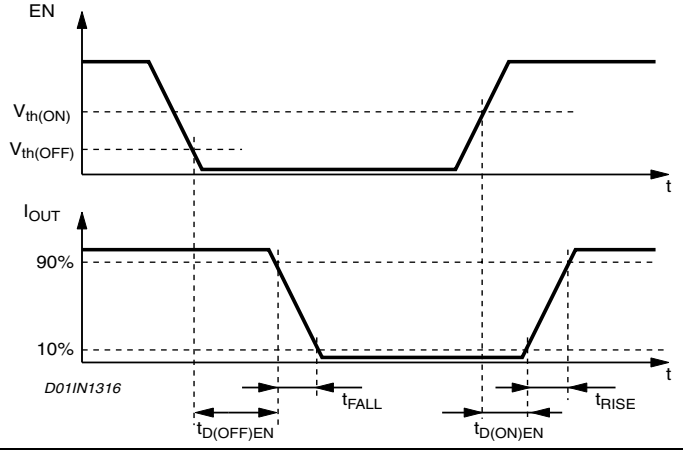
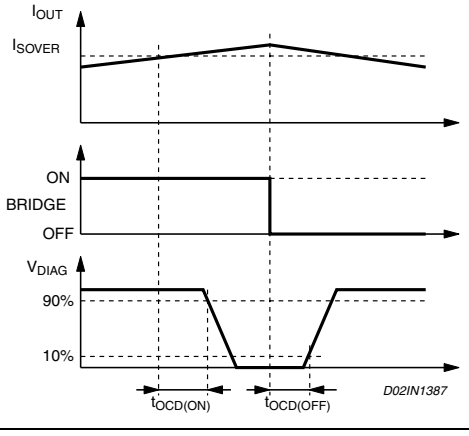


Figure 5. Overcurrent Detection Timing Definition



3 CIRCUIT DESCRIPTION

3.1 POWER STAGES and CHARGE PUMP

The L6229 integrates a Three-Phase Bridge, which consists of 6 Power MOSFETs connected as shown on the Block Diagram. Each Power MOS has an $R_{DS(ON)}$ = 0.73Ω (typical value @25°C) with intrinsic fast freewheeling diode. Switching patterns are generated by the PWM Current Controller and the Hall Effect Sensor Decoding Logic (see relative paragraphs). Cross conduction protection is implemented by using a dead time (t_{DT} = 1µs typical value) set by internal timing circuit between the turn off and turn on of two Power MOSFETs in one leg of a bridge.

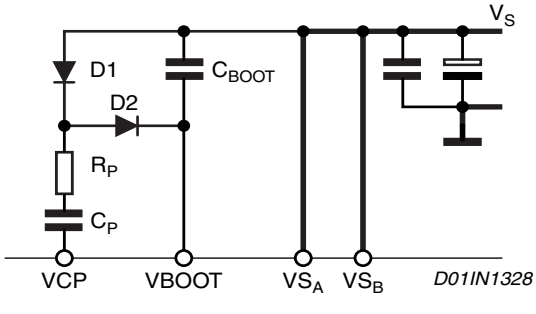
Pins VS_A and VS_B MUST be connected together to the supply voltage (V_S).

Using N-Channel Power MOS for the upper transistors in the bridge requires a gate drive voltage above the power supply voltage. The Bootstrapped Supply (V_{BOOT}) is obtained through an internal oscillator and few external components to realize a charge pump circuit as shown in Figure 6. The oscillator output (pin VCP) is a square wave at 600KHz (typically) with 10V amplitude. Recommended values/part numbers for the charge pump circuit are shown in Table 7.

Table 7. Charge Pump External Component Values.

C_{BOOT}	220nF
C_P	10nF
R_P	100Ω
D_1	1N4148
D_2	1N4148

Figure 6. Charge Pump Circuit



3.2 LOGIC INPUTS

Pins FWD/REV, BRAKE, EN, H_1, H_2 and H_3 are TTL/CMOS and µC compatible logic inputs. The internal structure is shown in Figure 4. Typical value for turn-ON and turn-OFF thresholds are respectively $V_{th(ON)}$ = 1.8V and $V_{th(OFF)}$ = 1.3V.

Pin EN (enable) may be used to implement Overcurrent and Thermal protection by connecting it to the open collector DIAG output If the protection and an external disable function are both desired, the appropriate connection must be implemented. When the external signal is from an open collector output, the circuit in Figure 8 can be used . For external circuits that are push pull outputs the circuit in Figure 9 could be used. The resistor R_{EN} should be chosen in the range from 2.2KΩ to 180KΩ. Recommended values for R_{EN} and C_{EN} are respectively 100KΩ and 5.6nF. More information for selecting the values can be found in the Overcurrent Protection section.

Figure 7. Logic Input Internal Structure

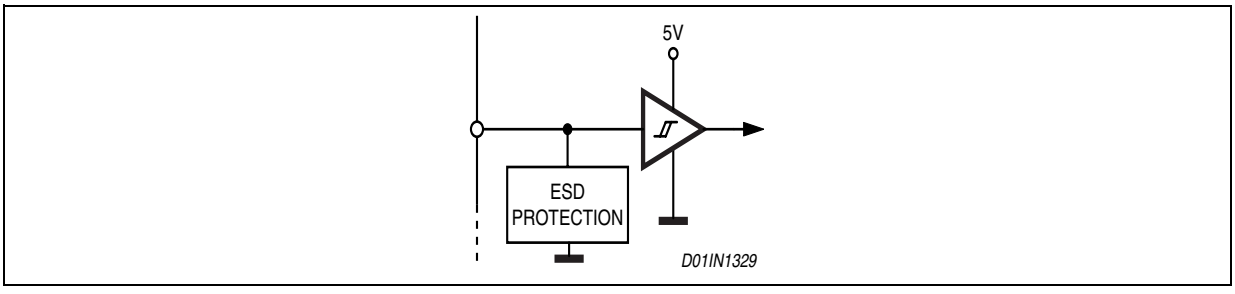


Figure 8. Pin EN Open Collector Driving

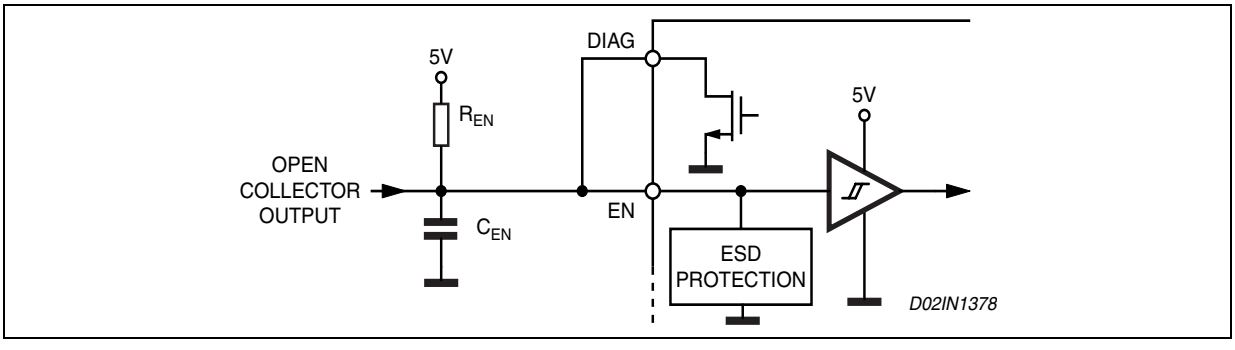
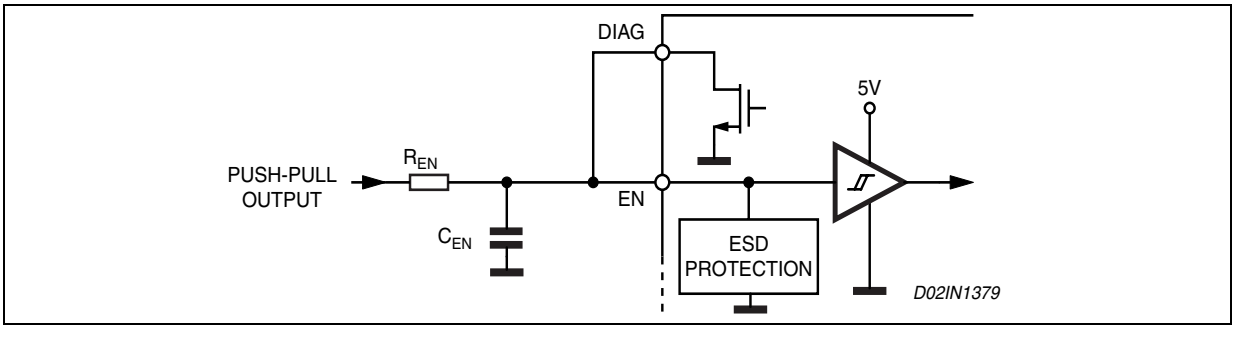


Figure 9. Pin EN Push-Pull Driving



3.3 PWM CURRENT CONTROL

The L6229 includes a constant off time PWM Current Controller. The current control circuit senses the bridge current by sensing the voltage drop across an external sense resistor connected between the source of the three lower power MOS transistors and ground, as shown in Figure 10. As the current in the motor increases the voltage across the sense resistor increases proportionally. When the voltage drop across the sense resistor becomes greater than the voltage at the reference input pin VREF the sense comparator triggers the monostable switching the bridge off. The power MOS remain off for the time set by the monostable and the motor current recirculates around the upper half of the bridge in Slow Decay Mode as described in the next section. When the monostable times out, the bridge will again turn on. Since the internal dead time, used to prevent cross conduction in the bridge, delays the turn on of the power MOS, the effective Off Time t_{OFF} is the sum of the monostable time plus the dead time.

Figure 11 shows the typical operating waveforms of the output current, the voltage drop across the sensing resistor, the pin RC voltage and the status of the bridge. More details regarding the Synchronous Rectification and the output stage configuration are included in the next section.

Immediately after the Power MOS turn on, a high peak current flows through the sense resistor due to the re-

verse recovery of the freewheeling diodes. The L6229 provides a 1µs Blanking Time t_{BLANK} that inhibits the comparator output so that the current spike cannot prematurely retrigger the monostable.

Figure 10. PWM Current Controller Simplified Schematic

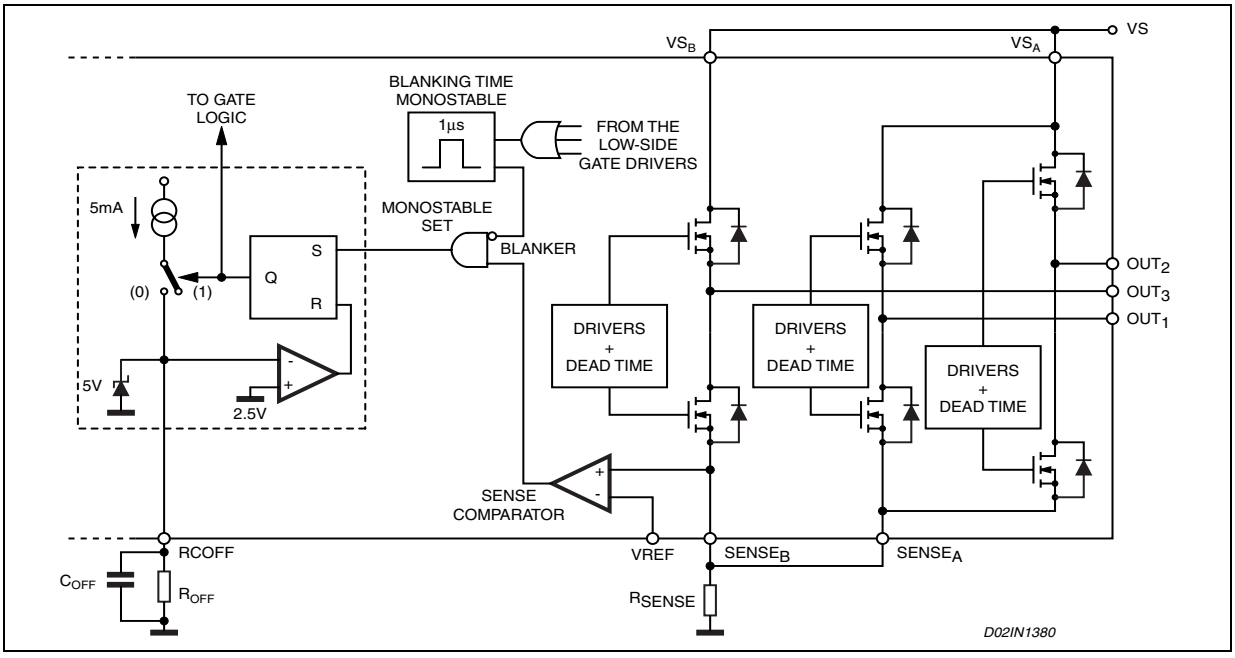


Figure 11. Output Current Regulation Waveforms

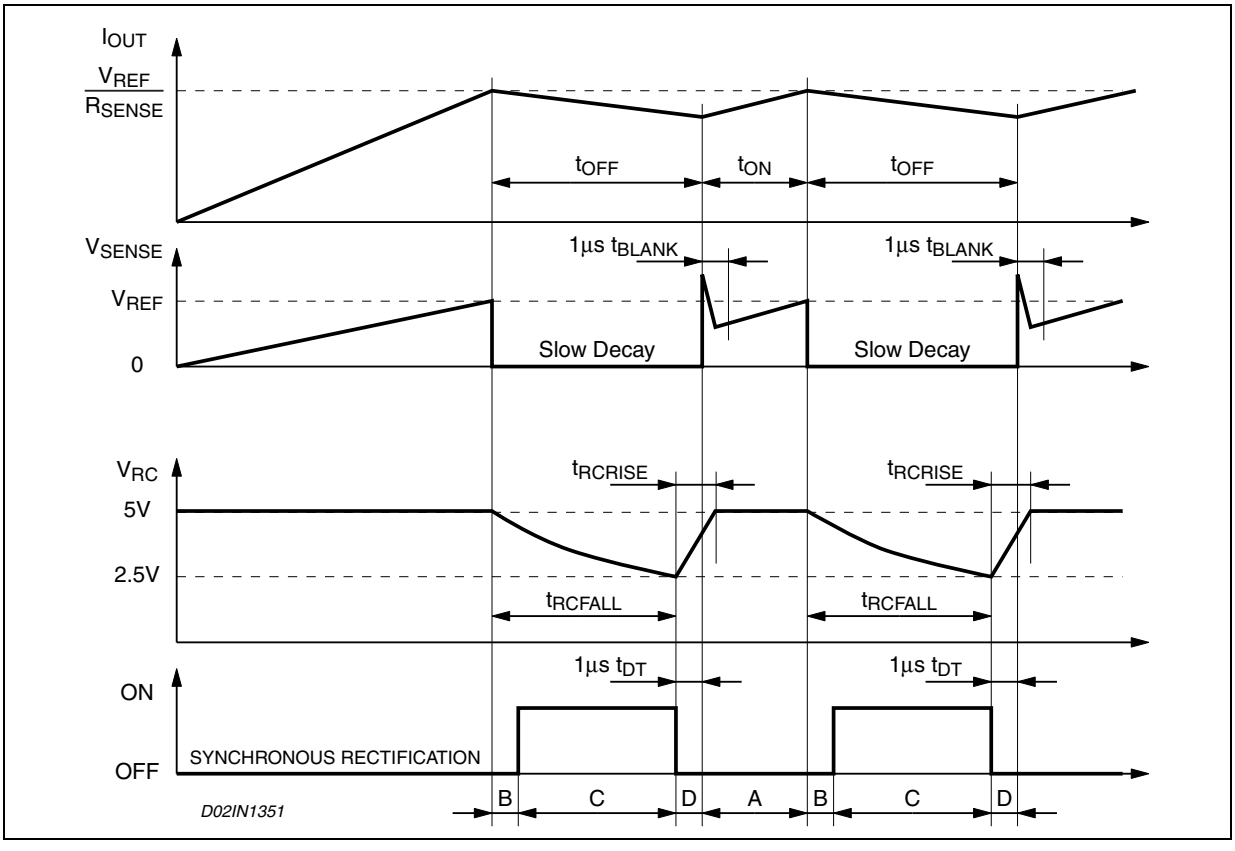


Figure 12 shows the magnitude of the Off Time t_{OFF} versus C_{OFF} and R_{OFF} values. It can be approximately calculated from the equations:

$$t_{RCFALL} = 0.6 \cdot R_{OFF} \cdot C_{OFF}$$

$$t_{OFF} = t_{RCFALL} + t_{DT} = 0.6 \cdot R_{OFF} \cdot C_{OFF} + t_{DT}$$

where R_{OFF} and C_{OFF} are the external component values and t_{DT} is the internally generated Dead Time with:

$20K\Omega \leq R_{OFF} \leq 100K\Omega$

$0.47nF \leq C_{OFF} \leq 100nF$

$t_{DT} = 1\mu s$ (typical value)

Therefore:

$$t_{OFF(MIN)} = 6.6\mu s$$

$$t_{OFF(MAX)} = 6ms$$

These values allow a sufficient range of t_{OFF} to implement the drive circuit for most motors.

The capacitor value chosen for C_{OFF} also affects the Rise Time t_{RCRISE} of the voltage at the pin RCOFF. The Rise Time t_{RCRISE} will only be an issue if the capacitor is not completely charged before the next time the monostable is triggered. Therefore, the On Time t_{ON}, which depends by motors and supply parameters, has to be bigger than t_{RCRISE} for allowing a good current regulation by the PWM stage. Furthermore, the On Time t_{ON} can not be smaller than the minimum on time $t_{ON(MIN)}$.

$$\begin{cases} t_{ON} > t_{ON(MIN)} = 2.5\mu s \text{ (typ. value)} \\ t_{ON} > t_{RCRISE} - t_{DT} \end{cases}$$

$$t_{RCRISE} = 600 \cdot C_{OFF}$$

Figure 13 shows the lower limit for the On Time t_{ON} for having a good PWM current regulation capacity. It has to be said that t_{ON} is always bigger than $t_{ON(MIN)}$ because the device imposes this condition, but it can be smaller than t_{RCRISE} - t_{DT}. In this last case the device continues to work but the Off Time t_{OFF} is not more constant.

So, small C_{OFF} value gives more flexibility for the applications (allows smaller On Time and, therefore, higher switching frequency), but, the smaller is the value for C_{OFF}, the more influential will be the noises on the circuit performance.

Figure 12. t_{OFF} versus C_{OFF} and R_{OFF}.

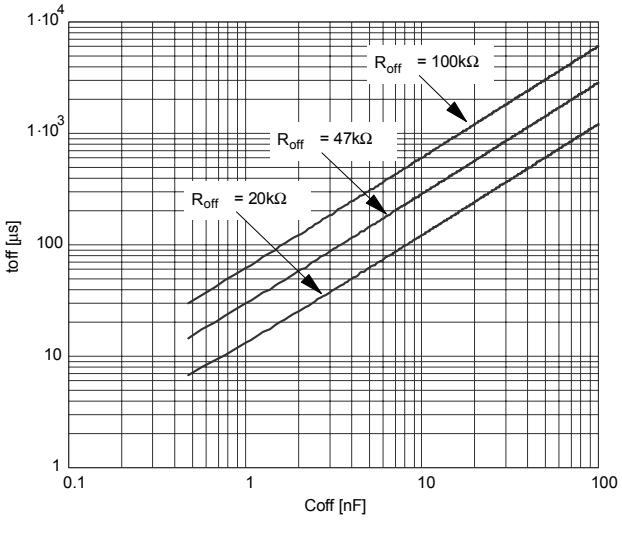
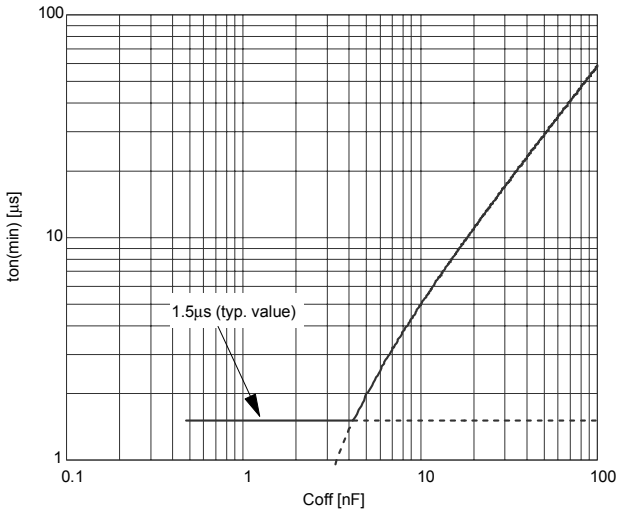


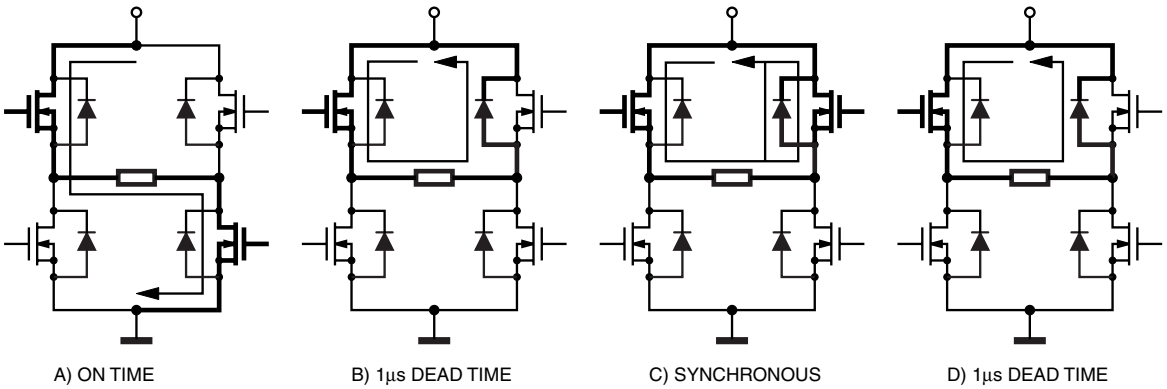
Figure 13. Area where t_{ON} can vary maintaining the PWM regulation.



3.4 SLOW DECAY MODE

Figure 14 shows the operation of the bridge in the Slow Decay mode during the Off Time. At any time only two legs of the three-phase bridge are active, therefore only the two active legs of the bridge are shown in the figure and the third leg will be off. At the start of the Off Time, the lower power MOS is switched off and the current recirculates around the upper half of the bridge. Since the voltage across the coil is low, the current decays slowly. After the Dead Time the upper power MOS is operated in the synchronous rectification mode reducing the impendence of the freewheeling diode and the related conducting losses. When the monostable times out, upper MOS that was operating the synchronous mode turns off and the lower power MOS is turned on again after some delay set by the Dead Time to prevent cross conduction.

Figure 14. Slow Decay Mode Output Stage Configurations



3.5 DECODING LOGIC

The Decoding Logic section is a combinatory logic that provides the appropriate driving of the three-phase bridge outputs according to the signals coming from the three Hall Sensors that detect rotor position in a 3-phase BLDC motor. This novel combinatory logic discriminates between the actual sensor positions for sensors spaced at 60, 120, 240 and 300 electrical degrees. This decoding method allows the implementation of a universal IC without dedicating pins to select the sensor configuration.

There are eight possible input combinations for three sensor inputs. Six combinations are valid for rotor positions with 120 electrical degrees sensor phasing (see Figure 15, positions 1, 2, 3a, 4, 5 and 6a) and six combinations are valid for rotor positions with 60 electrical degrees phasing (see Figure 17, positions 1, 2, 3b, 4, 5 and 6b). Four of them are in common (1, 2, 4 and 5) whereas there are two combinations used only in 120 electrical degrees sensor phasing (3a and 6a) and two combinations used only in 60 electrical degrees sensor phasing (3b and 6b).

The decoder can drive motors with different sensor configuration simply by following the Table 8. For any input configuration (H_1, H_2 and H_3) there is one output configuration (OUT_1, OUT_2 and OUT_3). The output configuration 3a is the same than 3b and analogously output configuration 6a is the same than 6b.

The sequence of the Hall codes for 300 electrical degrees phasing is the reverse of 60 and the sequence of the Hall codes for 240 phasing is the reverse of 120. So, by decoding the 60 and the 120 codes it is possible to drive the motor with all the four conventions by changing the direction set.

Table 8. 60 and 120 Electrical Degree Decoding Logic in Forward Direction.

Hall 120°	1	2	3a	-	4	5	6a	-
Hall 60°	1	2	-	3b	4	5	-	6b
H_1	H	H	L	H	L	L	H	L
H_2	L	H	H	H	H	L	L	L
H_3	L	L	L	H	H	H	H	L
OUT_1	Vs	High Z	GND	GND	GND	High Z	Vs	Vs
OUT_2	High Z	Vs	Vs	Vs	High Z	GND	GND	GND
OUT_3	GND	GND	High Z	High Z	Vs	Vs	High Z	High Z
Phasing	1->3	2->3	2->1	2->1	3->1	3->2	1->2	1->2

Figure 15. 120° Hall Sensor Sequence.

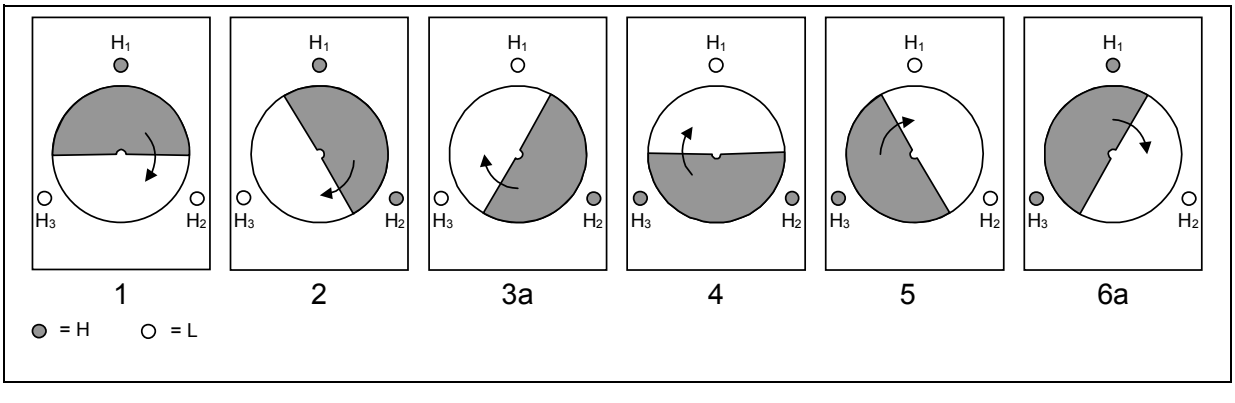
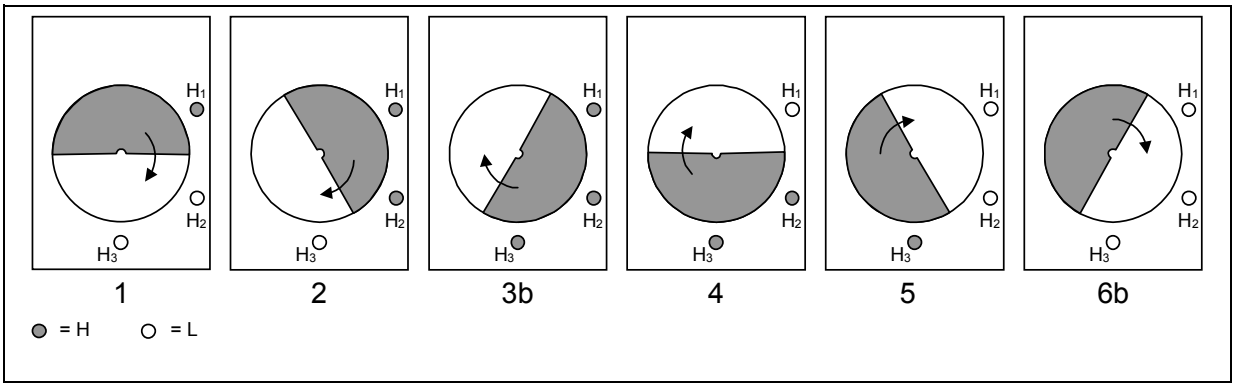


Figure 16. 60° Hall Sensor Sequence.



3.6 TACHO

A tachometer function consists of a monostable, with constant off time (t_{PULSE}), whose input is one Hall Effect signal (H_1). It allows developing an easy speed control loop by using an external op amp, as shown in Figure 18. For component values refer to Application Information section.

The monostable output drives an open drain output pin (TACHO). At each rising edge of the Hall Effect Sensors H_1, the monostable is triggered and the MOSFET connected to pin TACHO is turned off for a constant time t_{PULSE} (see Figure 17). The off time t_{PULSE} can be set using the external RC network (R_{PUL}, C_{PUL}) connected to the pin RCPULSE. Figure 19 gives the relation between t_{PULSE} and C_{PUL}, R_{PUL}. We have approximately:

$$t_{PULSE} = 0.6 \cdot R_{PUL} \cdot C_{PUL}$$

where C_{PUL} should be chosen in the range 1nF … 100nF and R_{PUL} in the range 20KΩ … 100KΩ.

By connecting the tachometer pin to an external pull-up resistor, the output signal average value V_M is proportional to the frequency of the Hall Effect signal and, therefore, to the motor speed. This realizes a simple Frequency-to-Voltage Converter. An op amp, configured as an integrator, filters the signal and compares it with a reference voltage V_{REF}, which sets the speed of the motor.

$$V_M = \frac{t_{PULSE}}{T} \cdot V_{DD}$$

Figure 17. Tacho Operation Waveforms.

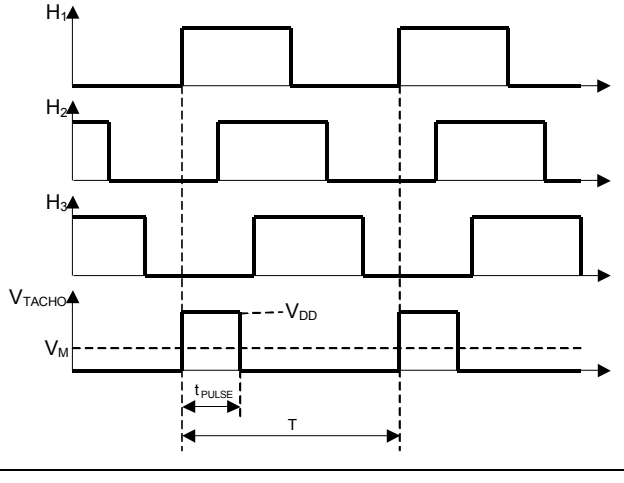


Figure 18. Tachometer Speed Control Loop.

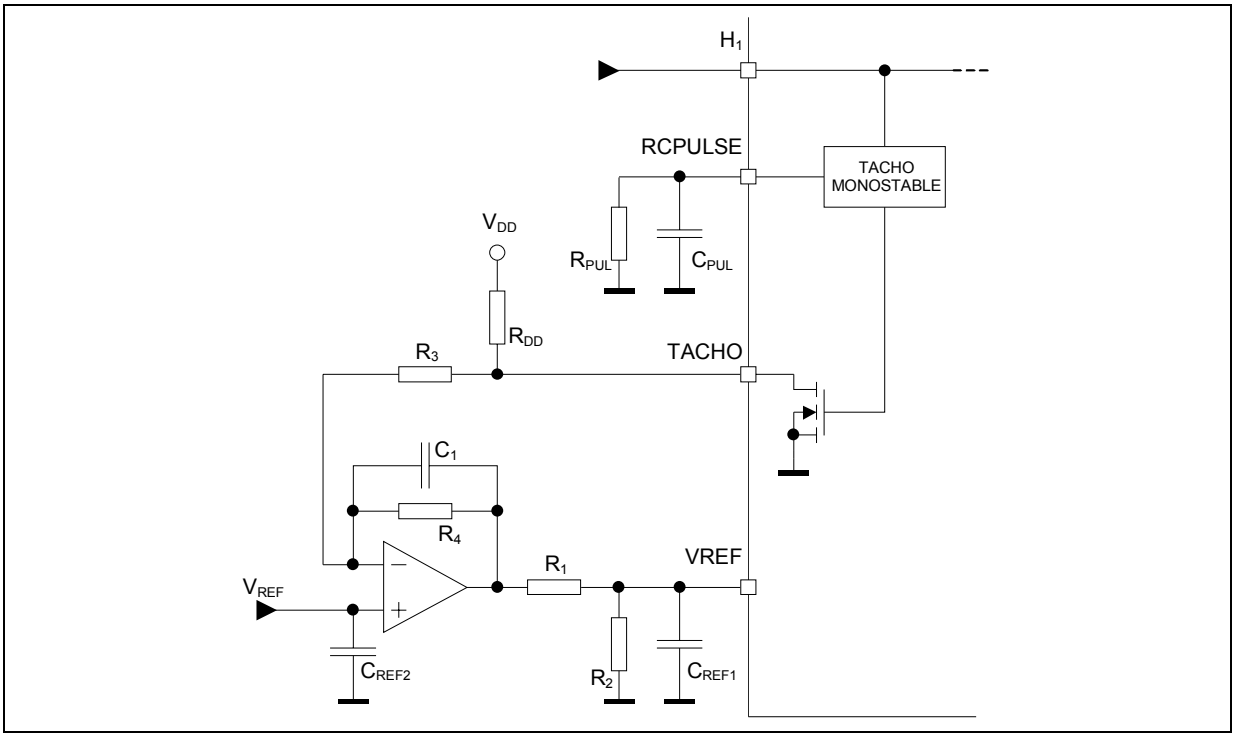
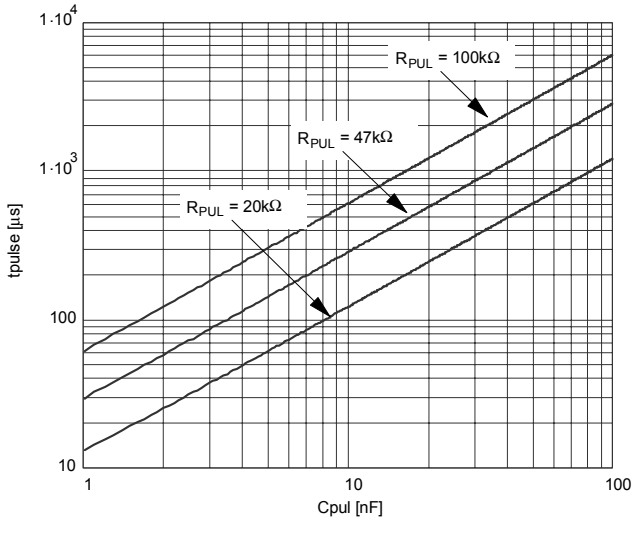


Figure 19. t_{PULSE} versus C_{PUL} and R_{PUL}.



3.7 NON-DISSIPATIVE OVERCURRENT DETECTION and PROTECTION

The L6229 integrates an Overcurrent Detection Circuit (OCD) for full protection. This circuit provides Output-to-Output and Output-to-Ground short circuit protection as well. With this internal over current detection, the external current sense resistor normally used and its associated power dissipation are eliminated. Figure 20 shows a simplified schematic for the overcurrent detection circuit.

To implement the over current detection, a sensing element that delivers a small but precise fraction of the output current is implemented with each High Side power MOS. Since this current is a small fraction of the output current there is very little additional power dissipation. This current is compared with an internal reference current I_{REF}. When the output current reaches the detection threshold (typically I_{SOVER} = 2.8A) the OCD comparator signals a fault condition. When a fault condition is detected, an internal open drain MOS with a pull down capability of 4mA connected to pin DIAG is turned on.

The pin DIAG can be used to signal the fault condition to a µC or to shut down the Three-Phase Bridge simply by connecting it to pin EN and adding an external R-C (see R_{EN}, C_{EN}).

Figure 20. Overcurrent Protection Simplified Schematic

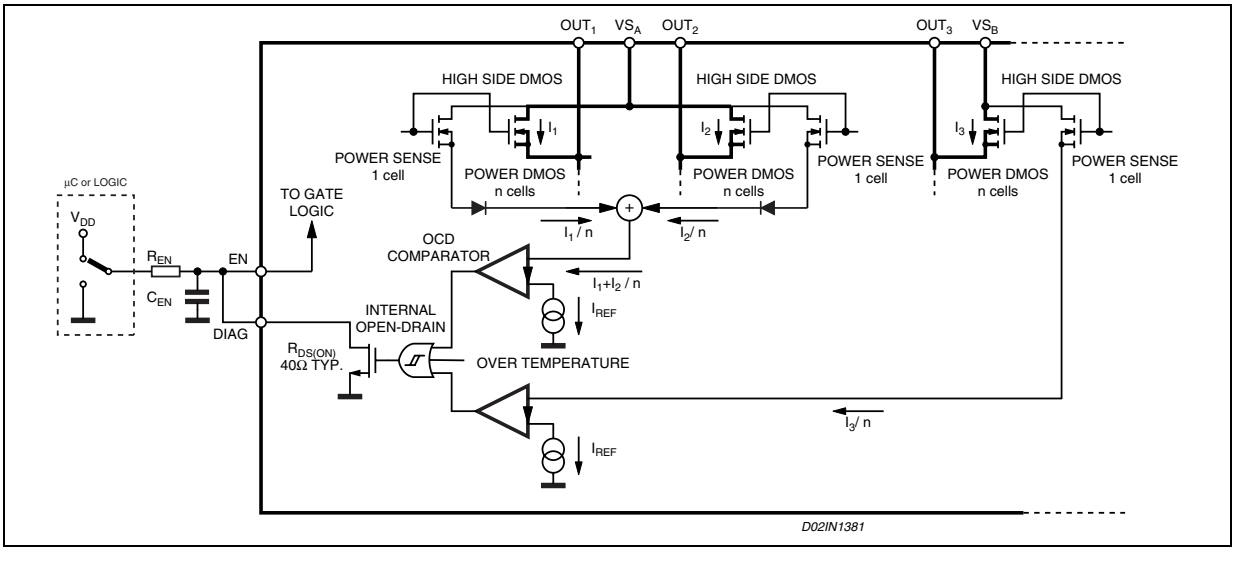


Figure 21 shows the Overcurrent Detetection operation. The Disable Time $t_{DISABLE}$ before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs. It is affected whether by C_{EN} and R_{EN} values and its magnitude is reported in Figure 22. The Delay Time t_{DELAY} before turning off the bridge when an overcurrent has been detected depends only by C_{EN} value. Its magnitude is reported in Figure 23

C_{EN} is also used for providing immunity to pin EN against fast transient noises. Therefore the value of C_{EN} should be chosen as big as possible according to the maximum tolerable Delay Time and the R_{EN} value should be chosen according to the desired Disable Time.

The resistor R_{EN} should be chosen in the range from 2.2KΩ to 180KΩ. Recommended values for R_{EN} and C_{EN} are respectively 100KΩ and 5.6nF that allow obtaining 200µs Disable Time.

Figure 21. Overcurrent Protection Waveforms

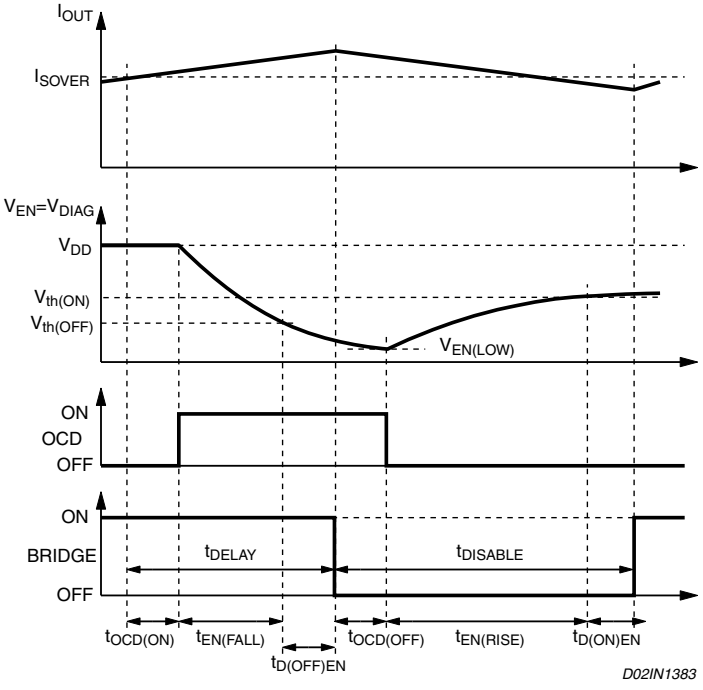


Figure 22. $t_{DISABLE}$ versus C_{EN} and R_{EN}.

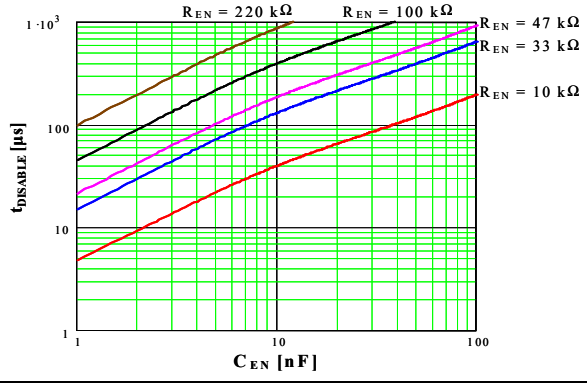
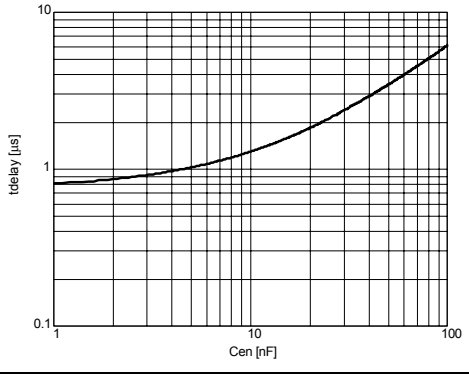


Figure 23. t_{DELAY} versus C_{EN}.



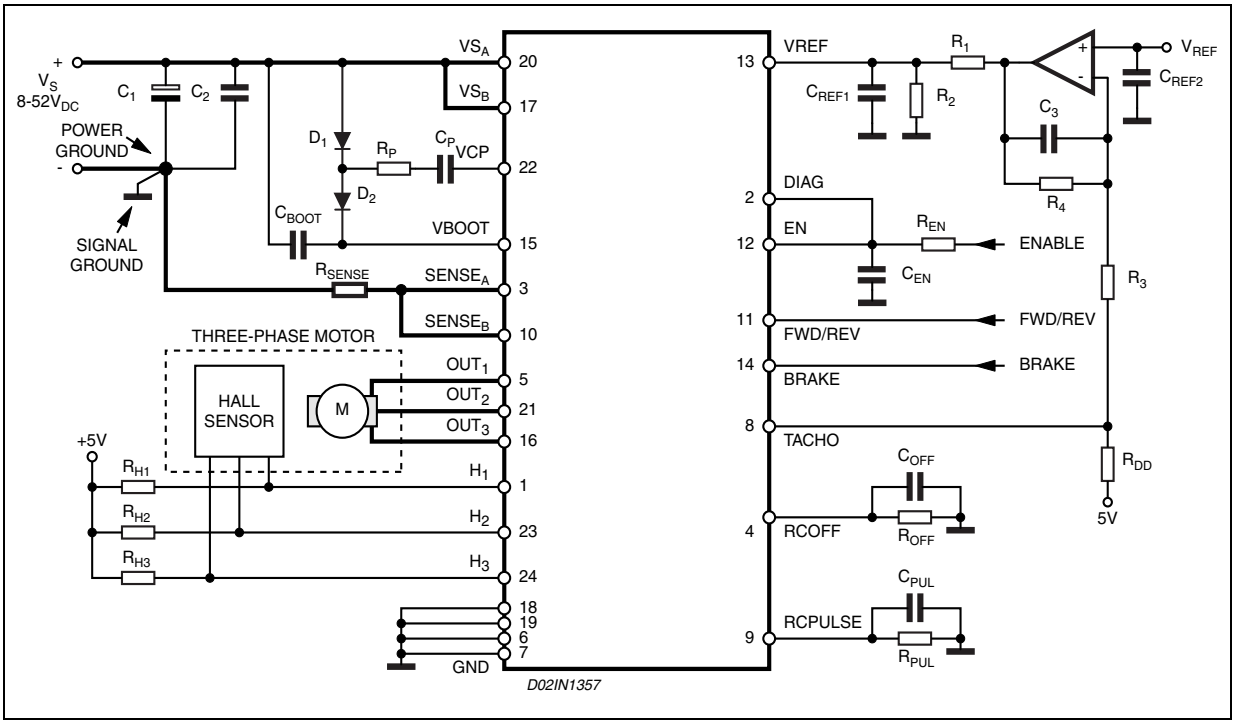
4 APPLICATION INFORMATION

A typical application using L6229 is shown in Figure 24. Typical component values for the application are shown in Table 9. A high quality ceramic capacitor (C_2) in the range of 100nF to 200nF should be placed between the power pins VS_A and VS_B and ground near the L6229 to improve the high frequency filtering on the power supply and reduce high frequency transients generated by the switching. The capacitor (C_{EN}) connected from the EN input to ground sets the shut down time when an over current is detected (see Overcurrent Protection). The two current sensing inputs ($SENSE_A$ and $SENSE_B$) should be connected to the sensing resistor R_{SENSE} with a trace length as short as possible in the layout. The sense resistor should be non-inductive resistor to minimize the di/dt transients across the resistor. To increase noise immunity, unused logic pins are best connected to 5V (High Logic Level) or GND (Low Logic Level) (see pin description). It is recommended to keep Power Ground and Signal Ground separated on PCB.

Table 9. Component Values for Typical Application.

C_1	100µF	R_1	5K6Ω
C_2	100nF	R_2	1K8Ω
C_3	220nF	R_3	4K7Ω
C_{BOOT}	220nF	R_4	1MΩ
C_{OFF}	1nF	R_{DD}	1KΩ
C_{PUL}	10nF	R_{EN}	100KΩ
C_{REF1}	33nF	R_P	100Ω
C_{REF2}	100nF	R_{SENSE}	0.6Ω
C_{EN}	5.6nF	R_{OFF}	33KΩ
C_P	10nF	R_{PUL}	47KΩ
D_1	1N4148	R_{H1}, R_{H2}, R_{H3}	10KΩ
D_2	1N4148		

Figure 24. Typical Application

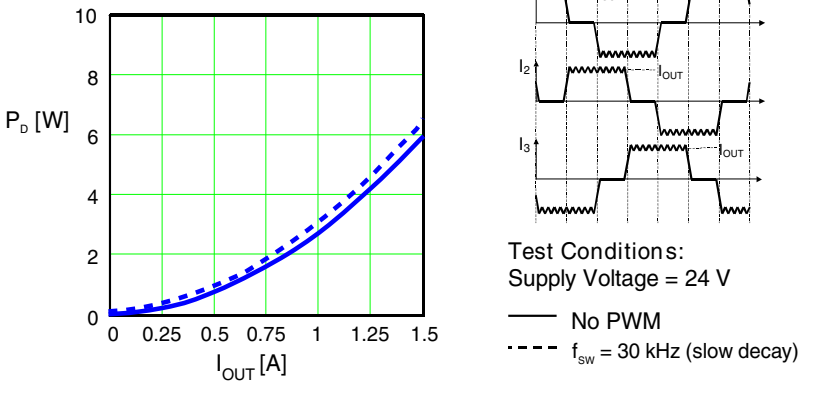


4.1 OUTPUT CURRENT CAPABILITY AND IC POWER DISSIPATION

In Figure 25 is shown the approximate relation between the output current and the IC power dissipation using PWM current control.

For a given output current the power dissipated by the IC can be easily evaluated, in order to establish which package should be used and how large must be the on-board copper dissipating area to guarantee a safe operating junction temperature (125°C maximum).

Figure 25. IC Power Dissipation versus Output Power.



4.2 THERMAL MANAGEMENT

In most applications the power dissipation in the IC is the main factor that sets the maximum current that can be delivered by the device in a safe operating condition. Selecting the appropriate package and heatsinking configuration for the application is required to maintain the IC within the allowed operating temperature range for the application. Figures 26, 27 and 28 show the Junction-to-Ambient Thermal Resistance values for the PowerSO36, PowerDIP24 and SO24 packages.

For instance, using a PowerSO package with copper slug soldered on a 1.5mm copper thickness FR4 board with 6cm^2 dissipating footprint (copper thickness of 35µm), the $R_{th(j\text{-}amb)}$ is about 35°C/W. Figure 29 shows mounting methods for this package. Using a multi-layer board with vias to a ground plane, thermal impedance can be reduced down to 15°C/W.

Figure 26. PowerSO36 Junction-Ambient thermal resistance versus on-board copper area.

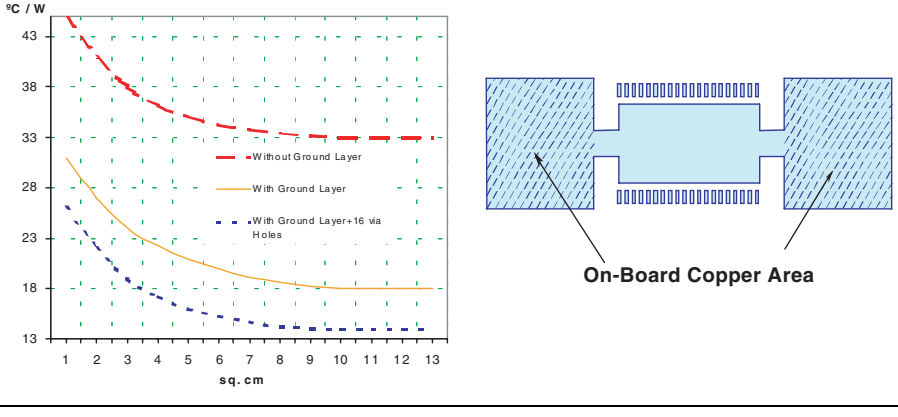


Figure 27. PowerDIP24 Junction-Ambient thermal resistance versus on-board copper area.

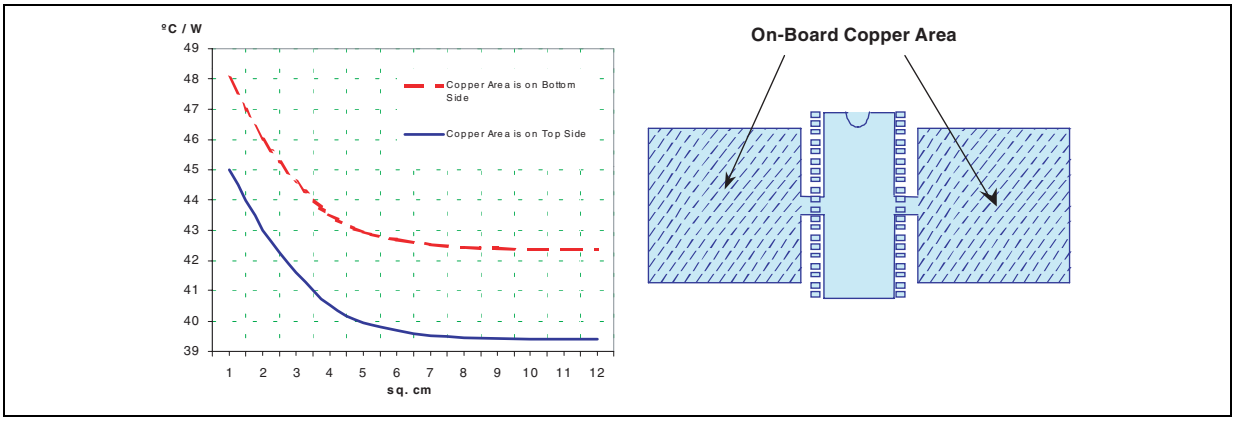


Figure 28. SO24 Junction-Ambient thermal resistance versus on-board copper area.

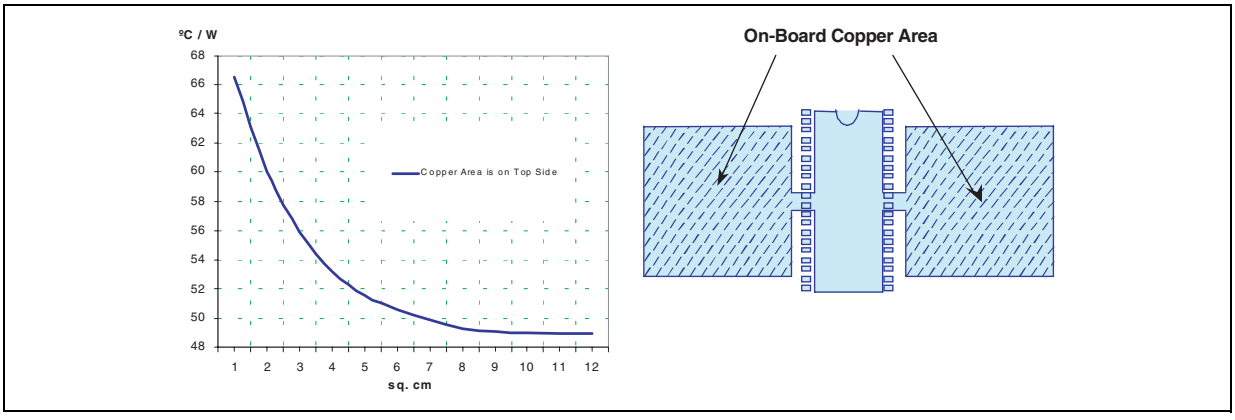


Figure 29. Mounting the PowerSO Package.

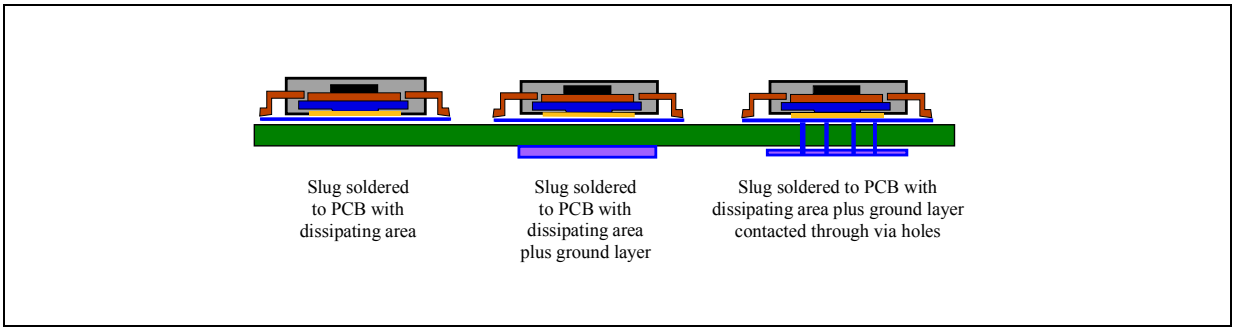
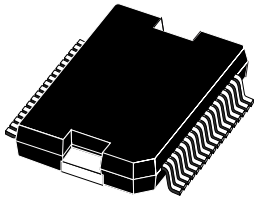


Figure 30. PowerSO36 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.25		3.5	0.128		0.138
A2			3.3			0.13
A4	0.8		1	0.031		0.039
A5		0.2			0.008	
a1	0		0.075	0		0.003
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D	15.8		16	0.622		0.630
D1	9.4		9.8	0.37		0.38
D2		1			0.039	
E	13.9		14.5	0.547		0.57
E1	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
E4	2.9		3.2	0.114		1.259
e		0.65			0.026	
e3		11.05			0.435	
G	0		0.075	0		0.003
H	15.5		15.9	0.61		0.625
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	10˚ (max)					
s	8˚ (max)					

Note: “D and E1” do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006”)
- Critical dimensions are "a3", "E" and "G".

OUTLINE AND MECHANICAL DATA



PowerSO36

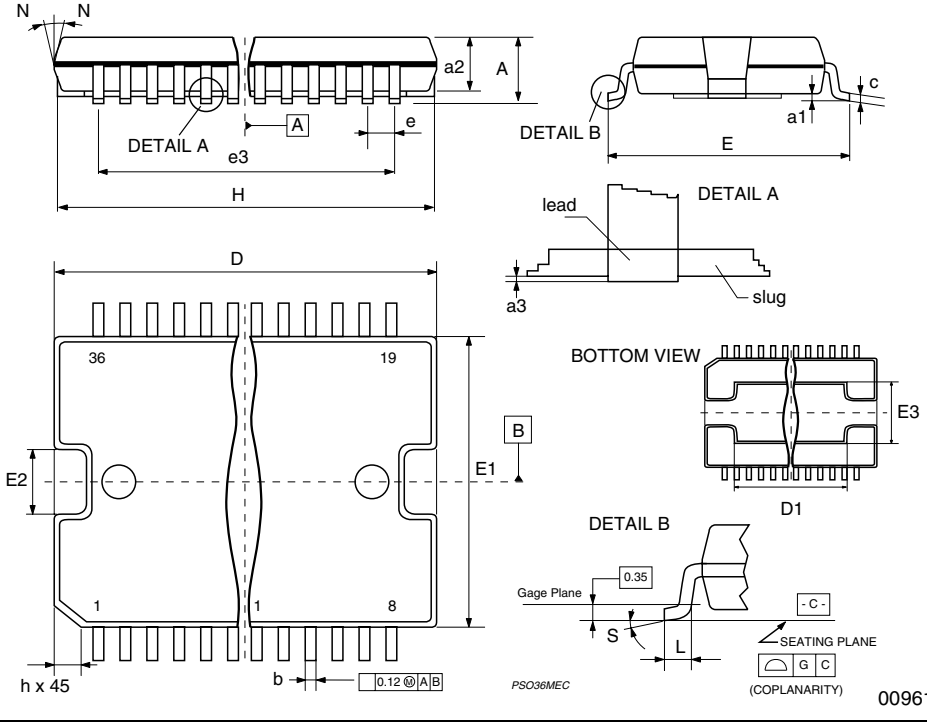
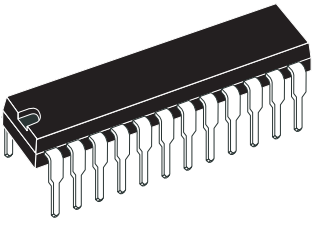


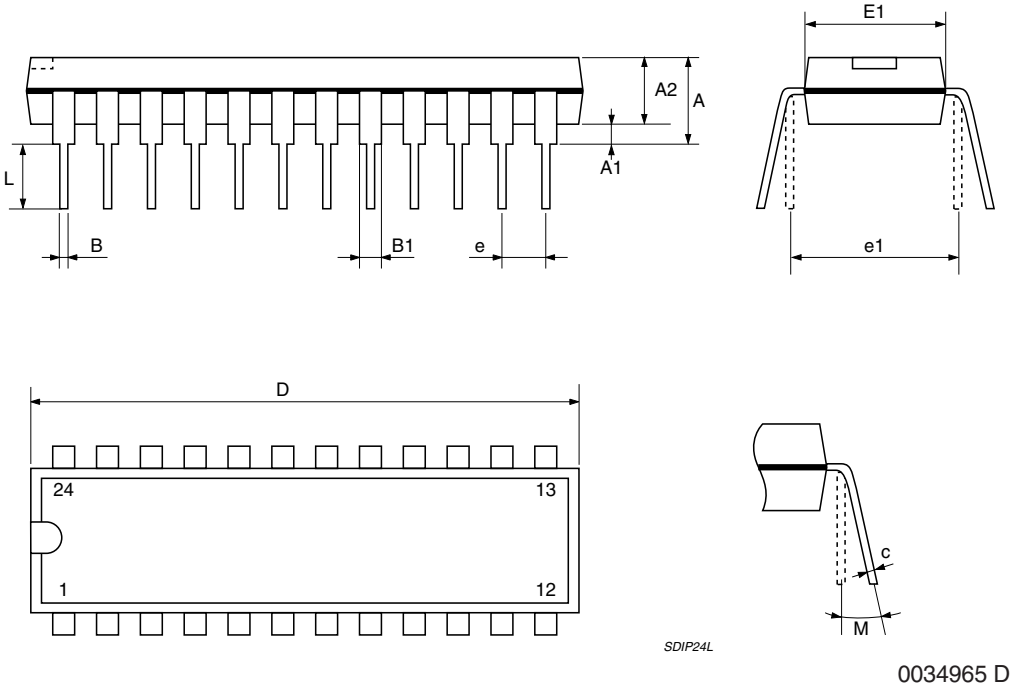
Figure 31. PDIP-24 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.320			0.170
A1	0.380			0.015		
A2		3.300			0.130	
B	0.410	0.460	0.510	0.016	0.018	0.020
B1	1.400	1.520	1.650	0.055	0.060	0.065
c	0.200	0.250	0.300	0.008	0.010	0.012
D	31.62	31.75	31.88	1.245	1.250	1.255
E	7.620		8.260	0.300		0.325
e		2.54			0.100	
E1	6.350	6.600	6.860	0.250	0.260	0.270
e1		7.620			0.300	
L	3.180		3.430	0.125		0.135
M	0° min, 15° max.					

OUTLINE AND MECHANICAL DATA



PDIP 24 (0.300")



0034965 D

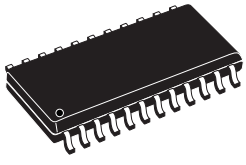
Figure 32. SO24 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	15.20		15.60	0.598		0.614
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA

Weight: 0.60gr



SO24

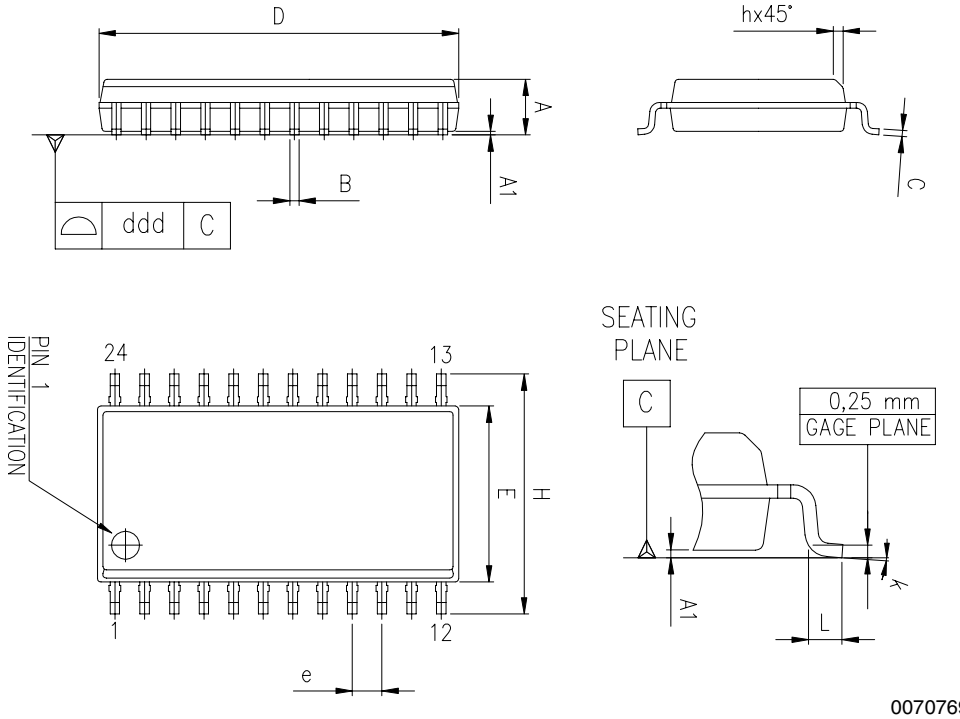


Table 10. Revision History

Date	Revision	Description of Changes
September 2003	1	First Issue
January 2004	2	Migration from ST-Press dms to EDOCS.
October 2004	3	Updated the style graphic form.