

**Stratix IV Device Handbook** 

# **Volume 4: Device Datasheet and Addendum**



101 Innovation Drive San Jose, CA 95134 www.altera.com

SIV5V4-5.3

© 2012 Altera Corporation. All rights reserved. ALTERA, ARRIA, CYCLONE, HARDCOPY, MAX, MEGACORE, NIOS, QUARTUS and STRATIX words and logos are trademarks of Altera Corporation and registered in the U.S. Patent and Trademark Office and in other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders as described at www.altera.com/common/legal.html. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.



## **Contents**



Chapter Revision Dates	 •••	. v

## Section I. Device Datasheet and Addendum for Stratix IV Devices

## Chapter 1. DC and Switching Characteristics for Stratix IV Devices

Electrical Characteristics	1–1
Operating Conditions	1–1
Absolute Maximum Ratings	1–1
Recommended Operating Conditions	
DC Characteristics	1–7
Internal Weak Pull-Up Resistor	1–11
I/O Standard Specifications	
Power Consumption	1–15
Switching Characteristics	
Transceiver Performance Specifications	
Transceiver Datapath PCS Latency	1–47
Core Performance Specifications	
Clock Tree Specifications	1–47
PLL Specifications	1–48
DSP Block Specifications	1–50
TriMatrix Memory Block Specifications	1–51
Configuration and JTAG Specifications	
Temperature Sensing Diode Specifications	1–53
Chip-Wide Reset (Dev_CLRn) Specifications	1–54
Periphery Performance	1–54
High-Speed I/O Specification	
OCT Calibration Block Specifications	
Duty Cycle Distortion (DCD) Specifications	1–62
I/O Timing	
Programmable IOE Delay	
Programmable Output Buffer Delay	1–63
Glossary	1–64
Document Revision History	1–67

### Chapter 2. Addendum to the Stratix IV Device Handbook

### **Additional Information**

How to Contact Altera	. 2	-1
Typographic Conventions	. 2	-1

## **Chapter Revision Dates**



The chapters in this document, Stratix IV Device Handbook, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

- Chapter 1. DC and Switching Characteristics for Stratix IV Devices Revised: July 2012 Part Number: SIV54001-5.3
- Chapter 2. Addendum to the Stratix IV Device Handbook Revised: *February* 2011 Part Number: *SIV54002-1.5*



## Section I. Device Datasheet and Addendum for Stratix IV Devices

This section includes the following chapters:

- Chapter 1, DC and Switching Characteristics for Stratix IV Devices
- Chapter 2, Addendum to the Stratix IV Device Handbook

## **Revision History**

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.



## 1. DC and Switching Characteristics for Stratix IV Devices

#### SIV54001-5.3

This chapter contains the following sections:

- "Electrical Characteristics"
- "Switching Characteristics"
- "I/O Timing"
- "Glossary"

## **Electrical Characteristics**

This chapter covers the electrical and switching characteristics for Stratix<sup>®</sup> IV devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This chapter also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.



For information regarding the densities and packages of devices in the Stratix IV family, refer to the *Stratix IV Device Family Overview* chapter.

## **Operating Conditions**

When you use Stratix IV devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Stratix IV devices, you must consider the operating requirements described in this chapter.

Stratix IV devices are offered in commercial, industrial, and military grades. Commercial devices are offered in -2 (fastest),  $-2\times$ , -3, and -4 speed grades. Industrial devices are offered in -1, -2, -3, and -4 speed grades. Military devices are offered in -3 speed grade.

For the Stratix IV GT -1 and -2 speed grade specifications, refer to the  $-2/-2 \times$  speed grade column. For the Stratix IV GT -3 speed grade specification, refer to the -3 speed grade column, unless otherwise specified.

### **Absolute Maximum Ratings**

Absolute maximum ratings define the maximum operating conditions for Stratix IV devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

© 2012 Altera Corporation. All rights reserved. ALTERA, ARRIA, CYCLONE, HARDCOPY, MAX, MEGACORE, NIOS, QUARTUS and STRATIX words and logos are trademarks of Altera Corporation and registered in the U.S. Patent and Trademark Office and in other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders as described at www.altera.com/common/legal.html. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and service at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.







Conditions other than those listed in Table 1–1, Table 1–2, and Table 1–3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Symbol	Description	Minimum	Maximum	Unit
V <sub>CC</sub>	Core voltage and periphery circuitry power supply	-0.5	1.35	V
V <sub>CCPT</sub>	Power supply for programmable power technology	-0.5	1.8	V
V <sub>CCPGM</sub>	Configuration pins power supply	-0.5	3.75	V
V <sub>CCAUX</sub>	Auxiliary supply for the programmable power technology	-0.5	3.75	V
V <sub>CCBAT</sub>	Battery back-up power supply for design security volatile key register	-0.5	3.75	V
V <sub>CCPD</sub>	I/O pre-driver power supply	-0.5	3.75	V
V <sub>CCIO</sub>	I/O power supply	-0.5	3.9	V
V <sub>CC_CLKIN</sub>	Differential clock input power supply	-0.5	3.75	V
V <sub>CCD_PLL</sub>	PLL digital power supply	-0.5	1.35	V
V <sub>CCA_PLL</sub>	PLL analog power supply	-0.5	3.75	V
VI	DC input voltage	-0.5	4.0	V
I <sub>OUT</sub>	DC output current per pin	-25	40	mA
TJ	Operating junction temperature	-55	125	°C
T <sub>STG</sub>	Storage temperature (No bias)	-65	150	°C

Table 1–1. Absolute Maximum Ratings for Stratix IV Devices

Table 1–2. Transceiver Power Supply Absolute Maximum Ratings for Stratix IV GX Devices

Symbol	Description	Minimum	Maximum	Unit
V <sub>CCA_L</sub>	Transceiver high voltage power (left side)	-0.5	3.75	V
V <sub>CCA_R</sub>	Transceiver high voltage power (right side)	-0.5	3.75	V
V <sub>CCHIP_L</sub>	Transceiver HIP digital power (left side)	-0.5	1.35	V
V <sub>CCHIP_R</sub>	Transceiver HIP digital power (right side)	-0.5	1.35	V
V <sub>CCR_L</sub>	Receiver power (left side)	-0.5	1.35	V
V <sub>CCR_R</sub>	Receiver power (right side)	-0.5	1.35	V
V <sub>CCT_L</sub>	Transmitter power (left side)	-0.5	1.35	V
V <sub>CCT_R</sub>	Transmitter power (right side)	-0.5	1.35	V
V <sub>CCL_GXBLn</sub> <sup>(1)</sup>	Transceiver clock power (left side)	-0.5	1.35	V
V <sub>CCL_GXBRn</sub> <sup>(1)</sup>	Transceiver clock power (right side)	-0.5	1.35	V
V <sub>CCH_GXBLn</sub> <sup>(1)</sup>	Transmitter output buffer power (left side)	-0.5	1.8	V
V <sub>CCH_GXBRn</sub> <sup>(1)</sup>	Transmitter output buffer power (right side)	-0.5	1.8	V

Note to Table 1–2:

(1) n = 0, 1, 2, or 3.

Symbol	Description	Minimum	Maximum	Unit
V <sub>CCA_L</sub>	Transceiver high voltage power (left side)	-0.5	3.75	V
V <sub>CCA_R</sub>	Transceiver high voltage power (right side)	-0.5	3.75	V
V <sub>CCHIP_L</sub>	Transceiver HIP digital power (left side)	-0.5	1.35	V
V <sub>CCHIP_R</sub>	Transceiver HIP digital power (right side)	-0.5	1.35	V
V <sub>CCR_L</sub>	Receiver power (left side)	-0.5	1.35	V
V <sub>CCR_R</sub>	Receiver power (right side)	-0.5	1.35	V
V <sub>CCT_L</sub>	Transmitter power (left side)	-0.5	1.35	V
V <sub>CCT_R</sub>	Transmitter power (right side)	-0.5	1.35	V
$V_{CCL\_GXBLn}$ (2)	Transceiver clock power (left side)	-0.5	1.35	V
V <sub>CCL_GXBRn</sub> <sup>(2)</sup>	Transceiver clock power (right side)	-0.5	1.35	V
$V_{CCH\_GXBLn}$ (2)	Transmitter output buffer power (left side)	-0.5	1.8	V
$V_{CCH\_GXBRn}$ <sup>(2)</sup>	Transmitter output buffer power (right side)	-0.5	1.8	V

Table 1–3. Transceiver Power Supply Absolute Maximum Ratings for Stratix IV GT Devices (1)

#### Notes to Table 1-3:

(1) For the absolute maximum ratings for Stratix IV GT engineering sample (ES1) devices, contact your local Altera sales representative.

(2) n = 0, 1, 2, or 3.

#### **Maximum Allowed Overshoot and Undershoot Voltage**

During transitions, input signals may overshoot to the voltage shown in Table 1–4 and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 1–4 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for ~5% over the lifetime of the device; for a device lifetime of 10 years, this amounts to half of a year.

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
		4.0	100.000	%
		4.05	79.330	%
		4.1	46.270	%
		4.15	27.030	%
		4.2	15.800	%
		4.25	9.240	%
Vi (AC)	AC input voltage	4.3	5.410	%
		4.35	3.160	%
		4.4	1.850	%
		4.45	1.080	%
		4.5	0.630	%
		4.55	0.370	%
		4.6	0.220	%

Table 1-4. Maximum Allowed Overshoot During Transitions

#### **Temperature Overshoot Above Maximum Allowed Temperature**

The maximum allowed operating temperature for Stratix IV industrial grade devices is 100 °C. It is recommended that the operating temperature of the device is maintained below 100 °C at all times. The temperature excursions over 100 °C due to internal heating of the device should not exceed the number of cycles as specified in the Table 1–5. Exceeding the recommended number of cycles may cause solder interconnect failures. Altera<sup>®</sup> recommends using the Stratix IV military grade devices if the application requires operating temperatures over 100 °C.

Description	Operating Temperature (°C)	Number of Cycles Over 100 °C
	100	3200
Device operating	105	768
	110	640
temperature (°C)	115	480
	120	320
	125	160

## **Recommended Operating Conditions**

This section lists the functional operation limits for AC and DC parameters for Stratix IV devices. Table 1–6 lists the steady-state voltage and current values expected from Stratix IV devices. Power supply ramps must all be strictly monotonic, without plateaus.

**For power supply ripple requirements, refer to the** *Device-Specific Power Delivery Network (PDN) Tool User Guide.* 

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V <sub>CC</sub> (Stratix IV GX and Stratix IV E)			0.87	0.90	0.93	V
V <sub>CC</sub> (Stratix IV GT)	Core voltage and periphery circuitry power supply	—	0.92	0.95	0.98	V
V <sub>CCPT</sub>	Power supply for programmable power technology	—	1.45	1.5	1.55	V
V <sub>CCAUX</sub>	Auxiliary supply for the programmable power technology	—	2.375	2.5	2.625	V
V (2)	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
V <sub>CCPD</sub> <sup>(2)</sup>	I/O pre-driver (2.5 V) power supply	_	2.375	2.5	2.625	V
	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	_	2.375	2.5	2.625	V
V <sub>CCIO</sub>	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	_	1.425	1.5	1.575	V
	I/O buffers (1.2 V) power supply	_	1.14	1.2	1.26	V
	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
V <sub>CCPGM</sub>	Configuration pins (2.5 V) power supply	_	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V <sub>CCA_PLL</sub>	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V <sub>CCD_PLL</sub> (Stratix IV GX and Stratix IV E)	PLL digital voltage regulator power supply	_	0.87	0.90	0.93	V
V <sub>CCD_PLL</sub> (Stratix IV GT)	PLL digital voltage regulator power supply	_	0.92	0.95	0.98	V
V <sub>CC_CLKIN</sub>	Differential clock input power supply	—	2.375	2.5	2.625	V
V <sub>CCBAT</sub> <sup>(1)</sup>	Battery back-up power supply (For design security volatile key register)	—	1.2	_	3.3	V
VI	DC input voltage	—	-0.5	_	3.6	V
V <sub>0</sub>	Output voltage	—	0	_	V <sub>CCIO</sub>	V
T (0)		Commercial	0	—	85	°C
$T_J$ (Stratix IV GX and Stratix IV E)	Operating junction temperature	Industrial	-40	—	100	°C
		Military	-55	—	125	°C
T <sub>J</sub> (Stratix IV GT)	Operating junction temperature	Industrial	0	_	100	°C

 Table 1–6. Recommended Operating Conditions for Stratix IV Devices (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
t <sub>RAMP</sub>	Power supply ramp time	Normal POR (PORSEL=0)	0.05	_	100	ms
	Power supply ramp time	Fast POR (PORSEL=1)	0.05		4	ms

Table 1–6. F	Recommended Op	perating Conditions	for Stratix IV Devices	(Part 2 of 2)
--------------	----------------	---------------------	------------------------	---------------

Notes to Table 1-6:

(1) If you do not use the volatile security key, you may connect the  $V_{CCBAT}$  to either GND or a 3.0-V power supply.

(2)  $V_{CCPD}$  must be 2.5 V when  $V_{CCIO}$  is 2.5, 1.8, 1.5, or 1.2 V.  $V_{CCPD}$  must be 3.0 V when  $V_{CCIO}$  is 3.0 V.

Table 1–7 lists the transceiver power supply recommended operating conditions for Stratix IV GX devices.

Table 1–7. Transceiver Power Supply Operating Conditions for Stratix IV
---

Symbol	Description	Minimum	Typical	Maximum	Unit
V <sub>CCA_L</sub>	Transceiver high voltage power (left side)	2.85/2.375	3.0/2.5 <sup>(2)</sup>	3.15/2.625	V
V <sub>CCA_R</sub>	Transceiver high voltage power (right side)	2.03/2.373	3.0/2.3	3.13/2.023	v
V <sub>CCHIP_L</sub>	Transceiver HIP digital power (left side)	0.87	0.9	0.93	V
V <sub>CCHIP_R</sub>	Transceiver HIP digital power (right side)	0.87	0.9	0.93	V
V <sub>CCR_L</sub>	Receiver power (left side)	1.045	1.1	1.155	V
V <sub>CCR_R</sub>	Receiver power (right side)	1.045	1.1	1.155	V
V <sub>CCT_L</sub>	Transmitter power (left side)	1.045	1.1	1.155	V
V <sub>CCT_R</sub>	Transmitter power (right side)	1.045	1.1	1.155	V
V <sub>CCL_GXBLn</sub> <sup>(3)</sup>	Transceiver clock power (left side)	1.05	1.1	1.15	V
V <sub>CCL_GXBRn</sub> <sup>(3)</sup>	Transceiver clock power (right side)	1.05	1.1	1.15	V
V <sub>CCH_GXBLn</sub> <sup>(3)</sup>	Transmitter output buffer power (left side)	1.33/1.425		1.47/1.575	V
V <sub>CCH_GXBRn</sub> <sup>(3)</sup>	Transmitter output buffer power (right side)	1.33/1.423	1.4/1.5 <sup>(4)</sup>	1.47/1.373	v

Notes to Table 1-7:

(1) Transceiver power supplies do not have power-on-reset (POR) circuitry. After initial power-up, violating the transceiver power supply operating conditions could lead to unpredictable link behavior.

(2) V<sub>CCA\_L/R</sub> must be connected to a 3.0-V supply if the clock multiplier unit (CMU) phase-locked loop (PLL), receiver clock data recovery (CDR), or both, are configured at a base data rate > 4.25 Gbps. For data rates up to 4.25 Gbps, you can connect V<sub>CCA\_L/R</sub> to either 3.0 V or 2.5 V.

(3) n = 0, 1, 2, or 3.

(4)  $V_{CCH\_GXBL/R}$  must be connected to a 1.4-V supply if the transmitter channel data rate is > 6.5 Gbps. For data rates up to 6.5 Gbps, you can connect  $V_{CCH\_GXBL/R}$  to either 1.4 V or 1.5 V.

Table 1–8 lists the recommended operating conditions for the Stratix IV GT transceiver power supply.

Table 1–8. Trans	sceiver Power Supply	<b>Operating Conditions f</b>	or Stratix IV GT Devices	(Part 1 of 2) <sup>(1)</sup> , <sup>(2)</sup>
------------------	----------------------	-------------------------------	--------------------------	---

Symbol	Symbol Description		Typical	Maximum	Unit
•	•	Minimum	<i>,</i> ,		
V <sub>CCA_L</sub>	Transceiver high voltage power (left side)	3.17	3.3	3.43	V
V <sub>CCA_R</sub>	Transceiver high voltage power (right side)	3.17	3.3	3.43	V
V <sub>CCHIP_L</sub>	Transceiver HIP digital power (left side)	0.92	0.95	0.98	V
V <sub>CCHIP_R</sub>	Transceiver HIP digital power (right side)	0.92	0.95	0.98	V
V <sub>CCR_L</sub>	Receiver power (left side)	1.15	1.2	1.25	V

Symbol	Description	Minimum	Typical	Maximum	Unit
V <sub>CCR_R</sub>	Receiver power (right side)	1.15	1.2	1.25	V
V <sub>CCT_L</sub>	Transmitter power (left side)	1.15	1.2	1.25	V
V <sub>CCT_R</sub>	Transmitter power (right side)	1.15	1.2	1.25	V
V <sub>CCL_GXBLn</sub> <sup>(3)</sup>	Transceiver clock power (left side)	1.15	1.2	1.25	V
V <sub>CCL_GXBRn</sub> <sup>(3)</sup>	Transceiver clock power (right side)	1.15	1.2	1.25	V
V <sub>CCH_GXBLn</sub> <sup>(3)</sup>	Transmitter output buffer power (left side)	1.33	1.4	1.47	V
V <sub>CCH_GXBRn</sub> <sup>(3)</sup>	Transmitter output buffer power (right side)	1.33	1.4	1.47	V

Table 1–8. Transceiver Power Supply Operating Conditions for Stratix IV GT Devices (Part 2 of 2)
--

Notes to Table 1-8:

- (1) For the recommended operating conditions for Stratix IV GT engineering sample (ES1) devices, contact your local Altera sales representative.
- (2) Transceiver power supplies do not have power-on-reset circuitry. After initial power-up, violating the transceiver power supply operating conditions could lead to unpredictable link behavior.

(3) n = 0, 1, 2, or 3.

### **DC Characteristics**

This section lists the supply current, I/O pin leakage current, bus hold, on-chip termination (OCT) tolerance, input pin capacitance, and hot socketing specifications.

#### **Supply Current**

Standby current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

#### I/O Pin Leakage Current

Table 1–9 lists the Stratix IV I/O pin leakage current specifications.

Table 1–9. I/O Pin Leakage Current for Stratix IV Devices <sup>(1)</sup>

Symbol	Description	Conditions	Min	Тур	Max	Unit
I	Input pin	$V_I = 0V$ to $V_{CCIOMAX}$	-20	_	20	μA
I <sub>OZ</sub>	Tri-stated I/O pin	$V_0 = 0V$ to $V_{CCIOMAX}$	-20		20	μA

Note to Table 1–9:

(1) V<sub>REF</sub> current refers to the input pin leakage current.

#### **Bus Hold Specifications**

Table 1–10 lists the Stratix IV device family bus hold specifications.

 Table 1–10.
 Bus Hold Parameters

			V <sub>CCI0</sub>										
Parameter	Symbol	Conditions	1.2	2 V	1.	5 V	1.8	3 V	2.	5 V	3.0	) V	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I <sub>SUSL</sub>	V <sub>IN</sub> > V <sub>IL</sub> (maximum)	22.5	_	25.0	_	30.0	_	50.0	_	70.0	_	μA
High sustaining current	I <sub>SUSH</sub>	V <sub>IN</sub> < V <sub>IH</sub> (minimum)	-22.5	_	-25.0	_	-30.0	_	-50.0	_	-70.0	_	μA
Low overdrive current	I <sub>odl</sub>	$0V < V_{IN} < V_{CCIO}$	_	120	_	160	_	200	_	300	_	500	μA
High overdrive current	I <sub>odh</sub>	$0V < V_{IN} < V_{CCIO}$		-120	_	-160		-200		-300		-500	μA
Bus-hold trip point	V <sub>trip</sub>		0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

### **On-Chip Termination (OCT) Specifications**

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 1–11 lists the Stratix IV OCT termination calibration accuracy specifications.

Table 1–11. OCT Calibration	<b>Accuracy Specifications f</b>	for Stratix IV Devices	(Part 1 of 2) <sup>(1)</sup>
-----------------------------	----------------------------------	------------------------	------------------------------

Cumhal	Description	Conditions	Calil	acy	Ilait	
Symbol	Description	Conditions	C2	C3,I3, M3	C4,14	Unit
25-Ω R <sub>S</sub> <sup>(2)</sup> 3.0, 2.5, 1.8, 1.5, 1.2	Internal series termination with calibration (25-Ω setting)	V <sub>CCIO</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	± 8	± 8	± 8	%
50-Ω R <sub>S</sub> 3.0, 2.5, 1.8, 1.5, 1.2	Internal series termination with calibration (50-Ω setting)	V <sub>CCIO</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	± 8	± 8	± 8	%
50-Ω R <sub>T</sub> 2.5, 1.8, 1.5, 1.2	Internal parallel termination with calibration (50-Ω setting)	V <sub>CCIO</sub> = 2.5, 1.8, 1.5, 1.2 V	± 10	± 10	± 10	%
20-Ω , 40-Ω , and 60-Ω R <sub>S</sub> <sup>(3)</sup> 3.0, 2.5, 1.8, 1.5, 1.2	Expanded range for internal series termination with calibration (20- $\Omega$ , 40- $\Omega$ , and 60- $\Omega$ R <sub>s</sub> setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	± 10	± 10	± 10	%

Symbol	Description	Conditions	Calit	Unit			
Symbol	Description	Conurtions	C2	C3,I3, M3	C4,14	Unit	
$\begin{array}{l} \textbf{25-}\Omega \; \textbf{R}_{S\_left\_shift} \\ \textbf{3.0, 2.5, 1.8, 1.5, 1.2} \end{array}$	Internal left shift series termination with calibration (25- $\Omega R_{S\_left\_shift}$ setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	± 10	± 10	± 10	%	

#### Notes to Table 1–11:

(1) OCT calibration accuracy is valid at the time of calibration only.

(2) 25- $\Omega$  R<sub>S</sub> is not supported for 1.5 V and 1.2 V in Row I/O.

(3) 20- $\Omega$  R<sub>s</sub> is not supported for 1.5 V and 1.2 V in Row I/O.

The calibration accuracy for calibrated series and parallel OCTs are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change. Table 1–12 lists the Stratix IV OCT without calibration resistance tolerance to PVT changes.

Table 1–12. OCT Without Calibration Resistance Tolerance Specifications for Stratix IV Devices

Sumbol	Description	Conditions	Resi	Unit			
Symbol	Description	Conditions	C2	C3,I3, M3 C4,I4		Unit	
25-Ω R <sub>S</sub> 3.0 and 2.5	Internal series termination without calibration (25- $\Omega$ setting)	$V_{CCIO} = 3.0$ and 2.5 V	± 30	± 40	± 40	%	
25-Ω R <sub>S</sub> 1.8 and 1.5	Internal series termination without calibration (25- $\Omega$ setting)	$V_{CCIO} = 1.8$ and 1.5 V	± 30	± 40	± 40	%	
25-Ω R <sub>S</sub> 1.2	Internal series termination without calibration (25- $\Omega$ setting)	V <sub>CCI0</sub> = 1.2 V	± 35	± 50	± 50	%	
50-Ω R <sub>S</sub> 3.0 and 2.5	Internal series termination without calibration (50- $\Omega$ setting)	$V_{CCIO} = 3.0$ and 2.5 V	± 30	± 40	± 40	%	
50-Ω R <sub>S</sub> 1.8 and 1.5	Internal series termination without calibration (50- $\Omega$ setting)	$V_{CCIO} = 1.8$ and 1.5 V	± 30	± 40	± 40	%	
50-Ω R <sub>S</sub> 1.2	Internal series termination without calibration (50- $\Omega$ setting)	V <sub>CCI0</sub> = 1.2 V	± 35	± 50	± 50	%	
100-Ω R <sub>D</sub> 2.5	Internal differential termination (100- $\Omega$ setting)	V <sub>CCI0</sub> = 2.5 V	± 25	± 25	± 25	%	

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 1–13 lists OCT variation with temperature and voltage after power-up calibration. Use Table 1–13 to determine the OCT variation after power-up calibration and Equation 1–1 to determine the OCT variation without re-calibration.

#### Equation 1–1. OCT Variation Without Re-Calibration <sup>(1)</sup>, <sup>(2)</sup>, <sup>(3)</sup>, <sup>(4)</sup>, <sup>(5)</sup>, <sup>(6)</sup>

$$R_{OCT} = R_{SCAL} \left( 1 + \langle \frac{dR}{dT} \times \Delta T \rangle \pm \langle \frac{dR}{dV} \times \Delta V \rangle \right)$$

#### Notes to Equation 1–1:

- (1) The R<sub>OCT</sub> value calculated from Equation 1–1 shows the range of OCT resistance with the variation of temperature and  $V_{CCIO}$ .
- (2)  $R_{SCAL}$  is the OCT resistance value at power-up.
- (3)  $\Delta T$  is the variation of temperature with respect to the temperature at power-up.
- (4)  $\Delta V$  is the variation of voltage with respect to the V<sub>CCIO</sub> at power-up.
- (5) dR/dT is the percentage change of  $R_{SCAL}$  with temperature.
- (6) dR/dV is the percentage change of R<sub>SCAL</sub> with voltage.

Table 1–13 lists the OCT variation after the power-up calibration.

Symbol	Description	V <sub>CCIO</sub> (V)	Typical	Unit
		3.0	0.0297	
		2.5	0.0344	
dR/dV	OCT variation with voltage without re-calibration	1.8	0.0499	%/mV
		1.5	0.0744	
		1.2	0.1241	
		3.0	0.189	
		2.5	0.208	
dR/dT	OCT variation with temperature without re-calibration	1.8	0.266	%/°C
		1.5	0.273	
		1.2	0.317	

Table 1–13. OCT Variation after Power-Up Calibration (1)

#### Note to Table 1-13:

(1) Valid for  $V_{CCIO}$  range of ±5% and temperature range of 0° to 85°C.

#### **Pin Capacitance**

Table 1–14 lists the Stratix IV device family pin capacitance.

Symbol	Description	Value	Unit
C <sub>IOTB</sub>	Input capacitance on the top and bottom I/O pins	4	pF
C <sub>IOLR</sub>	Input capacitance on the left and right I/O pins	4	pF
C <sub>CLKTB</sub>	Input capacitance on the top and bottom non-dedicated clock input pins	4	pF
C <sub>CLKLR</sub>	Input capacitance on the left and right non-dedicated clock input pins	4	pF

#### Table 1–14. Pin Capacitance for Stratix IV Devices (Part 2 of 2)

Symbol	Description	Value	Unit
C <sub>OUTFB</sub>	Input capacitance on the dual-purpose clock output and feedback pins	5	рF
$C_{\text{CLK1}},C_{\text{CLK3}},C_{\text{CLK8}},$ and $C_{\text{CLK10}}$	Input capacitance for dedicated clock input pins	2	pF

#### **Hot Socketing**

Table 1–15 lists the hot socketing specifications for Stratix IV devices.

Table 1–15.	. Hot Socketing Specifications for Stratix IV Devices
-------------	---

Symbol	Description	Maximum
I <sub>IOPIN (DC)</sub>	DC current per I/O pin	300 μA
I <sub>IOPIN (AC)</sub>	AC current per I/O pin	8 mA (1)
I <sub>XCVR-TX (DC)</sub>	DC current per transceiver TX pin	100 mA
I <sub>XCVR-RX (DC)</sub>	DC current per transceiver RX pin	50 mA

Note to Table 1-15:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns,  $|I_{10PIN}| = C dv/dt$ , in which C is the I/O pin capacitance and dv/dt is the slew rate.

## **Internal Weak Pull-Up Resistor**

Table 1–16 lists the weak pull-up resistor values for Stratix IV devices.

#### Table 1–16. Internal Weak Pull-Up Resistor for Stratix IV Devices (1), (3)

Symbol	Description	Conditions (V)	Value <sup>(4)</sup>	Unit
		$V_{CCIO} = 3.0 \pm 5\%$ <sup>(2)</sup>	25	kΩ
	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled.	$V_{CCIO} = 2.5 \pm 5\%$ <sup>(2)</sup>	25	kΩ
R <sub>PU</sub>		$V_{CCIO} = 1.8 \pm 5\%$ <sup>(2)</sup>	25	kΩ
		$V_{CCIO} = 1.5 \pm 5\%$ <sup>(2)</sup>	25	kΩ
		$V_{CCIO} = 1.2 \pm 5\%$ <sup>(2)</sup>	25	kΩ

Notes to Table 1–16:

(1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than  $V_{CCIO}$ .

(3) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 k $\Omega$ .

(4) These specifications are valid with  $\pm 10\%$  tolerances to cover changes over PVT.

## I/O Standard Specifications

Table 1–17 through Table 1–22 list the input voltage (V<sub>IH</sub> and V<sub>IL</sub>), output voltage (V<sub>OH</sub> and V<sub>OL</sub>), and current drive characteristics (I<sub>OH</sub> and I<sub>OL</sub>) for various I/O standards supported by Stratix IV devices. These tables also show the Stratix IV device family I/O standard specifications. V<sub>OL</sub> and V<sub>OH</sub> values are valid at the corresponding I<sub>OH</sub> and I<sub>OL</sub>, respectively.

For an explanation of terms used in Table 1–17 through Table 1–22, refer to "Glossary" on page 1–64.

l/0 Standard	V <sub>CCIO</sub> (V)		V <sub>IL</sub> (V)		V <sub>IH</sub> (V)		V <sub>OL</sub> (V)	V <sub>OH</sub> (V)	I <sub>OL</sub>	I <sub>OH</sub>	
	Min	Тур	Max	Min	Max	Min	Max	Max	Min	(mĀ)	(mÄ)
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	V <sub>CCI0</sub> - 0.2	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 * V <sub>CCI0</sub>	0.65 * V <sub>CCI0</sub>	V <sub>CCI0</sub> + 0.3	0.45	V <sub>CCIO</sub> - 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 * V <sub>CCI0</sub>	0.65 * V <sub>CCI0</sub>	V <sub>CCI0</sub> + 0.3	0.25 * V <sub>CCI0</sub>	0.75 * V <sub>CCIO</sub>	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 * V <sub>CCI0</sub>	0.65 * V <sub>CCI0</sub>	V <sub>CCI0</sub> + 0.3	0.25 * V <sub>CCI0</sub>	0.75 * V <sub>CCIO</sub>	2	-2
3.0-V PCI	2.85	3	3.15	_	0.3 * V <sub>CCI0</sub>	0.5 * V <sub>CCI0</sub>	3.6	0.1 * V <sub>CCIO</sub>	0.9 * V <sub>CCIO</sub>	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	_	0.35 * V <sub>CCI0</sub>	0.5 * V <sub>CCI0</sub>	_	0.1 * V <sub>CCIO</sub>	0.9 * V <sub>CCIO</sub>	1.5	-0.5

Table 1–17. Single-Ended I/O Standards

Table 1–18. Single-Ended SSTL and HSTL I/O Refe	rence Voltage Specifications
---	------------------------------

I/O Standard	V <sub>CCIO</sub> (V)			V <sub>REF</sub> (V)			V <sub>ττ</sub> (V)			
i/U Stailuaru	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 * V <sub>CCI0</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	V <sub>REF</sub> - 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04	
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V <sub>REF</sub> - 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04	
SSTL-15 Class I, II	1.425	1.5	1.575	0.47 * V <sub>CCI0</sub>	0.5 * V <sub>CCIO</sub>	0.53 * V <sub>CCIO</sub>	0.47 * V <sub>CCIO</sub>	V <sub>REF</sub>	0.53 * V <sub>CCI0</sub>	
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95		V <sub>CCI0</sub> /2	_	
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	_	V <sub>CCI0</sub> /2	—	
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 * V <sub>CCI0</sub>	0.5 * V <sub>CCIO</sub>	0.53 * V <sub>CCI0</sub>		V <sub>CCI0</sub> /2		

I/O Standard	V <sub>IL(DC)</sub> (V)		V <sub>IH(DC)</sub> (V)		V <sub>IL(AC)</sub> V <sub>IH(AC)</sub> (V) (V)		V <sub>OL</sub> (V)	V <sub>OH</sub> (V)	l <sub>ol</sub> (mA)	l <sub>oh</sub> (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	V <sub>CCI0</sub> + 0.3	V <sub>REF</sub> - 0.31	V <sub>REF</sub> + 0.31	V <sub>TT</sub> - 0.57	V <sub>TT</sub> + 0.57	8.1	-8.1
SSTL-2 Class II	-0.3	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	V <sub>CCI0</sub> + 0.3	V <sub>REF</sub> - 0.31	V <sub>REF</sub> + 0.31	V <sub>TT</sub> - 0.76	V <sub>TT</sub> + 0.76	16.2	-16.2
SSTL-18 Class I	-0.3	V <sub>REF</sub> - 0.125	V <sub>REF</sub> + 0.125	V <sub>CCI0</sub> + 0.3	V <sub>REF</sub> - 0.25	V <sub>REF</sub> + 0.25	V <sub>TT</sub> - 0.475	V <sub>TT</sub> + 0.475	6.7	-6.7
SSTL-18 Class II	-0.3	V <sub>REF</sub> - 0.125	V <sub>REF</sub> + 0.125	V <sub>CCI0</sub> + 0.3	V <sub>REF</sub> - 0.25	V <sub>REF</sub> + 0.25	0.28	V <sub>CCI0</sub> - 0.28	13.4	-13.4
SSTL-15 Class I	_	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.175	V <sub>REF</sub> + 0.175	0.2 * V <sub>CCI0</sub>	0.8 * V <sub>CCI0</sub>	8	-8
SSTL-15 Class II	_	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.175	V <sub>REF</sub> + 0.175	0.2 * V <sub>CCI0</sub>	0.8 * V <sub>CCI0</sub>	16	-16
HSTL-18 Class I	_	V <sub>REF</sub> -0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> - 0.4	8	-8
HSTL-18 Class II	_	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> - 0.4	16	-16
HSTL-15 Class I		V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> - 0.4	8	-8
HSTL-15 Class II	_	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> - 0.4	16	-16
HSTL-12 Class I	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCI0</sub> + 0.15	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	0.25* V <sub>CCI0</sub>	0.75* V <sub>CCIO</sub>	8	-8
HSTL-12 Class II	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	0.25* V <sub>CCIO</sub>	0.75* V <sub>CCIO</sub>	16	-16

Table 1–19. Single-Ended SSTL and HSTL I/O Standards Signal Specifications

#### Table 1–20. Differential SSTL I/O Standards

I/0	١	V <sub>CCIO</sub> (V	)	V <sub>SWIN</sub>	<sub>G(DC)</sub> (V)		V <sub>X(AC)</sub> (V)		V <sub>SWIN</sub>	<sub>G(AC)</sub> (V)		V <sub>ox(AC)</sub> (V)	
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max	Min	Тур	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V <sub>CCI0</sub> + 0.6	V <sub>CCI0</sub> /2 - 0.2	_	V <sub>CCI0</sub> /2 + 0.2	0.62	V <sub>CCI0</sub> + 0.6	V <sub>CCI0</sub> /2 - 0.15	_	V <sub>CCI0</sub> /2 + 0.15
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V <sub>CCIO</sub> + 0.6	V <sub>CCI0</sub> /2 - 0.175	_	V <sub>CCI0</sub> /2 + 0.175	0.5	V <sub>CCI0</sub> + 0.6	V <sub>CCI0</sub> /2 - 0.125	_	V <sub>CCI0</sub> /2 + 0.125
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	_	V <sub>CCI0</sub> /2	_	0.35	_	_	V <sub>CCI0</sub> /2	_

I/O		V <sub>CCIO</sub> (V)		V <sub>DIF(</sub>	<sub>DC)</sub> (V)		V <sub>X(AC)</sub> (V)	)		V <sub>CM(DC)</sub> (V	)	V <sub>DIF(</sub> /	<sub>AC)</sub> (V)
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-18 Class I	1.71	1.8	1.89	0.2	_	0.78	_	1.12	0.78	_	1.12	0.4	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.68	_	0.9	0.68	_	0.9	0.4	_
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V <sub>CCI0</sub> + 0.3	_	0.5* V <sub>CCI0</sub>	_	0.4* V <sub>CCIO</sub>	0.5* V <sub>CCIO</sub>	0.6* V <sub>CCIO</sub>	0.3	V <sub>CCI0</sub> + 0.48

Table 1–21. Differential HSTL I/O Standards

Table 1-22.	<b>Differential I/O Standard Specifications</b>	(1),	(2)	Part 1 of 2)
-------------	---	------	-----	--------------

I/O	Vc	:cio (V)	(3)		V <sub>ID</sub> (mV)			V <sub>ICM(DC)</sub> (V)		Vo	<sub>D</sub> (V) (	4)	V	<sub>DCM</sub> (V)	(4)
Standard	Min	Тур	Max	Min	Condition	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max
PCML							in spec	hins of high-s bifications, re page 1–25.							
2.5 V LVDS	2.375	2.5	2.625	100	V <sub>CM</sub> =	_	0.05 (5)	D <sub>MAX</sub> ≤ 700 Mbps	1.8 (5)	0.247		0.6	1.125	1.25	1.375
(HIO)	2.375	2.5	2.025	100	1.25 V	_	1.05 (5)	D <sub>MAX</sub> > 700 Mbps	1.55 ( 5)	0.247		0.6	1.125	1.25	1.375
2.5 V LVDS	2.375	2.5	2.625	100	V <sub>CM</sub> =	_	0.05	D <sub>MAX</sub> ≤ 700 Mbps	1.8	0.247		0.6	1	1.25	1.5
(VIO)	2.375	2.5	2.025	100	1.25 V	_	1.05	D <sub>MAX</sub> > 700 Mbps	1.55	0.247		0.6	1	1.25	1.5
RSDS (HIO)	2.375	2.5	2.625	100	V <sub>CM</sub> = 1.25 V	_	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
RSDS (VIO)	2.375	2.5	2.625	100	V <sub>CM</sub> = 1.25 V	_	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.5
Mini-LVDS (HIO)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25		0.6	1	1.2	1.4
Mini-LVDS (VIO)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25		0.6	1	1.2	1.5
LVPECL <sup>(7)</sup>	2.375	2.5	2.625	300	_	—	0.6 (6)	D <sub>MAX</sub> ≤ 700 Mbps	1.8 (6)	_		—	_	_	_
LVFEUL	2.375	2.5	2.625	300	_		<b>1</b> (6)	D <sub>MAX</sub> > 700 Mbps	1.6 (6)	_					

I/O	Vc	;cio (V)	(3)		V <sub>ID</sub> (mV)			V <sub>ICM(DC)</sub> (V)		Vo	<sub>D</sub> (V) (	4)	۷۵	<sub>ICM</sub> (V)	(4)
Standard	Min	Тур	Max	Min	Condition	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max
BLVDS (8)	2.375	2.5	2.625	100	—	—	—	—	_	—		_	_		_

#### Table 1–22. Differential I/O Standard Specifications <sup>(1)</sup>, <sup>(2)</sup> (Part 2 of 2)

#### Notes to Table 1-22:

(1) Vertical I/O (VIO) is top and bottom I/Os; horizontal I/O (HIO) is left and right I/Os.

(2) 1.4-V/1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 1–16.

(3) Differential clock inputs in column I/O are powered by V<sub>CC\_CLKIN</sub> which requires 2.5 V. Differential inputs that are not on clock pins in column I/O are powered by V<sub>CCPD</sub> which requires 2.5 V. All differential inputs in row I/O banks are powered by V<sub>CCPD</sub> which requires 2.5V.

(4) RL range:  $90 \le RL \le 110 \Omega$ .

(5) The receiver voltage input range for the data rate when  $D_{MAX} > 700$  Mbps is 1.0 V  $\leq V_{IN} \leq 1.6$  V. The receiver voltage input range for the data rate when  $D_{MAX} \leq 700$  Mbps is zero V  $\leq V_{IN} \leq 1.85$  V.

(6) The receiver voltage input range for the data rate when  $D_{MAX} > 700$  Mbps is 0.85 V  $\leq V_{IN} \leq 1.75$  V. The receiver voltage input range for the data rate when  $D_{MAX} \leq 700$  Mbps is 0.45 V  $\leq V_{IN} \leq 1.95$  V.

(7) Column and row I/O banks support LVPECL I/O standards for input operation only on dedicated clock input pins.

(8) For more information about BLVDS interface support in Altera devices, refer to *AN522: Implementing Bus LVDS Interfaces in Supported Altera Device Families.* 

## **Power Consumption**

Altera offers two ways to estimate power consumption for a design the Excel-based Early Power Estimator and the Quartus<sup>®</sup> II PowerPlay Power Analyzer feature.

You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.



 For more information about power estimation tools, refer to the PowerPlay Early Power Estimator User Guide and the PowerPlay Power Analysis chapter in the Quartus II Handbook.

## **Switching Characteristics**

This section provides performance characteristics of Stratix IV core and periphery blocks for commercial, industrial, and military grade devices.

The final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

## **Transceiver Performance Specifications**

This section describes transceiver performance specifications.

Table 1–23 lists the Stratix IV GX transceiver specifications.

#### Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 1 of 9)

Symbol/ Description	Conditions		Commer beed Gra		ln -2×	Commerc dustrial a Commer ced Grade	nd cial	Comm	3 Military and –4 ercial/Ind peed Gra	dustrial	Unit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
<b>Reference Clock</b>											
Supported I/O Standards	1.2 V PCM	L, 1.4 V	PCML 1	.5 V PC	ML, 2.5	V PCML,	Differen	tial LVPI	ECL <sup>(4)</sup> , L	VDS, HCS	SL
Input frequency from REFCLK input pins	_	50	_	697	50	_	697	50	_	637.5	MHz
Phase frequency detector (CMU PLL and receiver CDR)	_	50	_	425	50	_	325	50	_	325	MHz
Absolute V <sub>MAX</sub> for a REFCLK pin	_	_	_	1.6	_	_	1.6	_	_	1.6	V
Operational V <sub>MAX</sub> for a REFCLK pin	_	_	_	1.5	_	_	1.5	_	_	1.5	V
Absolute V <sub>MIN</sub> for a REFCLK pin	_	-0.4	_	_	-0.4	_	_	-0.4	_	_	V
Rise/fall time (21)	—	—		0.2			0.2		_	0.2	UI
Duty cycle	—	45		55	45		55	45	—	55	%
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	200	_	1600	mV
Spread-spectrum modulating clock frequency	PCle	30	_	33	30	_	33	30	_	33	kHz
Spread-spectrum downspread	PCle	_	0 to -0.5%	_	_	0 to -0.5%	_	_	0 to -0.5%	_	_
On-chip termination resistors	_	_	100	_		100	_	_	100	_	Ω
V <sub>ICM</sub> (AC coupled)	—			1	100 ± 10	%	mV				
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250	_	550	250	_	550	250	_	550	mV

Symbol/ Description	Conditions		Commer beed Gra		<b>in</b> -2×	Commerc dustrial a Commer eed Grade	nd cial	Comm	3 Military and –4 ercial/In peed Gra	dustrial	Unit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
	10 Hz		—	-50	—		-50	—	_	-50	dBc/Hz
	100 Hz		—	-80	—	—	-80	—	_	-80	dBc/Hz
Transmitter REFCLK	1 KHz	_	—	-110	—	—	-110	—	_	-110	dBc/Hz
Phase Noise	10 KHz		—	-120	—	—	-120	—	_	-120	dBc/Hz
	100 KHz	—		-120		—	-120		_	-120	dBc/Hz
	≥ 1 MHz	—	—	-130	—	—	-130	—	—	-130	dBc/Hz
Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK <sup>(3)</sup>	10 KHz to 20 MHz			3	_		3		_	3	ps
R <sub>REF</sub>	_	_	2000 ± 1%	—	_	2000 ± 1%	_	_	2000 ± 1%	_	Ω
Transceiver Clocks											
Calibration block clock frequency	_	10	_	125	10	_	125	10	_	125	MHz
fixedclk <b>clock</b> frequency	PCIe Receiver Detect		125	_	_	125	_	_	125	_	MHz
reconfig_clk <b>clock frequency</b>	Dynamic reconfiguration clock frequency	2.5/ 37.5 (5)	_	50	2.5/ 37.5 (5)	_	50	2.5/ 37.5 (5)	_	50	_
Delta time between reconfig_clks (19)	_	_	_	2	_	_	2	_	_	2	ms
Transceiver block minimum power-down (gxb_powerdown) pulse width	_	1			1			1		_	μs
Receiver											
Supported I/O Standards		1	.4 V PCI	VIL, 1.5	V PCML	., 2.5 V P(	CML, LVF	PECL, LV	'DS		
Data rate (Single width, non-PMA Direct)	_	600		3750	600		3750	600	_	3750	Mbps
Data rate (Double width, non-PMA Direct)	_	1000	_	8500	1000	_	6500	1000	_	6375 (22)	Mbps
Data rate (Single width, PMA Direct)	_	600	_	3250	600	_	3250	600	_	3250	Mbps
Data rate (Double width, PMA Direct)	_	1000		6500	1000	_	6500	1000		6375	Mbps

### Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 2 of 9)

Symbol/ Description	Conditions		Commer eed Gra		lno —2×	Commerc lustrial a Commer eed Grade	nd cial	Comm	3 Military and –4 ercial/In peed Gra	dustrial	Unit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Absolute $V_{MAX}$ for a receiver pin $^{(6)}$	_			1.6			1.6		_	1.6	V
Operational V <sub>MAX</sub> for a receiver pin	_			1.5			1.5	_	_	1.5	V
Absolute V <sub>MIN</sub> for a receiver pin	—	-0.4	_	_	-0.4	_	_	-0.4	_	_	V
Maximum peak-to-peak differential input voltage V <sub>ID</sub> (diff p-p) before device configuration	_	_	_	1.6	_	_	1.6	_	_	1.6	V
Maximum peak-to- peak differential	V <sub>ICM</sub> = 0.82 V setting			2.7			2.7		_	2.7	V
input voltage V <sub>ID</sub> (diff p-p) after device configuration	V <sub>ICM</sub> =1.1 V setting <sup>(7)</sup>	_	_	1.6	_	_	1.6	_	_	1.6	V
Minimum differential eye	Data Rate = 600 Mbps to 5 Gbps Equalization = 0 DC gain = 0 dB	100		_	100		_	165	_	_	mV
opening at receiver serial input pins <sup>(20)</sup>	Data Rate > 5 Gbps Equalization = 0 DC gain = 0 dB	165			165			165			mV
Maria	V <sub>ICM</sub> = 0.82 V setting	8	20 ± 109	%	ξ	320 ± 10%	/ 0	8	820 ± 109	%	mV
V <sub>ICM</sub>	V <sub>ICM</sub> = 1.1 V setting <sup>(7)</sup>	11	100 ± 10	%	1	100 ± 109	%	1	100 ± 10	%	mV
Receiver DC Coupling Support	_					ut receive Transceive					
	85– $\Omega$ setting		35 ± 20%			85 ± 20%			85 ± 20%		Ω
Differential on-chip termination	100– $\Omega$ setting	1	00 ± 209	/0	1	00 ± 20%	0	-	100 ± 20°	%	Ω
ermination esistors	120– $\Omega$ setting	1	20 ± 209	6	1	20 ± 20%	0	-	120 ± 20°	%	Ω

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 3 of 9)

150- $\Omega$  setting

150 ± 20%

150 ± 20%

150 ± 20%

Ω

Symbol/ Description	Conditions		Commer eed Gra		lno -2×	Commerc dustrial a Commer eed Grade	nd cial	Comm	3 Military and –4 ercial/In peed Gra	dustrial	Unit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Differential and common mode return loss	PCIe (Gen 1 and Gen 2), XAUI, HiGig+, CEI SR/LR, Serial RapidIO SR/LR, CPRI LV/HV, OBSAI, SATA					Complia	int				
Programmable PPM detector <sup>(8)</sup>						.5, 100, 1 , 300, 50					ppm
Run length		<u> </u>									UI
Programmable equalization <sup>(18)</sup>		_		16		_	16	_	_	16	dB
t <sub>LTR</sub> <sup>(9)</sup>		—		75			75			75	μs
t <sub>LTR_LTD_Manual</sub> <sup>(10)</sup>		15		—	15	_	_	15			μs
t <sub>LTD_Manual</sub> <sup>(11)</sup>		—		4000		_	4000	—	_	4000	ns
t <sub>LTD_Auto</sub> <sup>(12)</sup>				4000			4000			4000	ns
	PCIe Gen1					20 - 3	5				MHz
	PCIe Gen2					40 - 6	5				MHz
	(OIF) CEI PHY at 6.375 Gbps					20 - 3	5				MHz
	XAUI					10 - 18	8				MHz
Receiver CDR 3 dB Bandwidth in	Serial RapidIO 1.25 Gbps					10 - 18	8				MHz
lock-to-data (LTD) mode	Serial RapidIO 2.5 Gbps					10 - 18	8				MHz
	Serial RapidIO 3.125 Gbps					6 - 10	)				MHz
	GIGE					6 - 10					MHz
	SONET 0C12					3 - 6					MHz
	SONET OC48					14 - 19	9				MHz
Receiver buffer and CDR offset cancellation time (per channel)	_	1850				18500	recon fig_ clk <b>cycles</b>				

### Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 4 of 9)

Symbol/ Description	Conditions	-2 (	Commer eed Gra	cial	-3 Int -2×	Commerc dustrial a Commer eed Grade	nd cial	Comm	8 Military and –4 ercial/In peed Gra	dustrial	Unit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
	DC Gain Setting = 0	_	0	_	_	0	_	_	0	_	dB
	DC Gain Setting = 1	_	3	_	_	3	_	_	3	_	dB
Programmable DC gain	DC Gain Setting = 2	_	6	_	_	6	_	_	6	_	dB
	DC Gain Setting = 3	_	9	_	_	9	_	_	9	_	dB
	DC Gain Setting = 4	_	12	—		12	_	_	12	_	dB
EyeQ Data Rate		600		3250	600	_	3250	600	_	3250	Mbps
AEQ Data Rate	min V <sub>ID</sub> (diff p-p) outer envelope = 600 mV 8B/10B encoded data	2500		6500	2500		6500			_	Mbps
Decision Feedback Equalizer (DFE) Data Rate	min V <sub>ID</sub> (diff p-p) outer envelope = 500 mV	3125		6500	3125		6500	_	_	_	Mbps
Transmitter											
Supported I/O Standards				1.4	4 V PCM	L, 1.5 V F	CML				
Data rate (Single width, non-PMA Direct)	_	600		3750	600	_	3750	600	_	3750	Mbps
Data rate (Double width, non-PMA Direct)	_	1000		8500	1000	_	6500	1000	_	6375 (22)	Mbps
Data rate (Single width, PMA Direct)	_	600	_	3250	600	_	3250	600	_	3250	Mbps
Data rate (Double width, PMA Direct)	_	1000		6500	1000		6500	1000	_	6375	Mbps
V <sub>OCM</sub>	0.65 V setting		650	—		650	_		650	_	mV
	85– $\Omega$ setting	8	85 ± 15%	0		85 ± 15%			85 ± 15%	6	Ω
Differential on-chip termination	100– $\Omega$ setting	1	00 ± 15°	%	1	00 ± 15%	0		100 ± 15°	%	Ω
resistors	120– $\Omega$ setting	1	20 ± 15°	%		20 ± 15%			120 ± 15°		Ω
	150- $\Omega$ setting	1	50 ± 15°	%	1	50 ± 15%	0	-	150 ± 15°	%	Ω

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 5 of 9)

Symbol/ Description	Conditions		Commer eed Gra		lno -2×	Commerc lustrial a Commer eed Grade	nd cial	Comm	3 Military and –4 ercial/Ind peed Gra	dustrial	Unit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Differential and common mode return loss	$\begin{array}{c} \mbox{PCle Gen1 and} \\ \mbox{Gen2 (TX} \\ \mbox{V}_{0D}=4), \\ \mbox{XAUI (TX} \\ \mbox{V}_{0D}=6), \\ \mbox{HiGig}+ \\ \mbox{(TX V}_{0D}=6), \\ \mbox{CEI SR/LR} \\ \mbox{(TX V}_{0D}=8), \\ \mbox{Serial RapidIO} \\ \mbox{SR (V}_{0D}=6), \\ \mbox{Serial RapidIO} \\ \mbox{LR (V}_{0D}=8), \\ \mbox{CPRI LV} \\ \mbox{(V}_{0D}=6), \\ \mbox{CPRI LV} \\ \mbox{(V}_{0D}=6), \\ \mbox{CPRI HV} \\ \mbox{(V}_{0D}=2), \\ \mbox{OBSAI (V}_{0D}=4), \\ \mbox{SATA (V}_{0D}=4), \\ \end{array}$	Compliant 50 — 200 50 — 200 50 — 200									
Rise time <sup>(14)</sup>	—	50	_	200	50	—	200	50		200	ps
Fall time <sup>(14)</sup>	—	50	_	200	50	_	200	50		200	ps
XAUI rise time	—	60		130	60	_	130	60		130	ps
XAUI fall time	—	60		130	60	_	130	60		130	ps
Intra-differential pair skew	_		_	15		_	15	_	_	15	ps
Intra-transceiver block transmitter channel-to-channel skew	×4 PMA and PCS bonded mode Example: XAUI, PCIe ×4, Basic ×4	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $							ps		
Inter-transceiver block transmitter channel-to-channel skew	×8 PMA and PCS bonded mode Example: PCIe ×8, Basic ×8			500			500			500	ps

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 6 of 9)

Symbol/ Description	Conditions		Commer eed Gra		Inc -2×	Commerc lustrial a Commer eed Grade	nd cial	Comm	8 Military and –4 ercial/In peed Gra	dustrial	Unit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Inter-transceiver block skew in Basic (PMA Direct) ×N mode <sup>(15)</sup>	N < 18 channels located across three transceiver blocks with the source CMU PLL located in the center transceiver block		_	400	_	_	400	_		400	ps
	N ≥ 18 channels located across four transceiver blocks with the source CMU PLL located in one of the two center transceiver blocks		_	650	_		650		_	650	ps
CMU0 PLL and CMU1	PLL										
Supported Data Range	_	600		8500	600		6500	600		6375	Mbps
pll_powerdown minimum pulse width (tpll_powerdown)	_					1					μS
CMU PLL lock time from pll_powerdown de-assertion	_	_		100	_	_	100		_	100	μS

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 7 of 9)
--

Symbol/ Description	Conditions		Commer eed Gra		Ind -2×	Commerc dustrial a Commer eed Grade	nd cial	–÷ Comm S	Unit				
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max			
	PCIe Gen1					2.5 - 3.	5				MHz		
	PCIe Gen2					6 - 8					MHz		
(OIF) CEI PHY at 4.976 Gbps 7 - 11										MHz			
	(OIF) CEI PHY at 6.375 Gbps		5 - 10										
	XAUI	2 - 4											
-3 dB Bandwidth	Serial RapidIO 1.25 Gbps		3 - 5.5										
	Serial RapidIO 2.5 Gbps		3 - 5.5										
	Serial RapidIO 3.125 Gbps		2 - 4										
	GIGE 2.5 - 4.5		MHz										
	SONET 0C12					1.5 - 2.	5				MHz		
	SONET 0C48					3.5 - 6					MHz		
ATX PLL (6G)													
	/L = 1	4800-5400 and4800-5400 and4800-5400 and6000-65006000-65006000-6375							4000 0400 and 4000 0400 a				Mbps
Supported Data Range <sup>(16)</sup>	/L = 2	2400-2700 and 3000-3250				00-2700 a 3000-3250			and 7.5	Mbps			
	/L = 4	1200-1350 and         1200-1350 and         1200-1350 and           1500-1625         1500-1625         1500-1593.75					Mbps						
	PCIe Gen 2		1.5		1.5			—			MHz		
-3 dB Bandwidth	(OIF) CEI PHY at 6.375 Gbps		3 - 4.5 3 - 4.5 —								MHz		
Transceiver-FPGA Fa	bric Interface												
Interface speed (non-PMA Direct)	_	25	_	325	25	_	325	25	_	250	MHz		
Interface speed (PMA Direct)	_	50		325	50		325	50	_	325	MHz		

Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 8 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade	lno —2×	Commerc Iustrial a Commer ed Grado	nd cial	–3 Military <sup>(2)</sup> and –4 Commercial/Industrial Speed Grade			Unit		
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Digital reset pulse width	_			Min	imum is	two para	llel clocł	k cycles			_

#### Table 1–23. Transceiver Specifications for Stratix IV GX Devices (Part 9 of 9)

#### Notes to Table 1-23:

(1) The -2× speed grade is the fastest speed grade offered in the following Stratix IV GX devices: EP4SGX70DF29, EP4SGX110DF29, EP4SGX110FF35, EP4SGX10FF35, EP4SGX230FF35, EP4SGX230FF35, EP4SGX290FF35, EP4SGX290FF35, EP4SGX290FF35, and EPSGX360FH29.

(2) Stratix IV GX devices in military speed grade only support selected transceiver configuration up to 3125 Mbps. For more information, contact Altera sales representative.

(3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at 1 (0 MHz) = REFCLK rms phase jitter at 100 MHz \* 100/f.

(4) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

(5) The minimum reconfig\_clk frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum reconfig\_clk frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode. For more information, refer to the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

- (6) The device cannot tolerate prolonged operation at this absolute maximum.
- (7) You must use the 1.1-V RX V<sub>ICM</sub> setting if the input serial data standard is LVDS.
- (8) The rate matcher supports only up to  $\pm$  300 parts per million (ppm).
- (9) Time taken to rx pll locked goes high from rx analogreset de-assertion. Refer to Figure 1-2 on page 1-33.

(10) Time for which the CDR must be kept in lock-to-reference (LTR) mode after rx\_pll\_locked goes high and before rx\_locktodata is asserted in manual mode. Refer to Figure 1–2 on page 1–33.

- (11) Time taken to recover valid data after the rx locktodata signal is asserted in manual mode. Refer to Figure 1-2 on page 1-33.
- (12) Time taken to recover valid data after the rx freqlocked signal goes high in automatic mode. Refer to Figure 1-3 on page 1-33.
- (13) A GPLL may be required to meet the PMA-FPGA fabric interface timing above certain data rates. For more information, refer to the "Left/Right PLL Requirements in Basic (PMA Direct) Mode" section in the *Transceiver Clocking in Stratix IV Devices* chapter.
- (14) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (15) For applications that require low transmit lane-to-lane skew, use Basic (PMA Direct) xN to achieve PMA-Only bonding across all channels in the link. You can bond all channels on one side of the device by configuring them in Basic (PMA Direct) xN mode. For more information about clocking requirements in this mode, refer to the "Basic (PMA Direct) Mode Clocking" section in the *Transceiver Clocking in Stratix IV Devices* chapter.
- (16) The Quartus II software automatically selects the appropriate /L divider depending on the configured data.
- (17) The maximum transceiver-FPGA fabric interface speed of 265.625 MHz is allowed only in Basic low-latency PCS mode with a 32-bit interface width. For more information, refer to the "Basic Double-Width Mode Configurations" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
- (18) Figure 1–1 shows the AC gain curves for each of the 16 available equalization settings.
- (19) If your design uses more than one dynamic reconfiguration controller (altgx\_reconfig) instances to control the transceiver (altgx) channels physically located on the same side of the device AND if you use different reconfig\_clk sources for these altgx\_reconfig instances, the delta time between any two of these reconfig\_clk sources becoming stable must not exceed the maximum specification listed.
- (20) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level. Use H-Spice simulation to derive the minimum eye opening requirement with **Receiver Equalization** enabled.
- (21) The rise and fall time transition is specified from 20% to 80%.
- (22) Stratix IV GX devices in -4 speed grade support Basic mode and deterministic latency mode transceiver configurations up to 6375 Mbps. These configurations are shown in the figures 1-90, 1-92, 1-94, 1-96, and 1-101 in the *Transceiver Architecture in Stratix IV Devices* chapter.

Figure 1–1 shows the top-to-bottom AC gain curve for equalization settings 0 to 15.





Table 1–24 lists the Stratix IV GT transceiver specifications.

Symbol/	Conditions	–1 Industrial Speed Grade			–2 Industrial Speed Grade			-3 lı	Unit		
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max           CL <sup>(3)</sup> , LVD           706.25           425           1.6           1.5	
Reference Clock											
Supported I/O Standards	1.2 \	/ PCML, 1	.4 V P	CML, 1.5	V PCMI	_, 2.5 V	PCML, Dif	ferentia	I LVPEC	L <sup>(3)</sup> , LVDS	3
Input frequency from REFCLK input pins	_	50	_	706.25	50		706.25	50	_	706.25	MHz
Phase frequency detector (CMU PLL and receiver CDR)	_	50	_	425	50		425	50	_	425	MHz
Absolute V <sub>MAX</sub> for a REFCLK pin	_	_	_	1.6	_	_	1.6	_	_	1.6	V
Operational V <sub>MAX</sub> for a REFCLK pin	_	_	_	1.5	_	_	1.5	_	_	1.5	V
Absolute V <sub>MIN</sub> for a REFCLK pin	_	-0.3	_	_	-0.3	_	_	-0.3	_	_	V

Symbol/ Description	Conditions	–1 Ind	ustrial Grade	Speed	-2 li	ndustria Grad	al Speed e	-3 li	ndustria Grado	Unit	
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Rise/fall time	—	_	—	0.2	—	—	0.2	—	—	0.2	UI
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	_	200	_	1200	200		1200	200	_	1200	mV
On-chip termination resistors	_	_	100	_	_	100	_	_	100	_	Ω
VICM	—	12	00 ± 10	)%		1200 ± <sup>·</sup>	10%		1200 ± 1	0%	mV
	10 Hz		_	-50	—		-50	—	—	-50	dBc/Hz
	100 Hz		—	-80	—		-80	—	—	-80	dBc/Hz
Transmitter REFCLK	1 KHz		—	-110	—	—	-110	—	—	-110	dBc/Hz
Phase Noise	10 KHz		—	-120	-	—	-120	—	-	-120	dBc/Hz
	100 KHz	_	—	-120	—	—	-120	—	—	-120	dBc/Hz
	≥ 1 MHz		—	-130	—	—	-130	_	—	-130	dBc/Hz
Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK <sup>(2)</sup>	10 KHz to 20 MHz	_	_	3	_	_	3	_	_	3	ps
R <sub>REF</sub>	_	_		2000 ± 1%	_	2000 ± 1%	_	_	2000 ± 1%		Ω
Transceiver Clocks											
Calibration block clock frequency		10		125	10	_	125	10		125	MHz
reconfig_clk clock frequency	Dynamic reconfiguration clock frequency	2.5/ 37.5 (1)	_	_	2.5/ 37.5 (1)	_	50	2.5/ 37.5 (1)	_	50	MHz
fixedclk <b>clock</b> frequency	PCIe Receiver Detect	_	125	_		125	_	_	125	_	MHz
Delta time between reconfig_clks (15)	_	_	_	2	_	_	2	_	_	2	ms
Transceiver block minimum (gxb_powerdown) power-down pulse width	_	_	1	_	_	1	_	_	1	_	μs
Receiver											
Supported I/O Standards			1.4 V F	CML, 1.5	V PCN	IL, 2.5 \	/ PCML, L\	/PECL,	LVDS		
Data rate (Single width, non-PMA Direct)	_	600	_	3750	600	_	3750	600	_	3750	Mbps

Table 1-24.	Transceiver Specifications for Stratix IV GT Devices	(Part 2 of 8)
-------------	--	---------------

Symbol/ Description	Conditions	–1 Industrial Speed Grade			<b>-2 lr</b>	ndustria Grad	al Speed e	-3 lı	Unit		
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Data rate (Double width, non-PMA Direct)	_	1000	_	11300	1000	-	10312.5	1000		8500	Mbps
Data rate (Single width, PMA Direct)	_	600	-	3250	600	-	3250	600		3250	Mbps
Data rate (Double width, PMA Direct)	_	1000	-	6500	1000	-	6500	1000		6500	Mbps
Absolute V <sub>MAX</sub> for a receiver pin <sup>(4)</sup>	_	_	_	1.6	_		1.6	_		1.6	V
Operational V <sub>MAX</sub> for a receiver pin	_	_	_	1.5	_		1.5	_	_	1.5	V
Absolute V <sub>MIN</sub> for a receiver pin	_	_	-0.4	_	-0.4			-0.4	_	_	V
Maximum peak-to-peak differential input voltage V <sub>ID</sub> (diff p-p) before device configuration	_	_	_	1.6	_		1.6			1.6	V
Maximum peak-to-peak	V <sub>ICM</sub> = 0.82 V setting	_	_	2.7	_		2.7	_	_	2.7	V
differential input voltage V <sub>ID</sub> (diff p-p) after device configuration	V <sub>ICM</sub> = 1.2 V setting <sup>(5)</sup>	_	_	1.2	_	_	1.2	_	_	1.2	V
Minimum differential eye opening at the receiver serial input pins for data rates ≤ 10.3125 Gbps.	Equalization = 0 (6) DC gain = 0 dB	85		_	85		_	85		_	mV
Minimum differential eye opening at the receiver serial input pins for data rates > 10.3125 Gbps.	Equalization = 0 (6) DC gain = 0 dB	165		_	_		_			_	mV
V <sub>ICM</sub>	V <sub>ICM</sub> = 0.82 V setting	82	20 ± 10	1%		820 ± 1	0%		820 ± 1	0%	mV
<b>V</b> ICM	V <sub>ICM</sub> = 1.2 V setting <sup>(5)</sup>	12	00 ± 10	0%	1	1200 ±	10%	1	1200 ± 1	10%	mV

Symbol/ Description	Conditions	–1 Industrial Speed Grade			–2 Industrial Speed Grade			-3 li	ndustria Grad	Unit		
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max		
	85– $\Omega$ setting	8	5 ± 209	%		85 ± 20	)%		85 ± 20	)%	Ω	
Differential on-chip termination	100– $\Omega$ setting	10	)0 ± 20	%	100 ± 20%				Ω			
resistors	120– $\Omega$ setting	12	20 ± 20	%		120 ± 2	0%		120 ± 2	0%	Ω	
	150- $\Omega$ setting	15	50 ± 20	%		150 ± 2	0%		150 ± 2	0%	Ω	
Differential and common mode return loss	PCIe (Gen 1 and Gen 2), XAUI, HiGig+, CEI SR/LR, Serial RapidIO SR/LR, CPRI LV/HV, OBSAI, SATA		Compliant									
Programmable PPM detector <sup>(7)</sup>	_	_					100, 125, 2 00, 500, 10				ppm	
Run length	—	_	—	200			200		—	200	UI	
Programmable equalization	—	_	_	16			16		_	16	dB	
t <sub>LTR</sub> <sup>(8)</sup>	—	_	—	75	—	—	75	—	—	75	μs	
t <sub>LTR_LTD_Manual</sub> <sup>(9)</sup>	—	15	—	_	15		_	15	—	—	μs	
t <sub>LTD_Manual</sub> <sup>(10)</sup>	—	—	—	4000	—		4000	—	—	4000	ns	
t <sub>LTD_Auto</sub> <sup>(11)</sup>	—		—	4000			4000	—	—	4000	ns	
Receiver buffer and CDR offset cancellation time (per channel)	_	_	_	17000	_	_	17000		_	17000	reconfig_cl} CyCleS	
	DC Gain Setting = 0	_	0	—	_	0	_	_	0	_	dB	
	DC Gain Setting = 1	_	3	—	_	3	_	_	3	_	dB	
Programmable DC gain	DC Gain Setting = 2	_	6	_	_	6	_	_	6	_	dB	
	DC Gain Setting = 3	_	9	_	_	9	_	_	9	_	dB	
	DC Gain Setting = 4	_	12	_	_	12	_	_	12	_	dB	
EyeQ Max Data Rate				4.0	_		4.0		_	4.0	Gbps	

Table 1–24. Transceiver Specifications for Stratix IV GT Devices (Part 4 of 8)
Symbol/	Conditions	–1 Ind	ustrial Grade	Speed	—2 lr	idustria Grad	nl Speed e	-3 lı	ndustria Grado	ll Speed e	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
AEQ Data Rate	min V <sub>ID</sub> (diff p-p) outer envelope = 600 mV 8B/10B encoded data	2500	_	6500	2500		6500		_	_	Mbps
Decision Feedback Equalizer (DFE) Data Rate	min V <sub>ID</sub> (diff p-p) outer envelope = 600 mV	3125	_	6500	3125	_	6500	_	_	_	Mbps
Transmitter			•		•						
Supported I/O Standards		1.4 V PCML									
Data rate (Single width, non-PMA Direct)	_	600	_	3750	600		3750	600		3750	Mbps
Data rate (Double width, non-PMA Direct)	_	1000	_	11300	1000	_	10312.5	1000	_	8500	Mbps
Data rate (Single width, PMA Direct)	_	600	_	3250	600		3250	600	_	3250	Mbps
Data rate (Double width, PMA Direct) <sup>(12)</sup>	_	1000	_	6500	1000		6500	1000	_	6500	Mbps
V <sub>OCM</sub>	0.65 V setting		650	_	_	650		_	650		mV
	85– $\Omega$ setting		5 ± 15'			85 ± 1		85 ± 15%			Ω
Differential on-chip termination	100– $\Omega$ setting	10	)0 ± 15	%		100 ± 1	5%		100 ± 1	5%	Ω

120 ± 15%

150 ± 15%

Table 1-24.	<b>Transceiver S</b>	pecifications	for Stratix	<b>IV GT Devices</b>	(Part 5 of 8)

termination

resistors

120– $\Omega$  setting

150- $\Omega$  setting

120 ± 15%

150 ± 15%

120 ± 15%

150 ± 15%

Ω

Ω

Symbol/	Conditions	–1 Ind	ustrial Grade	Speed	-2 lı	ndustria Grad	al Speed e	-3 lı	ndustria Grad	ll Speed e	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Differential and common mode return loss	$\begin{array}{c} \mbox{PCle Gen1 and} \\ \mbox{Gen2 (TX} \\ \mbox{V}_{0D}=4), \\ \mbox{XAUI} \\ \mbox{(TX V}_{0D}=6), \\ \mbox{HiGig}+ \\ \mbox{(TX V}_{0D}=6), \\ \mbox{CEI SR/LR} \\ \mbox{(TX V}_{0D}=8), \\ \mbox{Serial RapidIO} \\ \mbox{SR (V}_{0D}=6), \\ \mbox{Serial RapidIO} \\ \mbox{LR (V}_{0D}=8), \\ \mbox{CPRI ApidIO} \\ \mbox{LR (V}_{0D}=6), \\ \mbox{CPRI LV} \\ \mbox{(V}_{0D}=6), \\ \mbox{CPRI HV} \\ \mbox{(V}_{0D}=2), \\ \mbox{OBSAI (V}_{0D}=6), \\ \mbox{SATA (V}_{0D}=4), \\ \end{array}$					Compli	ant				
Rise time (13)		50	—	200	50		200	50		200	ps
Fall time (13)		50	—	200	50	_	200	50		200	ps
XAUI rise time		60	—	130	60		130	60		130	ps
XAUI fall time		60	—	130	60	—	130	60	—	130	ps
Intra-differential pair skew	—		_	15	_	_	15	—	_	15	ps
Intra-transceiver block transmitter channel-to-channel skew	×4 PMA and PCS bonded mode Example: XAUI, PCIe, ×4, Basic ×4		_	120	_		120			120	ps
Inter-transceiver block transmitter channel-to-channel skew	×8 PMA and PCS bonded mode Example: PCIe ×8, Basic ×8		_	500	_	_	500	_	_	500	ps

Table 1–24. Transceiver Specifications for Stratix IV GT Devices (Part )
--

Symbol/	Conditions	–1 Ind	ustrial Grade		<b>-2 I</b> r	idustria Grad	al Speed e	-3 lı	ndustria Grad	ll Speed e	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	•
Inter-transceiver	N < 18 channels located across three transceiver blocks with the source CMU PLL located in the center transceiver block			400			400			400	ps
block skew in Basic (PMA Direct) ×N mode <sup>(14)</sup>	$N \ge 18$ channels located across four transceiver blocks with the source CMU PLL located in one of the two center transceiver blocks			650			650			650	ps
CMU PLLO and CMU	PLL1				1		1		1		
Supported data range	_	600	_	11300	600	_	10312.5	600	_	8500	Mbps
CMU PLL lock time from pll_powerdown de-assertion	_	_	_	100	_	_	100	_	_	100	μS
ATX PLL (6G)			•								
	/L = 1		)-5400 )00-65			00-540 6000-6			300-540 6000-6		Mbps
Supported Data Range	/L = 2		)-2700 )00-32			00-270 3000-3			100-270 3000-3		Mbps
	/L = 4		)-1350 600-16			200-135 1500-1			200-135 1500-1		Mbps
ATX PLL (10G)											
Supported Data Range		9900		11300	9900		10312.5				Mbps
Transceiver-FPGA Fa	bric Interface										
Interface speed (non-PMA Direct)	_	25	_	325	25		325	25	_	265.625	MHz
Interface speed (PMA Direct)	_	50	_	325	50		325	50		325	MHz

#### Table 1–24. Transceiver Specifications for Stratix IV GT Devices (Part 7 of 8)

Symbol/	Conditions	–1 Industrial Speed Grade			–2 Industrial Speed Grade			–3 Industrial Speed Grade			Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Digital reset pulse width	_			Minin	num is <sup>-</sup>	two par	allel clock	cycles			_

#### Table 1–24. Transceiver Specifications for Stratix IV GT Devices (Part 8 of 8)

#### Notes to Table 1-24:

- (1) The minimum reconfig\_clk frequency is 2.5 MHz if the transceiver channel is configured in Transmitter Only mode. The minimum reconfig\_clk frequency is 37.5 MHz if the transceiver channel is configured in Receiver only or Receiver and Transmitter mode. For more information, refer to the Dynamic Reconfiguration in Stratix IV Devices chapter.
- (2) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz \* 100/f.
- (3) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
- (4) The device cannot tolerate prolonged operation at this absolute maximum.
- (5) You must use the 1.2-V RXV<sub>ICM</sub> setting if the input serial data standard is LVDS.
- (6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level. Use H-Spice simulation to derive the minimum eye opening requirement with **Receiver Equalization** enabled.
- (7) The rate matcher supports only up to  $\pm$  300 ppm.
- (8) Time taken to rx pll locked goes high from rx analogreset de-assertion. Refer to Figure 1-2 on page 1-33.
- (9) Time for which the CDR must be kept in lock-to-reference mode after rx\_pll\_locked goes high and before rx\_locktodata is asserted in manual mode. Refer to Figure 1-2 on page 1-33.
- (10) Time taken to recover valid data after the rx locktodata signal is asserted in manual mode. Refer to Figure 1-2 on page 1-33.
- (11) Time taken to recover valid data after the rx freqlocked signal goes high in automatic mode. Refer to Figure 1-3 on page 1-33.
- (12) A GPLL may be required to meet the PMA-FPGA fabric interface timing above certain data rates. For more information, refer to the "Left/Right PLL Requirements in Basic (PMA Direct) Mode" section in the *Transceiver Clocking in Stratix IV Devices* chapter.
- (13) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (14) For applications that require low transmit lane-to-lane skew, use Basic (PMA Direct) xN to achieve PMA-Only bonding across all channels in the link. You can bond all channels on one side of the device by configuring them in Basic (PMA Direct) xN mode. For more information about clocking requirements in this mode, refer to the "Basic (PMA Direct) Mode Clocking" section in the *Transceiver Clocking in Stratix IV Devices* chapter.
- (15) If your design uses more than one dynamic reconfiguration controller (altgx\_reconfig) instances to control the transceiver (altgx) channels physically located on the same side of the device AND if you use different reconfig\_clk sources for these altgx\_reconfig instances, the delta time between any two of these reconfig\_clk sources becoming stable must not exceed the maximum specification listed.

Figure 1–2 shows the lock time parameters in manual mode.

LTD = Lock-To-Data; LTR = Lock-To-Reference





Figure 1–3 shows the lock time parameters in automatic mode.

Figure 1–3. Lock Time Parameters for Automatic Mode



Table 1–25 through Table 1–28 lists the typical differential  $V_{OD}$  termination settings for Stratix IV GX and GT devices.

Table 1–25.	Typical	VoD Setting,	TX Term	<b>= 85</b> Ω
-------------	---------	--------------	---------	---------------

Sumbol				V <sub>od</sub> Sett	ing (mV)			
Symbol	0	1	2	3	4	5	6	7
V <sub>OD</sub> differential peak-to-peak Typical (mV)	170 ± 20%	340 ± 20%	510 ± 20%	595 ± 20%	680 ± 20%	765 ± 20%	850 ± 20%	1020± 20%

#### Table 1–26. Typical V\_{\text{OD}} Setting, TX Term = 100 $\Omega$

Sumbol				V <sub>od</sub> Sett	ing (mV)			
Symbol	0	1	2	3	4	5	6	7
V <sub>OD</sub> differential peak-to-peak Typical (mV)	200 ± 20%	400 ± 20%	600 ± 20%	700 ± 20%	800 ± 20%	900 ± 20%	1000 ± 20%	1200 ± 20%

#### Table 1–27. Typical V<sub>oD</sub> Setting, TX Term = 120 $\Omega$

Symbol	V <sub>OD</sub> Setting (mV)										
Symbol	0	1	2	3	4	5	6				
V <sub>OD</sub> differential peak-to-peak Typical (mV)	240 ± 20%	480 ± 20%	720 ± 20%	840 ± 20%	960 ± 20%	1080 ± 20%	1200 ± 20%				

#### Table 1–28. Typical V<sub>OD</sub> Setting, TX Term = 150 $\Omega$

Symbol			V <sub>op</sub> Sett	ing (mV)		
Symbol	0	1	2	3	4	5
V <sub>OD</sub> differential peak-to-peak Typical (mV)	300 ± 20%	600 ± 20%	900 ± 20%	1050 ± 20%	1200 ± 20%	1350 ± 20%

Table 1–29 lists typical transmitter pre-emphasis levels in dB for the first post tap under the following conditions (low-frequency data pattern [five 1s and five 0s] at 6.25 Gbps). The levels listed in Table 1–29 are a representation of possible pre-emphasis levels under the specified conditions only and that the pre-emphasis levels may change with data pattern and data rate.

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Stratix IV HSSI HSPICE models.

#### Table 1–29. Transmitter Pre-Emphasis Levels for Stratix IV Devices (Part 1 of 2)

Pre-Emphasis 1st		V <sub>OD</sub> Setting										
Pre-Emphasis 1st Post-Tap Setting	0	1	2	3	4	5	6	7				
0	0	0	0	0	0	0	0	0				
1	N/A	0.7	0	0	0	0	0	0				
2	N/A	1	0.3	0	0	0	0	0				
3	N/A	1.5	0.6	0	0	0	0	0				

Pre-Emphasis 1st				V <sub>od</sub> S	etting			
Post-Tap Setting	0	1	2	3	4	5	6	7
4	N/A	2	0.7	0.3	0	0	0	0
5	N/A	2.7	1.2	0.5	0.3	0	0	0
6	N/A	3.1	1.3	0.8	0.5	0.2	0	0
7	N/A	3.7	1.8	1.1	0.7	0.4	0.2	0
8	N/A	4.2	2.1	1.3	0.9	0.6	0.3	0
9	N/A	4.9	2.4	1.6	1.2	0.8	0.5	0.2
10	N/A	5.4	2.8	1.9	1.4	1	0.7	0.3
11	N/A	6	3.2	2.2	1.7	1.2	0.9	0.4
12	N/A	6.8	3.5	2.6	1.9	1.4	1.1	0.6
13	N/A	7.5	3.8	2.8	2.1	1.6	1.2	0.6
14	N/A	8.1	4.2	3.1	2.3	1.7	1.3	0.7
15	N/A	8.8	4.5	3.4	2.6	1.9	1.5	0.8
16	N/A	N/A	4.9	3.7	2.9	2.2	1.7	0.9
17	N/A	N/A	5.3	4	3.1	2.4	1.8	1.1
18	N/A	N/A	5.7	4.4	3.4	2.6	2	1.2
19	N/A	N/A	6.1	4.7	3.6	2.8	2.2	1.4
20	N/A	N/A	6.6	5.1	4	3.1	2.4	1.5
21	N/A	N/A	7	5.4	4.3	3.3	2.7	1.7
22	N/A	N/A	8	6.1	4.8	3.8	3	2
23	N/A	N/A	9	6.8	5.4	4.3	3.4	2.3
24	N/A	N/A	10	7.6	6	4.8	3.9	2.6
25	N/A	N/A	11.4	8.4	6.8	5.4	4.4	3
26	N/A	N/A	12.6	9.4	7.4	5.9	4.9	3.3
27	N/A	N/A	N/A	10.3	8.1	6.4	5.3	3.6
28	N/A	N/A	N/A	11.3	8.8	7.1	5.8	4
29	N/A	N/A	N/A	12.5	9.6	7.7	6.3	4.3
30	N/A	N/A	N/A	N/A	11.4	9	7.4	N/A
31	N/A	N/A	N/A	N/A	12.9	10	8.2	N/A

 Table 1–29.
 Transmitter Pre-Emphasis Levels for Stratix IV Devices (Part 2 of 2)

Table 1–30 lists the Stratix IV GX transceiver jitter specifications for all supported protocols. For protocols supported by Stratix IV GT industrial speed grade devices, refer to the Stratix IV GX –2 commercial speed grade column in Table 1–30.

Table 1-30.	. Transceiver Block Jitter Specifications for Stratix IV GX Devices <sup>(1)</sup> , <sup>(2)</sup>	(Part 1 of 9)
-------------	---	---------------

Symbol/ Description	Conditions		Commo eed G	ercial rade						ercial/ Speed	Unit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
SONET/SDH Transmit Jitt	er Generation <sup>(4)</sup>										
Peak-to-peak jitter at 622.08 Mbps	Pattern = PRBS15	_		0.1	_	_	0.1	_		0.1	UI
RMS jitter at 622.08 Mbps	Pattern = PRBS15	_	_	0.01	-	_	0.01	_	_	0.01	UI
Peak-to-peak jitter at 2488.32 Mbps	Pattern = PRBS15	_	_	0.1	_	_	0.1	_		0.1	UI
RMS jitter at 2488.32 Mbps	Pattern = PRBS15	_	_	0.01	_	_	0.01	_	_	0.01	UI
SONET/SDH Receiver Jit	ter Tolerance <sup>(4)</sup>	· · · · ·									
	Jitter frequency = 0.03 KHz		> 15			> 15			> 1	5	UI
	Pattern = PRBS15										
Jitter tolerance at 622.08 Mbps	Jitter frequency = 25 KHZ	> 1.5				> 1.5			> 1.	5	UI
	Pattern = PRBS15										
	Jitter frequency = 250 KHz		> 0.15 > 0.15				> 0.15			UI	
	Pattern = PRBS15										
	Jitter frequency = 0.06 KHz		> 15		> 15 > 15		5	UI			
	Pattern = PRBS15										
	Jitter frequency = 100 KHZ	> 1.5 > 1.5 > 1.5		5	UI						
Jitter tolerance at 2488.32 Mbps	Pattern = PRBS15										
	Jitter frequency = 1 MHz		> 0.15 > 0.15		5		> 0.1	5	UI		
	Pattern = PRBS15										
	Jitter frequency = 10 MHz Pattern = PRBS15	> 0.15			> 0.15	j.	> 0.15			UI	
	Jitter Generation <sup>(5)</sup> , <sup>(13)</sup>	1	1	1	1	1	1	1	1		1
Total jitter FC-1	Pattern = CRPAT		—	0.23	—		0.23		-	0.23	UI
Deterministic jitter FC-1	Pattern = CRPAT		-	0.11	—		0.11		-	0.11	UI
Total jitter FC-2	Pattern = CRPAT		<u> </u>	0.33	—		0.33		<u> </u>	0.33	UI
Deterministic jitter FC-2	Pattern = CRPAT	_	—	0.2	—	—	0.2	—		0.2	UI

Symbol/ Description	Conditions		Comm eed G		-3 Commercial/ I Industrial and -2× Commercial Speed Grade		-4 (	Comm	y <sup>(3)</sup> and ercial/ Speed le	Unit	
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Total jitter FC-4	Pattern = CRPAT	—	—	0.52	—	—	0.52	—	—	0.52	UI
Deterministic jitter FC-4	Pattern = CRPAT	_	_	0.33	_	_	0.33	— — 0.33		0.33	UI
Fibre Channel Receiver	Jitter Tolerance <sup>(5)</sup> , <sup>(14)</sup>										
Deterministic jitter FC-1	Pattern = CJTPAT		> 0.3	7		> 0.37	,		> 0.3	37	UI
Random jitter FC-1	Pattern = CJTPAT		> 0.3	1		> 0.31			> 0.3	31	UI
Sinusoidal jitter FC-1	Fc/25000		> 1.5	5		> 1.5			> 1.	5	UI
Sinusolual jiller ru-r	Fc/1667		> 0.1			> 0.1			> 0.	1	UI
Deterministic jitter FC-2	Pattern = CJTPAT		> 0.3	3		> 0.33	}		> 0.3	3	UI
Random jitter FC-2	Pattern = CJTPAT		> 0.29 > 0.29			> 0.2	29	UI			
Sinusoidal jitter FC-2	Fc/25000		> 1.5 > 1.5			> 1.	5	UI			
•	Fc/1667		> 0.1 > 0.1			> 0.	1	UI			
Deterministic jitter FC-4	Pattern = CJTPAT				> 0.3	3	UI				
Random jitter FC-4	Pattern = CJTPAT		> 0.29 > 0.29			> 0.2	29	UI			
Sinusoidal jitter FC-4	Fc/25000		> 1.5 > 1.5			> 1.		UI			
	Fc/1667		> 0.1			> 0.1			> 0.	1	UI
XAUI Transmit Jitter Gen	eration <sup>(6)</sup>										
Total jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.3		—	0.3	_	—	0.3	UI
Deterministic jitter at 3.125 Gbps	Pattern = CJPAT	_	_	0.17	_	_	0.17	_	_	0.17	UI
XAUI Receiver Jitter Tole	erance <sup>(6)</sup>	•				•	•				
Total jitter	_		> 0.6	5		> 0.65	;		> 0.6	65	UI
Deterministic jitter	—		> 0.3	7		> 0.37	,	> 0.37		37	UI
Peak-to-peak jitter	Jitter frequency = 22.1 KHz		> 8.5	5		> 8.5		> 8.5		5	UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz		> 0.1 > 0.1 > 0.1		1	UI					
Peak-to-peak jitter	Jitter frequency = 20 MHz	> 0.1 > 0.1 > 0.1		1	UI						
PCIe Transmit Jitter Gen	eration <sup>(7)</sup>				I						
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern		_	0.25	_	_	0.25	_	_	0.25	UI
Total jitter at 5 Gbps (Gen2) <sup>(15)</sup>	Compliance pattern	_	—	0.25	-	_	0.25	-	—	_	UI
PCIe Receiver Jitter Tole	erance <sup>(7)</sup>		I	I	1	1	1	L	1		J
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern		> 0.6		> 0.6			> 0.6			UI

## Table 1–30. Transceiver Block Jitter Specifications for Stratix IV GX Devices <sup>(1)</sup>, <sup>(2)</sup> (Part 2 of 9)

Symbol/ Description	Conditions			commercial -3 Commercial/ -3 Military <sup>(3)</sup> and Industrial -4 Commercial/ and -2× Commercial Industrial Speed Speed Grade Grade				ercial/ Speed	Unit		
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Total jitter at 5 Gbps (Gen2)	Compliance pattern	C	omplia	ant	(	Complia	int				UI
PCIe (Gen 1) Electrical Id	lle Detect Threshold										
V <sub>RX-IDLE-DETDIFFp-p</sub> (16)	Compliance pattern	65	—	175	65	—	175	65	—	175	UI
Serial RapidIO Transmit	litter Generation <sup>(8)</sup>										
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps	_		0.17	_	_	0.17	_		0.17	UI
(peak-to-peak)	Pattern = CJPAT										
Total jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps	_		0.35	_	_	0.35	_		0.35	UI
0	Pattern = CJPAT										
Serial RapidIO Receiver A Deterministic jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps		> 0.37 > 0.37			> 0.37		UI			
	Pattern = CJPAT										
Combined deterministic and random jitter	Data Rate = 1.25, 2.5, 3.125 Gbps		> 0.5	5	> 0.55			> 0.5	5	UI	
tolerance (peak-to-peak)	Pattern = CJPAT										
	Jitter Frequency = 22.1 KHz Data Rate = 1.25, 2.5, 3.125 Gbps		> 8.5	i		> 8.5			> 8.5		UI
	Pattern = CJPAT										
	Jitter Frequency = 1.875 MHz										
Sinusoidal jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps	> 0.1			> 0.1				> 0.	1	UI
	Pattern = CJPAT										
	Jitter Frequency = 20 MHz										
	Data Rate = 1.25, 2.5, 3.125 Gbps		> 0.1		> 0.1				> 0.	1	UI
	Pattern = CJPAT										
GIGE Transmit Jitter Gen	eration <sup>(9)</sup>										
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	_	—	0.14	_	_	0.14	_	_	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	_		0.279		_	0.279			0.279	UI

Table 1–30. Transceiver Block Jitter Specifications for Stratix IV GX Devices <sup>(1)</sup> , <sup>(2)</sup> (Par	rt 3 of 9)
--	------------

Symbol/ Description	Conditions	–2 Commercial Speed Grade			–3 Commercial/ Industrial and –2× Commercial Speed Grade			–3 Military <sup>(3)</sup> and –4 Commercial/ Industrial Speed Grade			Unit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
GIGE Receiver Jitter Tole	rance <sup>(9)</sup>			-	-						
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4		> 0.4			UI	
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.6	6	UI	
HiGig Transmit Jitter Gen	eration <sup>(10)</sup>										
Deterministic jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	_		0.17	_	_	_				UI
Total jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	_		0.35	_	_	_	_	_		UI
HiGig Receiver Jitter Tol	erance <sup>(10)</sup>					1	1				
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT		> 0.3	7	_	_	_		_		UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT		> 0.6	5	_	_		_	_		UI
	Jitter Frequency = 22.1 KHz Data Rate = 3.75 Gbps Pattern = CJPAT		> 8.5	j	_		_	_	_	_	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 1.875MHz Data Rate = 3.75 Gbps		> 0.1								UI
	Pattern = CJPAT Jitter Frequency = 20 MHz Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.1								UI	
(OIF) CEI Transmitter Jitt	er Generation <sup>(11)</sup>										
Total jitter (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS15 BER = 10 <sup>-12</sup>	_		0.3	_	_	0.3	_		0.3	UI
(OIF) CEI Receiver Jitter	Tolerance <sup>(11)</sup>		•			•			•		•
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10 <sup>-12</sup>			> 0.675 > 0.675 — — >0.675				>0.675	UI		

### Table 1–30. Transceiver Block Jitter Specifications for Stratix IV GX Devices <sup>(1)</sup>, <sup>(2)</sup> (Part 4 of 9)

Symbol/ Description	Conditions		–2 Commercial Speed Grade		–3 Commercial/ Industrial and –2× Commercial Speed Grade			-4 (	y <sup>(3)</sup> and ercial/ Speed le	Unit	
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern=PRBS31 BER = 10 <sup>-12</sup>		> 0.98	8		> 0.988	3	_	_	>0.988	UI
	Jitter Frequency = 38.2 KHz										
	Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10 <sup>-12</sup>		> 5		> 5		_		> 5	UI	
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 3.82 MHz										
	Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10 <sup>-12</sup>	> 0.05		> 0.05			_	_	> 0.05	UI	
	Jitter Frequency = 20 MHz										
	Data Rate= 6.375 Gbps Pattern = PRBS31 BER = 10 <sup>-12</sup>		> 0.0	5	> 0.05		_	_	> 0.05	UI	
SDI Transmitter Jitter Ge	neration <sup>(12)</sup>										
Alignment jitter	Data Rate = 1.485 Gbps (HD) Pattern = Color Bar Low-Frequency Roll-Off = 100 KHz	0.2	_		0.2	_		0.2	_		UI
(peak-to-peak)	Data Rate = 2.97 Gbps (3G) Pattern = Color Bar Low-Frequency Roll-Off = 100 KHz	0.3			0.3			0.3	_		UI

Table 1–30. Transceiver Block Jitter Specifications for Stratix IV GX Devices <sup>(1)</sup>, <sup>(2)</sup> (Part 5 of 9)

Symbol/ Description	Conditions	-	Commo eed Gi				Industrial and –2× Commercial		-4 Commercial/			Unit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max		
SDI Receiver Jitter Tolera	ance <sup>(12)</sup>											
	Jitter Frequency = 15 KHz											
	Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar	> 2			> 2			> 2			UI	
Sinusoidal jitter	Jitter Frequency = 100 KHz		> 0.3 > 0.3									
tolerance (peak-to-peak)	Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar				> 0.3	3	UI					
	Jitter Frequency = 148.5 MHz											
	Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar	> 0.3 > 0.3			> 0.3	UI						
	Jitter Frequency = 20 KHz											
	Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar	>1 >1		>1		UI						
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 100 KHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar	> 0.2 > 0.2 > 0.2		2	UI							
	Jitter Frequency = 148.5 MHz											
	Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar	> 0.2 > 0.2		> 0.2	2	UI						
SAS Transmit Jitter Gene	ration <sup>(17)</sup>											
Total jitter at 1.5 Gbps (G1)	Pattern = CJPAT			0.55			0.55			0.55	UI	
Deterministic jitter at 1.5 Gbps (G1)	Pattern = CJPAT	_		0.35			0.35			0.35	UI	
Total jitter at 3.0 Gbps (G2)	Pattern = CJPAT	_		0.55	_		0.55		_	0.55	UI	
Deterministic jitter at 3.0 Gbps (G2)	Pattern = CJPAT			0.35	_		0.35			0.35	UI	
Total jitter at 6.0 Gbps (G3)	Pattern = CJPAT	_	_	0.25			0.25	_	_	0.25	UI	

Table 1–30. Transceiver Block Jitter Specifications for Stratix IV GX Devices <sup>(1)</sup> , <sup>(2)</sup> (Part 6 of 9)	Table 1-30	Transceiver Block	Jitter Specifications	s for Stratix IV GX Devi	ces <sup>(1)</sup> , <sup>(2)</sup>	(Part 6 of 9)
---	------------	-------------------	-----------------------	--------------------------	-------------------------------------	---------------

Symbol/ Description	Conditions	-2 (		ercial	–3 Commercial/ Industrial and –2× Commercial Speed Grade			–3 Military <sup>(3)</sup> and –4 Commercial/ Industrial Speed Grade			Unit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Random jitter at 6.0 Gbps (G3)	Pattern = CJPAT			0.15			0.15			0.15	UI
SAS Receiver Jitter Tole	rance <sup>(17)</sup>										
Total Jitter tolerance at 1.5 Gbps (G1)	Pattern = CJPAT	> 0.65 > 0.65 > 0.65			65	UI					
Deterministic Jitter tolerance at 1.5 Gbps (G1)	Pattern = CJPAT	> 0.35 > 0.35			> 0.3	35	UI				
Sinusoidal Jitter tolerance at 1.5 Gbps	Jitter Frequency = 900 KHz to 5 MHz	>01 >01			× 0.1	1	UI				
(G1)	Pattern = CJTPAT BER = 1E-12	> 0.1 > 0.1			> 0.1		1	UI			
<b>CPRI Transmit Jitter Ger</b>	eration <sup>(18)</sup>										
	E.6.HV, E.12.HV Pattern = CJPAT	_	_	0.279	_	_	0.279	_	_	0.279	UI
Total Jitter	E.6.LV, E.12.LV, E.24.LV, E.30.LV			0.35			0.35			0.35	UI
	Pattern = CJTPAT										
	E.6.HV, E.12.HV Pattern = CJPAT	_	_	0.14	_	_	0.14	_	_	0.14	UI
Deterministic Jitter	E.6.LV, E.12.LV, E.24.LV, E.30.LV			0.17		_	0.17			0.17	UI
	Pattern = CJTPAT										
<b>CPRI Receiver Jitter Tol</b>	erance <sup>(18)</sup>										
Total jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT		> 0.6	6		> 0.66	6		> 0.6	6	UI
Deterministic jitter	E.6.HV, E.12.HV		> 0.4	1		> 0.4			> 0.4	4	UI
tolerance	Pattern = CJPAT		/ 0	r		<i>&gt;</i> 0.न			20.	т	01
Total jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV	> 0.65 > 0.65			> 0.6	65	UI				
	Pattern = CJTPAT										
Deterministic jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV	> 0.37		> 0.37			> 0.37			UI	
	Pattern = CJTPAT										
Combined deterministic and random jitter	E.6.LV, E.12.LV, E.24.LV, E.30.LV		> 0.5	5		> 0.55	5	> 0.55			UI
tolerance	Pattern = CJTPAT										

Table 1-30.	Transceiver Block Jitter Specifications for Str	atix IV GX Devices <sup>(1)</sup> , <sup>(2)</sup>	(Part 7 of 9)
Table 1-00.		ally in the methods $(1, 1)$	(1 a) (1 0) 3)

Symbol/ Description	Conditions		Comm eed G	ercial rade	–3 Commercial/ Industrial and –2× Commercial Speed Grade			–3 Military <sup>(3)</sup> and –4 Commercial/ Industrial Speed Grade			Unit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
OBSAI Transmit Jitter Ge	neration <sup>(19)</sup>										
Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6MHz Pattern = CJPAT	_	_	0.35	_		0.35	_	_	0.35	UI
Deterministic jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6MHz Pattern = CJPAT	_	_	0.17	_	_	0.17	_	_	0.17	UI
<b>OBSAI Receiver Jitter To</b>	lerance <sup>(19)</sup>										
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.37		> 0.37			> 0.37			UI	
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.55		> 0.55		> 0.55		UI			
Sinusoidal Jitter	Jitter Frequency = 5.4 KHz Pattern = CJPAT		> 8.5	j		> 8.5		> 8.5			UI
tolerance at 768 Mbps	Jitter Frequency = 460 MHz to 20 MHz Pattern = CJPAT		> 0.1			> 0.1			> 0.1		
Sinusoidal Jitter	Jitter Frequency = 10.9 KHz Pattern = CJPAT		> 8.5	j		> 8.5			> 8.	5	UI
tolerance at 1536 Mbps	Jitter Frequency = 921.6 MHz to 20 MHz Pattern = CJPAT		> 0.1			> 0.1			> 0.1		UI

## Table 1–30. Transceiver Block Jitter Specifications for Stratix IV GX Devices <sup>(1)</sup>, <sup>(2)</sup> (Part 8 of 9)

Symbol/ Description	Conditions	–2 Commercial Speed Grade		–3 Commercial/ Industrial and –2× Commercial Speed Grade			–3 Military <sup>(3)</sup> and –4 Commercial/ Industrial Speed Grade			Unit	
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Sinusoidal Jitter	Jitter Frequency = 21.8 KHz Pattern = CJPAT	> 8.5 > 8.5 > 8.5		ō	UI						
tolerance at 3072 Mbps	Jitter Frequency = 1843.2 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI

#### Table 1–30. Transceiver Block Jitter Specifications for Stratix IV GX Devices (1), (2) (Part 9 of 9)

#### Notes to Table 1-30:

- (1) Dedicated refclk pins were used to drive the input reference clocks.
- (2) The Jitter numbers are valid for the stated conditions only.

(3) Stratix IV GX devices in military speed grade only support selected transceiver configuration up to 3125 Mbps. For more information, contact Altera sales representative.

- (4) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
- (5) The jitter numbers for Fibre Channel are compliant to the FC-PI-4 Specification revision 6.10.
- (6) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
- (7) The jitter numbers for PCI Express (PIPE) (PCIe) are compliant to the PCIe Base Specification 2.0.
- (8) The jitter numbers for Serial RapidIO are compliant to the RapidIO Specification 1.3.
- (9) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
- (10) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.
- (11) The jitter numbers for (OIF) CEI are compliant to the OIF-CEI-02.0 Specification.
- (12) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
- (13) The fibre channel transmitter jitter generation numbers are compliant to the specification at  $\delta_T$  interoperability point.
- (14) The fibre channel receiver jitter tolerance numbers are compliant to the specification at  $\delta_{R}$  interoperability point.
- (15) You must use the ATX PLL adjacent to the transceiver channels to meet the transmitter jitter generation compliance in PCIe Gen2 ×8 modes.
- (16) Stratix IV PCIe receivers are compliant to this specification provided the V<sub>TX-CM-DC-ACTIVEIDLE-DELTA</sub> of the upstream transmitter is less than 50mV.
- (17) The jitter numbers for Serial Attached SCSI (SAS) are compliant to the SAS-2.1 Specification.
- (18) The jitter numbers for CPRI are compliant to the CPRI Specification V3.0.
- (19) The jitter numbers for OBSAI are compliant to the OBSAI RP3 Specification V4.1.

Table 1–31 lists the transceiver jitter specifications for protocols supported by Stratix IV GT devices.

Symbol/ Description	Conditions		ustrial S Grade	Speed	—2 Ind	ustrial Grade		–3 Industrial Speed Grade			Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
XLAUI/CAUI Trans	mit Jitter Generation <sup>(1)</sup> , <sup>(3)</sup>										
Total Jitter	Pattern = PRBS-31		—	0.30			0.30		—	0.30	UI
	V <sub>0D</sub> = 800 mV										
Deterministic	REFCLK = 644.53 MHz				_	— 0.17			0.47		
Jitter	4 (XLAUI)/ 10 (CAUI) channels in Basic ×1 mode	—	_	0.17			0.17	_	_	0.17	UI
XLAUI/CAUI Rece	iver Jitter Tolerance <sup>(1)</sup>			•					•		•
Total Jitter tolerance	Pattern = PRBS-31	> 0.62				> 0.62					UI
Sinusoidal Jitter	Jitter Frequency = 40 KHz Pattern = PRBS-31 Equalization = Disabled	> 5 > 5 —					UI				
	BER = 1E-12										
tolerance	Jitter Frequency ≥ 4 MHz Pattern = PRBS-31	> 0.05			> 0.05			_			UI
	Equalization = Disabled BER = 1E-12										
XFI Transmitter J	itter Generation <sup>(2)</sup> , <sup>(3)</sup>		-	_		-	_	-	_	-	
	Pattern = PRBS-31										
Total jitter at	Vod = 800 mV			0.3			0.3				UI
10.3125 Gbps	REFCLK = 644.53 MHz	_		0.5			0.3	_		_	UI
	10 channels in Basic ×1 mode										
OTL 4.10 <sup>(1)</sup> , <sup>(3)</sup>							1		•		1
Total Jitter at 11.18 Gbps	Pattern = PRBS-31 - V <sub>OD</sub> = 800 mV	-	-	0.30	-	-	0.30	_		0.30	UI
Deterministic Jitter	refclk = 698.75 MHz	_	_	0.17	_	_	0.17	_	_	0.17	UI

Table 1–31. Transceiver Jitter Specifications for Protocols by Stratix IV GT Devices (Part 1 of 2)

Symbol/ Description	Conditions		ustrial S Grade						–3 Industrial Speed Grade		
Description		Min	Тур	Max	Grade Grade Unit						
	Jitter Frequency = 40 KHz										
	Pattern = PRBS-31				. <b>F</b>						111
	Equalization = Disabled	> 5			> 0						UI
Sinusoidal Jitter	BER = 1E-12										
tolerance	Jitter Frequency $\geq$ 4 MHz										
	Pattern = PRBS-31		0.05			0.05					
	Equalization = Disabled								U		
	BER = 1E-12										

#### Table 1–31. Transceiver Jitter Specifications for Protocols by Stratix IV GT Devices (Part 2 of 2)

#### Notes to Table 1-31:

(1) The jitter numbers for XLAUI/CAUI are compliant to the IEEE P802.3ba specification.

(2) Stratix IV GT transceivers are compliant to the XFI datacom transmitter jitter specifications in Table 9 of XFP Revision 4.1.

(3) Contact Altera for board and link best practices at BER = 1E-15.

Table 1–32. SFI-S Transmitter Jitter S	Specifications for Stratix IV GT Devices <sup>(1)</sup> , <sup>(2)</sup>
--	--

Symbol/Description	Conditions	-1 Industrial Speed Grade Mean	-2 Industrial Speed Grade Mean	-3 Industrial Speed Grade Mean	Unit
Total Transmitter jitter at 11.3 Gbps <sup>(4)</sup>	Pattern = PRBS-31 Vod = 800 mV REFCLK = 706.25 MHz 12 channels in Basic ×1 mode	0.23 UI <sup>(3)</sup>	_	_	UI

#### Notes to Table 1-32:

(1) Dedicated refclk pins were used to drive the input reference clocks.

- (2) The jitter numbers are valid for stated conditions only.
- (3) Two hundred channels were characterized to derive the mean transmitter jitter specification of 0.23 UI. The maximum jitter across the 200 units characterized was 0.30 UI.
- (4) Contact Altera for board and link best practices at BER = 1E-15.

### **Transceiver Datapath PCS Latency**

**For more information about:** 

- Basic mode PCS latency, refer to Figure 1-90 through Figure 1-97 in the *Transceiver Architecture in Stratix IV Devices* chapter.
- PCIe mode PCS latency, refer to Figure 1-102 in the *Transceiver Architecture in* Stratix IV Devices chapter.
- XAUI mode PCS latency, refer to Figure 1-119 in the *Transceiver Architecture in Stratix IV Devices* chapter.
- GIGE mode PCS latency, refer to Figure 1-128 in the *Transceiver Architecture in Stratix IV Devices* chapter.
- SONET/SDH mode PCS latency, refer to Figure 1-136 in the *Transceiver Architecture in Stratix IV Devices* chapter.
- SDI mode PCS latency, refer to Figure 1-141 in the *Transceiver Architecture in Stratix IV Devices* chapter.
- (OIF) CEI PHY mode PCS latency, refer to Figure 1-143 in the *Transceiver Architecture in Stratix IV Devices* chapter.

## **Core Performance Specifications**

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), TriMatrix, configuration, JTAG, and chip-wide reset (Dev\_CLRn) specifications.

For the Stratix IV GT -1 and -2 speed grade specifications, refer to the  $-2/-2 \times$  speed grade column. For the Stratix IV GT -3 speed grade specification, refer to the -3 speed grade column, unless otherwise specified.

### **Clock Tree Specifications**

Table 1–33 lists the clock tree specifications for Stratix IV devices.

Table 1–33. Clock Tree Performance for Stratix IV Devices

Performance								
Symbol	–2/–2× Speed Grade	–3 Speed Grade	–4 Speed Grade	Unit				
Global clock and Regional clock	800	700	500	MHz				
Periphery clock	550	500	500	MHz				

## **PLL Specifications**

Table 1–34 lists the Stratix IV PLL specifications when operating in the commercial (0° to 85°C), industrial (–40° to 100°C), and military (–55°C to 125°C) junction temperature ranges.

Table 1–34. PLL Specifications for Stratix IV Devices (Part 1 of 2)

Symbol	Parameter	Min	Тур	Max	Unit
	Input clock frequency (-2/-2x speed grade)	5	—	800 (1)	MHz
f <sub>IN</sub>	Input clock frequency (-3 speed grade)	5	—	717 <sup>(1)</sup>	MHz
	Input clock frequency (-4 speed grade)	5		717 <sup>(1)</sup>	MHz
f <sub>INPFD</sub>	Input frequency to the PFD	5		325	MHz
	PLL VCO operating range (-2 speed grade)	600		1600	MHz
f <sub>VC0</sub> (2)	PLL VCO operating range (-3 speed grade)	600	—	1300	MHz
	PLL VCO operating range (-4 speed grade)	600		1300	MHz
t <sub>einduty</sub>	Input clock or external feedback clock input duty cycle	40		60	%
	Output frequency for internal global or regional clock $(-2/-2x \text{ speed grade})$	_	_	800 <sup>(3)</sup>	MHz
f <sub>OUT</sub>	Output frequency for internal global or regional clock (-3 speed grade)	_	_	717 <sup>(3)</sup>	MHz
	Output frequency for internal global or regional clock (-4 speed grade)		_	717 <sup>(3)</sup>	MHz
	Output frequency for external clock output (-2 speed grade)		—	800 <sup>(3)</sup>	MHz
f <sub>OUT_EXT</sub>	Output frequency for external clock output (-3 speed grade)			717 <sup>(3)</sup>	MHz
	Output frequency for external clock output (-4 speed grade)		—	717 <sup>(3)</sup>	MHz
t <sub>outduty</sub>	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t <sub>FCOMP</sub>	External feedback clock compensation time			10	ns
t <sub>configpll</sub>	Time required to reconfigure scan chain	_	3.5	_	scanclk cycles
t <sub>configphase</sub>	Time required to reconfigure phase shift	_	1	_	scanclk cycles
f <sub>scanclk</sub>	scanclk frequency	_		100	MHz
t <sub>LOCK</sub>	Time required to lock from end-of-device configuration or de-assertion of areset	_	_	1	ms
t <sub>DLOCK</sub>	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	_	_	1	ms
	PLL closed-loop low bandwidth	_	0.3	—	MHz
f <sub>CLBW</sub>	PLL closed-loop medium bandwidth		1.5	—	MHz
	PLL closed-loop high bandwidth <sup>(8)</sup>		4	—	MHz
t <sub>PLL_PSERR</sub>	Accuracy of PLL phase shift		—	±50	ps
t <sub>ARESET</sub>	Minimum pulse width on the areset signal	10	—	—	ns
+ (4) (5)	Input clock cycle to cycle jitter ( $F_{\text{REF}} \geq 100 \text{ MHz})$	—	—	0.15	UI (p-p)
t <sub>INCCJ</sub> <sup>(4)</sup> , <sup>(5)</sup>	Input clock cycle to cycle jitter (F <sub>REF</sub> < 100 MHz)	—	—	±750	ps (p-p)
+ (6)	Period Jitter for dedicated clock output ( $F_{OUT} \geq 100 \text{ MHz})$	—	—	175	ps (p-p)
t <sub>outpj_dc</sub> (6)	Period Jitter for dedicated clock output (F <sub>OUT</sub> < 100 MHz)	_	—	17.5	mUI (p-p)

Symbol	Parameter	Min	Тур	Max	Unit
t <sub>outccj_dc</sub> (6)	Cycle to Cycle Jitter for dedicated clock output ( $F_{OUT} \geq 100 \text{ MHz}$ )		_	175	ps (p-p)
LOUTCCJ_DC	Cycle to Cycle Jitter for dedicated clock output $(F_{OUT} < 100 \text{ MHz})$	_	_	17.5	mUI (p-p)
t <sub>outpj_io</sub> (6),	Period Jitter for clock output on regular I/O $(F_{OUT} \ge 100 \text{ MHz})$	_	_	600	ps (p-p)
(9)	Period Jitter for clock output on regular I/O (F <sub>OUT</sub> < 100 MHz)	_	_	60	mUI (p-p)
t <sub>outccj_lo</sub> <sup>(6)</sup> ,	Cycle to Cycle Jitter for clock output on regular I/O $(F_{0UT} \geq 100 \text{ MHz})$	_	_	600	ps (p-p)
(9)	Cycle to Cycle Jitter for clock output on regular I/O (F <sub>OUT</sub> < 100 MHz)	_	_	60	mUI (p-p)
t <sub>casc_outpj_dc</sub>	Period Jitter for dedicated clock output in cascaded PLLs ( $F_{OUT} \ge 100MHz$ )	_	_	250	ps (p-p)
(6), (7)	Period Jitter for dedicated clock output in cascaded PLLs $(F_{OUT} < 100MHz)$		_	25	mUI (p-p)
f <sub>DRIFT</sub>	Frequency drift after PFDENA is disabled for duration of 100 us	_		±10	%

#### Table 1–34. PLL Specifications for Stratix IV Devices (Part 2 of 2)

#### Notes to Table 1-34:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) The VCO frequency reported by the Quartus II software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f<sub>VCO</sub> specification.

(3) This specification is limited by the lower of the two: I/O  $F_{MAX}$  or  $F_{OUT}$  of the PLL.

- (4) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 120 ps.
- (5)  $F_{REF}$  is fIN/N when N = 1.

(6) Peak-to-peak jitter with a probability level of  $10^{-12}$  (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 1–51 on page 1–62.

- (7) The cascaded PLL specification is only applicable with the following condition: A. Upstream PLL: 0.59Mhz  $\leq$  Upstream PLL BW < 1 MHz B. Downstream PLL: Downstream PLL BW > 2 MHz
- (8) High bandwidth PLL settings are not supported in external feedback mode.
- (9) External memory interface clock output jitter specifications use a different measurement method, which is available in Table 1–49 on page 1–61.

## **DSP Block Specifications**

Table 1–35 lists the Stratix IV DSP block performance specifications.

Table 1-35	Block Performance S	Specifications for Stratix IV DSP De	vices <sup>(1)</sup>
------------	---------------------	--------------------------------------	----------------------

	Resources Used		Pe	rformance			
Mode	Number of Multipliers	–1 Industrial and–2/–2× Commercial/ Industrial Speed Grade	–3 Commercial Speed Grade	–3 Industrial Speed Grade	–4 Commercial Speed Grade	–4 Industrial Speed Grade	Unit
9×9-bit multiplier (A, C, E, G) <sup>(2)</sup>	1	520	460	460	400	400	MHz
9×9-bit multiplier (B, D, F, H) <sup>(2)</sup>	1	520	460	460	400	400	MHz
12×12-bit multiplier (A, E) <sup>(3)</sup>	1	540	500	500	440	440	MHz
12×12-bit multiplier (B, D, F, H) <sup>(3)</sup>	1	540	500	500	440	430	MHz
18×18-bit multiplier	1	600	550	550	480	480	MHz
36×36-bit multiplier	1	480	440	440	380	380	MHz
18×18-bit multiply accumulator	4	490	440	440	380	380	MHz
18×18-bit multiply adder	4	510	470	470	410	400	MHz
18×18-bit multiply adder-signed full precision	2	490	450	440	390	390	MHz
18×18-bit multiply adder with loopback <sup>(4)</sup>	2	390	350	350	310	300	MHz
36-bit shift (32-bit data)	1	490	440	440	380	380	MHz
Double mode	1	480	440	440	380	370	MHz

#### Notes to Table 1-35:

(1) Maximum is for fully pipelined block with Round and Saturation disabled.

(2) The DSP block implements eight independent 9b '9b multiplies using A, B, C, D for the top DSP half block and E, F, G, H for the bottom DSP half block multipliers.

(3) The DSP block implements six independent 12b'12b multiplies using A, B, D for the top DSP half block and E, F, H for the bottom DSP half block multipliers.

(4) Maximum for loopback input registers disabled, Round and Saturation disabled, and pipeline and output registers enabled.

## **TriMatrix Memory Block Specifications**

Table 1–36 lists the Stratix IV TriMatrix memory block specifications.

		Resou	rces Used	Performance								
Memory	Mode	ALUTS	TriMatrix Memory	–1 Industrial and –2 /–2× Commercial/ Industrial Speed Grade	–3 Commercial/ Industrial/ Military Speed Grade	–4 Commercial/ Industrial Speed Grade	–3 Industrial/ Military Speed Grade (2)	–4 Industrial Speed Grade (2)	Unit			
	Single port 64×10	0	1	600	500	450	500	450	MHz			
MLAB	Simple dual-port 32×20	0	1	600	500	450	500	450	MHz			
(3)	Simple dual-port 64×10	0	1	600	500	450	500	450	MHz			
	ROM 64×10	0	1	600	500	450	500	450	MHz			
	ROM 32×20	0	1	600	500	450	500	450	MHz			
	Single-port 256×36	0	1	600	540	475	540	475	MHz			
	Simple dual-port 256×36	0	1	550	490	420	490	420	MHz			
	Simple dual-port 256×36, with the read-during-write option set to <b>Old</b> <b>Data</b>	0	1	375	340	300	340	300	MHz			
M9K	True dual port 512×18	0	1	490	430	370	430	370	MHz			
Block (3)	True dual-port 512×18, with the read-during-write option set to <b>Old</b> <b>Data</b>	0	1	375	335	290	335	290	MHz			
	ROM 1 Port	0	1	600	540	475	540	475	MHz			
	ROM 2 Port	0	1	600	540	475	540	475	MHz			
	Min Pulse Width (clock high time)	_	_	750	800	850	800	850	ps			
	Min Pulse Width (clock low time)		_	500	625	690	625	690	ps			

		Resou	rces Used	Performance								
Memory	Mode	ALUTs TriMatrix Memory		–1 Industrial and –2 /–2× Commercial/ Industrial Speed Grade	and –2 /–2× Commercial/ Industrial Military		–3 Industrial/ Military Speed Grade (2)	–4 Industrial Speed Grade (2)	Unit			
	Single-port 4K×36	0	1	475	440	380	400	350	MHz			
	Simple dual-port 2K×72	0	1	465	435	385 375		325	MHz			
	Simple dual-port 2K×72, with the read-during-write option set to <b>Old</b> <b>Data</b>	0	1	260	240	205	225	200	MHz			
M144K	Simple dual-port 2K×64 (with ECC)	0	1	335	300	255	295	250	MHz			
Block (3)	True dual-port 4K×36	0	1	400	375	330	350	310	MHz			
	True dual-port 4K×36, with the read-during-write option set to <b>Old</b> <b>Data</b>	0	1	245	230	205	225	200	MHz			
	ROM 1 Port	0	1	540	500	435	450	420	MHz			
	ROM 2 Port	0	1	500	465	400	425	400	MHz			
	Min Pulse Width (clock high time)	_	_	700	755	860	860	950	ps			
	Min Pulse Width (clock low time)			500	625	690	690	690	ps			

Table 1-36.	TriMatrix Memory Block Performance Specifications for Stratix IV Devices <sup>(1)</sup>	(Part 2 of 2)
-------------	---	---------------

Notes to Table 1-36:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to 50% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) This is only applicable to the Stratix IV E and GX devices.

(3) When you use the error detection CRC feature, there is no degradation in  $F_{\text{MAX}}$ 

## **Configuration and JTAG Specifications**

Table 1–37 lists the Stratix IV configuration mode specifications.

Table 1–37. Configuration Mode Specifications for Stratix IV Devices

Drogromming Mode		Unit		
Programming Mode	Min	Тур	Max	Unit
Passive serial	—	—	125	MHz
Fast passive parallel (1)	—	—	125	MHz
Fast active serial	17	26	40	MHz

Programming Mode		- Unit		
	Min	Тур	Max	UIII
Remote update only in fast AS mode	4.3	5.3	10	MHz

Note to Table 1-37:

(1) This denotes the maximum frequency supported in the FPP configuration scheme. The frequency supported for each device may vary depending on device density. For more information, refer to the *Configuration, Design* Security, and Remote System Upgrades in Stratix IV Devices chapter.

Table 1–38 lists the JTAG timing parameters and values for Stratix IV devices.

 Table 1–38.
 JTAG Timing Parameters and Values for Stratix IV Devices

Symbol	Description	Min	Max	Unit
t <sub>JCP</sub>	TCK clock period	30	—	ns
t <sub>JCH</sub>	TCK clock high time	14	—	ns
t <sub>JCL</sub>	TCK clock low time	14	—	ns
t <sub>JPSU (TDI)</sub>	TDI JTAG port setup time	1	—	ns
t <sub>JPSU (TMS)</sub>	TMS JTAG port setup time	3	—	ns
t <sub>JPH</sub>	JTAG port hold time	5	—	ns
t <sub>JPCO</sub>	JTAG port clock to output	—	11 <sup>(1)</sup>	ns
t <sub>JPZX</sub>	JTAG port high impedance to valid output	—	14 <sup>(1)</sup>	ns
t <sub>JPXZ</sub>	JTAG port valid output to high impedance	—	<b>14</b> <sup>(1)</sup>	ns

Note to Table 1-38:

(1) A 1 ns adder is required for each  $V_{CCI0}$  voltage step down from 3.0 V. For example,  $t_{JPC0} = 12$  ns if  $V_{CCI0}$  of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

### **Temperature Sensing Diode Specifications**

Table 1–39 lists the specifications for the Stratix IV temperature sensing diode.

Table 1–39. External Temperature Sensing Diode Specifications for Stratix IV Devices

Description	Min	Тур	Max	Unit
I <sub>bias</sub> , diode source current	8	—	500	μΑ
V <sub>bias,</sub> voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 5	Ω
Diode ideality factor	1.026	1.028	1.030	—

Table 1–40 lists the specifications for the Stratix IV internal temperature sensing diode.

Table 1–40. Internal Temperature Sensing Diode Specifications for Stratix IV Devices

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with No Missing Codes	
–40 to 100 °C	±8 °C	No	Frequency: 500 kHz, 1 MHz	< 100 ms	8 bits	8 bits	

## Chip-Wide Reset (Dev\_CLRn) Specifications

Table 1–41 lists the specifications for the Stratix IV chip-wide reset (Dev\_CLRn). This specifications denote the minimum pulse width of the Dev\_CLRn signal required to clear all the device registers.

Table 1-41. Chip-Wide Reset (DEV\_CLRn) Specifications

Description	Min	Тур	Max	Unit
Dev_CLRn	500			μS

## **Periphery Performance**

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the LVDS high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-LVTTL/LVCMOS are capable of typical 167 MHz and 1.2 LVCMOS at 100 MHz interfacing frequency with 10 pF load.

For the Stratix IV GT -1 and -2 speed grade specifications, refer to the  $-2/-2 \times$  speed grade column. For the Stratix IV GT -3 speed grade specification, refer to the -3 speed grade column, unless otherwise specified.

Actual achievable frequency depends on design- and system-specific factors. You must perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

## **High-Speed I/O Specification**

Table 1–42 lists the high-speed I/O timing for Stratix IV devices.

-2/-2× Speed Grade -3 Speed Grade -4 Speed Grade Symbol Conditions Unit Min Typ Max Min Typ Max Min Typ Max f<sub>HSCLK\_in</sub> (input clock frequency) Clock boost factor W = 1 to 40 5 800 5 5 717 MHz 717 True Differential I/O (3) Standards f<sub>HSCLK in</sub> (input clock frequency) Clock boost factor W = 1 to 40 5 800 5 5 717 MHz 717 Single Ended I/O (3) Standards (10) f<sub>HSCLK\_in</sub> (input clock frequency) Clock boost factor W = 1 to 40 5 520 5 420 5 420 MHz Single Ended I/O (3) Standards (11)  $f_{HSCLK\_OUT}$  (output 800 717 717 5 5 5 MHz clock frequency) (8) (8) (8)

Table 1-42. High-Speed I/O Specifications <sup>(1)</sup>, <sup>(2)</sup> (Part 1 of 3)

	• •	–2/–2× Speed Grade			–3 Speed Grade			–4 Speed Grade			
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Transmitter											
	SERDES factor J = 3 to 10 <sup>(9)</sup>	(4)		1600	(4)		1250	(4)		1250	Mbps
True Differential I/O Standards - f <sub>HSDR</sub>	SERDES factor J = 2, Uses DDR Registers	(4)	_	(5)	(4)	_	(5)	(4)	_	(5)	Mbps
(data rate)	SERDES factor J = 1, Uses an SDR Register	(4)	_	(5)	(4)		(5)	(4)	_	(5)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f <sub>HSDR</sub> (data rate) <sup>(6)</sup>	SERDES factor J = 4 to 10			1250	(4)		1152	(4)		800	Mbps
Emulated Differential I/O Standards with One External Output Resistor - f <sub>HSDR</sub> (data rate)			_	311	(4)	_	200	(4)	_	200	Mbps
t <sub>x Jitter</sub> - True Differential I/O	Total Jitter for Data Rate, 600 Mbps to 1.6 Gbps		_	160	_		160	_	_	160	ps
Standards	Total Jitter for Data Rate, < 600 Mbps	_	_	0.1	_	_	0.1	_	_	0.1	UI
t <sub>x Jitter</sub> - Emulated Differential I/O	Total Jitter for Data Rate, 600 Mbps to 1.25 Gbps	_	_	300	_	_	300	_	_	325	ps
Standards with Three External Output Resistor Network	Total Jitter for Data Rate < 600 Mbps	_	_	0.2	_	_	0.2	_	_	0.25	UI
t <sub>x Jitter</sub> - Emulated Differential I/O Standards with One External Output Resistor Network	—	_	_	0.125	_	_	0.15	_	_	0.15	UI
t <sub>duty</sub>	Tx output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
	True Differential I/O Standards			160			200			200	ps
t <sub>RISE &amp;</sub> t <sub>FALL</sub>	Emulated Differential I/O Standards with Three External Output Resistor Networks		_	250			250		_	300	ps
	Emulated Differential I/O Standards with One External Output Resistor		_	460	_	_	500	_	_	500	ps

#### Table 1–42. High-Speed I/O Specifications <sup>(1)</sup>, <sup>(2)</sup> (Part 2 of 3)

Cumhal	Conditions	-2/-2	× Spee	d Grade	-3	Speed (	Grade	-4	Speed (	Grade	11
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
	True Differential I/O Standards	—	—	100		_	100	_	_	100	ps
TCCS	Emulated Differential I/o Standards	_	_	250	_		250			250	ps
Receiver											
True Differential I/O Standards - f <sub>HSDRDPA</sub> (data rate)	SERDES factor J = 3 to 10	150	_	1600	150	_	1250	150	_	1250	Mbps
	SERDES factor J = 3 to 10	(4)	—	(7)	(4)		(7)	(4)		(7)	Mbps
f <sub>HSDR</sub> (data rate)	SERDES factor J = 2, Uses DDR Registers	(4)	_	(5)	(4)	_	(5)	(4)	_	(5)	Mbps
	SERDES factor J = 1, Uses an SDR Register	(4)	_	(5)	(4)		(5)	(4)		(5)	Mbps
DPA Mode										•	
DPA run length	_			10000			10000			10000	UI
Soft CDR mode											
Soft-CDR PPM tolerance	_	_	_	300	_	_	300	_	_	300	± PPM
Non DPA Mode											
Sampling Window	_			300			300			300	ps

#### Table 1-42. High-Speed I/O Specifications <sup>(1)</sup>, <sup>(2)</sup> (Part 3 of 3)

Notes to Table 1-42:

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) Clock Boost Factor (W) is the ratio between input data rate to the input clock rate.

(4) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(5) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (f<sub>OUT</sub>) provided you can close the design timing and the signal integrity simulation is clean.

(6) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(7) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and the receiver sampling margin to determine the maximum data rate supported.

(8) This is achieved by using the LVDS and DPA clock network.

(9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(10) This only applies to DPA and soft-CDR modes.

(11) This only applies to LVDS source synchronous mode.

Table 1–43 lists the DPA lock time specifications for Stratix IV ES devices.

Standard	Training Pattern	Number of Data Transitions in one repetition of training pattern	Number of repetitions per 256 data transitions (4)	Condition	Maximum
SPI-4	0000000000111111111	2	128	without DPA PLL calibration	256 data transitions
511-4	000000000000000000000000000000000000000		120	with DPA PLL calibration	3x256 data transitions + 2x96 slow clock cycles <sup>(5)</sup>
	00001111	2	128	without DPA PLL calibration	256 data transitions
Parallel Rapid	00001111	2	120	with DPA PLL calibration	3x256 data transitions + 2x96 slow clock cycles (5)
I/O	10010000	4	64	without DPA PLL calibration	256 data transitions
		4		with DPA PLL calibration	3x256 data transitions + 2x96 slow clock cycles (5)
	10101010	0	20	without DPA PLL calibration	256 data transitions
Mianallanaaua	10101010	8	32	with DPA PLL calibration	3x256 data transitions + 2x96 slow clock cycles (5)
Miscellaneous	01010101	0	20	without DPA PLL calibration	256 data transitions
	01010101	8	32	with DPA PLL calibration	3x256 data transitions + 2x96 slow clock cycles <sup>(5)</sup>

Table 1–43. DP/	A Lock Time Specifications-	-Stratix IV ES Devices Only	(1), (2),	(3)
-----------------	-----------------------------	-----------------------------	-----------	-----

Notes to Table 1-43:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time applies to commercial, industrial, and military speed grades.

(4) This is the number of repetition for the stated training pattern to achieve 256 data transitions.

(5) Slow clock = Data rate (Mbps)/Deserialization factor.

Figure 1–4 shows the DPA lock time specifications with DPA PLL calibration enabled.

#### Figure 1–4. DPA Lock Time Specification with DPA PLL Calibration Enabled



Table 1-44 lists the DPA lock time specifications for Stratix IV GX and GT devices.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (4)	Maximum	
SPI-4	0000000001111111111	2	128	640 data transitions	
Parallel Rapid	00001111	2	128	640 data transitions	
I/O	10010000	4	64	640 data transitions	
Miscellaneous	10101010	8	32	640 data transitions	
MISCENATEOUS	01010101	8	32	640 data transitions	

Table 1-44. DPA Lock Time Specifications—Stratix IV GX and GT Devices Only (1), (2), (3)

Notes to Table 1-44:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in the table applies to commercial, industrial, and military speed grades.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 1–5 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate equal to or higher than 1.25 Gbps. Table 1–45 lists this information in table form.

# Figure 1–5. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to or Higher Than 1.25 Gbps



Table 1–45 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate equal to or higher than 1.25 Gbps.

Table 1–45. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to or Higher than 1.25 Gbps

Jitter Free	Sinusoidal Jitter (UI)			
F1	10,000 25.000			
F2	17,565	25.000		
F3	1,493,000	0.350		
F4	50,000,000	0.350		

Figure 1–6 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate less than 1.25 Gbps.





When the data rate is equals to 800 Mbps, the LVDS soft-CDR/DPA sinusoidal jitter tolerance allows up to 0.1 UI (125 ps) for jitter frequencies between 479.9 kHz and 20 MHz.

#### **DLL and DQS Logic Block Specifications**

Table 1–46 lists the DLL frequency range specifications for Stratix IV devices.

Table 1–46. DLL Frequency Range Specifications for Stratix IV Devices (Part 1 of 2)

Fromuonov	Freq	uency Range (M	Hz)		DOC Deloy Buffer	Number of
Frequency Mode	–2/–2× Speed Grade	–3 Speed Grade	–4 Speed Grade	Available Phase Shift	DQS Delay Buffer Mode <sup>(1)</sup>	Delay Chains
0	90-140	90-130	90-120	22.5°, 45°, 67.5°, 90°	Low	16
1	120-180	120-170	120-160	30°, 60°, 90°, 120°	Low	12
2	150-220	150-210	150-200	36°, 72°, 108°, 144°	Low	10
3	180-280	180-260	180-240	45°, 90°,135°, 180°	Low	8

Eroguopoy	Freq	uency Range (M			DQS Delay Buffer	Number of
Frequency Mode	–2/–2× Speed Grade	–3 Speed Grade	–4 Speed Grade	Available Phase Shift	Mode <sup>(1)</sup>	Delay Chains
4	240-350	240-320	240-290	30°, 60°, 90°, 120°	High	12
5	290-430	290-380	290-360	36°, 72°, 108°, 144°	High	10
6	360-540	360-450	360-450	45°, 90°, 135°, 180°	High	8
7	470-700	470-630	470-590	60°, 120°, 180°, 240°	High	6

#### Table 1–46. DLL Frequency Range Specifications for Stratix IV Devices (Part 2 of 2)

#### Note to Table 1-46:

(1) Low indicates a 6-bit DQS delay setting; high indicates a 5-bit DQS delay setting.

Table 1-47 lists the DQS phase offset delay per stage for Stratix IV devices.

Table 1–47. DQS Phase Offset Delay Per Setting for Stratix IV Devices (1), (2), (3)

Speed Grade	Min	Max	Unit
-2/-2×	7	13	ps
-3	7	15	ps
-4	7	16	ps

#### Notes to Table 1-47:

- (1) The valid settings for phase offset are -64 to +63 for frequency modes 0 to 3 and -32 to +31 for frequency modes 4 to 6.
- (2) The typical value equals the average of the minimum and maximum values.
- (3) The delay settings are linear, with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -2 speed grade and applying a 10 phase offset settings to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10.5 ps) ± 20 ps] = 730 ps ± 20 ps.

Table 1–48 lists the DQS phase shift error for Stratix IV devices.

Table 1–48.	DQS Phase Shift Error Specification for DLL-Delayed Clock (t <sub>DOS PSERR</sub> ) for Stratix IV
Devices <sup>(1)</sup>	

Number of DQS Delay Buffer	–2/–2X Speed Grade	–3 Speed Grade	–4 Speed Grade	Unit
1	26	28	30	ps
2	52	56	60	ps
3	78	84	90	ps
4	104	112	120	ps

Note to Table 1-48:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -2/-2x speed grade is ± 78 ps or ± 39 ps.

Table 1–49 lists the memory output clock jitter specifications for Stratix IV devices.

Parameter	Clock Network	Symbol		–2X Grade	_ Speed	3 Grade	_ Speed	4 Grade	Unit
NGLWUIK	-	Min	Max	Min	Max	Min	Max		
Clock period jitter	Regional	$t_{JIT(per)}$	-50	50	-55	55	-55	55	ps
Cycle-to-cycle period jitter	Regional	$t_{\text{JIT}(\text{cc})}$	-100	100	-110	110	-110	110	ps
Duty cycle jitter	Regional	t <sub>JIT(duty)</sub>	-50	50	-82.5	82.5	-82.5	82.5	ps
Clock period jitter	Global	t <sub>JIT(per)</sub>	-75	75	-82.5	82.5	-82.5	82.5	ps
Cycle-to-cycle period jitter	Global	$t_{\text{JIT(cc)}}$	-150	150	-165	165	-165	165	ps
Duty cycle jitter	Global	t <sub>JIT(duty)</sub>	-75	75	-90	90	-90	90	ps

Table 1–49. Memory Output Clock Jitter Specification for Stratix IV Devices (1), (2), (3)

Notes to Table 1-49:

(1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

(2) The clock jitter specification applies to memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a regional or global clock network as specified. Altera recommends using regional clock networks whenever possible.

(3) The memory output clock jitter stated in Table 1–49 is applicable when an input jitter of 30 ps is applied.

## **OCT Calibration Block Specifications**

Table 1–50 lists the OCT calibration block specifications for Stratix IV devices.

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	_	20	MHz
T <sub>OCTCAL</sub>	Number of OCTUSRCLK clock cycles required for OCT $\rm R_S/R_T$ calibration	_	1000	_	Cycles
T <sub>OCTSHIFT</sub>	Number of OCTUSRCLK clock cycles required for OCT code to shift out	_	28	_	Cycles
T <sub>RS_RT</sub>	Time required between the <code>dyn_term_ctrl</code> and <code>oe</code> signal transitions in a bidirectional I/O buffer to dynamically switch between OCT $\rm R_S$ and $\rm R_T$	_	2.5	_	ns

Figure 1–7 shows the timing diagram for the oe and dyn\_term\_ctrl signals.

Figure 1–7. Timing Diagram for the oe and dyn\_term\_ctrl Signals



### **Duty Cycle Distortion (DCD) Specifications**

Table 1-51 lists the worst-case DCD for Stratix IV devices.

Table 1–51. Worst-Case DCD on Stratix IV I/O Pins (1)

Symbol		/–2× d Grade		-3 I Grade		-4 I Grade	Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

Note to Table 1-51:

(1) The listed specification is only applicable to the output buffer across different I/O standards.

## I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O Timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

The Excel-based I/O Timing spreadsheet is downloadable from the Literature: Stratix IV Devices webpage.

## **Programmable IOE Delay**

Table 1–52 lists the Stratix IV IOE programmable delay settings.

Table 1–52. IOE Programmable Delay for Stratix IV Devices

Doromotor Availab	Available	Min Offset	Fast Model		Slow Model						
Parameter (1)	Settings		(2)	Industrial/ Military	Commercial	C2 <sup>(3)</sup>	C3	C4	I3/M3	14	Unit
D1	16	0	0.462	0.505	0.732	0.795	0.857	0.801	0.864	ns	
D2	8	0	0.234	0.232	0.337	0.372	0.407	0.371	0.405	ns	
D3	8	0	1.700	1.769	2.695	2.927	3.157	2.948	3.178	ns	
D4	16	0	0.508	0.554	0.813	0.882	0.952	0.889	0.959	ns	
D5	16	0	0.472	0.500	0.747	0.799	0.875	0.817	0.882	ns	
D6	8	0	0.186	0.195	0.294	0.319	0.345	0.321	0.347	ns	

#### Notes to Table 1-52:

(1) You can set this value in the Quartus II software by selecting D1, D2, D3, D4, D5, and D6 in the Assignment Name column.

(2) Minimum offset does not include the intrinsic delay.

(3) For the EP4SGX530 device density, the IOE programmable delays have an additional 5% maximum offset.

## **Programmable Output Buffer Delay**

Table 1–53 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

#### Table 1–53. Programmable Output Buffer Delay (1)

Symbol	Parameter	Typical	Unit
		0 (default)	ps
D	Rising and/or falling edge	50 ps	ps
D <sub>OUTBUF</sub>	delay	100	ps
		150	ps

Note to Table 1–53:

(1) You can set the programmable output buffer delay in the Quartus II software by setting the Output Buffer Delay Control assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the Output Buffer Delay assignment.

# Glossary

Table 1–54 lists the glossary for this chapter.

Table 1-54. Glossary Table (Part 1 of 4)

Letter	Subject	Definitions
A, B, C	—	—
D	Differential I/O Standards	Receiver Input Waveforms         Single-Ended Waveform       Positive Channel (p) = V <sub>IH</sub> Negative Channel (n) = V <sub>IL</sub> Ground         Differential Waveform $p - n = 0$ V         Transmitter Output Waveforms       Single-Ended Waveform         Von       Positive Channel (p) = V <sub>OH</sub> Von       Receiver Channel (p) = V <sub>OH</sub> Von       Positive Channel (p) = V <sub>OH</sub> Von       Ground         Differential Waveform       Positive Channel (p) = V <sub>OL</sub> Von       Pon = 0 V
E		_
	f <sub>HSCLK</sub>	Left/right PLL input clock frequency.
F	f <sub>HSDR</sub>	High-speed I/O block: Maximum/minimum LVDS data transfer rate $(f_{HSDR} = 1/TUI)$ , non-DPA.
	f <sub>hsdrdpa</sub>	High-speed I/O block: Maximum/minimum LVDS data transfer rate $(f_{HSDRDPA} = 1/TUI)$ , DPA.
G, H, I		—

### Table 1–54. Glossary Table (Part 2 of 4)

Letter	Subject	Definitions
	J	High-speed I/O block: Deserialization factor (width of parallel data bus).
J	JTAG Timing Specifications	JTAG Timing Specifications: TMS TDI $t_{JCP}$ $t_{JCH}$ $t_{JPSU}$ $t_{JPSU}$ $t_{JPSU}$ $t_{JPSU}$ $t_{JPXZ}$ TDO $t_{JPXZ}$
K, L, M, N, O		_
Ρ	PLL Specifications	Diagram of PLL Specifications (1)
Q		_
R	RL	Receiver differential input discrete resistor (external to Stratix IV device).

Letter	Subject	Definitions					
	SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:         Bit Time         0.5 x TCCS       RSKM         Sampling Window       RSKM         (SW)       RSKM					
S	Single-ended voltage referenced I/O standard	The JEDEC standard for SSTI and HSTL I/O defines both the AC and DC input signal values.         The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.         The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing, as shown:         Single-Ended Voltage Referenced I/O Standard         VoH       Viel(AC)         Viel(AC)         Viel(AC)         VoH       Viel(AC)         Viel(AC)         Voltage       Viel(AC)         Viel(AC)       Viel(AC)					
	t <sub>C</sub>	High-speed receiver/transmitter input and output clock period.					
	TCCS (channel- to-channel-skew)	The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under <b>SW</b> in this table).					
		High-speed I/O block: Duty cycle on high-speed transmitter output clock.					
т	t <sub>DUTY</sub>	<b>Timing Unit Interval (TUI)</b> The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = $1/(\text{Receiver Input Clock Frequency Multiplication Factor}) = t_c/w)$					
	t <sub>FALL</sub>	Signal high-to-low transition time (80-20%)					
	t <sub>INCCJ</sub>	Cycle-to-cycle jitter tolerance on the PLL clock input					
	t <sub>OUTPJ_IO</sub>	Period jitter on the general purpose I/O driven by a PLL					
	t <sub>OUTPJ_DC</sub>	Period jitter on the dedicated clock output driven by a PLL					
	t <sub>RISE</sub>	Signal low-to-high transition time (20-80%)					
	1	+					

#### Table 1–54. Glossary Table (Part 3 of 4)

Letter	Subject	Definitions
	V <sub>CM(DC)</sub>	DC Common mode input voltage.
	V <sub>ICM</sub>	Input Common mode voltage—The common mode of the differential signal at the receiver.
	V <sub>ID</sub>	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V <sub>DIF(AC)</sub>	AC differential input voltage—Minimum AC input differential voltage required for switching.
	V <sub>DIF(DC)</sub>	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V <sub>IH</sub>	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	V <sub>IH(AC)</sub>	High-level AC input voltage
	V <sub>IH(DC)</sub>	High-level DC input voltage
V	V <sub>IL</sub>	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	V <sub>IL(AC)</sub>	Low-level AC input voltage
	V <sub>IL(DC)</sub>	Low-level DC input voltage
	V <sub>OCM</sub>	Output Common mode voltage—The common mode of the differential signal at the transmitter.
	V <sub>OD</sub>	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V <sub>SWING</sub>	Differential input voltage
	V <sub>X</sub>	Input differential cross point voltage
	V <sub>OX</sub>	Output differential cross point voltage
W	W	High-speed I/O block: Clock Boost Factor
X, Y, Z		_

#### Table 1–54. Glossary Table (Part 4 of 4)

## **Document Revision History**

Table 1–55 lists the revision history for this chapter.

Table 1–55. Document Revision History (Part 1 of 3)

Date	Version	Changes
		<ul> <li>Added Table 1–5 and Table 1–40.</li> </ul>
July 2012	5.3	<ul> <li>Updated Table 1–15, Table 1–22, Table 1–23, Table 1–30, Table 1–33, Table 1–35, Table 1–36, Table 1–39, Table 1–42 and Table 1–51.</li> </ul>
		<ul> <li>Removed "Schmitt Trigger Input" section.</li> </ul>
December 2011	5.2	Added Figure 1–7.
	0.2	<ul> <li>Updated Table 1–22 and Table 1–41.</li> </ul>
		<ul> <li>Added military speed grade information.</li> </ul>
		<ul> <li>Updated Table 1–1 and Table 1–30.</li> </ul>
June 2011	5.1	<ul> <li>Updated (Note 3) in Table 1–42 and (Note 3) in Table 1–43.</li> </ul>
		<ul> <li>Added military speed grade to Table 1–5, Table 1–10, Table 1–11, Table 1–23, Table 1–30, Table 1–36, and Table 1–51.</li> </ul>

Date	Version	Changes
April 2011	5.0	<ul> <li>Updated Table 1–1, Table 1–5, Table 1–6, Table 1–13, Table 1–16, Table 1–23, and Table 1–24.</li> </ul>
March 2011	4.9	■ Updated Table 1–24.
March 2011	4.8	Removed (Note 17) in Table 1-24.
February 2011	4.7	Added (Note 17) to Table 1–24.
		<ul> <li>Updated Table 1–1, Table 1–5, Table 1–23, Table 1–24, Table 1–30, Table 1–31, Table 1–32, Table 1–34, Table 1–37, Table 1–41, and Table 1–51.</li> </ul>
February 2011	4.6	<ul> <li>Updated the "Recommended Operating Conditions" section.</li> </ul>
-		<ul> <li>Added the "Schmitt Trigger Input" section.July</li> </ul>
		<ul> <li>Minor text edits.</li> </ul>
		■ Updated Table 1–29.
November 2010	4.5	<ul> <li>Updated chapter title.</li> </ul>
		<ul> <li>Minor text edits.</li> </ul>
Cantanahan 0010		Applied new template.
September 2010	4.4	Updated Table 1–1 and Table 1–5.
		<ul> <li>Updated Table 1–7, Table 1–22, Table 1–23, Table 1–33, Table 1–35, Table 1–36, and Table 1–40.</li> </ul>
July 2010	4.3	Added Table 1–39.
		<ul> <li>Changed "PCI Express" to "PCIe" throughout.</li> </ul>
		<ul> <li>Minor text edits</li> </ul>
		■ Updated Table 1–22, Table 1–23, Table 1–30, Table 1–46, and Table 1–49.
March 2010	4.2	Added Table 1–31.
		<ul> <li>Minor text edits.</li> </ul>
		<ul> <li>Updated Table 1–11, Table 1–22, Table 1–23, Table 1–24, Table 1–25, Table 1–26, Table 1–27, Table 1–29, Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–39, Table 1–40, Table 1–43, Table 1–46, and Table 1–49.</li> </ul>
February 2010	4.1	<ul> <li>Added Stratix IV GT speed grade note to Table 1–32, Table 1–35, Table 1–39, Table 1–43, Table 1–44, Table 1–45, and Table 1–46.</li> </ul>
		<ul> <li>Added Table 1–28 and Table 1–30.</li> </ul>
		<ul> <li>Minor text edits.</li> </ul>
		<ul> <li>Added Table 1–9, Table 1–15, Table 1–38, and Table 1–39.</li> </ul>
		<ul> <li>Added Figure 1–5 and Figure 1–6.</li> </ul>
		<ul> <li>Added the "Transceiver Datapath PCS Latency" section.</li> </ul>
		<ul> <li>Updated the "Electrical Characteristics", "Operating Conditions", and "I/O Timing" sections.</li> </ul>
November 2009	4.0	<ul> <li>All tables updated except Table 1–16, Table 1–24, Table 1–25, Table 1–26, Table 1–27, Table 1–33, Table 1–34, and Table 1–45.</li> </ul>
		<ul> <li>Updated Figure 1–2 and Figure 1–3.</li> </ul>
		<ul> <li>Updated Equation 1–1.</li> </ul>
		Deleted Table 1-28, Table 1-29, Table 1-30, Table 1-42, Table 1-43, and Table 1-44.
		<ul> <li>Minor text edits.</li> </ul>

Table 1–55. Document Revision History (Part 2 of 3)

Table 1-55.	Document Revision His	story (Part 3 of 3)
-------------	-----------------------	---------------------

Date	Version	Changes		
		<ul> <li>Added "Preliminary Specifications" to the footer of each page.</li> </ul>		
June 2009	3.1	<ul> <li>Updated Table 1–1, Table 1–2, Table 1–7, Table 1–10, Table 1–11, Table 1–12, Table 1–21, Table 1–22, Table 1–23, Table 1–25, Table 1–37, Table 1–38, Table 1–39, Table 1–40, and Table 1–44.</li> </ul>		
		<ul> <li>Minor text edits.</li> </ul>		
		<ul> <li>Replaced Table 1–31 and Table 1–37.</li> </ul>		
		<ul> <li>Updated Table 1–1, Table 1–2, Table 1–5, Table 1–19, Table 1–41, Table 1–44, Table 1–45, Table 1–49, and Table 1–51.</li> </ul>		
March 2009	3.0	<ul> <li>Added Table 1–21, Table 1–46, and Table 1–47</li> </ul>		
		Added Figure 1–3.		
		<ul> <li>Removed "Timing Model", "Preliminary and Final Timing", "I/O Timing Measurement Methodology", "I/O Default Capacitive Loading", and "Referenced Documents" sections.</li> </ul>		
December 2008	2.1	Minor changes.		
		<ul> <li>Minor text edits.</li> </ul>		
November 2008	2.0	<ul> <li>Updated Table 1–19, Table 1–32, Table 1–34 - Table 1–39.</li> </ul>		
		<ul> <li>Minor text edits.</li> </ul>		
		<ul> <li>Updated Table 1–1, Table 1–2, Table 1–4, Table 1–5, and Table 1–26.</li> </ul>		
August 2008	1.1	<ul> <li>Removed figures from "Transceiver Performance Specifications" on page 1–10 that are repeated in the glossary.</li> </ul>		
		<ul> <li>Minor text edits and an additional note to Table 1–26.</li> </ul>		
May 2008	1.0	Initial release.		



## 2. Addendum to the Stratix IV Device Handbook

SIV54002-1.5

This chapter describes changes to the published version of the *Stratix IV Device Handbook*. All changes from Revision 1.4 of this chapter are now incorporated in the main handbook chapters or in *AN 612: Decision Feedback Equalization in Stratix IV Devices*.

## **Adaptive Equalization (AEQ)**

This AEQ information is now located in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

## **Decision Feedback Equalization (DFE)**

For more information about the DFE feature, refer to *AN 612: Decision Feedback Equalization in Stratix IV Devices*.

## **Power-On Reset Circuitry**

The Power-On Reset Circuitry information is now located in the *Hot Socketing and Power-On Reset in Stratix IV Devices* chapter.

## **Power-On Reset Specifications**



• The Power-On Reset Specification information is now located in the *Hot Socketing and Power-On Reset in Stratix IV Devices* chapter.

© 2012 Altera Corporation. All rights reserved. ALTERA, ARRIA, CYCLONE, HARDCOPY, MAX, MEGACORE, NIOS, QUARTUS and STRATIX words and logos are trademarks of Altera Corporation and registered in the U.S. Patent and Trademark Office and in other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders as described at www.altera.com/common/legal.html. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.





<sup>•••</sup> 

# **Document Revision History**

Table 2–5 lists the revision history for this chapter.	Table 2–5 lists	the revision	history	for this chapter.
--	-----------------	--------------	---------	-------------------

Table 2–1.	Document Re	evision History
------------	-------------	-----------------

Date	Version	Changes
February 2011	1.5	<ul> <li>Removed the "Decision Feedback Equalization (DFE)" section now that AN 612: Decision Feedback Equalization in Stratix IV Devices is published.</li> </ul>
		<ul> <li>Moved the "Adaptive Equalization (AEQ)" sections to the Dynamic Reconfiguration in Stratix IV Devices chapter.</li> </ul>
		<ul> <li>Moved the "Power-On Reset Circuitry" and "Power-On Reset Specifications" sections to the Hot Socketing and Power-On Reset in Stratix IV Devices chapter.</li> </ul>
		<ul> <li>Minor text edits.</li> </ul>
September 2010	1.4	<ul> <li>Added corrections for the Adaptive Equalization (AEQ) section of the Stratix IV Dynamic Reconfiguration chapter.</li> </ul>
		<ul> <li>Added new information for the Decision Feedback Equalization (DFE) feature.</li> </ul>
April 2010	1.3	<ul> <li>Added corrections for the "Power-On Reset Circuitry" and "Power-On Reset Specifications" sections to of the Hot Socketing and Power-On Reset in Stratix IV Devices chapter.</li> </ul>
		Moved the "Power-On Reset Circuitry", "Power-On Reset Specifications", "Correct Power-Up Sequence for Production Devices", and "Correct Power-Up Sequence for Production Devices" sections to the Hot Socketing and Power-On Reset in Stratix IV Devices chapter.
March 2010	1.2	<ul> <li>Moved the "Power-On Reset Circuit" and "JTAG TMS and TDI Pin Pull-Up Resistor Value Specification" sections to the Configuration, Design Security, Remote System Upgrades with Stratix IV Devices chapter.</li> </ul>
		<ul> <li>Moved the "Summary of OCT Assignments" section to the I/O Features in Stratix IV Devices chapter.</li> </ul>
February 2010	1.1	<ul> <li>Added the "Power-On Reset Circuitry", "Power-On Reset Specifications", "Correction to POR Signal Pulse Width Delay Times", "Correct Power-Up Sequence for Production Devices", "Power-On Reset Circuit", "Summary of OCT Assignments", and "JTAG TMS and TDI Pin Pull-Up Resistor Value Specification" sections.</li> </ul>
		<ul> <li>Minor text edits.</li> </ul>
November 2009	1.0	Stratix IV GX enhanced transceiver data rate specifications in -4 commercial speed grade.
	1.0	<ul> <li>Initial release.</li> </ul>



This chapter provides additional information about the document and Altera.

## **About this Handbook**

This handbook provides comprehensive information about the Altera<sup>®</sup> Stratix<sup>®</sup> IV family of devices.

## **How to Contact Altera**

To locate the most up-to-date information about Altera products, refer to the following table.

Contact <sup>(1)</sup>	<b>Contact Method</b>	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
rechnical training	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

# **Typographic Conventions**

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, <b>Save As</b> dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, <b>\qdesigns</b> directory, <b>D:</b> drive, and <b>chiptrip.gdf</b> file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, Stratix IV Design Guidelines.
	Indicates variables. For example, $n + 1$ .
italic type	Variable names are enclosed in angle brackets (< >). For example, <i><file name=""></file></i> and <i><project name="">.pof</project></i> file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."

Visual Cue	Meaning
	Indicates signal, port, register, bit, block, and primitive names. For example, data1, tdi, and input. The suffix n denotes an active-low signal. For example, resetn.
Courier type	Indicates command line commands and anything that must be typed exactly as it appears. For example, c:\qdesigns\tutorial\chiptrip.gdf.
	Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword SUBDESIGN), and logic function names (for example, TRI).
ч	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
	Bullets indicate a list of items when the sequence of the items is not important.
IP	The hand points to information that requires special attention.
?	The question mark directs you to a software help system with related information.
•••	The feet direct you to another document or website with related information.
<b>I</b> , <b>™</b> I	The multimedia icon directs you to a related multimedia presentation.
CAUTION	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
WARNING	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.