DP83TG720S-Q1 1000BASE-T1 Automotive Ethernet PHY

1 Features

- IEEE802.3bp-1000BASE-T1 and Open Alliance (OA) compliant
  - IEEE PMA compliance
  - OA TC12 for interoperability and EMC
- EMC/EMI compliant
  - SAE J9262-3 compliant
  - OA TC12 immunity level-4 compliant over UTP (unshielded twisted pair)
  - OA TC12 emission compliant over UTP
- Integrated LPF on MDI pins
- Pin-to-pin compatible with TI's 100BASE-T1 PHY
  - enables single board for 100BASE-T1 and 1000BASE-T1
- Power savings features:
  - standby and sleep
  - local and remote wake-up
- Diagnostic tool kit
  - high accuracy temperature monitor
  - voltage monitor
  - ESD event monitor
  - Data throughput calculator : inbuilt MAC packet generator, counter and error checker
  - link quality monitoring
  - cable open and short fault detection
  - loopback modes
- MAC Interfaces: RGMII and SGMII
- Supported I/O voltages: 3.3 V, 2.5 V, and 1.8 V
- 25MHz clock output source
- VQFN, wettable flank packaging
- AEC-Q100 Qualified
  - Inbuilt ESD protection : IEC61000-4-2 ESD : ±8-kV contact discharge
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature

2 Applications

- Telematics control unit (TCU, TBOX)
- Backbone network
- Gateway and body control
- ADAS: LIDAR, RADAR

3 Description

The DP83TG720S-Q1 device is an IEEE 802.3bp and Open Alliance compliant automotive Ethernet physical layer transceiver. It provides all physical layer functions needed to transmit and receive data over unshielded/shielded single twisted-pair cables. The device provides xMII flexibility with support for RGMII and SGMII MAC interfaces.

DP83TG720 is compliant to Open Alliance EMC and interoperable specifications over unshieleded twisted cable. DP83TG720 is pin-2-pin compatible to TI's 100Base-T1 PHY enabling design scability with single board across for both speeds.This device offers the Diagnostic Tool Kit, with an extensive list of real-time monitoring tools, debug tools and test modes. Within the tool kit is the first integrated electrostatic discharge (ESD) monitoring tool. It is capable of counting ESD events on both the xMII and MDI as well as providing real-time monitoring through the use of a programmable interrupt. Additionally, the DP83TG720S-Q1 includes a data generation and checker tool to generate customizable MAC packets and check the errors on incoming packets.This enables system level datapath tests/optimizations without dependency on MAC.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DP83TG720S-Q1	VQFN (36)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

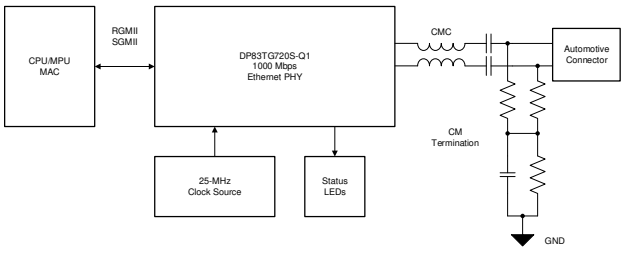

Figure 3-1. Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2020	*	Advance Information release. Release

5 Pin Configuration and Functions

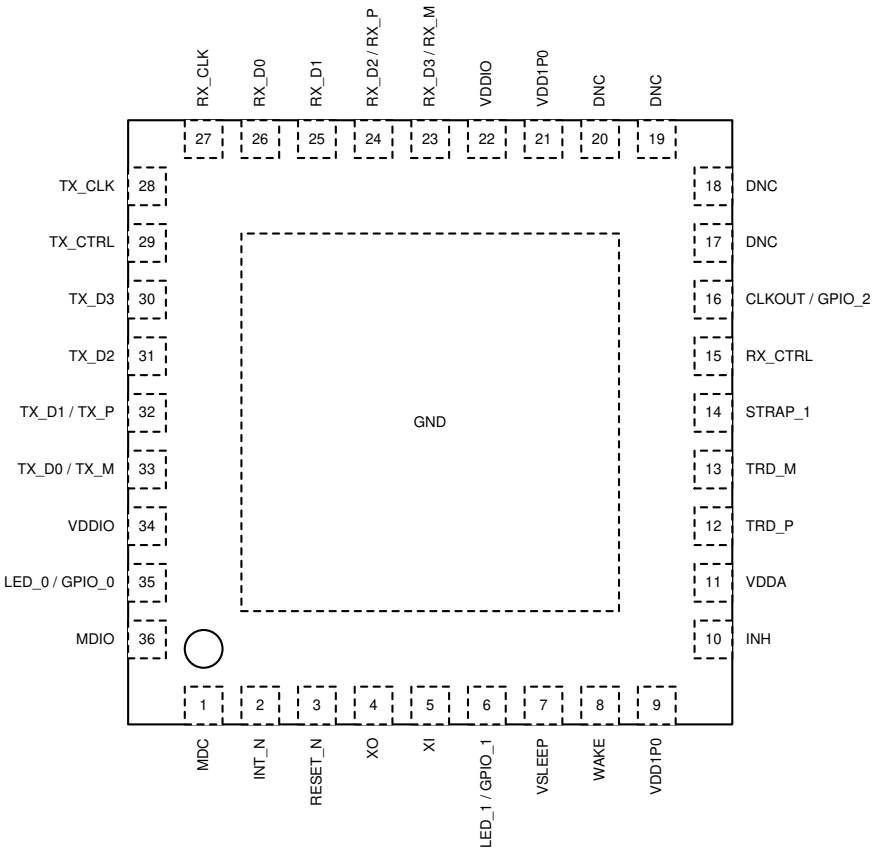

Figure 5-1. RHA Package 36-Pin VQFN Top View

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Pin Functions

PIN		STATE[1]	DESCRIPTION
NAME	NO.		
MAC INTERFACE			
RX_D3 RX_M	23	S, PD, O	**Receive Data:** Symbols received on the cable are decoded and transmitted out of these pins synchronous to the rising edge of RX_CLK. They contain valid data when RX_DV(decoded from RX_CTL) is asserted. A nibble, RX_D[3:0], is transmitted in RGMII mode. **RX_M / RX_P:** Differential SGMII Data Output. These pins transmit data from the PHY to the MAC.
RX_D2 RX_P	24		
RX_D1	25		
RX_D0	26		
RX_CLK	27	O	**Receive Clock:** In RGMII mode, PHY provides this 125-MHz clock to MAC. **Unused in SGMII mode**
RX_CTRL	15	S, PD, O	**RGMII Receive Control:** Receive control combines receive data valid indication and receive error indication into a single signal. RX_DV is presented on the rising edge of RX_CLK and RX_ER is presented on the falling edge of RX_CLK. **Used only as strap in SGMII mode**
TX_CLK	28	I	**Transmit Clock:** In RGMII mode, MAC provides this 125-MHz clock to PHY. **Unused in SGMII mode**
TX_CTRL	29	I	**RGMII Transmit Control:** Transmit control combines transmit enable and transmit error indication into a single signal. TX_EN is presented prior to the rising edge of TX_CLK; TX_ER is presented on the falling edge of TX_CLK. **Unused in SGMII mode**
TX_D3	30	I	**Transmit Data:** In RGMII mode, the transmit data nibble, TX_D[3:0], is received from the MAC . **TX_M / TX_P:** Differential SGMII Data Input. These pins receive data that is transmitted from the MAC to the PHY.
TX_D2	31		
TX_D1 TX_P	32		
TX_D0 TX_M	33		
SERIAL MANAGEMENT INTERFACE			
MDC	1	I	**Management Data Clock:** Synchronous clock to the MDIO serial management input and output data.
MDIO	36	OD, IO	**Management Data Input/Output:** Bidirectional management data signal that may be sourced by the management station or the PHY. This pin requires an external pull-up resistor (recommended value = 2.2-kΩ) .
CONTROL INTERFACE			
$\overline{\text{INT}}$	2	PU, OD, O	**Interrupt:** Active-LOW output, which will be asserted LOW when an interrupt condition occurs. This pin has a weak internal pullup. Register access is necessary to enable various interrupt triggers. Once an interrupt event flag is set, register access is required to clear the interrupt event on this pin. This pin can be configured as an Active-HIGH output using register[0x0011].
$\overline{\text{RESET}}$	3	PU, I	**RESET:** Active-LOW input, which initializes or reinitializes the DP83TG720S-Q1. Asserting this pin LOW for at least 10 µs will force a reset process to occur. All internal registers will reinitialize to their default states as specified for each bit in the Register Map section. All bootstrap pins are resampled upon deassertion of reset.
INH	10	PMOS OD	**INH:** Active-HIGH PMOS open-drain output. When the PHY enters the sleep state, PHY will release the INH pin to allow an external pull-down resistor (recommended value = 10 kΩ) to pull the line to ground. When in any other state, the INH pin will drive a HIGH state to the VSLEEP rail.
WAKE	8	PD, I	**WAKE:** Active-HIGH (this pin works on VSLEEP domain) pulse on wake-up pin wakes up the PHY from the sleep state. For pulse width, refer to timing section. This pin can be directly tied to the VSLEEP rail when the sleep state is not used or left float.
STRP_1	14	PD, I	**Strap 1:** This pin is for strapping PHY_AD bits.
CLOCK INTERFACE			
XI	5	I	**Reference Clock Input:** Reference clock 25-MHz ±100 ppm-tolerance crystal or oscillator input. The device supports either an external crystal resonator connected across pins XI and XO, or an external CMOS-level oscillator connected to pin XI only and XO left floating.

PIN		STATE[1]	DESCRIPTION
NAME	NO.		
XO	4	O	**Reference Clock Output:** XO pin is used for crystal only. This pin should be left floating when a CMOS-level oscillator is connected to XI.
LED/GPIO INTERFACE			
LED_0 / GPIO_0	35	S, PD, IO	**LED_0:** Link Status
LED_1 / GPIO_1	6	S, PD, IO	**LED_1:** Link Status and BLINK for TX/RX Activity
CLKOUT / GPIO_2	16	IO	**Clock Output:** 25-MHz reference clock(buffered replication of XI) by default. Can be configured to output different clock sources.
MEDIUM DEPENDENT INTERFACE			
TRD_M	13	IO	**Differential Transmit and Receive:** Bidirectional differential signaling configured for 1000BASE-T1 operation, IEEE 802.3bp compliant.
TRD_P	12		
POWER AND GROUND CONNECTIONS			
VDDA3P3	11	SUPPLY	**Core Supply:** 3.3 V. Refer to power supply recommendations for decoupling network.
VDDIO	22, 34	SUPPLY	**IO Supply:** 1.8 V, 2.5 V, or 3.3 V. Refer to power supply recommendations for decoupling network.
VDD1P0	9, 21	SUPPLY	**Core Supply:** 1.0 V. Refer to power supply recommendations for decoupling network.
VSLEEP	7	SUPPLY	**Sleep Supply:** 3.3 V. Refer to power supply recommendations for decoupling network. This pin shall be tied to VDDA3P3 if sleep functionality is not used.
GROUND	DAP	GROUND	**Ground**
DO NOT CONNECT			
DNC	17, 18, 19, 20	DNC	**DNC:** Do Not Connect (floating)

(1) Type: I = Input
O = Output
IO = Input/Output
OD = Open Drain
PD = Internal Pulldown
PU = Internal Pullup
S = Strap: Configuration pin (all configuration pins have weak internal pullups or pulldowns)

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Table 5-1. Pin States - RGMII

PIN NAME	POWER-UP / RESET			NORMAL OPERATION - RGMII		
	PIN STATE	PULL TYPE	PULL VALUE (kΩ)	PIN STATE	PULL TYPE	PULL VALUE (kΩ)
MDC	I	none	-	I	none	-
INT_N	I	PU	9	OD	PU	9
RESET_N	I	PU	9	I	PU	9
XO	O	none	-	O	none	-
XI	I	none	-	I	none	-
LED_1	I	PD	9	O	none	-
WAKE	I	PD	50	I	PD	50
STRP_1	I	PD	6	I	none	-
INH	I	none	-	PMOS OD, O	none	-
RX_CTRL	I	PD	6	O	none	-
CLKOUT/GPIO_2	O	none	-	O	none	-
RX_D3	I	PD	9	O	none	-
RX_D2	I	PD	9	O	none	-
RX_D1	I	PD	9	O	none	-
RX_D0	I	PD	9	O	none	-
RX_CLK	I	PD	9	O	none	-
TX_CLK	I	none	-	I	none	-
TX_CTRL	I	none	-	I	none	-
TX_D3	I	none	-	I	none	-
TX_D2	I	none	-	I	none	-
TX_D1	I	none	-	I	none	-
TX_D0	I	none	-	I	none	-
LED_0	I	PD	9	O	none	-
MDIO	I	none	-	IO	none	-

Table 5-2. Pin States - SGMII

PIN NAME	POWER-UP / RESET			NORMAL OPERATION - SGMII		
	PIN STATE	PULL TYPE	PULL VALUE (kΩ)	PIN STATE	PULL TYPE	PULL VALUE (kΩ)
MDC	I	none	-	I	none	-
INT_N	I	PU	9	OD	PU	9
RESET_N	I	PU	9	I	PU	9
XO	O	none	-	O	none	-
XI	I	none	-	I	none	-
LED_1	I	PD	9	O	none	-
WAKE	I	PD	50	I	PD	50
STRP_1	I	PD	6	I	none	-
INH	I	none	-	PMOS OD, O	none	-
RX_CTRL	I	PD	6	Hi-Z	PD	6
CLKOUT/GPIO_2	O	none	-	O	none	-
RX_D3	I	PD	9	O	none	-
RX_D2	I	PD	9	O	none	-
RX_D1	I	PD	9	Hi-Z	PD	9
RX_D0	I	PD	9	Hi-Z	PD	9
RX_CLK	I	PD	9	Hi-Z	PD	9
TX_CLK	I	none	-	Hi-Z	none	-
TX_CTRL	I	none	-	Hi-Z	none	-
TX_D3	I	none	-	Hi-Z	none	-
TX_D2	I	none	-	Hi-Z	none	-
TX_D1	I	none	-	I	none	-
TX_D0	I	none	-	I	none	-
LED_0	I	PD	9	O	none	-
MDIO	I	none	-	IO	none	-

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Table 5-3. Pin States - Sleep and Isolate

PIN NAME	MAC ISOLATE			SLEEP		
	PIN STATE	PULL TYPE	PULL VALUE (kΩ)	PIN STATE	PULL TYPE	PULL VALUE (kΩ)
MDC	I	none	-	Float	none	-
INT_N	O	PU	9	Float	none	-
RESET_N	I	PU	9	Float	none	-
XO	O	none	-	Float	none	-
XI	I	none	-	Float	none	-
LED_1	O	none	-	Float	none	-
WAKE	I	PD	50	I	none	50
STRP_1	I	none	-	Float	none	-
INH	I	none	-	PMOS OD, O	none	-
RX_CTRL	I	PD	6	Float	none	-
CLKOUT/GPIO_2	O	none	-	Float	none	-
RX_D3	I	PD	9	Float	none	-
RX_D2	I	PD	9	Float	none	-
RX_D1	I	PD	9	Float	none	-
RX_D0	I	PD	9	Float	none	-
RX_CLK	I	PD	9	Float	none	-
TX_CLK	I	none	-	Float	none	-
TX_CTRL	I	none	-	Float	none	-
TX_D3	I	none	-	Float	none	-
TX_D2	I	none	-	Float	none	-
TX_D1	I	none	-	Float	none	-
TX_D0	I	none	-	Float	none	-
LED_0	O	none	-	Float	none	-
MDIO	IO	none	-	Float	none	-

Note

For sleep mode entry vdda, vddio and vdd1p0 are supposed to be powered-down. See figure Required Implementation of Sleep Mode for further details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	TYP	MAX	UNIT
Supply Voltage	VDDA3P3	–0.3		4	V
Supply Voltage	VDD1P0	–0.3		1.4	V
Supply Voltage	VDDIO (3.3V)	–0.3		4	V
Supply Voltage	VDDIO (2.5V)	-0.3		2.9	V
Supply Voltage	VDDIO (1.8V)	-0.3		2.2	V
Supply Voltage	V_{SLEEP}	-0.3		4	V
LVCMOS/ LVTTL Input Voltage	MDC, $\overline{RESET}$, XI, LED_1, STRP_1, RX_CTRL, CLKOUT, RX_D[3:0], TX_CLK, $\overline{TX\_CTRL}$, $\overline{TX\_D[3:0]}$, LED_0, MDIO	–0.3		VDDIO + 0.3	V
LVCMOS/ LVTTL Input Voltage	WAKE	-0.3		V_{SLEEP} + 0.3	V
LVCMOS/ LVTTL Output Voltage	$\overline{INT}$, LED_1, RX_CTRL, CLKOUT, RX_D[3:0], RX_CLK, LED_0, MDIO	–0.3		VDDIO + 0.3	V
LVCMOS/ LVTTL Output Voltage	INH	-0.3		VSLEEP + 0.3	V
T_J	Junction Temperature			150	°C
T_{stg}	Storage temperature	–65		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011	All pins	±500	V
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	TRD_N, TRD_P	±8000	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDIO	IO Supply Voltage, 1.8V operation	1.62	1.8	1.98	V
	IO Supply Voltage, 2.5V operation	2.25	2.5	2.75	
	IO Supply Voltage, 3.3V operation	2.97	3.3	3.63	
VDDA3P3	Core Supply Voltage, 3.3V	2.97	3.3	3.63	V
VDDA1P0	Core Supply Voltage, 1.0V	0.95	1	1.1	V
V_{SLEEP}	Sleep Supply Voltage, 3.3V	2.97	3.3	3.63	V

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over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DP83TG720 RHA (VQFN) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
WAKE pin	WAKE pin	WAKE pin	WAKE pin	WAKE pin	WAKE pin	WAKE pin
V_{IH}	High-level Input Voltage	V_{SLEEP} = 3.3V ± 10%	2			V
V_{IL}	Low-level Input Voltage	V_{SLEEP} = 3.3V ± 10%			0.8	V
INH pin	INH pin	INH pin	INH pin	INH pin	INH pin	INH pin
V_{OH}	High-level Output Voltage	I_{OH} = -2mA, V_{SLEEP} = 3.3V ± 10%	2.4			V
3.3V VDDIO (2)						
V_{OH}	High-level Output Voltage	I_{OH} = -2mA, VDDIO = 3.3V ± 10%	2.4			V
V_{OL}	Low-level Output Voltage	I_{OL} = 2mA, VDDIO = 3.3V ± 10%			0.4	V
V_{IH}	High-level Input Voltage	VDDIO = 3.3V ± 10%	2			V
V_{IL}	Low-level Input Voltage	VDDIO = 3.3V ± 10%			0.8	V
2.5V VDDIO (2)						
V_{OH}	High-level Output Voltage	I_{OH} = -2mA, VDDIO = 2.5V ± 10%	2			V
V_{OL}	Low-level Output Voltage	I_{OL} = 2mA, VDDIO = 2.5V ± 10%			0.4	V
V_{IH}	High-level Input Voltage	VDDIO = 2.5V ± 10%	1.7			V
V_{IL}	Low-level Input Voltage	VDDIO = 2.5V ± 10%			0.7	V
1.8V VDDIO (2)						
V_{OH}	High-level Output Voltage	I_{OH} = -2mA, VDDIO = 1.8V ± 10%	VDDIO – 0.45			V
V_{OL}	Low-level Output Voltage	I_{OL} = 2mA, VDDIO = 1.8V ± 10%			0.45	V
V_{IH}	High-level Input Voltage	VDDIO = 1.8V ± 10%	0.7 * VDDIO			V
V_{IL}	Low-level Input Voltage	VDDIO = 1.8V ± 10%			0.3 * VDDIO	V
I_{IH}	Input High Current (RGMII Input pin, MDC, MDIO)	VIN = VCC, -40°C to 125°C	-60		60	µA
I_{IL}	Input Low Current (RGMII Input pin, MDC, MDIO)	VIN = GND, -40°C to 125°C	-60		60	µA

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Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OZ}	Tri-state Output Current (2)	VOUT = VCC, VOUNT = GND, -40°C to 125°C	-60		60	µA
C_{IN}	Input Capacitance	LVCMOS/LVTTL pins (3)		2		pF
C_{IN}	Input Capacitance	LVCMOS/LVTTL pins (4)		4		pF
		XI		1		pF
C_{OUT}	Output Capacitance	LVCMOS/LVTTL pins (3)		2		pF
C_{OUT}	Output Capacitance	LVCMOS/LVTTL pins (4)		4		pF
		XO		1		pF
$R_{pull-up}$	Integrated Pull-Up Resistance	$\overline{INT}$, $\overline{RESET}$	6.5	9	12.5	kΩ
$R_{pull-down}$	Integrated Pull-Down Resistance	STRP_1, RX_CTRL		6.3		kΩ
$R_{pull-down}$	Integrated Pull-Down Resistance	LED_1, RX_D[3:0], RX_CLK, LED_0	6.75	9	14.5	kΩ
		WAKE	37.5	50	62.5	kΩ
$R_{pull-down}$	Integrated Pull-Up Resistance when Active	INH				kΩ
R_{series}	Integrated MAC Series Termination Resistor (Default)	RX_D[3:0], RX_CTRL, and RX_CLK		42		Ω
CURRENT CONSUMPTION, SLEEP MODE						
I_{SLEEP}	Sleep Supply Current	V_{SLEEP}		485		µA
CURRENT CONSUMPTION, RESET ASSERTED						
I_{DDIO}	IO Supply Current, VDDIO = 1.8V	VDDIO		1		mA
I_{DDIO}	IO Supply Current, VDDIO = 2.5V	VDDIO		3		mA
I_{DDIO}	IO Supply Current, VDDIO = 3.3V	VDDIO		4		mA
I_{DDA3P3}	Core Supply Current, 3.3V	VDDA3P3		5		mA
I_{DD1P0}	Core Supply Current, 1.0V			50		mA
CURRENT CONSUMPTION, ACTIVE MODE, Voltage: +/- 10%, Traffic : 100%,Packet Size: 1518, Content : Random						
I_{DDIO}	IO Supply Current, VDDIO = 1.8V	RGMII		20	25	mA
I_{DDIO}	IO Supply Current, VDDIO = 2.5V	RGMII		26	30	mA
I_{DDIO}	IO Supply Current, VDDIO = 3.3V	RGMII		33	40	mA
I_{DDIO}	IO Supply Current, VDDIO = 1.8V	SGMII		1.5	2.5	mA
I_{DDIO}	IO Supply Current, VDDIO = 2.5V	SGMII		3.5	5	mA
I_{DDIO}	IO Supply Current, VDDIO = 3.3V	SGMII		5.5	7	mA
I_{DDA3P3}	Core Supply Current, 3.3V	RGMII		81	85	mA
I_{DD1P0}	Core Supply Current, 1.0V	RGMII		160	225	mA
I_{DDA3P3}	Core Supply Current, 3.3V	SGMII		95	100	mA
I_{DD1P0}	Core Supply Current, 1.0V	SGMII		200	260	mA
MDI CHARACTERISTICS						
V_{OD-MDI}	Output Differential Voltage	$R_{L(diff)}$ = 100 Ω			1.3	V
$R_{MDI-DIFF}$	Integrated Differential MDI Termination (Active State)	TRD_P, TRD_N		100		Ω
$R_{MDI-DIFF}$	Integrated Differential MDI Termination (Sleep State)	TRD_P, TRD_N		100		Ω
SGMII DRIVER DC SPECIFICATIONS						
$V_{OD-SGMII}$	Output Differential Voltage	$R_{L(diff)}$ = 100 Ω	150		400	mV
$R_{OUT-DIFF}$	Integrated Differential Output Termination	RX_P, RX_M		100		Ω
SGMII RECEIVER DC SPECIFICATIONS						
V_{IDTH}	Input Differential Threshold		100			mV

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Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{IN-DIFF}$	Integrated Differential Input Termination	TX_P, TX_M		100		Ω
BOOTSTRAP DC CHARACTERISTICS						
Vbsl_1v8	Bootstrap Threshold	Mode 1, VDDIO = 1.8V ± 10%, 2-level	0		0.35*VDDIO	V
Vbsh_1v8	Bootstrap Threshold	Mode 2, VDDIO = 1.8V ± 10%, 2-level	0.65*VDDIO		VDDIO	V
Vbsl_2v5	Bootstrap Threshold	Mode 1, VDDIO = 2.5V ± 10%, 2-level	0		0.7	V
Vbsh_2v5	Bootstrap Threshold	Mode 2, VDDIO = 2.5V ± 10%, 2-level	1.7		VDDIO	V
Vbsl_3v3	Bootstrap Threshold	Mode 1, VDDIO = 3.3V ± 10%, 2-level	0		0.7	V
Vbsh_3v3	Bootstrap Threshold	Mode 2, VDDIO = 3.3V ± 10%, 2-level	2		VDDIO	V
V_{bs1_1V8}	Bootstrap Threshold	Mode 1, VDDIO = 1.8V ± 10%, 3-level	0		0.35 * VDDIO	V
V_{bs2_1V8}	Bootstrap Threshold	Mode 2, VDDIO = 1.8V ± 10%, 3-level	0.40 * VDDIO		0.75 * VDDIO	V
V_{bs3_1V8}	Bootstrap Threshold	Mode 3, VDDIO = 1.8V ± 10%, 3-level	0.84 * VDDIO		VDDIO	V
V_{bs1_2V5}	Bootstrap Threshold	Mode 1, VDDIO = 2.5V ± 10%, 3-level	0		0.25 * VDDIO	V
V_{bs2_2V5}	Bootstrap Threshold	Mode 2, VDDIO = 2.5V ± 10%, 3-level	0.29 * VDDIO		0.56 * VDDIO	V
V_{bs3_2V5}	Bootstrap Threshold	Mode 3, VDDIO = 2.5V ± 10%, 3-level	0.65 * VDDIO		VDDIO	V
V_{bs1_3V3}	Bootstrap Threshold	Mode 1, VDDIO = 3.3V ± 10%, 3-level	0		0.18 * VDDIO	V
V_{bs2_3V3}	Bootstrap Threshold	Mode 2, VDDIO = 3.3V ± 10%, 3-level	0.22 * VDDIO		0.42 * VDDIO	V
V_{bs3_3V3}	Bootstrap Threshold	Mode 3, VDDIO = 3.3V ± 10%, 3-level	0.46 * VDDIO		VDDIO	V
Temperature Sensor						
	Temperature Sensor Resolution (LSB)	-40℃ to 125℃		1.5		℃
	Temperature Sensor Accuracy (Voltage and Temperature Variation on single part)	-40℃ to 125℃		7.5		℃
	Temperature Sensor Accuracy (Voltage, Temperature and Part-to-Part variation)	-40℃ to 125℃	-21.5		20	℃
	Temperature Sensor Range		-40		140	℃
Voltage Sensor						
	VDDA3P3 Sensor Range		2.66	3.3	3.96	V
	VDDA3P3 Sensor Resolution (LSB)	-40℃ to 125℃		8.6		mV
	VDDA3P3 Sensor Accuracy (Voltage and Temperature Variation)	-40℃ to 125℃		8.6		mV
	VDDA3P3 Sensor Accuracy Part-to-Part	-40℃ to 125℃	-68.8		68.8	mV
	VDD1P0 Sensor Range		0.8		1.2	V
	VDD1P0 Sensor Resolution (LSB)	-40℃ to 125℃		2.8		mV
	VDD1P0 Sensor Accuracy (Voltage and Temperature Variation)	-40℃ to 125℃		2.8		mV
	VDD1P0 Sensor Accuracy Part-to-Part	-40℃ to 125℃	-22.4		22.4	mV
	VDDIO Sensor Range		1.44		3.8	V
	VDDIO Sensor Resolution (LSB)	-40℃ to 125℃		15.4		mV

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	VDDIO Sensor Accuracy (Voltage and Temperature Variation)	-40℃ to 125℃			15.4	mV
	VDDIO Sensor Accuracy Part-to-Part	-40℃ to 125℃			15.4	mV

(1) Ensured by production test, characterization or design
(2) For pins: MDC, $\overline{INT}$, $\overline{RESET}$, LED_1, STRP_1, RX_CTRL, CLKOUT, RX_D[3:0], RX_CLK, TX_CLK, TX_CTRL, TX_D[3:0], LED_0, and MDIO
(3) For pins: MDC, $\overline{INT}$, $\overline{RESET}$, LED_1, STRP_1, RX_CTRL, CLKOUT, RX_D0, RX_D1, RX_CLK, TX_CLK, TX_CTRL, TX_D2, TX_D3, LED_0, and MDIO
(4) For pins: TX_D0, TX_D1, RX_D2, and RX_D3

6.6 Timing Requirements

(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
POWER-UP TIMING						
T5.1	VDDA3P3 Duration(2)	0% to 100% (+/- 10 VDDA3P3)	0.5		40	ms
T5.2	VDD1P0 Duration(2)	0% to 100% (+/- 10 VDD1P0)	0.1		40	ms
T5.2	VDDIO Duration(2)	VDDIO = 1.8V	0.1		40	ms
T5.2	VDDIO Duration(2)	VDDIO = 2.5V	0.1		40	ms
T5.2	VDDIO Duration(2)	VDDIO = 3.3V	0.1		40	ms
T5.2	$V_{SLEEP\ Duration}$ (2)	0% to 100% (+/- 10 V_{SLEEP})	0.1		40	ms
T5.3	Crystal stabilization-time post power-up (from last power rail ramp to 100%)			1500		µs
T5.4	Osillator stabilization-time post power-up (from last power rail ramp to 100%)(3)				20	ms
T5.5	Post power-up stabilization-time prior to MDC preamble for register access		65			ms
T5.6	Hardware configuration latch-in time from power-up				60	ms
T5.7	Hardware configuration pins transition to functional mode from latch-in completion				110	ns
T5.8	PAM3 IDLE Stream from power-up (Master Mode)				60	ms
RESET TIMING (RESET_N)						
T6.1	RESET pulse width		5			µs
T6.2	Post reset stabilization-time prior to MDC preamble for register access		1			ms
T6.3	Hardware configuration latch-in time from reset				2	µs
T6.4	Hardware configuration pins transition to functional mode from latch-in completion				1.5	µs
T6.5	PAM3 IDLE Stream from reset (Master Mode)				1500	µs
SMI TIMING						
T4.1	MDC to MDIO (Output) Delay Time (25 pF load)		0	6	10	ns
T4.2	MDIO (Input) to MDC Setup Time		10			ns
T4.3	MDIO (Input) to MDC Hold Time		10			ns
	MDC Frequency (25 pF load)			2.5	20	MHz
RECEIVE LATENCY TIMING						
	SSD symbol on MDI to Rising edge of RGMII RX_CLK with assertion of RX_CTRL				8	µs

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(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
	SSD symbol on MDI to Rising edge of RGMII RX_CLK with assertion of RX_CTRL (RS-FEC bypass mode)				400	ns
	SSD symbol on MDI to first symbol of SGMII				9	µs
	SSD symbol on MDI to first symbol of SGMII (RS-FEC bypass mode)				450	ns
TRANSMIT LATENCY TIMING						
	RGMII Rising edge TX_CLK with assertion TX_CTRL to SSD symbol on MDI				8	µs
	RGMII Rising edge TX_CLK with assertion TX_CTRL to SSD symbol on MDI (RS-FEC bypass mode)				600	ns
	First symbol of SGMII to SSD symbol on MDI				9	µs
	First symbol of SGMII to SSD symbol on MDI (RS-FEC bypass mode)				700	ns
25 MHz OSCILLATOR REQUIREMENTS						
	Frequency (XI)			25		MHz
	Frequency Tolerance and Stability Over temperature and aging		–100		100	ppm
	Rise / Fall Time (10% - 90%)				8	ns
	Jitter (RMS)			3.6		ps
	Duty Cycle			50		%
RGMII TIMING						
T_{setupR}	TX_D[3:0], TX_CTRL Setup to TX_CLK	on PHY pins	1	2		ns
T_{holdR}	TX_D[3:0], TX_CTRL Hold from TX_CLK (5)	on PHY pins	1	2		ns
T_{skewT}	RX_D[3:0], RX_CTRL Delay from RX_CLK (Align Mode Enabled)	On PHY Pins	-500	0	500	ps
T_{skewT} (Shift)	RX_D[3:0], RX_CTRL Delay from RX_CLK (Shift Mode Enabled, default)(4)	On PHY Pins	2.240	2.650	2.970	ns
T_{cyc}	Clock Cycle Duration	RX_CLK	7.2	8	8.8	ns
T_{cyc}	Clock Cycle Duration	TX_CLK	7.2	8	8.8	ns
Duty_G	Duty Cycle	RX_CLK	45	50	55	%
Duty_G	Duty Cycle	TX_CLK	45	50	55	%
Tr	Rise Time (20% - 80%)	CL=Ctrace=5pF			0.75	ns
Tf	Fall Time (20% - 80%)	$C_{L=Ctrace}$ = 5pF			0.75	ns
RGMII Shift Mode Delays	DLL DLL_RX_DELAY_CTRL_SL=0(4)		0.330	0.650	0.970	ns
	DLL DLL_RX_DELAY_CTRL_SL=1(4)		0.580	0.900	1.220	ns
	DLL DLL_RX_DELAY_CTRL_SL=2(4)		0.830	1.150	1470	ns
	DLL DLL_RX_DELAY_CTRL_SL=3(4)		1.080	1.400	1.720	ns
	DLL DLL_RX_DELAY_CTRL_SL=4(4)		1.240	1.650	1.970	ns
	DLL DLL_RX_DELAY_CTRL_SL=5(4)		1.490	1.990	2.220	ns
	DLL DLL_RX_DELAY_CTRL_SL=6(4)		1.740	2.150	2.470	ns
	DLL DLL_RX_DELAY_CTRL_SL=7(4)		1.990	2.400	2.730	ns
	DLL DLL_RX_DELAY_CTRL_SL=8(4)		2.240	2.650	2.970	ns
	DLL DLL_RX_DELAY_CTRL_SL=9(4)		2.490	2.900	3.220	ns
SGMII TRANSMITTER AC TIMING						
	Clock signal duty cycle at 625 MHz		48		52	%
T_{rise}	Vod Rise Time		100		200	ps

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(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
T_{fall}	Vod Fall Time		100		200	ps
Jitter	Output jitter			300		ps
25 MHz CRYSTAL REQUIREMENTS						
	Frequency			25		MHz
	Frequency Tolerance and Stability Over temperature and aging		–100		100	ppm
	Equivalent Series Resistance				50	Ω
OUTPUT CLOCK TIMING (CLKOUT)						
	Frequency			25		MHz
	Duty Cycle (With XI source as 50%)		48		52	%
	Rise / Fall Time (10% - 90%)				2.5	ns
	Jitter (RMS) (Slave Mode, MAC Iinterface : SGMII)				3.6	ps
	Jitter (RMS) (Master Mode, MAC Iinterface : SGMII)				2.4	ps
	Jitter (RMS) (Slave Mode, MAC Interface : RGMII)				11	ps
	Jitter (RMS) (Master Mode, MAC Interface : RGMII)				15	ps
Sleep Entry and Wake-Up						
	MDI Energy Loss to Sleep Entry; INH Transition LOW	Normal Mode, WAKE = LOW, sleep_en = TRUE	4			ms
	Local Wake-Up Pulse Duration	Sleep Mode, WAKE pin	48		80	µs
	MDI Energy Detection Wake-Up Pulse Duration	Sleep Mode	0.75		1.25	ms

(1) Ensured by production test or characterization or design.
(2) No supply sequencing constraint across power rails
(3) In case OSC clock is delayed, additional reset is needed post Osc clock stablisation
(4) Refer register[0x0430] for programmability of RX delay codes
(5) PHY provides internal delays on TX_CLK to TX_D[3:0] to add additional skew upto 2 ns. Refer to register[0x0430] for programmability

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6.7 Timing Diagrams

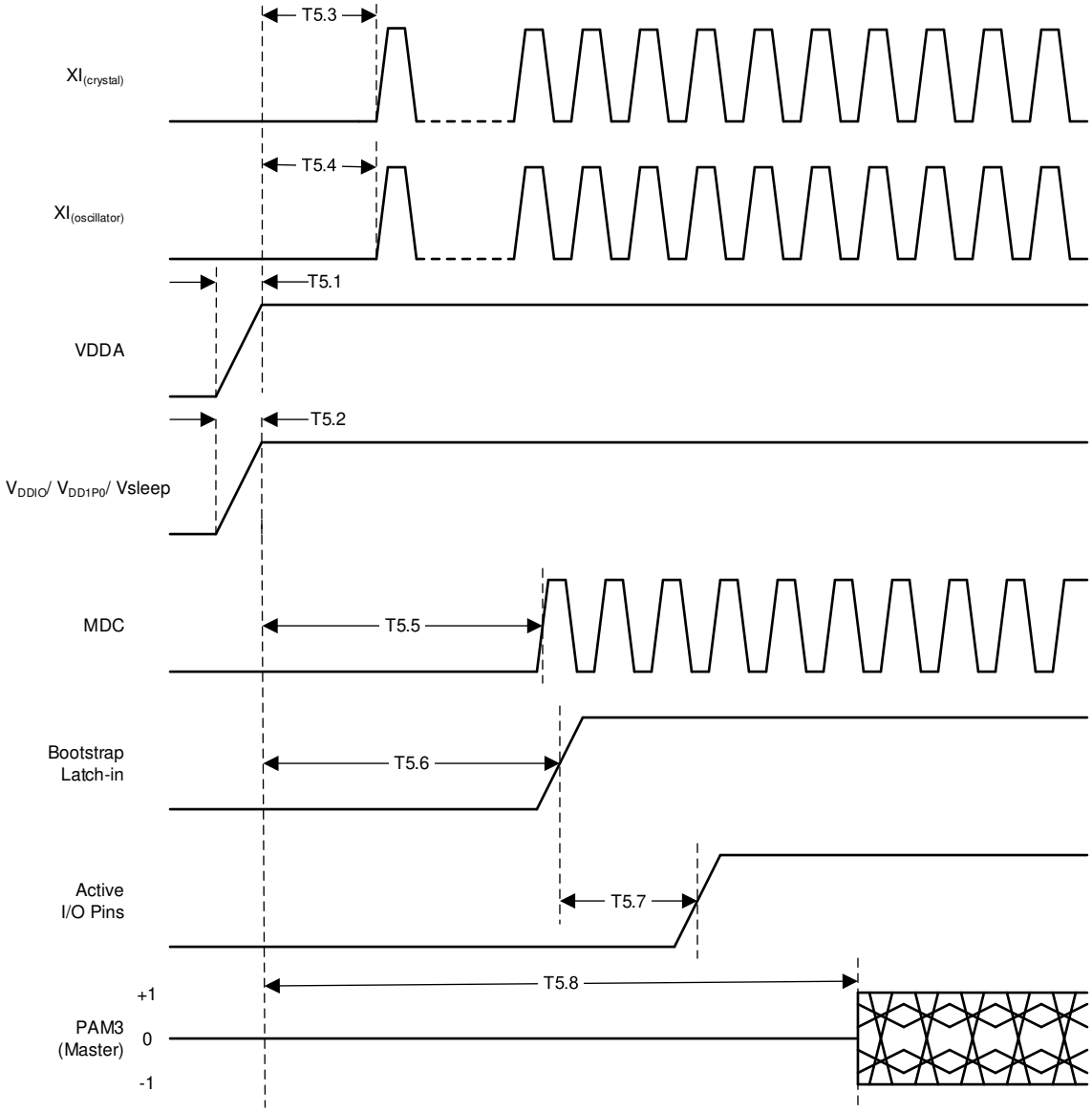

Figure 6-1. Power Up Timing

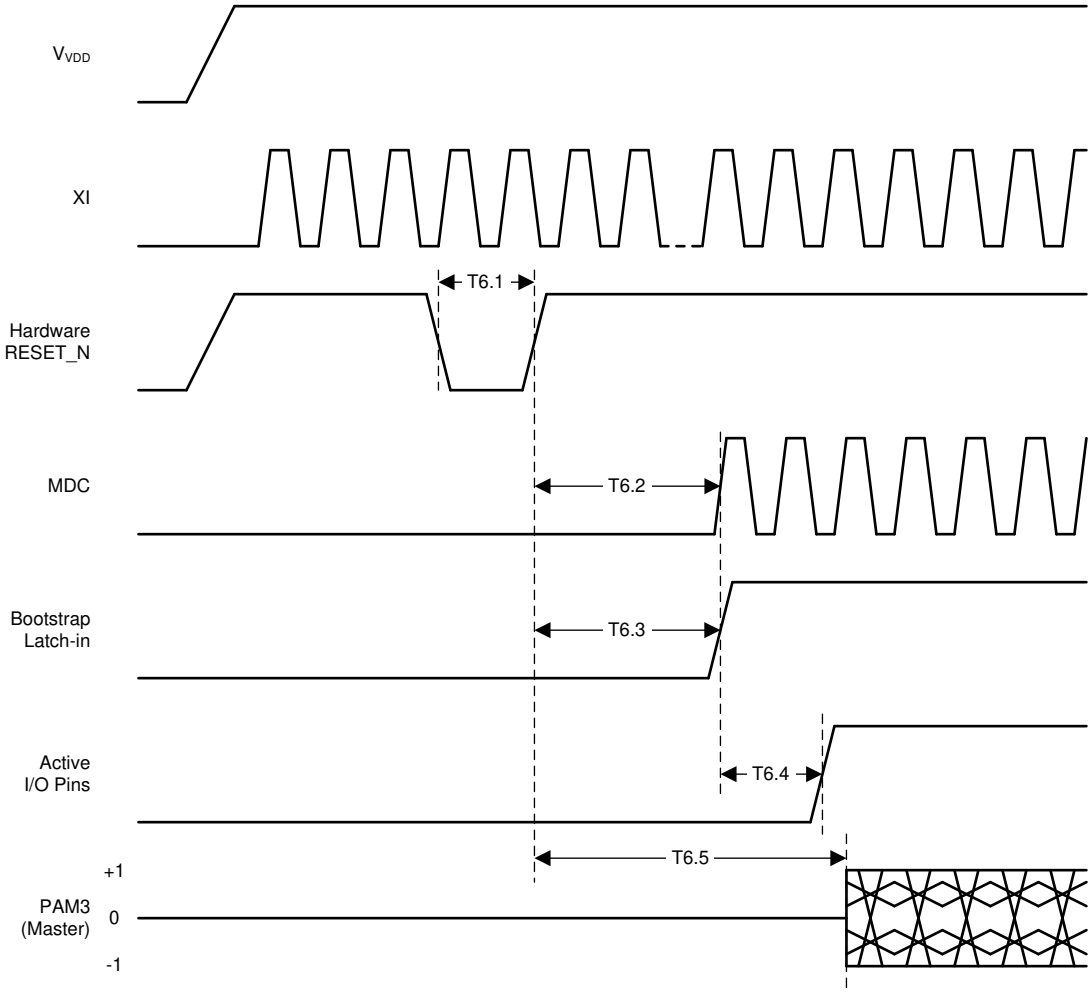

Figure 6-2. Reset Timing

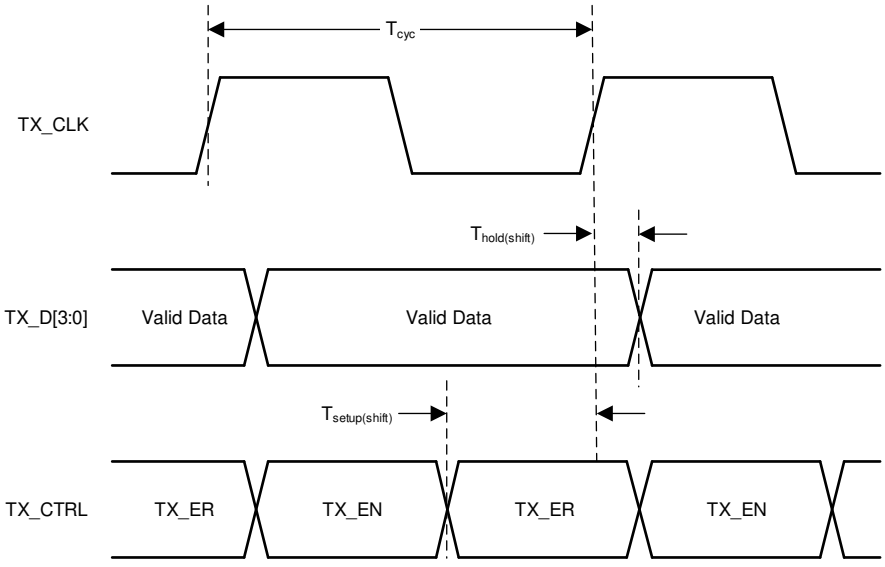

Figure 6-3. RGMII Transmit Timing (Internal Delay Enabled)

ADVANCE INFORMATION

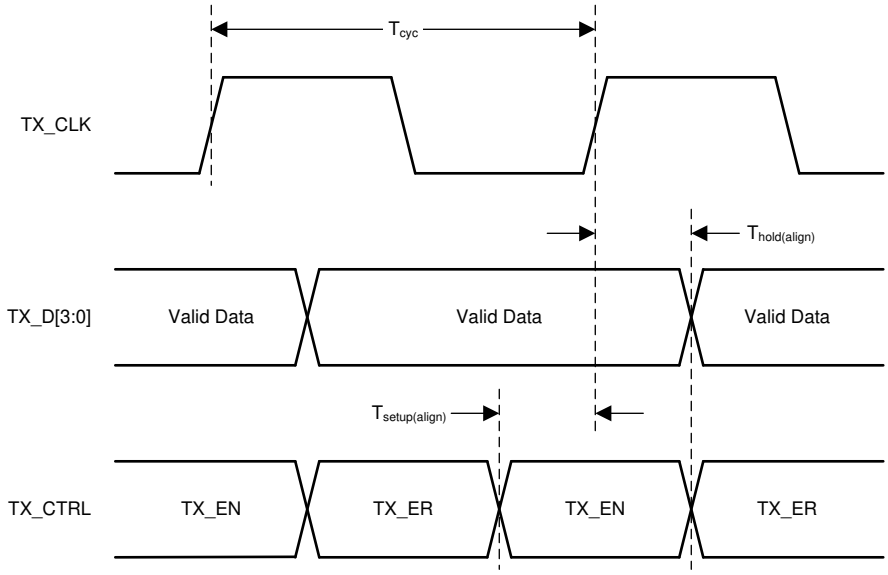

Figure 6-4. RGMII Transmit Timing (Internal Delay Disabled)

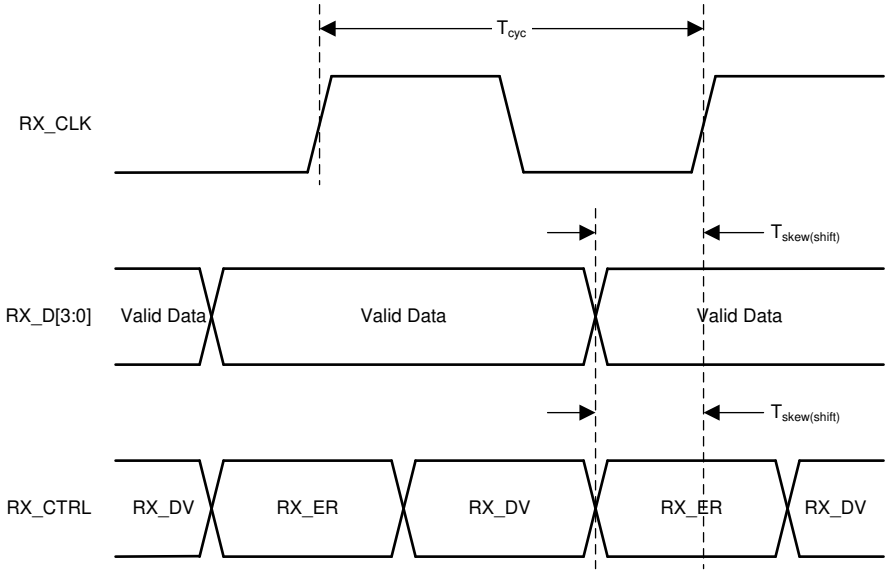

Figure 6-5. RGMII Receive Timing (Internal Delay Enabled)

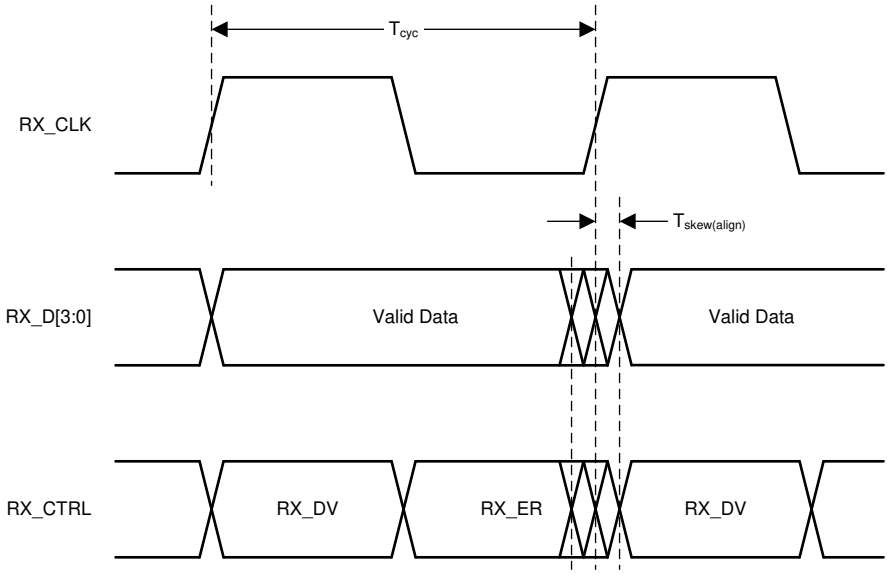

Figure 6-6. RGMII Receive Timing (Internal Delay Disabled)

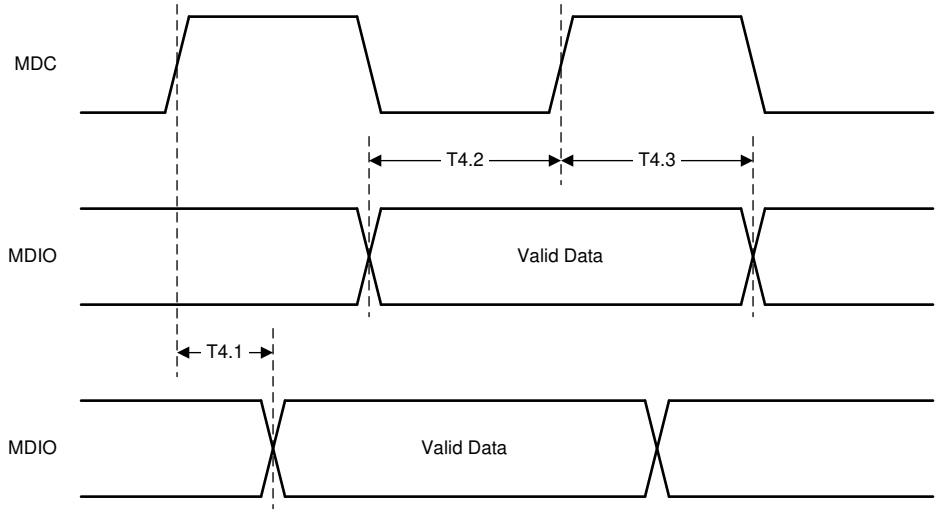

Figure 6-7. Serial Management Timing

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The DP83TG720S-Q1 is a 1000BASE-T1 automotive Ethernet Physical Layer transceiver. It is IEEE 802.3bp compliant and AEC-Q100 qualified for automotive applications.

This device is specifically designed to operate at 1-Gbps speed while meeting stringent automotive EMC requirements. The DP83TG720S-Q1 transmits PAM3 ternary symbols at 750-MBd over unshielded/shielded single-twisted pair cable. It is designed for RGMII or SGMII support in a single 36-pin VQFN wettable flank package.

7.2 Functional Block Diagram

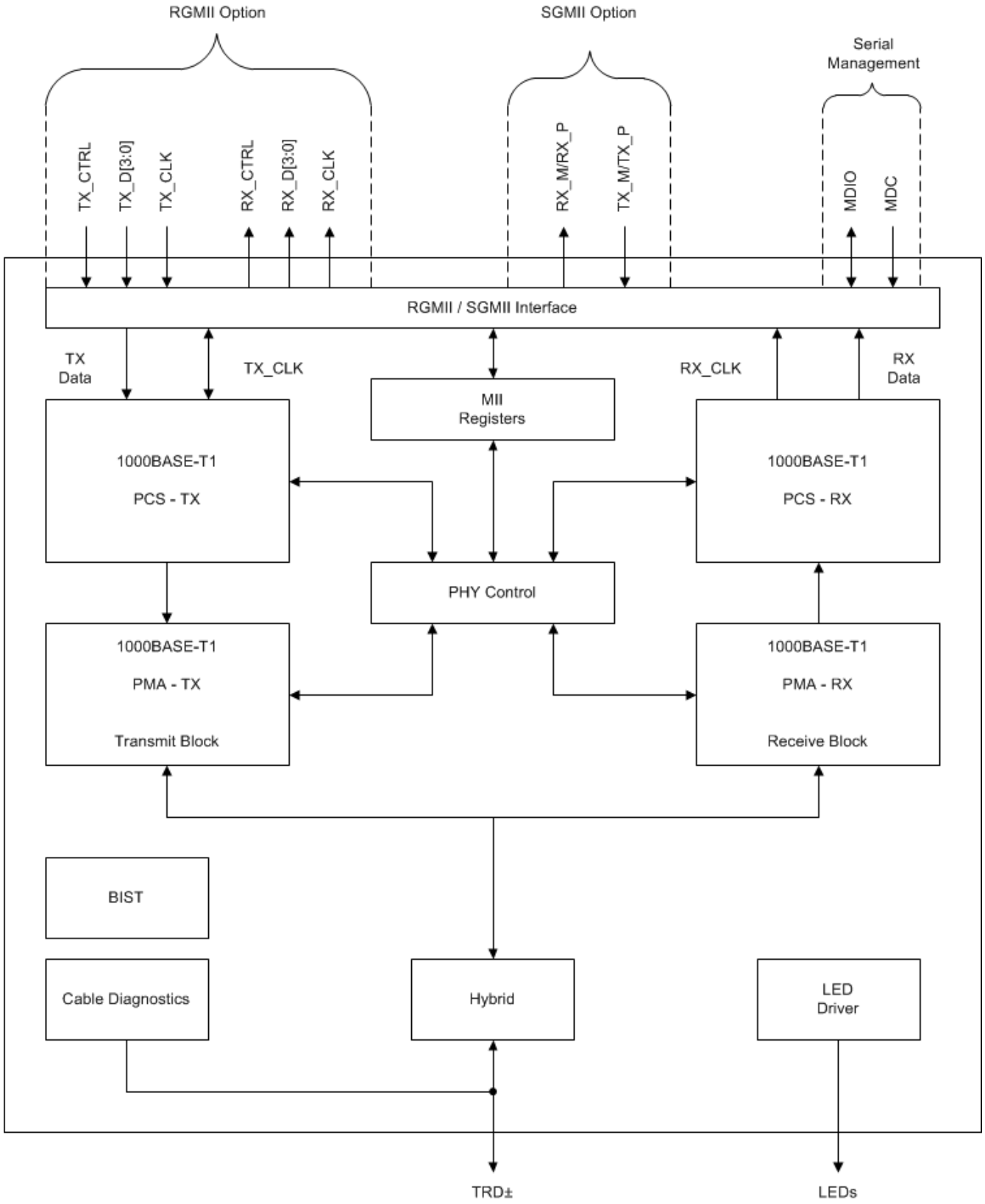

Figure 7-1. DP83TG720S-Q1 Functional Block Diagram

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7.3 Feature Description

7.3.1 Diagnostic Tool Kit

The DP83TG720S-Q1 diagnostic tool kit provides mechanisms for monitoring normal operation, device-level debugging, system-level debugging, fault detection, and compliance testing. This tool kit includes a built-in self-test with PRBS data, various loopback modes, Signal Quality Indicator (SQI), Time Domain Reflectometry (TDR), voltage monitor, temperature monitor, electrostatic discharge monitor, and IEEE 802.3bp test modes.

7.3.1.1 Signal Quality Indicator

When the DP83TG720S-Q1 is active, the Signal Quality Indicator may be used to determine the quality of link based on SNR readings made by the device. SQI is presented as a eight-level indication based on the calculated SNR value. Signal quality indication is accessible through the bits [3:1] of register<0x0871>.

SQI is continuously monitored by the DP83TG720S-Q1 to allow for real-time link signal quality status.

7.3.1.2 Time Domain Reflectometry

Time domain reflectometry helps detecting and estimating the location of OPEN and SHORT faults along a cable.

TDR is activated by setting bit[15] = 'b1 in the register[0x001E]. When TDR diagnostic process gets completed successfully, Bit[1:0] of register[0x001E] will become 'b10. After this status change, TDR results can be read in the register of following table.

Table 7-1. TDR Result Registers : 0x030F

Register Bits	Description
[1:0]	• 01 = TDR Activation • 10 = TDR On • 00,11 = TDR Not Available
[3:2]	Reserved
[7:4]	• 0011 = Short • 0110 = Open • 0101 = Noise • 0111 = Cable OK • 1000 = Test in progress; initial value with TDR ON • 1101 = Test not possible (e.g. noise; active link) • Other values are not valid
[13:8]	• Fault distance = Value in decimal of [13:8] • 'b111111 = Resolution not possible/out of distance
[15:14]	Reserved

Note

TDR should not be run if the link is already active. Running TDR on active line can make TDR fail and also can result in disruption of link.

7.3.1.3 Built-In Self-Test For Datapath

The DP83TG720S-Q1 incorporates a data-path's Built-In-Self-Test (BIST) to check the PHY level and system level data-paths. BIST has following integrated features which make the system level data transfer tests (through-put etc) and diagnostics possible without relying on MAC or external data generator hardware/software.

1. Loopback modes
2. Data generator
   a. Customizable MAC packets generator.
   b. Transmitted packet counter.
   c. PRBS stream generator.

3. Data checker
   a. Received MAC packets error checker.
   b. Received packet counter: Counts total packets received and packets received with errors.
   c. PRBS lock and PRBS error checker.

7.3.1.3.1 Loopback Modes

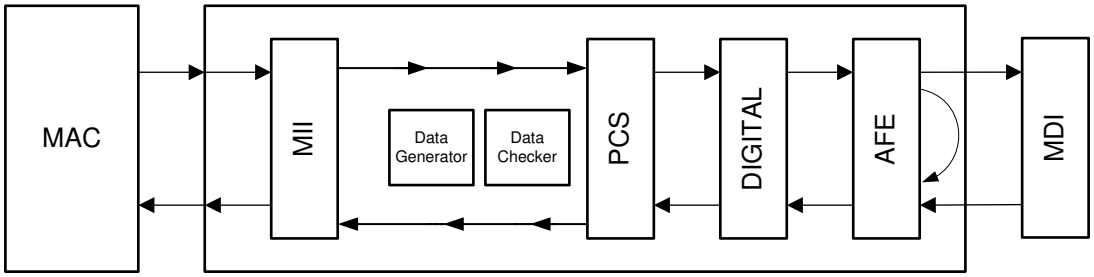

Figure 7-2. All Loopbacks

There are several loopback options within the DP83TG720S-Q1. Enabling different loopback modes enables/ bypass different data-paths according to system verification requirements. Different loopbacks can be enabled along-side following data generation options :

a. Inbuilt data-generator

b. External data-generator (on Ethernet cable or MAC side)

Following diagrams illustrate data-flow during different loopback options :

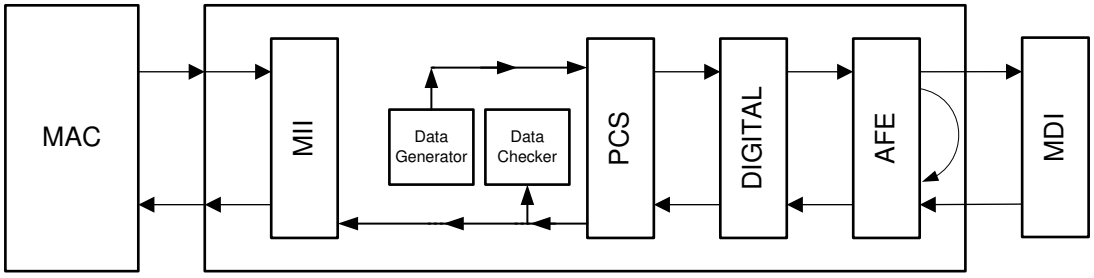

Figure 7-3. Analog Loopback With Inbuilt Data-Gen

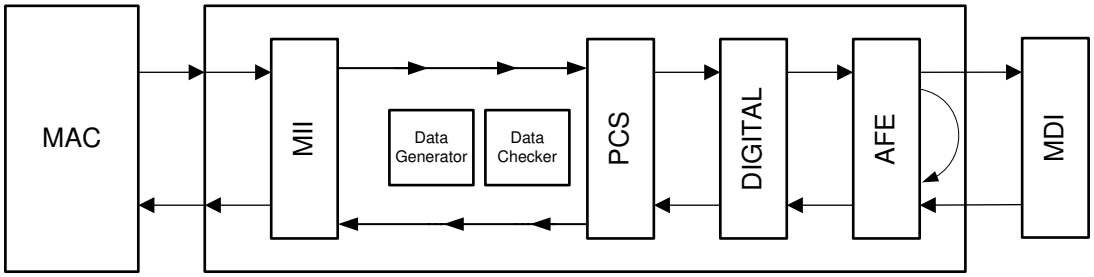

Figure 7-4. Analog Loopback With External Data-Gen

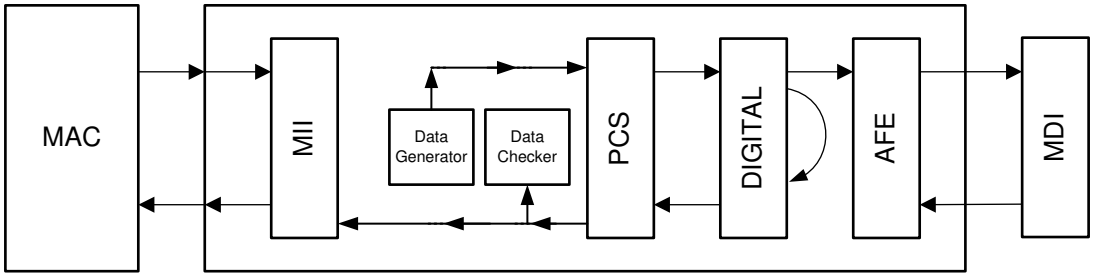

Figure 7-5. Digital Loopback With Inbuilt Data-Gen

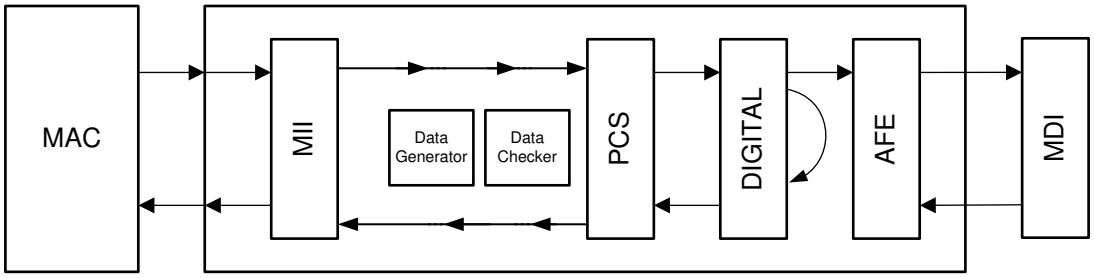

Figure 7-6. Digital Loopback With External Data-Gen

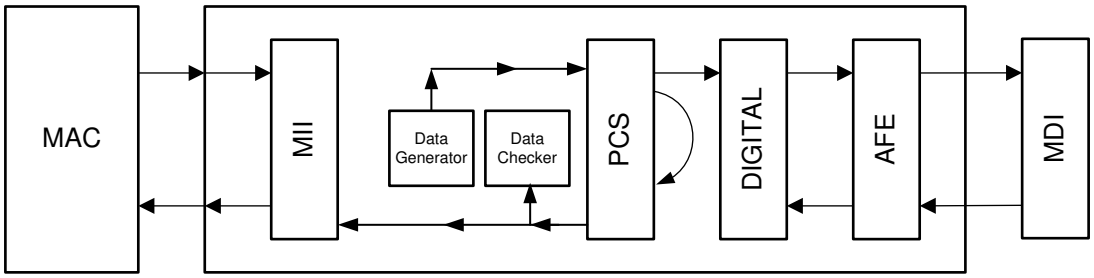

Figure 7-7. PCS Loopback With Inbuilt Data-Gen

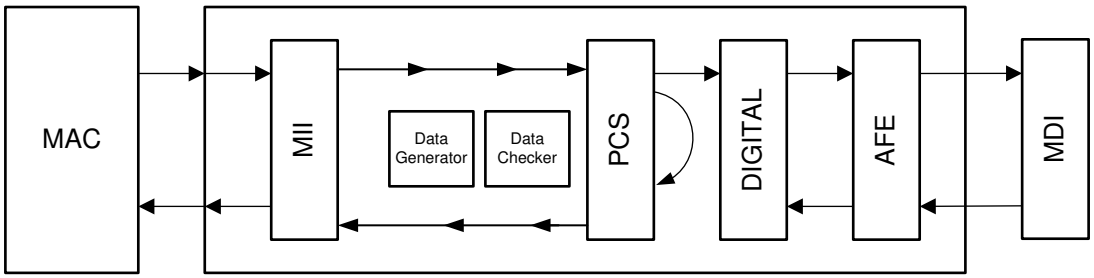

Figure 7-8. PCS Loopback With External Data-Gen

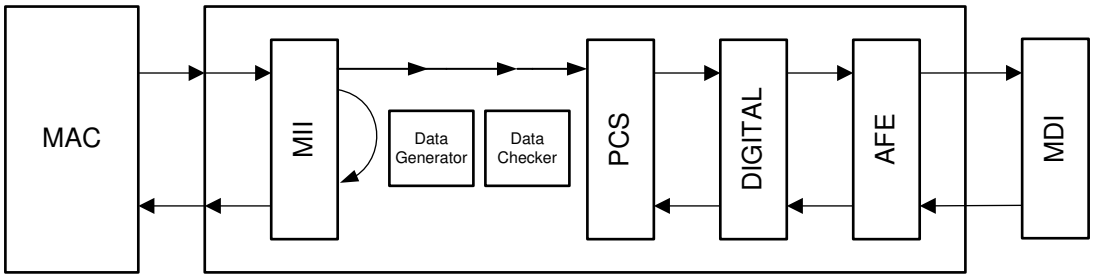

Figure 7-9. xMII Loopback With External Data-Gen

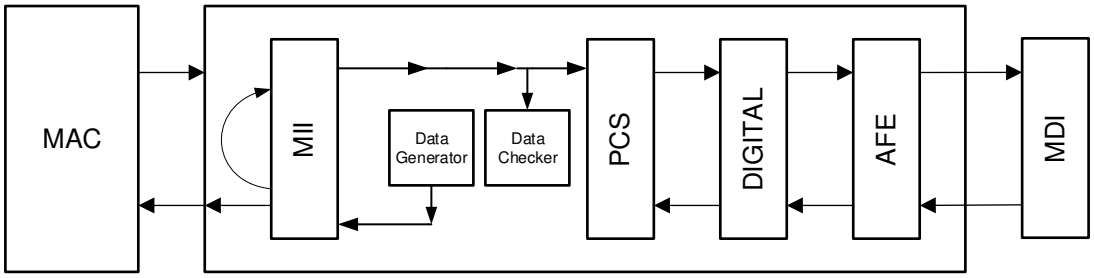

Figure 7-10. xMII Reverse Loopback With Inbuilt Data-Gen

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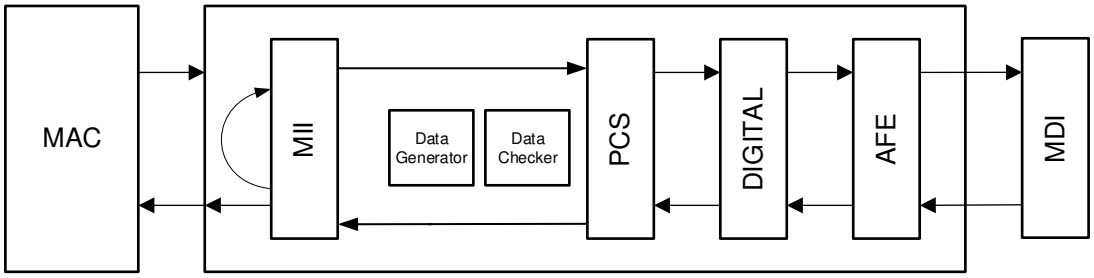

Figure 7-11. xMII Reverse Loopback With External Data-Gen

7.3.1.3.2 Data Generator

Data generator can be programmed to generate either user defined MAC packets or PRBS stream.

Following parameters of generated MAC packets can be configured (refer to registers<0x061B>,register<0x061A> and register<0x0624> for required configuration) :

- Packet Length
- Inter-packet gap
- Defined number of packets to be sent or continuous transmission
- Packet data-type : Incremental/Fixed/PRBS
- Number of valid bytes per packet

7.3.1.3.3 Programming Datapath BIST

Following register settings enable different loopbacks, data genaration and data checker procedures :

Table 7-2. Datapath BIST Programming

	Loopback Mode	To enable loopback mode	To enable data generator and checker : MAC packets	To check in-coming MAC packets status	To enable data generator and checker : PRBS stream	To check in-coming PRBS status : PRBS stream	Other care-abouts
1	Analog loopback	• write : reg[0x0016]=0x0008 • write: reg[0x0405]=0x2800	• write : reg[0x0619]=0x1555 • write : reg[0x0624]=0x55BF	• read : reg[0x063C] for (15:0) of total received packets count. • read : reg[0x063D] for (31:16) of total received packets count. • read : reg[0x063E] for Packets received with CRC errors	• write : reg[0x0619]=0x0557 • write : reg[0x0624]=0x55BF	Step 1 : write : reg[0x0620](1) = 1'b1 Step 2 : • read : reg[0x0620](7:0) = Number of error bytes received. • read : reg[0x0620](8) (1 indicates PRBS data is coming in and checker is locked)	• Disconnect the cable/ link-partner. • Generated data will be going to MAC side, to disable MAC side : write reg[0x0000]=0x0540
2	Digital loopback	• write : reg[0x0016] = 0x0004	• write : reg[0x0619]=0x1555 • write : reg[0x0624]=0x55BF	• read : reg[0x063C] = [15:0] of total received packets count. • read : reg[0x063D]= [31:16] of total received packets count. • read : reg<0x063E> -> Packets received with CRC errors	• write : reg[0x0619]=0x0557 • write : reg[0x0624]=0x55BF	Step 1 : write : reg[0x0620][1] = 1'b1 Step 2 : • read : reg[0x0620][7:0] = Number of error bytes received. • read : reg[0x0620][8] (1 indicates PRBS data is coming in and checker is locked)	• Generated data will be going to Cu cable side, to disable this transmission : write reg[0x041F] = 0x1000 • Generated data will be going to MAC side, to disable MAC side : write reg[0x0000]=0x0540

Table 7-2. Datapath BIST Programming (continued)

	Loopback Mode	To enable loopback mode	To enable data generator and checker : MAC packets	To check in-coming MAC packets status	To enable data generator and checker : PRBS stream	To check in-coming PRBS status : PRBS stream	Other care-abouts
3	PCS loopback	• write : reg<0x0016 > = 0x0001	• write : reg[0x0619]=0x1555 • write : reg[0x0624]=0x55BF	• read : reg[0x063C]= [15:0] of total received packets count. • read : reg[0x063D]= [31:16] of total received packets count. • read : reg[0x063E]= Packets received with CRC errors	• write : reg[0x0619]=0x0557 • write : reg[0x0624]=0x55BF	Step 1 : write : reg[0x0620][1] = 1'b1 Step 2 : • read : reg[0x0620] [7:0] = Number of error bytes received. • read : reg[0x0620] [8] (1 indicates PRBS data is coming in and checker is locked)	• Generated data will be going to Cu cable side, to disable this transmissio n : write reg[0x041F] = 0x1000 • Generated data will be going to MAC side, to disable MAC side : write reg[0x0000]=0x0540
4	RGMII loopback	• write : reg<0x0000 > = 0x4140	• Data is generated externally at Rgmii TX pins • Write : reg[0x0619]= 0x1004	• Data can be verified at Rgmii RX pins. • Packet errors can additionaly be checked internally by : – read : reg[0x0 63C]= [15:0] of total receive d packets count. – read : reg[0x0 63D] = [31:16] of total receive d packets count. – read : reg[0x0 63E]= Packets receive d with CRC errors	• Data is generated externally at Rgmii Tx pins.	• Not applicable as data is external. • PRBS stream checker works only with internal data generator.	• Generated data will be going to Cu cable side, to disable this transmissio n : write reg[0x041F] = 0x1000

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Table 7-2. Datapath BIST Programming (continued)

	Loopback Mode	To enable loopback mode	To enable data generator and checker : MAC packets	To check in-coming MAC packets status	To enable data generator and checker : PRBS stream	To check in-coming PRBS status : PRBS stream	Other care-abouts
5	SGMII loopback	• write : reg[0x0000] = 0x4140	• Data is generated externally at Sgmii TX pins • Write : reg[0x0619] = 0x1114	• Data can be verified at Sgmii RX pins. • Packet errors can additionaly be checked internally by : – read : reg[0x063C]= [15:0] of total received packets count. – read : reg[0x063D] = [31:16] of total received packets count. – read : reg[0x063E] = Packets received with CRC errors	• Data is generated externally at Sgmii Tx pins.	• Not applicable as data is external. • PRBS stream checker works only with internal data generator.	• Generated data will be going to Cu cable side, to disable this transmission : write reg[0x041F] = 0x1000
6	RGMII Reverse loopback	• write : reg[0x0016] = 0x0010	• write : reg[0x0619]=0x1005 • write : reg[0x0624]=0x55BF	• read : reg[0x063C] = [15:0] of total received packets count. • read : reg[0x063D] = [31:16] of total received packets count. • read : reg[0x063E] = Packets received with CRC errors	• write : reg[0x0619]=0x0557 • write : reg[0x0624]=0x55BF	Step 1 : write : reg[0x0620][1] = 1'b1 Step 2 : • read : reg[0x0620][7:0] = Number of error bytes received. • read : reg[0x0620][8] (1 indicates PRBS data is coming in and checker is locked)	• Generated data will be going to Cu cable side, to disable this transmission : write reg[0x041F] = 0x1000

Table 7-2. Datapath BIST Programming (continued)

	Loopback Mode	To enable loopback mode	To enable data generator and checker : MAC packets	To check in-coming MAC packets status	To enable data generator and checker : PRBS stream	To check in-coming PRBS status : PRBS stream	Other care-abouts
7	SGMII Reverse loopback	• write : reg[0x042C] = 0x0010	• write : reg[0x0619]=0x1115 • write : reg[0x0624]=0x55BF	• read : reg[0x063C] for [15:0] of total received packets count. • read : reg[0x063D] for [31:16] of total received packets count. • read : reg[0x063E] for Packets received with CRC errors	• write : reg[0x0619]=0x0557 • write : reg[0x0624]=0x55BF	Step 1 : write : reg[0x0620][1] = 1'b1 Step 2 : • read : reg[0x0620][7:0] for Number of error bytes received. • read : reg[0x0620][8] (1 indicates PRBS data is coming in and checker is locked)	• Generated data will be going to Cu cable side, to disable this transmission : write reg[0x041F] = 0x1000

Note : Different MAC packet parameters can be further configured with register[0x061B] and register[0x0624]

7.3.1.4 Temperature and Voltage Sensing

Temperature sensor of PHY can be used to give the indication of the temperature of the system and reading can be taken on the fly by reading the temperature sensor output register.

Voltage sensor senses the voltage of all the supply pins : vdda, vddio and vdd1p0. Each pins active voltage can be sensed by reading the corresponding voltage sensor output register.

All sensors are always active and monitor state machine polls the value of each sensor periodically. Monitor state machine can be further programmed to give higher priority/sampling time to one sensor over another by using MONITOR_CTRL_3 register.

Following software sequence can be used to read out any sensor's output :

- Step1 : Program register[0x0467] = 0x6004 ; Initial configuration of monitors
- Step 2 : Program register [0x046A] = 0x00A6 and then register [0x046A]=0x00A3; Refresh the monitors
- Step 3 : Program register[0x0468] to select the corresponding sensor to be polled and read register [0x047B] [14:7] for selected sensor's output code.
- Step 4 : Feed the values of read sensor's output code (in decimal) in following equations to get the sensor's output value in decimals. Refer to Sensor Select Table for required value of constants to be used in equations :
  - vdda_value = 3.3 + (vdda_output_code - vdda_output_mean_code)*slope_vdda_sensor
  - vdd1p0_value = 1.0 + (vdd1p0_output_code - vdd1p0_ouput_mean_code)*slope_vdd1p0_sensor
  - vddio_calculated = 3.3 + (vddio_ouput_code - vddio_output_mean_code)*slope_vddio_sensor
  - temperature_calculated = 25 + (temperature_output_code - temperature_output_mean_code)*slope_temperature_sensor

Table 7-3. Sensor Select Table

Register[0x0468]	Sensor Selected To Read-out
0x1920	VDDA Voltage Sensor
0x2920	VDD1P0 Voltage Sensor
0x3920	VDDIO Voltage Sensor

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Table 7-3. Sensor Select Table (continued)

Register[0x0468]	Sensor Selected To Read-out
0x4920	Temperature Sensor

Table 7-4. Sensor's Constant Values

Constant	Value (in decimal)
vdda_output_mean_code	128
slope_vdda3p3_sensor	8.63014e-3
vdd1p0_output_mean_code	93
slope_vdd1p0_sensor	2.85714e-3
vddio_output_mean_code	224
slope_vddio_sensor	15.686e-3
temperature_output_mean_code	161
slope_temperature_sensor	1.5

Note

Accuracy of temperature sensor can be maximized (3degreeC for temperature < 105C and 7.5 degreeC for temperature > 105C), if customer can sample "temperature_output_code" at 25C and use it as "temperature_output_mean_code".

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7.3.1.5 Electrostatic Discharge Sensing

Electrostatic discharge is a serious issue for electronic circuits and if not properly mitigated can create short-term issues (signal integrity, link drops, packet loss) as well as long-term reliability faults. The DP83TG720S-Q1 has robust integrated ESD circuitry and offers an ESD sensing architecture. ESD events can be detected on MDI pins for further analysis and debug.

The ESD sensing tool is useful for both prototyping and end-applications. Additionally, the DP83TG720S-Q1 provides an interrupt status flag; when an ESD event is logged in the register<0x0442>. Hardware and software resets are ignored by the ESDS register to prevent unwarranted clearing.

Table 7-5. ESD Sensing : Interrupt Setting and Count Reading

Function	Required Read/Write
Interrupt Enable	• Write register<0x0012>[3] = 1
ESD Event Counter	• Read register<0x0442>[14:9] • Value in decimal indicates the ESD strikes since power-up.

7.3.2 Compliance Test Modes

The six test modes for the DP83TG720S-Q1 are compliant to IEEE 802.3bp, Sub-clause 97.5.2. Supported test modes allow testing of the transmitter waveform Power Spectral Density (PSD) mask, distortion, MDI Master jitter, MDI Slave jitter, droop, transmitter frequency, frequency tolerance, BER monitoring, return loss, and mode conversion. Any of the three GPIOs can be used to output TX_TCLK for MDI Slave jitter measurement.

7.3.2.1 Test Mode 1

Test mode 1 tests the transmitter clock jitter when linked to a partner. In test mode 1, the DP83TG720S-Q1 PHYs are connected over link segment defined in section 97.6 within IEEE 802.3bp. TX_TCLK125 is a divided clock derived from TX_TCLK, which is one sixth the frequency.

7.3.2.2 Test Mode 2

Test mode 2 tests the transmitter MDI Master mode jitter. In test mode 2, the DP83TG720S-Q1 will transmit a continuous pattern of three {+1} symbols followed by three {-1} symbols. The transmitted symbols are timed from the 750-MHz source, which results in a 125-MHz signal.

7.3.2.3 Test Mode 4

Test mode 4 tests the transmitter distortion. In test mode 4, the DP83TG720S-Q1 will transmit the sequence of symbols generated by Equation 1:

$$g(x) = 1 + x^9 + x^{11} \quad (1)$$

The bit sequences, x0n and x1n, are generated from combinations of the scrambler in accordance to and :

$$'x0_n = Scr_n[0] \quad (2)$$

$$x1_n = Scr_n[1] \wedge Scr_n[4] \quad (3)$$

$$x2_n = Scr_n[1] \wedge Scr_n[5] \quad (4)$$

Example streams of the 3-bit nibbles are shown in Table 7-6.

Table 7-6. Transmitter Test Mode 4 Symbol Mapping

x2n	x1n	x0n	T1n	T0n
0	0	0	-1	-1
0	0	1	0	-1
0	1	0	-1	0
0	1	1	-1	+1
1	0	0	+1	0
1	0	1	+1	-1
1	1	0	+1	+1
1	1	1	0	+1

7.3.2.4 Test Mode 5

Test mode 5 tests the transmitter PSD mask. In test mode 5, the DP83TG720S-Q1 will transmit normal Inter-Frame IDLE PAM3 symbols.

7.3.2.5 Test Mode 6

Test mode 6 tests the transmitter droop. In test mode 6, the DP83TG720S-Q1 transmits fifteen {+1} symbols followed by fifteen {-1} symbols with symbol transmission at 750-MHz. This 25-MHz pattern is repeated continuously until the test mode is disabled.

7.3.2.6 Test Mode 7

Test mode 7 enabled bit error rate measurement on a link segment. This mode uses zero data pattern on the MDI to check BER by comparing an expected zero data pattern to any non-zero bit received. Error checking is performed after FEC and 80B/81B decoding.

Table 7-7. Test Mode Register Setting

MMD	Register	Value	Test Mode
MMD1	0x0904	0x2000	Test Mode 1 : Tx_Tclk 125MHz is routed to clkout pin.
MMD1	0x0904	0x4000	Test Mode 2
MMD1	0x0904	0x8000	Test Mode 4 : Tx_Tclk 125MHz is routed to clkout pin.
MMD1F	0x0453	0x0019	
MMD1	0x0904	0xA000	Test Mode 5
MMD1	0x0904	0xC000	Test Mode 6
MMD1	0x0904	0xE000	Test Mode 7

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7.4 Device Functional Modes

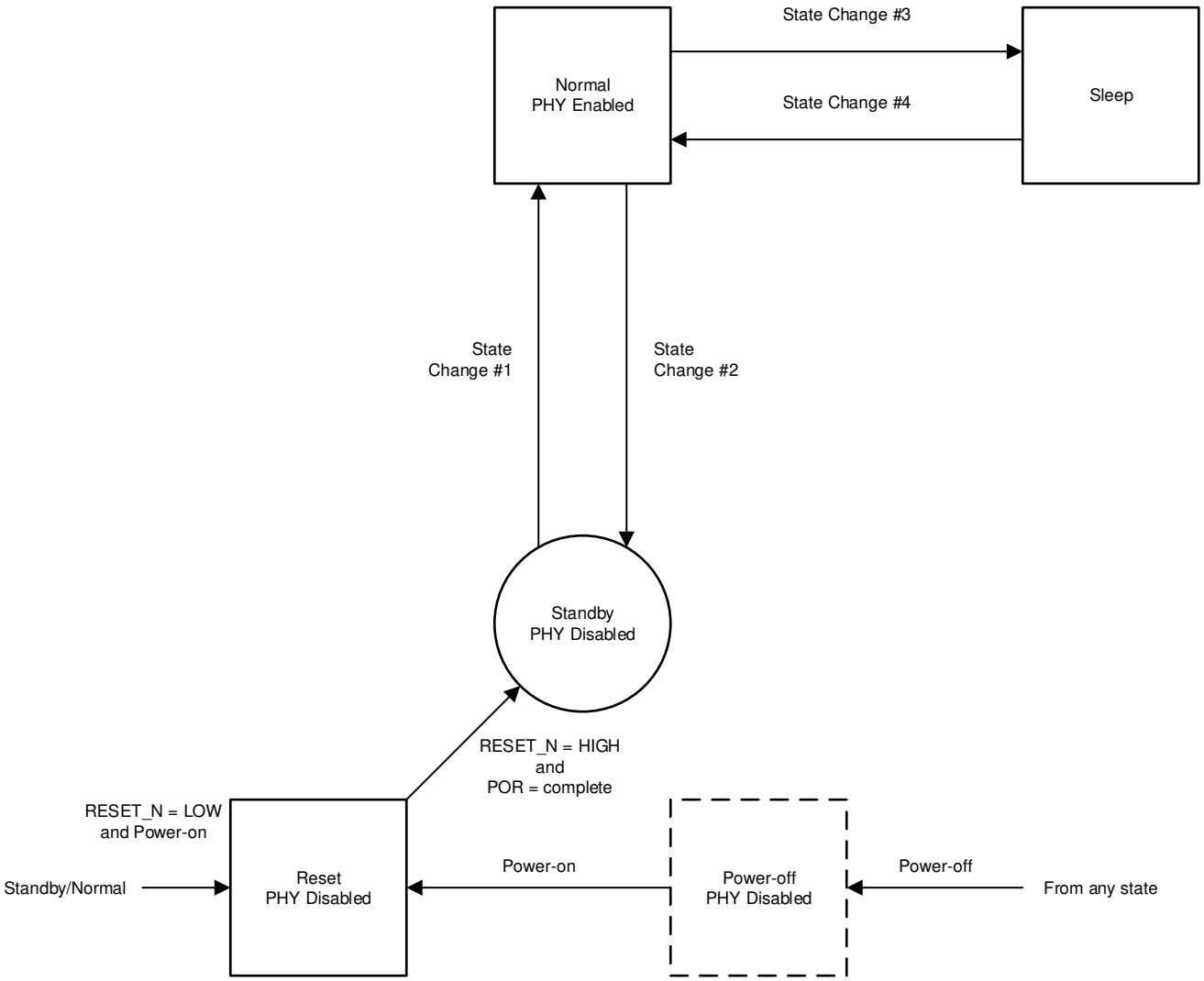

Figure 7-12. PHY Operation State Diagram

7.4.1 Power Down

When VDDA3P3 or VDDIO or VDD1P0 is below the POR threshold, the DP83TG720S-Q1 is in a power-down state. All digital IOs will remain in high impedance state and analog blocks are disabled. PMA termination is not present when in power-down.

7.4.2 Reset

Reset is activated upon power-up, when RESET_N is pulled LOW (for the minimum reset pulse time) or if hardware reset is initiated by setting bit[15] in the register[0x001F].

- Digital state machine restarts after reset and all the register settings are cleared to the boot-up state.
- 25MHz clock on clkout pin will remain active during reset state also.
- MDI/PMA will not have termination during reset state.

Note

Straps are re-latched only with pin reset and not by hardware reset through register (register [0x001F] = x8000.

7.4.3 Standby

The device (MDI Master mode or MDI Slave mode) automatically enters into standby post power-up and reset so long that the device is bootstrapped for managed operation.

In standby, all PHY functions are operational except for PCS and PMA blocks. Link establishment is not possible in standby and data cannot be transmitted or received. SMI functions are operational and register configurations are maintained.

If the device is configured for autonomous operation through bootstrap setting, the PHY automatically switches to normal operation once powered on and reset complete.

7.4.4 Normal

Normal mode can be entered from either autonomous or managed operation. When in autonomous operation, the PHY will automatically try to establish link with a valid Link Partner once powered on.

In managed operation, SMI access is required to allow the device to exit standby; commands issued through the SMI allow the device to exit standby and enables both the PCS and PMA blocks. All device features are operational in normal mode.

Autonomous operation can be enabled through SMI access by setting bit[6] in register 0x18B.

7.4.5 Sleep

Once in sleep mode, all PHY blocks are disabled except for energy detection. All register configurations are lost in sleep mode. No link can be established, data cannot be transmitted or received and SMI access is not available when in sleep mode.

To use sleep mode of PHY refer to implementation highlighted in following figure.

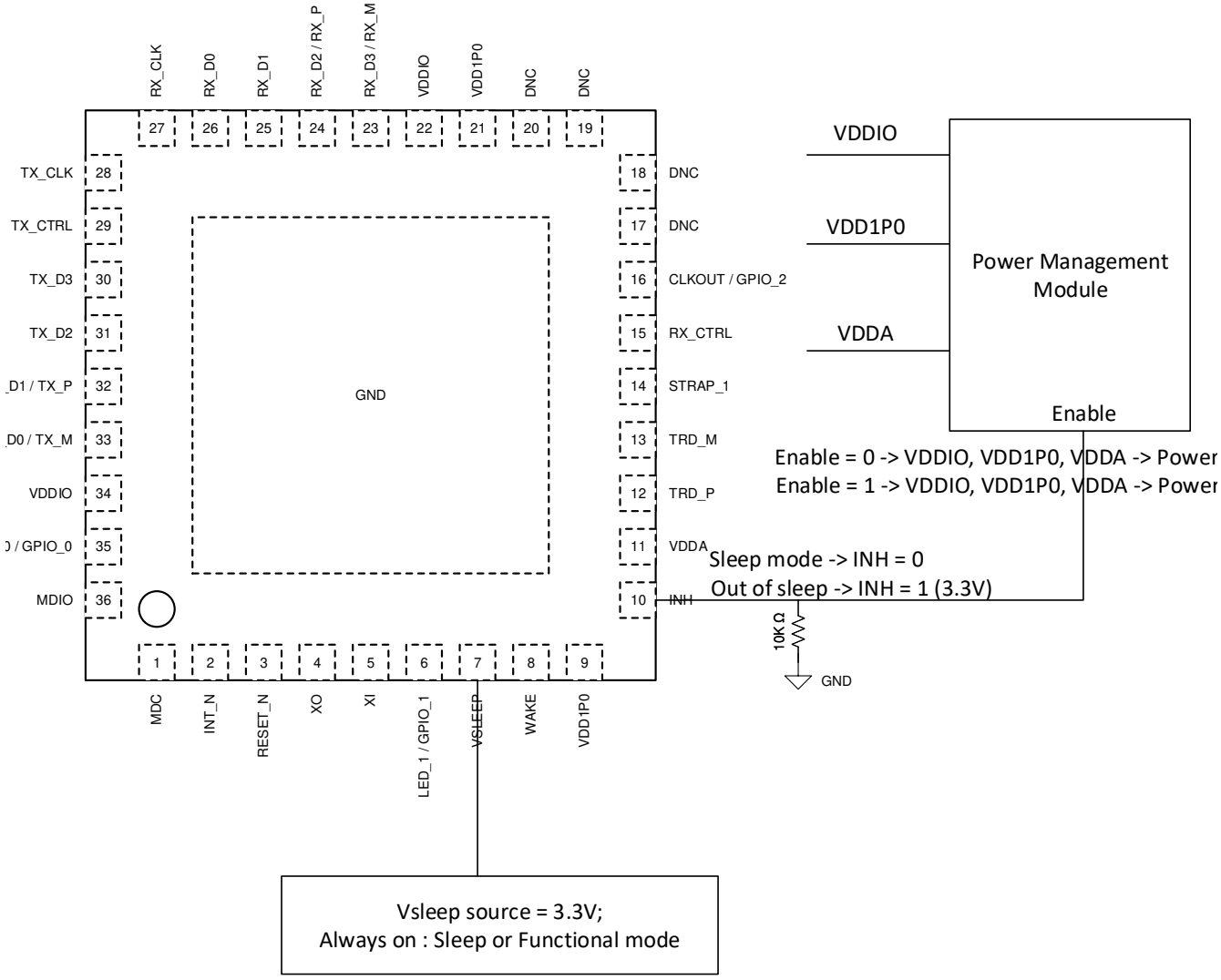

Figure 7-13. Required Implementation for Sleep Mode

Note

Phy will not go into sleep mode if supply sources are not disabled as per above figure.

7.4.6 State Transitions

7.4.6.1 State Transition #1 - Standby to Normal

Autonomous Operation: The PHY will automatically transition to Normal state upon POR completion.

Managed Operation: The PHY will transition to Normal state out of Standby only after writing register <0x018C> = 0x001.

7.4.6.2 State Transition #2 - Normal to Standby

The PHY can be forced back into Standby when in Normal state by writing register <0x018C> = 0x0010.

7.4.6.3 State Transition #3 - Normal to Sleep

Sleep state can be entered either locally (pin/register-write) or by remote link-partner.

Local sleep entry for Master mode phy :

- Step 1 : Write bit[7] = 'b1 of register[0x0182].
- Step 2 : Make "wake" pin low.

Local sleep entry for Slave mode phy :

- Step 1 : Write bit[8] = 'b0 of register[0x0182] register.
- Step 2 : Write bit[7] = 'b1 of register[0x0182] register.
- Step 3 : Make "wake" pin low.

Remote sleep entry for Master mode phy :

- Master mode phy can not be made to enter sleep mode by link-partner

Remote sleep entry for Slave mode phy :

- Step 1 : Write bit[7] = 'b1 of register[0x0182] register.
- Step 2 : Phy will go into sleep mode with loss of energy on line (when master will go quite : no data, no send-s)

Note

Phy will go into sleep mode only if power supplies are disconnected using INH signal as shown in figure **Required Implementation for Sleep Mode**.

7.4.6.4 State Transition #4 - Sleep to Normal

Sleep state can be exited either locally (pin/register-write) or by remote link-partner.

Local sleep exit for Master mode phy by :

- Making "wake" pin high (3.3V).

Local sleep exit for Slave mode phy by :

- Making "wake" pin high (3.3V).

Remote sleep exit for Master mode phy by :

- Link-partner sending TC-10 compliant wake-up energy.
- Link-partner sending 1000BT1 IEEE compliant training signal : "Send-s".

Remote sleep exit for Slave mode phy by :

- Link-partner sending TC-10 compliant wake-up energy.
- Link-partner sending 1000BT1 IEEE compliant training signal : "Send-s".

7.4.7 Media Dependent Interface

7.4.7.1 MDI Master and MDI Slave Configuration

MDI Master and MDI Slave are configured using either hardware bootstraps or through register access.

LED_0 controls the MDI Master and MDI Slave bootstrap configuration. By default, MDI Slave mode is configured because there is an internal pulldown resistor on LED_0 pin. If MDI Master mode configuration through hardware bootstrap is preferred, an external pullup resistor is required.

Additionally, bit[14] in the PMA_CTRL2 egister controls the MDI Master and MDI Slave configuration. When this bit is set, MDI Master mode is enabled.

7.4.7.2 Auto-Polarity Detection and Correction

During the link training process, the DP83TG720S-Q1 as MDI receiver is able to detect polarity reversal and automatically correct for the error. Both master and slave detects and do the required correction in the receiver polarity.

7.4.8 MAC Interfaces

7.4.8.1 Reduced Gigabit Media Independent Interface

The DP83TG720S-Q1 also supports Reduced Gigabit Media Independent Interface (RGMII) as specified by RGMII version 2.0. RGMII is designed to reduce the number of pins required to connect MAC and PHY. To

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accomplish this goal, the control signals are multiplexed. Both rising and falling edges of the clock are used to sample the control signal pin on transmit and receive paths. For 1-Gbps operation, RX_CLK and TX_CLK operate at 125 MHz.

The RGMII signals are summarized in Table 7-8:

Table 7-8. RGMII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Control Signals	TX_CTRL
	RX_CTRL
Clock Signals	TX_CLK
	RX_CLK

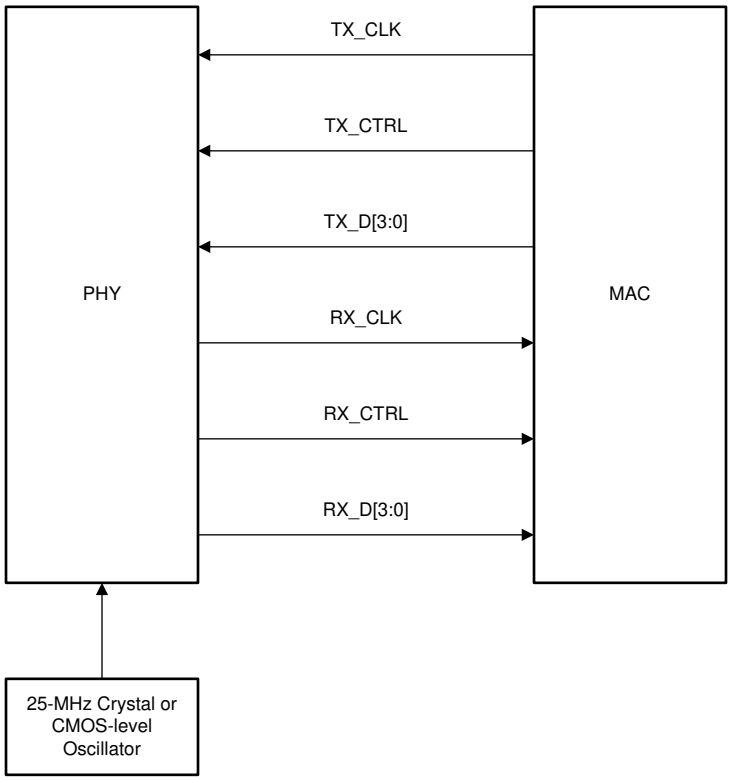

Figure 7-14. RGMII Connections

Table 7-9. RGMII Transmit Encoding

TX_CTRL (POSITIVE EDGE)	TX_CTRL (NEGATIVE EDGE)	TX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000 through 1111	Reserved
1	0	0000 through 1111	Normal Data Transmission
1	1	0000 through 1111	Transmit Error Propagation

Table 7-10. RGMII Receive Encoding

RX_CTRL (POSITIVE EDGE)	RX_CTRL (NEGATIVE EDGE)	RX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000 through 1101	Reserved
0	1	1110	False Carrier Indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal Data Reception
1	1	0000 through 1111	Data Reception with Errors

The DP83TG720S-Q1 supports in-band status indication to help simplify link status detection. Inter-frame signals on RX_D[3:0] pins as specified in Table 7-11.

Table 7-11. RGMII In-Band Status

RX_CTRL	RX_D3	RX_D[2:1]	RX_D0
0 **Note:** In-band status is only valid when RX_CTRL is low	**Duplex Status:** 0 = Half-Duplex 1 = Full-Duplex	**RX_CLK Clock Speed:** 00 = 2.5 MHz 01 = 25 MHz 10 = 125 MHz 11 = Reserved	**Link Status:** 0 = Link not established 1 = Valid link established

RGMII MAC Interface for Gigabit Ethernet has stringent timing requirements to meet system level performance. To meet these timing requirements and to operate with different MACs over RGMII, it is advised to take the following requirements into consideration when designing PCB. It is also recommended to check board level signal integrity by using the DP83TG720 IBIS model.

RGMII-TX Requirements

- RGMII TX signals should be routed on board with control impedance of 50Ohm +/-15%.
- Max routing length should be limited to 5inch for better signal integrity performance.
- Figure 7-15 shows a RGMII interface requirements for TX* signals. MAC RGMII driver output impedance should be 50Ohm+/-20%.
- Skew for all RGMII TX signals at TP2, in Figure 7-15, should be <±500ps.
- Signal Integrity at TP1 and TP2, in Figure 7-15, should be verified with IBIS model simulation and ensured conformance to following requirements:
  - At TP2, signal should meet rise/fall time of 1ns (20-80%) of signal amplitude.
  - Rise/fall time should be monotonic between VIH/VIL level at TP2.

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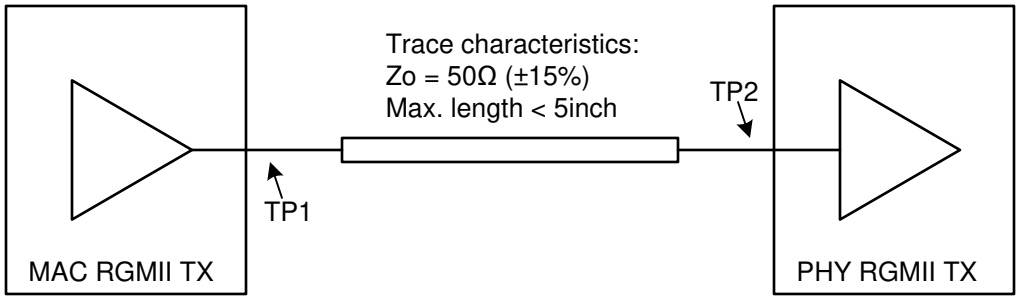

Figure 7-15. RGMII TX Requirements

RGMII-RX Requirements

- RGMII RX signals should be routed on board with control impedance of 50Ohm +/-15%.
- Max routing length should be limited to 5inch for better signal integrity performance.
- No damping resistors should be added at TP3/TP4, in Figure 7-16, as that will impact signal integrity of RX signals.
- Figure 7-16 shows a RGMII interface requirements for RX* signals. MAC RGMII driver output impedance should be 50Ohm+/-20%.
- Signal Integrity at TP3 and TP4, in Figure 7-16, should be verified with IBIS model simulation and ensured conformance to following requirements:
  - At TP4, signal should meet rise/fall time of 1ns (20-80%) of signal amplitude.
  - Rise/fall time should be monotonic between VIH/VIL level at TP4.

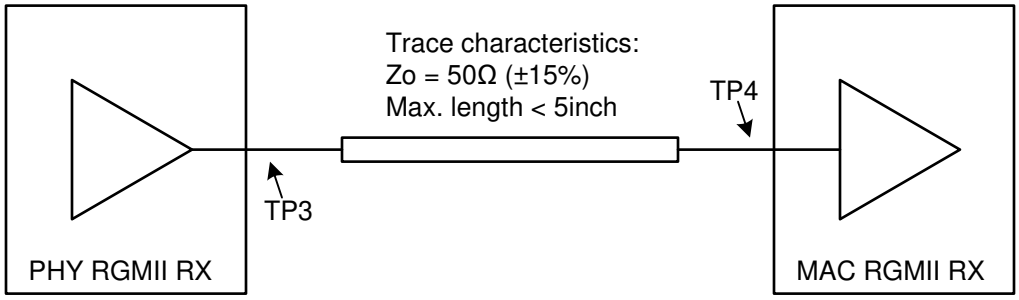

Figure 7-16. RGMII RX Requirements

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7.4.8.2 Serial Gigabit Media Independent Interface

The Serial Gigabit Media Independent Interface (SGMII) provides a means for data transfer between MAC and PHY with significantly less signal pins (4 pins) compared to RGMII (12 pins). SGMII uses low-voltage differential signaling (LVDS) to reduce emissions and improve signal quality.

The DP83TG720S-Q1 SGMII is capable of operating in 4-wire mode. In 4-wire operation, two differential pairs are used to transmit and receive data. Clock and data recovery are performed in the MAC and in the PHY in the case of the RX and TX directions, respectively.

SGMII Auto-Negotitation can be disabled by setting bit[0] = 0b0 in the SGMII Configuration Register (SGMIICTL, address 0x608).

The SGMII signals are summarized in Table 7-12.

Table 7-12. SGMII Signals

FUNCTION	PINS
Data Signals	TX_M, TX_P
	RX_M, RX_P

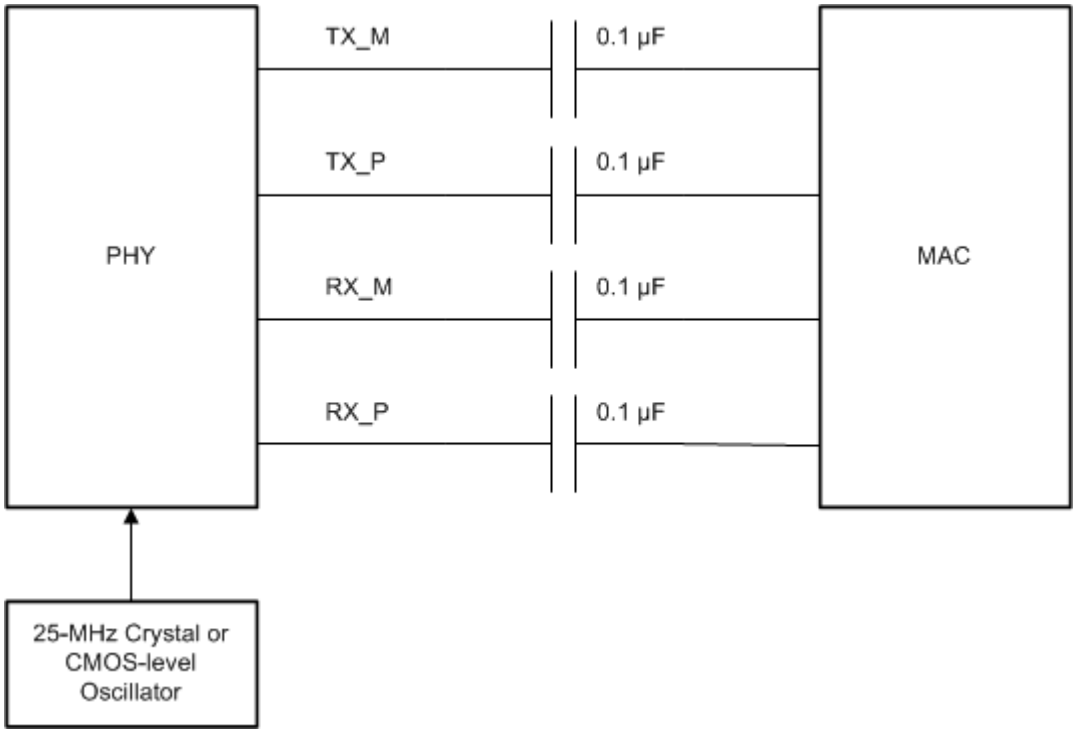

Figure 7-17. SGMII Connections

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7.4.9 Serial Management Interface

The Serial Management Interface provides access to the DP83TG720S-Q1 internal register space for status information and configuration. The SMI is compatible with IEEE 802.3 clause 22. The implemented register set consists of the registers required by the IEEE 802.3 plus several others to provide additional visibility and controllability of the DP83TG720S-Q1.

The SMI includes the management clock (MDC) and the management input and output data pin (MDIO). MDC is sourced by the external management entity, also called Station (STA). MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC. MDIO pin requires a pullup resistor (2.2 KΩ), which pulls MDIO high during IDLE and turnaround.

Up to 9 DP83TG720S-Q1 PHYs can share a common SMI bus. To distinguish between the PHYs, a 3-bit address is used. During power-up-reset, the DP83TG720S-Q1 latches the PHY_AD configuration pins to determine its address.

The management entity must not start an SMI transaction in the first cycle after power-up-reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after hard reset is deasserted. In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device may actively drive the MDIO signal during the first bit of turnaround. The addressed DP83TG720S-Q1 drives the MDIO with a zero for the second bit of turnaround and follows this with the required data.

For write transactions, the station-management entity writes data to the addressed DP83TG720S-Q1, thus eliminating the requirement for MDIO Turnaround. The turnaround time is filled by the management entity by inserting <10>.

Table 7-13. SMI Protocol Structure

SMI PROTOCOL	<idle> <start> <op code> <device address> <reg address> <turnaround> <data> <idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><XXXX XXXX XXXX XXXX><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><XXXX XXXX XXXX XXXX><idle>

7.4.10 Direct Register Access

Direct register access can be used for the first 31 registers (0x0h through 0x1Fh).

7.4.11 Extended Register Space Access

The DP83TG720S-Q1 SMI function supports read and write access to the extended register set using registers REGCR (0x000Dh) and ADDAR (0x000Eh) and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah Draft for Clause 22 for accessing the Clause 45 extended register set.

REGCR (0x000Dh) is the MDIO Manageable MMD access control. In general, register REGCR[4:0] is the device address DEVAD that directs any accesses of ADDAR (0x000Eh) register to the appropriate MMD.

The DP83TG720S-Q1 supports 4 MMD device addresses. The 4 MMD register spaces are:

1. DEVAD[4:0] = 11111 (0x1F) is used for IEEE defined registers (0x00 to 0x1F) and vendor specific registers. This register space is called MMD1F
2. DEVAD[4:0] = 00001 (0x01) is used for 100BASE-T1 PMA MMD register accesses. This register space is called MMD1.
3. DEVAD[4:0] = 00011 (0x03) is used for vendor specific registers. This register space is called MMD3
4. DEVAD[4:0] = 00111 (0x07) is used for vendor specific registers. This register space is called MMD7

Table 7-14. MMD Register Space Division

MMD Register Space	Register Address Range
MMD1F	0x000 - 0x0EFD
MMD1	0x1000 - 0x1904
MMD3	0x3000 - 0x390D
MMD7	0x7000 - 0x7200

Note

For MMD1/3/7, most significant nibble of the register address is used to denote the respective MMD space. This should be ignored during actual register access operation. For example to access register 0x1904 use 0x0904 as the register address and x01 as the MMD.

All accesses through register REGCR and ADDAR must use the correct DEVAD. Transactions with other DEVADs are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01), data with post increment on read and writes (10) and data with post increment on writes only (11).

- ADDAR is the address and data MMD register. ADDAR is used in conjunction with REGCR to provide the access to the extended register set. If register REGCR[15:14] is (00), then ADDAR holds the address of the extended address space register. Otherwise, ADDAR holds the data as indicated by the contents of its address register. When REGCR[15:14] is set to (00), accesses to register ADDAR modify the extended register set address register. This address register must always be initialized in order to access any of the registers within the extended register set.
- When REGCR[15:14] is set to (01), accesses to register ADDAR access the register within the extended register set selected by the value in the address register.
- When REGCR[15:14] is set to (10), access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.
- When REGCR[15:14] is set to (11), access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for write access only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR.

7.4.12 Write Address Operation

To set the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the register address to register ADDAR.

Subsequent writes to register ADDAR (step 2) continue to write the address register.

7.4.12.1 Example - Write Address Operation

For writing register addresses within MMD1 field:

1. Write the value 0x0001 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the register address to register ADDAR.

7.4.13 Read Address Operation

To read the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Read the register address from register ADDAR.

Subsequent reads to register ADDAR (step 2) continue to read the address register.

7.4.13.1 Example - Read Address Operation

For reading register addresses within MMD1 field:

1. Write the value 0x0001 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Read the register address from register ADDAR.

7.4.14 Write Operation (No Post Increment)

To write a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = '11111') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register was previously configured.

7.4.14.1 Example - Write Operation (No Post Increment)

To write a register in the MMD1 extended register set:

1. Write the value 0x0001 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x4001 (data, no post increment function field = 01, DEVAD = '00001') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

7.4.15 Read Operation (No Post Increment)

To read a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = '11111') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) continue to reading the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register was previously configured.

7.4.15.1 Example - Read Operation (No Post Increment)

To read a register in the MMD1 extended register set:

1. Write the value 0x0001 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x4001 (data, no post increment function field = 01, DEVAD = '00001') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

7.4.16 Write Operation (Post Increment)

To write a register in the extended register set with post increment:

1. Write the value 0x001F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment function field = 10, DEVAD = '11111') or the value 0xC01F (data, post increment on writes function field = 11, DEVAD = '11111') to register REGCR.

4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) write the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

7.4.16.1 Example - Write Operation (Post Increment)

To write a register in the MMD1 extended register set with post increment:

1. Write the value 0x0001 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x8001 (data, post increment function field = 10, DEVAD = '00001') or the value 0xC001 (data, post increment on writes function field = 11, DEVAD = '00001') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

7.4.17 Read Operation (Post Increment)

To read a register in the extended register set and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x001F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment function field = 10, DEVAD = '11111') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) read the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

7.4.17.1 Example - Read Operation (Post Increment)

To read a register in the MMD1 extended register set and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x0001 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x8001 (data, post increment function field = 10, DEVAD = '00001') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

7.5 Programming

7.5.1 Strap Configuration

The DP83TG720S-Q1 uses functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up and hardware reset (through either the RESET_N pin or register access). The strap pins support 2-levels and 3-levels, which are described in greater detail below. Configuration of the device may be done through strapping or through serial management interface.

Note

Because strap pins are functional pins after reset is deasserted, they should not be connected directly to VCC or GND. Either pullup resistors, pulldown resistors, or both are required for proper operation.

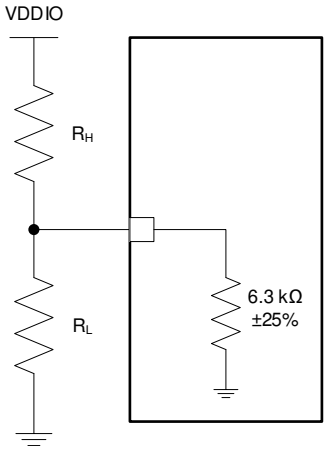

Figure 7-18. 3 Level Strap Circuit

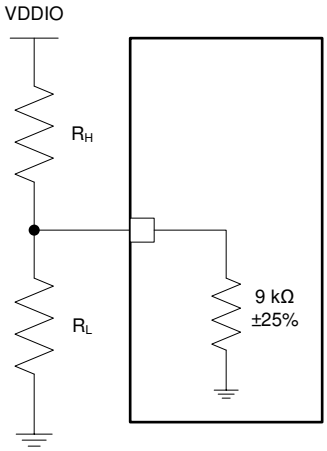

Figure 7-19. 2 Level Strap Circuit

Table 7-15. Recommended 3-level Strap Resistor Ratios

MODE	IDEAL RH (kΩ) for VDDIO = 3.3 V	IDEAL RH (kΩ) for VDDIO = 2.5 V	IDEAL RH (kΩ) for VDDIO = 1.8V
1	OPEN	OPEN	OPEN
2	13	8.5	4
3	4.5	2	0.8

Table 7-16. Recommended 2-level Strap Resistor

MODE	IDEAL RH (kΩ)
1	OPEN
2	2.49

The following table describes the DP83TG720S-Q1 configuration bootstraps:

Table 7-17. 2-level Bootstraps

PIN NAME	PIN NO.	STRAP MODE	STRAP FUNCTION	DESCRIPTION
RX_D0	26	1 (default)	MAC[0] = 0	MAC Interface Selection [0]. Refer to Table 7-18 for full description.
		2	MAC[0] = 1	
RX_D1	25	1 (default)	MAC[1] = 0	MAC Interface Selection [1]. Refer to Table 7-18 for full description.
		2	MAC[1] = 1	
RX_D2	24	1 (default)	MAC[2] = 0	MAC Interface Selection [2]. Refer to Table 7-18 for full description.
		2	MAC[2] = 1	
LED_0	1	1 (default)	MS = 0	MDI Master Slave Select. MS = 0 Slave MS = 1 Master
		2	MS = 1	
LED_1	6	1 (default)	$\overline{\text{AUTO}}$ = 0	Autonomous Disable $\overline{\text{AUTO}}$ = 0 Autonomous $\overline{\text{AUTO}}$ = 1 Managed
		2	$\overline{\text{AUTO}}$ = 1	

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Table 7-18. MAC Interface Selection Bootstraps

MAC[2]	MAC[1]	MAC[0]	DESCRIPTION
0	0	0	SGMII (4-wire)
0	0	1	RESERVED
0	1	0	RESERVED
0	1	1	RESERVED
1	0	0	RGMII (Align Mode)
1	0	1	RGMII (TX Shift Mode)
1	1	0	RGMII (TX and RX Shift Mode)
1	1	1	RGMII (RX Shift Mode)

Table 7-19. 3-Level Bootstrap: PHY Address

PHY_AD[3:0]	RX_CTRL STRAP MODE	STRP_1 STRAP MODE	DESCRIPTION
0000	1	1	PHY Address: 0x0000 (0)
0001	-	-	RESERVED
0010	-	-	RESERVED
0011	-	-	RESERVED
0100	2	1	PHY Address: 0x0004 (4)
0101	3	1	PHY Address: 0x0005 (5)
0110	-	-	RESERVED
0111	-	-	RESERVED
1000	1	2	PHY Address: 0x0008 (8)
1001	-	-	RESERVED
1010	1	3	PHY Address: 0x000A (10)
1011	-	-	RESERVED
1100	2	2	PHY Address: 0x000C (12)
1101	3	2	PHY Address: 0x000D (13)
1110	2	3	PHY Address: 0x000E (14)
1111	3	3	PHY Address: 0x000F (15)

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7.5.2 LED Configuration

The DP83TG720S-Q1 supports up to three configurable Light Emitting Diode (LED) pins: LED_0, LED_1, and LED_2 (CLKOUT). Several functions can be multiplexed onto the LEDs for different modes of operation. LED operations are selected using registers 0x0450 and 0x0451.

Note

CLKOUT has 25MHz clock output as default and needs to be configured to LED2 using register 0x0453.

Because the LED output pins are also used as strap pins, external components required for strapping and the user must consider the LED usage to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding input upon power up or hardware reset.

Figure 7-20 shows the two proper ways of connecting LEDs directly to the DP83TG720S-Q1.

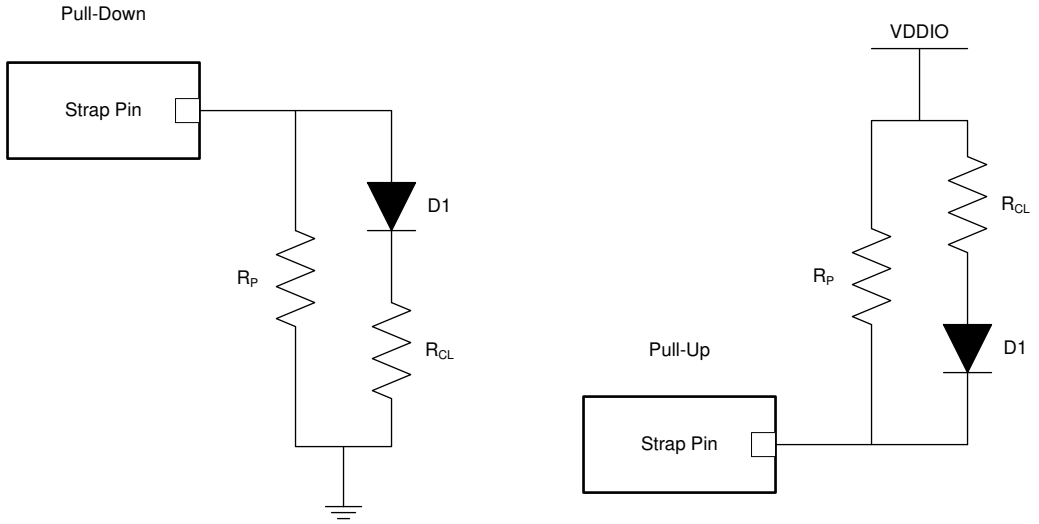

Figure 7-20. Example Strap Connections

7.5.3 PHY Address Configuration

The DP83TG720S-Q1 can be set to respond to any of 9 possible PHY addresses through bootstrap pins. The PHY address is latched into the device upon power-up or hardware reset. Each DP83TG720S-Q1 or port sharing PHY on the serial management bus in the system must have a unique PHY address. The DP83TG720S-Q1 supports PHY address as described in Table 7-19.

By default, the DP83TG720S-Q1 will latch to a PHY address of 0 ([0000]). This address can be changed by adding pullup resistors to bootstrap pins found in Table 7-17.

7.6 Register Maps

7.6.1 Register Access Summary

There are two different methods for accessing registers within the field. Direct register access method is only allowed for the first 31 registers (0x0h through 0x1Fh) of MMD1F register space. Registers beyond 0x1Fh must be accessed by use of the Indirect Method (Extended Register Space) described in *Section 7.4.11*.

Table 7-20. MMD Register Space Division

MMD REGISTER SPACE	REGISTER ADDRESS RANGE
MMD1F	0x000 - 0x0EFD
MMD1	0x1000 - 0x1904
MMD3	0x3000 - 0x390D
MMD7	0x7000 - 0x7200

Table 7-21. Register Access Summary

REGISTER FIELD	REGISTER ACCESS METHODS
0x0h through 0x1Fh	Direct Access
	Indirect Access, MMD1F = '11111' **Example:** to read register 0x17h in MMD1F field with no post increment Step 1) write 0x1Fh to register 0xDh Step 2) write 0x17h to register 0xEh Step 3) write 0x401Fh to register 0xDh Step 4) read register 0xEh
MMD1F Field 0x20h - 0xFFFh	Indirect Access, MMD1F = '11111' **Example:** to read register 0x462h in MMD1F field with no post increment Step 1) write 0x1Fh to register 0xDh Step 2) write 0x462h to register 0xEh Step 3) write 0x401Fh to register 0xDh Step 4) read register 0xEh
MMD1 Field 0x0000h - 0x0FFFh	Indirect Access, MMD1 = '00001' **Example:** to read register 0x7h in MMD1 field with no post increment Step 1) write 0x1h to register 0xDh Step 2) write 0x7h to register 0xEh Step 3) write 0x4001h to register 0xDh Step 4) read register 0xEh

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7.6.2 DP83TG720 Registers

Table 7-22 lists the DP83TG720 registers. All register offset addresses not listed in Table 7-22 should be considered as reserved locations and the register contents should not be modified.

Table 7-22. DP83TG720 Registers

Address	Acronym	Register Name	Section
0x0	BMCR		Go
0x1	BMSR		Go
0x2	PHYID1		Go
0x3	PHYID2		Go
0xF	MII_REG_F		Go
0x10	MII_REG_10		Go
0x11	MII_REG_11		Go
0x12	MII_REG_12		Go
0x13	MII_REG_13		Go
0x16	MII_REG_16		Go
0x18	MII_REG_18		Go
0x19	MII_REG_19		Go
0x1E	MII_REG_1E		Go
0x1F	MII_REG_1F		Go
0x180	C_AND_S_STATUS		Go
0x181	PM_TOP_CFG		Go
0x182	CLK_CTRL_CFG		Go
0x183	LPS_CFG		Go
0x18B	LPS_CFG2		Go
0x18C	LPS_CFG3		Go
0x18E	LPS_STATUS		Go
0x300	TDR_TX_CFG		Go
0x301	TDR_PROCESS_CFG		Go
0x302	TDR_CFG1		Go
0x303	TDR_CFG2		Go
0x304	TDR_CFG3		Go
0x305	TDR_CFG4		Go
0x309	TDR_STATUS0		Go
0x30A	TDR_STATUS1		Go
0x30B	TDR_STATUS2		Go
0x30C	TDR_STATUS3		Go
0x30D	TDR_STATUS4		Go
0x30E	TDR_STATUS5		Go
0x30F	TDR_TC12		Go
0x45D	SOR_VECTOR_1		Go
0x45E	SOR_VECTOR_2		Go
0x466	REV_ID		Go
0x514	LPS_CONTROL_1		Go
0x515	LPS_CONTROL_2		Go
0x518	MAXWAIT_TIMER		Go
0x519	PHY_CTRL_1G		Go
0x531	TEST_MODE		Go

Table 7-22. DP83TG720 Registers (continued)

Address	Acronym	Register Name	Section
0x543	LINK_QUAL_1		Go
0x544	LINK_QUAL_2		Go
0x545	LINK_DOWN_LATCH_STAT		Go
0x547	LINK_QUAL_3		Go
0x548	LINK_QUAL_4		Go
0x559	PMA_WATCHDOG		Go
0x55A	DATA_SCR_CFG		Go
0x55B	SYMB_POL_CFG		Go
0x55C	OAM_CFG		Go
0x561	TEST_MEM_CFG		Go
0x580	MBIST_CTRL		Go
0x581	MBIST_STAT		Go
0x600	RGMII_CTRL		Go
0x601	RGMII_FIFO_STATUS		Go
0x602	RGMII_DELAY_CTRL		Go
0x608	SGMII_CTRL_1		Go
0x609	SGMII_EEE_CTRL_1		Go
0x60A	SGMII_STATUS		Go
0x60B	SGMII_EEE_CTRL_2		Go
0x60C	SGMII_CTRL_2		Go
0x60D	SGMII_FIFO_STATUS		Go
0x618	PRBS_STATUS_1		Go
0x619	PRBS_CTRL_1		Go
0x61A	PRBS_CTRL_2		Go
0x61B	PRBS_CTRL_3		Go
0x61C	PRBS_STATUS_2		Go
0x61D	PRBS_STATUS_3		Go
0x61E	PRBS_STATUS_4		Go
0x620	PRBS_STATUS_6		Go
0x622	PRBS_STATUS_8		Go
0x623	PRBS_STATUS_9		Go
0x624	PRBS_CTRL_4		Go
0x625	PRBS_CTRL_5		Go
0x626	PRBS_CTRL_6		Go
0x627	PRBS_CTRL_7		Go
0x628	PRBS_CTRL_8		Go
0x629	PRBS_CTRL_9		Go
0x62A	PRBS_CTRL_10		Go
0x638	CRC_STATUS		Go
0x639	PKT_STAT_1		Go
0x63A	PKT_STAT_2		Go
0x63B	PKT_STAT_3		Go
0x63C	PKT_STAT_4		Go
0x63D	PKT_STAT_5		Go
0x63E	PKT_STAT_6		Go

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Table 7-22. DP83TG720 Registers (continued)

Address	Acronym	Register Name	Section
0x8AD	SQI_1		Go
0x8ED	SQI_2		Go
0x8EF	SQI_3		Go
0x8F0	SQI_4		Go
0x8F1	SQI_5		Go
0x8F2	SQI_6		Go
0xA40	DSP_DEBUG2_REG_40		Go
0xA41	DSP_DEBUG2_REG_41		Go
0xA42	DSP_DEBUG2_REG_42		Go
0xA81	DSP_DEBUG2_REG_81		Go
0xA86	DSP_DEBUG2_REG_86		Go
0x1000	PMA_PMD_CONTROL_1		Go
0x1007	PMA_PMD_CONTROL_2		Go
0x1009	PMA_PMD_TRANSMIT_DISABLE		Go
0x100B	PMA_PMD_EXTENDED_ABILITY2		Go
0x1012	PMA_PMD_EXTENDED_ABILITY		Go
0x1834	PMA_PMD_CONTROL		Go
0x1900	PMA_CONTROL		Go
0x1901	PMA_STATUS		Go
0x1902	TRAINING		Go
0x1903	LP_TRAINING		Go
0x1904	TEST_MODE_CONTROL		Go
0x3000	PCS_CONTROL_COPY		Go
0x3900	PCS_CONTROL		Go
0x3901	PCS_STATUS		Go
0x3902	PCS_STATUS_2		Go
0x3904	OAM_TRANSMIT		Go
0x3905	OAM_TX_MESSAGE_1		Go
0x3906	OAM_TX_MESSAGE_2		Go
0x3907	OAM_TX_MESSAGE_3		Go
0x3908	OAM_TX_MESSAGE_4		Go
0x3909	OAM_RECEIVE		Go
0x390A	OAM_RX_MESSAGE_1		Go
0x390B	OAM_RX_MESSAGE_2		Go
0x390C	OAM_RX_MESSAGE_3		Go
0x390D	OAM_RX_MESSAGE_4		Go
0x7200	AN_CFG		Go

Complex bit access types are encoded to fit into small table cells. Table 7-23 shows the codes that are used for access types in this section.

Table 7-23. DP83TG720 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		

Table 7-23. DP83TG720 Access Type Codes (continued)

Access Type	Code	Description
W	W	Write
W0C	W 0C	Write 0 to clear
W0S	W 0S	Write 0 to set
WMC	W	Write
WMC,0	W	Write
WMC,1	W	Write
WSC	W	Write
WSC,0	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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7.6.2.1 BMCR Register (Address = 0x0) [reset = 0x140]

BMCR is shown in Table 7-24.

Return to the Summary Table.

Table 7-24. BMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	mii_reset	R/WMC	1b0	MII Reset 1b0 = No reset 1b1 = Digital in reset and all MII regs (0x0 - 0xF) reset to default
14	loopback	R/W	1b0	MII loopback enable 1b0 = No MII loopback 1b1 = MII loopback
13	speed_sel_lsb	R	1b0	Speed selection LSB 1b0 = 10 Mb/s 1b1 = 100 Mb/s 1b10 = 1000 Mb/s 1b11 = Reserved
12	mr_an_enable	R	1b0	Reserved
11	power_down	R/W	1b0	Power down mode enable 1b0 = Normal mode 1b1 = Power down via register or pin
10	isolate	R/W	1b0	Isolate mode enable 1b0 = Normal mode 1b1 = Isolate mode
9	mr_restart_an	R	1b0	Reserved
8	duplex_mode	R	1b1	Duplex mode 1b0 = Half duplex 1b1 = Full duplex
7	col_test	R	1b0	Reserved
6	speed_sel_msb	R	1b1	Speed selection MSB 1b0 = 10 Mb/s 1b1 = 100 Mb/s 1b10 = 1000 Mb/s 1b11 = Reserved
5	unidirectional_ability	R	1b0	Reserved
4-0	RESERVED	R	5b00000	Reserved

7.6.2.2 BMSR Register (Address = 0x1) [reset = 0x141]

BMSR is shown in Table 7-25.

Return to the Summary Table.

Table 7-25. BMSR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ieee_100baset4	R	1b0	1 = PHY able to perform 100BASE-T4 0 = PHY not able to perform 100BASE-T4 1b0 = PHY not able to perform 100BASE-T4 1b1 = PHY able to perform 100BASE-T4
14	ieee_100basex_fd	R	1b0	1 = PHY able to perform full duplex 100BASE-X 0 = PHY not able to perform full duplex 100BASE-X 1b0 = PHY not able to perform full duplex 100BASE-X 1b1 = PHY able to perform full duplex 100BASE-X
13	ieee_100basex_hd	R	1b0	1 = PHY able to perform half duplex 100BASE-X 0 = PHY not able to perform half duplex 100BASE-X 1b0 = PHY not able to perform half duplex 100BASE-X 1b1 = PHY able to perform half duplex 100BASE-X
12	ieee_10mb_fd	R	1b0	1 = PHY able to operate at 10 Mb/s in full duplex mode 0 = PHY not able to operate at 10 Mb/s in full duplex mode 1b0 = PHY not able to operate at 10 Mb/s in full duplex mode 1b1 = PHY able to operate at 10 Mb/s in full duplex mode
11	ieee_10mb_hd	R	1b0	1 = PHY able to operate at 10 Mb/s in half duplex mode 0 = PHY not able to operate at 10 Mb/s in half duplex mode 1b0 = PHY not able to operate at 10 Mb/s in half duplex mode 1b1 = PHY able to operate at 10 Mb/s in half duplex mode
10	ieee_100baset2_fd	R	1b0	1 = PHY able to perform full duplex 100BASE-T2 0 = PHY not able to perform full duplex 100BASE-T2 1b0 = PHY not able to perform full duplex 100BASE-T2 1b1 = PHY able to perform full duplex 100BASE-T2
9	ieee_100baset2_hd	R	1b0	1 = PHY able to perform half duplex 100BASE-T2 0 = PHY not able to perform half duplex 100BASE-T2 1b0 = PHY not able to perform half duplex 100BASE-T2 1b1 = PHY able to perform half duplex 100BASE-T2
8	extended_status	R	1b1	Extended staus in register 0xf 1b0 = No extended status information in Register 15 1b1 = Extended status information in Register 15
7	unidirectional_ability	R	1b0	Reserved
6	preamble_supression	R	1b1	MF preamble supression 1b0 = PHY will not accept management frames with preamble suppressed 1b1 = PHY will accept management frames with preamble suppressed.
5	aneg_complete	R	1b0	Reserved

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Table 7-25. BMSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	remote_fault	R/W0C	1b0	Reserved
3	aneg_ability	R	1b0	Reserved
2	link_status	R/W0S	1b0	Link status latch low 1b0 = link had been down 1b1 = link is up
1	jabber_detect	R/W0C	1b0	Reserved
0	extended_capability	R	1b1	Extended capabilities status 1b0 = basic register set capabilities only 1b1 = extended register capabilities

7.6.2.3 PHYID1 Register (Address = 0x2) [reset = 0x2000]

PHYID1 is shown in Table 7-26.

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Table 7-26. PHYID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	oui_21_16	R	16b0010000 000000000	

7.6.2.4 PHYID2 Register (Address = 0x3) [reset = 0xA284]

PHYID2 is shown in Table 7-27.

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Table 7-27. PHYID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	oui_5_0	R	6b101000	
9-4	model_number	R	6b101000	
3-0	rev_number	R	4b0100	

7.6.2.5 MII_REG_F Register (Address = 0xF) [reset = 0x0]

MII_REG_F is shown in Table 7-28.

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Table 7-28. MII_REG_F Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ieee_1000basex_fd	R	1b0	1 = PHY able to perform full duplex 1000BASE-X 0 = PHY not able to perform full duplex 1000BASE-X 1b0 = PHY not able to perform full duplex 1000BASE-X 1b1 = PHY able to perform full duplex 1000BASE-X
14	ieee_1000basex_hd	R	1b0	1 = PHY able to perform half duplex 1000BASE-X 0 = PHY not able to perform half duplex 1000BASE-X 1b0 = PHY not able to perform half duplex 1000BASE-X 1b1 = PHY able to perform half duplex 1000BASE-X
13	ieee_1000baset_fd	R	1b0	1 = PHY able to perform full duplex 1000BASE-T 0 = PHY not able to perform full duplex 1000BASE-T 1b0 = PHY not able to perform full duplex 1000BASE-T 1b1 = PHY able to perform full duplex 1000BASE-T
12	ieee_1000baset_hd	R	1b0	1 = PHY able to perform half duplex 1000BASE-T 0 = PHY not able to perform half duplex 1000BASE-T 1b0 = PHY not able to perform half duplex 1000BASE-T 1b1 = PHY able to perform half duplex 1000BASE-T
11-0	RESERVED	R	12b000000000000	Reserved

7.6.2.6 MII_REG_10 Register (Address = 0x10) [reset = 0x4]

MII_REG_10 is shown in Table 7-29.

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Table 7-29. MII_REG_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	5b00000	Reserved
10	signal_detect	R/W0S	1b0	Channel ok latch low 1b0 = Channel ok had been reset 1b1 = Channel ok is set
9	descr_lock_bit	R/W0S	1b0	Descrambler lock latch low 1b0 = Descrmabler had been locked 1b1 = Descrambler is locked
8	RESERVED	R	1b0	Reserved
7	mii_int_bit		1b0	Interrupts pin status, cleared on reading 0x12 1b0 = Interrupts pin not set 1b1 = Interrupt pin had been set
6-4	RESERVED	R	3b000	Reserved
3	mii_loopback	R	1b0	MII loopback status 1b0 = No MII loopback 1b1 = MII loopback
2	duplex_mode_env	R	1b1	Duplex mode status 1b0 = Half duplex 1b1 = Full duplex
1	RESERVED	R	1b0	Reserved
0	link_status_bit	R	1b0	Latch low link status 1b0 = link had been down 1b1 = link is up

7.6.2.7 MII_REG_11 Register (Address = 0x11) [reset = 0xB]

MII_REG_11 is shown in Table 7-30.

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Table 7-30. MII_REG_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	dis_clk_125	R/W	1b0	Disable MAC clock 1b0 = keep clk_125 to MAC 1b1 = stop clk_125 to MAC on IEEE power save mode
14	power_save_mode_en	R/W	1b0	Enable power save mode config from reg
13-12	power_save_mode	R/W	2b00	Power mode 2b00 = Normal mode 2b01 = Reserved 2b10 = Active sleep 2b11 = Passive sleep
11	sgmii_soft_reset	R/WSC	1b0	Reset SGMII
10	use_phyad0_as_isolate	R/W	1b0	Use PHY ADDRESS 5'b0 as isolate
9	channel_debug_mode	R/W	1b0	Enable channel debug mode
8	debug_mode	R/W	1b0	Enable debug mode
7	RESERVED	R	1b0	Reserved
6	cfg_soft_reset_non_clear	R/W	1b0	To make 0x1F = 4000 (digital reset) non self clearing 1b11111 = 4000 is self clearing
5-4	cfg_reset_time_sel	R/W	2b00	To configure duration of soft reset 00b = 120ns (duration calculated post pll lock) 01b = 32us 10b = 256us 11b = 1024us 2b00 = 120ns 2b01 = 32us 2b10 = 256us 2b11 = 1024us
3	int_polarity	R/W	1b1	Interrupts polarity 1b0 = Active high 1b1 = Active low
2	force_interrupt	R/W	1b0	Force interrupt pin 1b0 = Do not force interrupt pin 1b1 = Force interrupt pin
1	int_en	R/W	1b1	Enable interrupts 1b0 = Disable interrupts 1b1 = Enable interrupts
0	int_oe	R/W	1b1	Interrupt/Power down pin configuration 1b0 = PIN is a power down PIN (input) 1b1 = PIN is an interrupt pin (output)

7.6.2.8 MII_REG_12 Register (Address = 0x12) [reset = 0x0]

MII_REG_12 is shown in Table 7-31.

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Table 7-31. MII_REG_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	link_qual_int	R	1b0	Link quality bad interrupt status
14	energy_det_int	R	1b0	Energy det change interrupt status
13	link_int	R	1b0	Link status change interrupt status
12	RESERVED	R	1b0	Reserved
11	esd_int	R	1b0	ESD fault detected interrupt status
10	ms_train_done_int	R	1b0	Training done interrupt status
9	RESERVED	R	1b0	Reserved
8	RESERVED	R	1b0	Reserved
7	link_qual_int_en	R/W	1b0	Link quality bad interrupt enable
6	energy_det_int_en	R/W	1b0	Energy det change interrupt enable
5	link_int_en	R/W	1b0	Link status change interrupt enable
4	unused_int_3	R/W	1b0	Reserved
3	esd_int_en	R/W	1b0	ESD fault detected interrupt enable
2	ms_train_done_int_en	R/W	1b0	Training done interrupt enable
1	unused_int_2	R/W	1b0	Reserved
0	unused_int_1	R/W	1b0	Reserved

7.6.2.9 MII_REG_13 Register (Address = 0x13) [reset = 0x0]

MII_REG_13 is shown in Table 7-32.

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Table 7-32. MII_REG_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	under_volt_int	R	1b0	Under volt interrupt status
14	over_volt_int	R	1b0	Over volt interrupt status
13	RESERVED	R	1b0	Reserved
12	RESERVED	R	1b0	Reserved
11	over_temp_int	R	1b0	Over temp interrupt status
10	sleep_int	R	1b0	Sleep mode change interrupt status
9	pol_change_int	R	1b0	Data polarity change interrupt status
8	not_one_hot_int	R	1b0	Not one hot interrupt status
7	under_volt_int_en	R/W	1b0	Under volt interrupt enable
6	over_volt_int_en	R/W	1b0	Over volt interrupt enable
5	unused_int_6	R/W	1b0	Reserved
4	unused_int_5	R/W	1b0	Reserved
3	over_temp_int_en	R/W	1b0	Over temp interrupt enable
2	sleep_int_en	R/W	1b0	Sleep mode change interrupt enable
1	pol_change_int_en	R/W	1b0	Data Polarity change interrupt enable
0	not_one_hot_int_en	R/W	1b0	Not one hot interrupt enable

7.6.2.10 MII_REG_16 Register (Address = 0x16) [reset = 0x0]

MII_REG_16 is shown in Table 7-33.

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Table 7-33. MII_REG_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	5b00000	Reserved
10	prbs_sync_loss	R/W0C	1b0	Prbs lock lost latch status 1b0 = Prbs lock never lost 1b1 = Prbs lock had been lost
9	RESERVED	R	1b0	Reserved
8	core_pwr_mode	R	1b0	1b = Core is is normal power mode 0b = Core is in power down or sleep mode 1b0 = Core is in power down or sleep mode 1b1 = Core is is normal power mode
7	cfg_dig_pcs_loopback	R/W	1b0	PCS digital loopback
6-0	loopback_mode	R/W	7b0000000	Bits[4:0]: 000001b = PCS loop 000010b = RS loop 000100b = Digital loop 001000b = Analog loop 010000b = Reverse loop Bit[5] (should be set only in reverse loop) 1 = Transmit data to MAC in reverse loop 0 = Suppress data to MAC in reverse loop Bit[6] (should be set only in MII loop) 1 = Transmit data to MDI in MII loop 0 = Suppress data to MDI in MII loop 7b0000001 = PCS loop 7b0000010 = RS loop 7b0000100 = Digital loop 7b0010000 = Reverse loop

7.6.2.11 MII_REG_18 Register (Address = 0x18) [reset = 0x8]

MII_REG_18 is shown in Table 7-34.

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Table 7-34. MII_REG_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ack_received_int	R	1b0	Ack received interrupt status (OAM)
14	tx_valid_clr_int	R	1b0	mr_tx_valid clear interrupt status (OAM)
13	link_state_ind_fall_bmw_int	R	1b0	BMW interrupt status (see advanced features)
12	link_state_ind_rise_bmw_int	R	1b0	BMW interrupt status(see advanced features)
11	por_done_int	R	1b0	POR done interrupt status
10	no_frame_int	R	1b0	No frame detect interrupt status
9	wake_req_int	R	1b0	Wake request interrupt status
8	lps_int	R	1b0	LPS interrupt status
7	ack_received_int_en	R/W	1b0	Ack received interrupt enable (OAM)
6	tx_valid_clr_int_en	R/W	1b0	mr_tx_valid clear interrupt enable (OAM)
5	link_state_ind_fall_bmw_int_en	R/W	1b0	BMW interrupt (see advanced features)
4	link_state_ind_rise_bmw_int_en	R/W	1b0	BMW interrupt (see advanced features)
3	por_done_int_en	R/W	1b1	POR done interrupt enable
2	no_frame_int_en	R/W	1b0	No frame detect interrupt enable
1	wake_req_int_en	R/W	1b0	Wake request interrupt enable
0	lps_int_en	R/W	1b0	LPS interrupt enable

7.6.2.12 MII_REG_19 Register (Address = 0x19) [reset = X]

MII_REG_19 is shown in Table 7-35.

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Table 7-35. MII_REG_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	5b00000	Reserved
10	dsp_energy_detect	R	1b0	DSP energy detected status
9-5	RESERVED	R	5b00000	Reserved
4-0	SOR_PHYADDR	R	X	PHY ADDRESS latched from strap

7.6.2.13 MII_REG_1E Register (Address = 0x1E) [reset = 0x0]

MII_REG_1E is shown in Table 7-36.

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Table 7-36. MII_REG_1E Register Field Descriptions

Bit	Field	Type	Reset	Description
15	tdr_start	R/WMC	1b0	Start TDR manually 1b0 = No TDR 1b1 = TDR start
14	cfg_tdr_auto_run	R/W	1b0	Enable TDR auto run on link down 1b0 = TDR start manually 1b1 = TDR start automatically on link down
13-2	RESERVED	R	12b000000000000	Reserved
1	tdr_done	R	1b0	TDR done status
0	tdr_fail	R	1b0	TDR fail status

7.6.2.14 MII_REG_1F Register (Address = 0x1F) [reset = 0x0]

MII_REG_1F is shown in Table 7-37.

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Table 7-37. MII_REG_1F Register Field Descriptions

Bit	Field	Type	Reset	Description
15	sw_global_reset	R/WMC	1b0	Hardware reset - Reset digital + register file
14	digital_reset	R/WMC	1b0	Soft reset - Reset only digital core
13	sor_debug_option	R/W	1b0	Use sw_global_reset as RESET pin source
12-8	tp_sel_1_9_5	R/W	5b00000	Test port select[9:5] - Select module
7	standby_mode	R/W	1b0	Reserved
6	standby_mode_ch_sel_B_An	R/W	1b0	Reserved
5	RESERVED	R	1b0	Reserved
4-0	tp_sel_1_4_0	R/W	5b00000	Test port select[4:0] - Select signals within module

7.6.2.15 C_AND_S_STATUS Register (Address = 0x180) [reset = 0x0]

C_AND_S_STATUS is shown in Table 7-38.

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Table 7-38. C_AND_S_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	link_up	R	1b0	link up defined by CnS
14	link_down	R	1b0	link down as defined by CnS
13	phy_ctrl_send_data	R	1b0	phy control in send data status
12	link_status	R	1b0	link status
11-8	pm_coded_state	R	4b0000	pm state
7	sel_osc25_clk_n	R	1b0	25MHz clock select
6	pll_clk_sel	R	1b0	Pll clock select
5	pwr_seq_done	R	1b0	Power seq done status
4	slave_ph1_done	R	1b0	slave ph1 done status
3	channel_ok	R	1b0	channel okay status
2	descr_sync	R	1b0	Descrambler lock status
1	loc_rcvr_status	R	1b0	Local receiver status
0	rem_rcvr_status	R	1b0	Remote receiver status

7.6.2.16 PM_TOP_CFG Register (Address = 0x181) [reset = 0x440]

PM_TOP_CFG is shown in Table 7-39.

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Table 7-39. PM_TOP_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	4b0000	Reserved
11	cfg_lps_xtal_pwrdn_en	R/W	1b0	
10	cfg_lps_mac_pwrdn_en	R/W	1b1	Enable power down of mac inf during Low power mode
9	cfg_lps_pll_pwrdn_en	R/W	1b0	
8	cfg_lps_dbg_mode	R/W	1b0	LPS debug mode enable to reduce the sleep request timeout
7-6	cfg_lps_slp_rqst_to	R/W	2b01	Sleep rquest timer threshold. 2'b00 = 0.4ms, 2'b01 = 1ms, 2'b10 = 4ms, 2'b11 = 16ms
5-4	ld_pwr_up_wait	R/W	2b00	Determine additional wait time between de-assertion reset to last DDS to assertion of pwr_seq_done: 00: no additional wait 01: 1ms 10: 2ms 11: 4ms This value should deal with potential problem in Line Driver power-up time.
3	pll_gf_reset_reg	R/W	1b0	1 = Reset is high 0 = Reset is low
2	force_pll_gf_reset	R/W	1b0	1 = Force pll_clk mux reset to value defined in bit[8] 0 = Normal mode
1	pll_clk_sel_reg	R/W	1b0	1: select PLL clock 0: select REF clock
0	force_pll_ctrl	R/W	1b0	1: force pll_clk_mux selec to value defined in Bit[2] 0: Do not force pll_clk_mux select (Normal)

7.6.2.17 CLK_CTRL_CFG Register (Address = 0x182) [reset = 0x0]

CLK_CTRL_CFG is shown in Table 7-40.

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Table 7-40. CLK_CTRL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	cfg_force_mas_mode_clk_ctrl_val	R/W	1b0	Force value for master/slave control for clock control
14	cfg_force_mas_mode_clk_ctrl_en	R/W	1b0	Force enable for master/slave control for clock control
13	cfg_200m_clk_sel_force_val	R/W	1b0	Force value for sys clock mux select
12	cfg_200m_clk_sel_force_en	R/W	1b0	Force enable for sys clock mux select
11-0	gate_clk_dis	R/W	12b000000000000	Allows the user to disable clock gating (keep clock/s enable). Every bit, when set to one constantly enables one clock as specifies bellow: Bit[11]: sgmii_clk Bit[10]: wol_clk Bit[9]: rgmii_clk Bit[8]: rmii_clk Bit[7]: rx10_sf_clk Bit[6]: txg_sf_clk Bit[5]: reg_file_clk Bit[4]: top_clk Bit[3]: an_clk Bit[2]: core_10m_clk Bit[1]: 100m_tx_clk Bit[0]: 100m_rx_clk, ce_a_clk

7.6.2.18 LPS_CFG Register (Address = 0x183) [reset = 0x0]

LPS_CFG is shown in Table 7-41.

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Table 7-41. LPS_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	8b00000000	Reserved
7	cfg_force_lps_st_en	R/W	1b0	Enable force lps state
6-0	cfg_force_lps_st	R/W	7b0000000	Force lps state

7.6.2.19 LPS_CFG2 Register (Address = 0x18B) [reset = 0x0]

LPS_CFG2 is shown in Table 7-42.

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Table 7-42. LPS_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	7b0000000	Reserved
8	ed_en	R/W	1b0	1b = Enable energy detection on MDI 0b = Disable energy detection on MDI 1b0 = Disable energy detection on MDI 1b1 = Enable energy detection on MDI
7	sleep_en	R/W	1b0	1b = Allow PHY to enter sleep 0b = Do not allow PHY to enter sleep 1b0 = Do not allow PHY to enter sleep 1b1 = Allow PHY to enter sleep
6	cfg_auto_mode_en_strap	R/WMC,1	1b0	LPS autonomous mode enable 1b = PHY enters normal mode on power up 0b = PHY enters standby mode on power up 1b0 = PHY enters standby mode on power up 1b1 = PHY enters normal mode on power up
5	cfg_lps_mon_en_strap	R/W	1b0	1b = Enable normal to standby transition on over temp/under volt 0b = Disable normal to standby transition on over temp/under volt 1b0 = Disable normal to standby transition on over temp/under volt 1b1 = Enable normal to standby transition on over temp/under volt
4	cfg_lps_sleep_auto	R/W	1b0	Reserved
3	cfg_lps_slp_confirm	R/W	1b0	Reserved
2	cfg_lps_auto_pwrdn	R/W	1b0	Reserved
1	cfg_lps_sleep_en	R/W	1b0	Reserved
0	cfg_lps_sm_en	R/W	1b0	Reserved

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7.6.2.20 LPS_CFG3 Register (Address = 0x18C) [reset = 0x0]

LPS_CFG3 is shown in Table 7-43.

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Table 7-43. LPS_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	8b00000000	Reserved
7	cfg_lps_pwr_mode_7	R/WMC,0	1b0	Reserved
6	cfg_lps_pwr_mode_6	R/WMC,0	1b0	Reserved
5	cfg_lps_pwr_mode_5	R/WMC,0	1b0	Reserved
4	cfg_lps_pwr_mode_4	R/WMC,0	1b0	Set to enter standby mode
3	cfg_lps_pwr_mode_3	R/WMC,0	1b0	Reserved
2	cfg_lps_pwr_mode_2	R/WMC,0	1b0	Reserved
1	cfg_lps_pwr_mode_1	R/WMC,0	1b0	Reserved
0	cfg_lps_pwr_mode_0	R/WMC,0	1b0	Set to enter normal mode

7.6.2.21 LPS_STATUS Register (Address = 0x18E) [reset = 0x0]

LPS_STATUS is shown in Table 7-44.

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Table 7-44. LPS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	9b000000000	Reserved
6-0	status_lps_st	R	7b0000000	Observe LPS state : 0x2 = Standby mode 0x4 = Normal mode

7.6.2.22 TDR_TX_CFG Register (Address = 0x300) [reset = 0x3E8]

TDR_TX_CFG is shown in Table 7-45.

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Table 7-45. TDR_TX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	cfg_tdr_tx_duration	R/W	16b0000001 111101000	TDR transmit duration in usec 16b0000000000000000 = allow tx_err assertion to PHY when tx_en set to zero 16b0000000000000001 = suppress tx_err in full duplex mode when tx_en set to zero

7.6.2.23 TDR_PROCESS_CFG Register (Address = 0x301) [reset = 0xD716]

TDR_PROCESS_CFG is shown in Table 7-46.

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Table 7-46. TDR_PROCESS_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_end_tap_index	R/W	8b11010111	End tap index for echo coeff sweep
7-0	cfg_start_tap_index	R/W	8b00010110	Start tap index for echo coeff sweep

7.6.2.24 TDR_CFG1 Register (Address = 0x302) [reset = 0x45]

TDR_CFG1 is shown in Table 7-47.

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Table 7-47. TDR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	8b00000000	Reserved
7-4	cfg_forward_shadow	R/W	4b0100	Forward shadow
3-2	cfg_post_silence_time	R/W	2b01	Post silence time 2b00 = 0 ms 2b01 = 10 ms 2b10 = 100 ms 2b11 = 1000 ms
1-0	cfg_pre_silence_time	R/W	2b01	Pre silence time 2b00 = 0 ms 2b01 = 10 ms 2b10 = 100 ms 2b11 = 1000 ms

7.6.2.25 TDR_CFG2 Register (Address = 0x303) [reset = 0x172D]

TDR_CFG2 is shown in Table 7-48.

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Table 7-48. TDR_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_tdr_flt_loc_offset	R/W	8b00010111	tap index offset of dyamic peak equation
7-0	cfg_tdr_flt_init	R/W	8b00101101	Offset of dynamic peak equation

7.6.2.26 TDR_CFG3 Register (Address = 0x304) [reset = 0x3]

TDR_CFG3 is shown in Table 7-49.

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Table 7-49. TDR_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	8b00000000	Reserved
7-0	cfg_tdr_flt_slope	R/W	8b00000011	Slope of dynamic peak equation (0.4)

7.6.2.27 TDR_CFG4 Register (Address = 0x305) [reset = 0x5]

TDR_CFG4 is shown in Table 7-50.

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Table 7-50. TDR_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	7b0000000	Reserved
8	mas_mode_tdr	R/W	1b0	Master slave config during TDR
7-6	pi_pud_ctrl_tdr	R/W	2b00	PUD control during TDR
5	pi_pud_clk_tdr	R/W	1b0	PUD clock during TDR
4-2	hpf_gain_tdr	R/W	3b001	HPF gain during TDR
1-0	pga_gain_tdr	R/W	2b01	PGA gain during TDR

7.6.2.28 TDR_STATUS0 Register (Address = 0x309) [reset = 0x0]

TDR_STATUS0 is shown in Table 7-51.

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Table 7-51. TDR_STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	peak1_loc	R	8b00000000	Peak 1 location in tap index
7-0	peak0_loc	R	8b00000000	Peak 0 location in tap index

7.6.2.29 TDR_STATUS1 Register (Address = 0x30A) [reset = 0x0]

TDR_STATUS1 is shown in Table 7-52.

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Table 7-52. TDR_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	peak3_loc	R	8b00000000	Peak 3 location in tap index
7-0	peak2_loc	R	8b00000000	Peak 2 location in tap index

7.6.2.30 TDR_STATUS2 Register (Address = 0x30B) [reset = 0x0]

TDR_STATUS2 is shown in Table 7-53.

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Table 7-53. TDR_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	peak0_amp	R	8b00000000	Peak 0 amplitude in echo coeff
7-0	peak4_loc	R	8b00000000	Peak 4 location in tap index

7.6.2.31 TDR_STATUS3 Register (Address = 0x30C) [reset = 0x0]

TDR_STATUS3 is shown in Table 7-54.

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Table 7-54. TDR_STATUS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	peak2_amp	R	8b00000000	Peak 2 amplitude in echo coeff
7-0	peak1_amp	R	8b00000000	Peak 1 amplitude in echo coeff

7.6.2.32 TDR_STATUS4 Register (Address = 0x30D) [reset = 0x0]

TDR_STATUS4 is shown in Table 7-55.

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Table 7-55. TDR_STATUS4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	peak4_amp	R	8b00000000	Peak 4 amplitude in echo coeff
7-0	peak3_amp	R	8b00000000	Peak 3 amplitude in echo coeff

7.6.2.33 TDR_STATUS5 Register (Address = 0x30E) [reset = 0x0]

TDR_STATUS5 is shown in Table 7-56.

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Table 7-56. TDR_STATUS5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	11b00000000000	Reserved
4	peak4_sign	R	1b0	Peak 4 sign
3	peak3_sign	R	1b0	Peak 3 sign
2	peak2_sign	R	1b0	Peak 2 sign
1	peak1_sign	R	1b0	Peak 1 sign
0	peak0_sign	R	1b0	Peak 0 sign

7.6.2.34 TDR_TC12 Register (Address = 0x30F) [reset = 0x0]

TDR_TC12 is shown in Table 7-57.

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Table 7-57. TDR_TC12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	2b00	Reserved
13-8	fault_loc	R	6b000000	See TC12
7-4	tdr_state	R	4b0000	See TC12
3-2	RESERVED	R	2b00	Reserved
1-0	tdr_activation	R	2b00	See TC12

7.6.2.35 SOR_VECTOR_1 Register (Address = 0x45D) [reset = 0x0]

SOR_VECTOR_1 is shown in Table 7-58.

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Table 7-58. SOR_VECTOR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	sor_vector_1	R	16b0000000000000000	SOR_VECTOR_1 16b0000000000000100 = 0 - CFG_PHY_AD 5 - MASTER 16b0000000000001000 = 6 - MAC 16b0000000000001011 = 9 - TEST_MODE 12 - CFG_RGMII_EN_STRAP 13 - CFG_SGMII_EN_STRAP 14 - CFG_RX_SHIFT 15 - CFG_TX_SHIFT

7.6.2.36 SOR_VECTOR_2 Register (Address = 0x45E) [reset = 0x0]

SOR_VECTOR_2 is shown in Table 7-59.

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Table 7-59. SOR_VECTOR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	sor_vector_2	R	16b0000000 000000000	SOR_VECTOR_2

7.6.2.37 REV_ID Register (Address = 0x466) [reset = 0x0]

REV_ID is shown in Table 7-60.

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Table 7-60. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	12b000000000000	Reserved
3-0	si_rev_id	R	4b0000	SI_REV_ID

7.6.2.38 LPS_CONTROL_1 Register (Address = 0x514) [reset = 0x8E3]

LPS_CONTROL_1 is shown in Table 7-61.

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Table 7-61. LPS_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	4b0000	Reserved
11-9	cfg_tx_wake_cg	R/W	3b100	Control code to send on Tx for wake indication
8-6	cfg_tx_sleep_cg	R/W	3b011	Control code to send on Tx for sleep indication
5-3	cfg_rx_wake_cg	R/W	3b100	Control code to expect on Rx for wake indication
2-0	cfg_rx_sleep_cg	R/W	3b011	Control code to expect on Rx for sleep indication

7.6.2.39 LPS_CONTROL_2 Register (Address = 0x515) [reset = 0x808]

LPS_CONTROL_2 is shown in Table 7-62.

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Table 7-62. LPS_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	1b0	Reserved
14-8	cfg_wake_cg_cnt_th	R/W	7b0001000	Number of continuous expected wake code groups required to acknowledge and set LPS wake command received.
7	RESERVED	R	1b0	Reserved
6-0	cfg_sleep_cg_cnt_th	R/W	7b0001000	Number of continuous expected sleep code groups required to acknowledge and set LPS sleep command received.

7.6.2.40 MAXWAIT_TIMER Register (Address = 0x518) [reset = 0x17CE]

MAXWAIT_TIMER is shown in Table 7-63.

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Table 7-63. MAXWAIT_TIMER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	cfg_maxwait_timer_init	R/W	16b0001011 111001110	Maxwait timer value in us (value internally multiplied by 16)

7.6.2.41 PHY_CTRL_1G Register (Address = 0x519) [reset = 0x3D]

PHY_CTRL_1G is shown in Table 7-64.

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Table 7-64. PHY_CTRL_1G Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	1b0	Reserved
14	cfg_phy_ctrl_fallback_on_energy_lost_loc_rcvr	R/W	1b0	Allow phy control to go from TRAINING to COUNTDOWN to SILENT on energy lost and loc_rcvr lock Note : Should be enabled only if 0x519[13] is disabled
13	cfg_phy_ctrl_fallback_on_energy_lost	R/W	1b0	Allow phy control to go from TRAINING to COUNTDOWN to SILENT on energy lost Note : Should be enabled only if 0x519[14] is disabled
12	cfg_bypass_dsp_reset	R/W	1b0	Bypass dsp reset from pcs
11	cfg_force_link_stat_val	R/W	1b0	Forced link status value Valid only if 0x519[10] is set
10	cfg_force_link_stat	R/W	1b0	Enable forcing link status value
9	cfg_link_control_override_val	R/W	1b0	Override Value for link control (only valid is autoneg is enabled) Valid only if 0x519[8] is set
8	cfg_link_control_override_en	R/W	1b0	Override Enable for link control (only valid is autoneg is enabled) 1b0 = Link_control override disbale 1b1 = Link_control override Eanable
7-0	cfg_minwait_timer_init	R/W	8b00111101	Minwait timer value in us (value internally multiplied by 16)

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7.6.2.42 TEST_MODE Register (Address = 0x531) [reset = 0x0]

TEST_MODE is shown in Table 7-65.

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Table 7-65. TEST_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	7b0000000	Reserved
8	cfg_test_mode4_tx_order	R/W	1b0	Order of symbols to be transmitted in Test mode 4 1b0 = T1 followed by T2 1b1 = T2 followed by T1
7-0	cfg_test_mode_7_data	R/W	8b00000000	GMII data to transmit in Test mode 7

7.6.2.43 LINK_QUAL_1 Register (Address = 0x543) [reset = 0x0]

LINK_QUAL_1 is shown in Table 7-66.

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Table 7-66. LINK_QUAL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	8b00000000	Reserved
7-0	link_training_time	R	8b00000000	Link training time in ms (TC12)

7.6.2.44 LINK_QUAL_2 Register (Address = 0x544) [reset = 0x0]

LINK_QUAL_2 is shown in Table 7-67.

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Table 7-67. LINK_QUAL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	remote_receiver_time	R	8b00000000	Remote receiver time in ms (TC12)
7-0	local_receiver_time	R	8b00000000	Local receiver time in ms (TC12)

7.6.2.45 LINK_DOWN_LATCH_STAT Register (Address = 0x545) [reset = 0x0]

LINK_DOWN_LATCH_STAT is shown in Table 7-68.

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Table 7-68. LINK_DOWN_LATCH_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	10b0000000000	Reserved
5	channel_ok_ll	R/W0C	1b0	Channel ok latch low indication 1b0 = Channel ok was de-asserted 1b1 = Channel ok was never de-asserted
4	link_fail_inhibit_lh	R/W0C	1b0	Latch high link fail inhibit indication 1b0 = Link fail inhibit assertion was never reported 1b1 = Link fail inhibit assertion was reported
3	send_s_sigdet_lh	R/W0C	1b0	Latch high send_s_sigdet 1b0 = Send s sigdet assertion was never reported 1b1 = Send s sigdet assertion was reported
2	hi_rfer_lh	R/W0C	1b0	Latch high hi rfer 1b0 = High ri rfer assertion was never reported 1b1 = High ri rfer assertion was reported
1	block_lock_ll	R/W0S	1b0	Latch low block lock 1b0 = Block lock de-assertion was never reported 1b1 = Block lock de-assertion was never reported
0	pma_watchdog_ll	R/W0S	1b0	Latch low pma watchdog status 1b0 = Low pma watchdof was reported 1b1 = Low pma watchdog was never reported

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7.6.2.46 LINK_QUAL_3 Register (Address = 0x547) [reset = 0x0]

LINK_QUAL_3 is shown in Table 7-69.

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Table 7-69. LINK_QUAL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	link_loss_cnt	R	6b000000	Link loss count since last power cycle (TC12)
9-0	link_fail_cnt	R	10b0000000000	Link fail without link loss count since last power cycle (TC12)

7.6.2.47 LINK_QUAL_4 Register (Address = 0x548) [reset = 0x0]

LINK_QUAL_4 is shown in Table 7-70.

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Table 7-70. LINK_QUAL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	15b000000000000000	Reserved
0	comm_ready	R	1b0	Communication ready status (TC12)

7.6.2.48 PMA_WATCHDOG Register (Address = 0x559) [reset = 0x51]

PMA_WATCHDOG is shown in Table 7-71.

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Table 7-71. PMA_WATCHDOG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	9b000000000	Reserved
6	cfg_pma_watchdog_force_val	R/W	1b1	Force value for pma watchdog
5	cfg_pma_watchdog_force_en	R/W	1b0	Enable forcing pma watchdog
4	cfg_ieee_watchdog_en	R/W	1b1	1 : watchdog counters are started after link up 0: TBD 1b0 = TBD 1b1 = watchdog counters are started after link up
3-0	cfg_watchdog_cnt_clr_th	R/W	4b0001	Number of 0, +1, -1 symbols to be seen in their respective watchdog counter window to prevent them for asserting pma_watchdog_status

7.6.2.49 DATA_SCR_CFG Register (Address = 0x55A) [reset = 0x0]

DATA_SCR_CFG is shown in Table 7-72.

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Table 7-72. DATA_SCR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	1b0	Reserved
14-6	cfg_ecc_error	R/W	9b000000000	9 bit error val xor'ed to memory data input for ECC testing
5	cfg_ecc_corrupt	R/W	1b0	Enable corruption of memory data for ECC testing
4	cfg_rx_delay_data_scr	R/W	1b0	Delay generation of rx descrmabler symbols by 1 bit 1b0 = Do not delay generation of rx descrmabler symbols by 1 bit 1b1 = Delay generation of rx descrmabler symbols by 1 bit
3	cfg_tx_delay_data_scr	R/W	1b0	Delay generation of tx scrmabler symbols by 1 bit 1b0 = Do not delay generation of tx scrmabler symbols by 1 bit 1b1 = Delay generation of tx scrmabler symbols by 1 bit
2	cfg_rx_data_scr_order_inv	R/W	1b0	Enable to generate rx descrambler symbols from S[0] instead of S[14] Valid only if LP's 0x55A[1] is set (TI-TI link) 1b0 = Use S[14] as rx descrambler symbols 1b1 = Use S[0] as rx descrmabler symbols
1	cfg_tx_data_scr_order_inv	R/W	1b0	Enable to generate tx scrambler symbols from S[0] instead of S[14] Valid only if LP's 0x55A[2] is set (TI-TI link) 1b0 = Use S[14] as tx scrambler symbols 1b1 = Use S[0] as tx scrmabler symbols
0	cfg_data_scr_bypass	R/W	1b0	Bypass data scrmabler on Tx as well as Rx path 1b0 = Do not bypass data scramblers 1b1 = Bypass data scramblers

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7.6.2.50 SYMB_POL_CFG Register (Address = 0x55B) [reset = 0x0]

SYMB_POL_CFG is shown in Table 7-73.

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Table 7-73. SYMB_POL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	11b00000000000	Reserved
4	cfg_slave_auto_pol_correction_en	R/W	1b0	Correct tx polarity for slave based on received polarity 1b0 = Slave tx polarity independent of slave rx polarity 1b1 = Slave tx polarity to match received polarity
3	cfg_rx_symb_order_inv	R/W	1b0	Order of received symbols S0 to S6 reversed to S6 to S0 Valid only if LP's 0x55B[1] is set (TI-TI link) 1b0 = Order of received symbols S0 to S6 unchanged 1b1 = Order of received symbols S0 to S6 reversed to S6 to S0
2	cfg_rx_symb_pol_inv	R/W	1b0	Invert polarity of received symbols 1b0 = Unchanged polarity of received symbols 1b1 = Invert polarity of received symbols
1	cfg_tx_symb_order_inv	R/W	1b0	Order of transmit symbols S0 to S6 reversed to S6 to S0 Valid only if LP's 0x55B[3] is set (TI-TI link) 1b0 = Order of transmit symbols S0 to S6 unchanged 1b1 = Order of transmit symbols S0 to S6 reversed to S6 to S0
0	cfg_tx_symb_pol_inv	R/W	1b0	Invert polarity of transmit symbols 1b0 = Unchanged polarity of transmit symbols 1b1 = Invert polarity of transmit symbols

7.6.2.51 OAM_CFG Register (Address = 0x55C) [reset = 0x0]

OAM_CFG is shown in Table 7-74.

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Table 7-74. OAM_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	14b00000000000000	Reserved
1	cfg_rx_oam_crc_data_in_order	R/W	1b0	Reverse order of data input to CRC checker in rx oam to MSB first 1b0 = Order of data input to CRC checker in rx oam is LSB first 1b1 = Order of data input to CRC checker in rx oam is MSB first
0	cfg_tx_oam_crc_data_in_order	R/W	1b0	Reverse order of data input to CRC calculator in tx oam to MSB first 1b0 = Order of data input to CRC calculator in tx oam is LSB first 1b1 = Order of data input to CRC calculator in tx oam is MSB first

7.6.2.52 TEST_MEM_CFG Register (Address = 0x561) [reset = 0x17A0]

TEST_MEM_CFG is shown in Table 7-75.

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Table 7-75. TEST_MEM_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	3b000	Reserved
12-6	cfg_wait_time_xcorr_wen	R/W	7b1011110	Wait timer after TX_SEND_S after which testmem is written on energy fall Note : Valid only if 0x561[3] is set
5	cfg_xcorr_dbg_sel	R/W	1b1	0b = Select xcorr from aligned detector to write to test mem 1b = Select xcorr from shifted detector to write to test mem Note : Valid only if 0x561[3] is set
4	cfg_send_s_infinite_loop	R/W	1b0	enable transmitting infinite send_s sequence. For send_s debug. Valid only in master and when 0x56A[15] is set. 1b0 = disable infinte send_s mode 1b1 = enable infinite send_s mode
3	cfg_xcorr_dbg_test_mem	R/W	1b0	enabled xcorr debug for send_s. Valid only if 0x561[0] is 1'b0 1b0 = Normal send_s debug. Refer to 0x561[1] 1b1 = Enabled xcorr debug
2	cfg_ecc_en	R/W	1b0	Enable ECC logic for RS decoder memory 1b0 = ECC encoding/decoding is disabled 1b1 = ECC encoding/decoding is enabled
1	cfg_test_mem_sigdet_debug	R/W	1b0	Enable sidget debug mode in test mem send s mode Valid only if 0x561[0] is 1'b0 1b0 = Test mem written in send s mode only on state transition 1b1 = Enable sigdet debug mode in test mem send s mode
0	cfg_pcs_test_mem_mode	R/W	1b0	Choose send s or train rx test mem mode 1b0 = Send s info on test mem 1b1 = Train rx info on test mem

7.6.2.53 MBIST_CTRL Register (Address = 0x580) [reset = 0x0]

MBIST_CTRL is shown in Table 7-76.

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Table 7-76. MBIST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	9b000000000	Reserved
6	dftreadb_0	R/W	1b0	
5	dftreada_0	R/W	1b0	
4	test_resume_h	R/W	1b0	
3	rst_l	R/W	1b0	
2	test_h	R/W	1b0	
1	tmb_0	R/W	1b0	
0	tma_0	R/W	1b0	

7.6.2.54 MBIST_STAT Register (Address = 0x581) [reset = 0x0]

MBIST_STAT is shown in Table 7-77.

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Table 7-77. MBIST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	13b0000000000000	Reserved
2	fail_h_0	R	1b0	
1	tst_done	R	1b0	
0	start_retention_h	R	1b0	

7.6.2.55 RGMII_CTRL Register (Address = 0x600) [reset = 0x120]

RGMII_CTRL is shown in Table 7-78.

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Table 7-78. RGMII_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	6b000000	Reserved
9-7	rgmii_rx_half_full_th	R/W	3b010	RGMII RX sync FIFO half full threshold
6-4	rgmii_tx_half_full_th	R/W	3b010	RGMII TX sync FIFO half full threshold
3	rgmii_tx_if_en	R/W	1b0	RGMII enable bit Default from strap 1b0 = RGMII disable 1b1 = RGMII enable
2	invert_rgmii_txd	R/W	1b0	Invert RGMII Tx wire order - full swap [3:0] to [0:3] 1b0 = Keep RGMII Tx wire order same - [3: 1b1 = Invert RGMII Tx wire order - [3:
1	invert_rgmii_rxd	R/W	1b0	Invert RGMII Rx wire order - full swap [3:0] to [0:3] 1b0 = Keep RGMII Rx wire order same - [3: 1b1 = Invert RGMII Rx wire order - [3:
0	sup_tx_err_fd	R/W	1b0	1: suppress tx_err in full duplex mode when tx_en set to zero 0: allow tx_err assertion to PHY when tx_en set to zero (this bit can disable the TX_ERR indication input) 1b0 = allow tx_err assertion to PHY when tx_en set to zero 1b1 = suppress tx_err in full duplex mode when tx_en set to zero

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7.6.2.56 RGMII_FIFO_STATUS Register (Address = 0x601) [reset = 0x0]

RGMII_FIFO_STATUS is shown in Table 7-79.

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Table 7-79. RGMII_FIFO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	12b000000000000	Reserved
3	rgmii_rx_af_full_err	R/W0C	1b0	RGMII RX fifo full error 1b0 = No empty fifo error 1b1 = RGMII TX full error has been indicated
2	rgmii_rx_af_empty_err	R/W0C	1b0	RGMII RX fifo empty error 1b0 = No empty fifo error 1b1 = RGMII RX empty error has been indicated
1	rgmii_tx_af_full_err	R/W0C	1b0	RGMII TX fifo full error 1b0 = No empty fifo error 1b1 = RGMII TX full error has been indicated
0	rgmii_tx_af_empty_err	R/W0C	1b0	RGMII TX fifo empty error 1b0 = No empty fifo error 1b1 = RGMII TX empty error has been indicated

7.6.2.57 RGMII_DELAY_CTRL Register (Address = 0x602) [reset = 0x0]

RGMII_DELAY_CTRL is shown in Table 7-80.

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Table 7-80. RGMII_DELAY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	14b00000000000000	Reserved
1	rx_clk_sel	R/W	1b0	In RGMII mode, Enable or disable the internal delay for RXD wrt RX_CLK (use this mode when RGMII_RX_CLK and RGMII_RXD are aligned). The delay magnitude can be configured by programming register 0x430[7:4] 1b0 = clock and data are aligned 1b1 = clock on PIN is delayed by 90 degrees relative to RGMII_RX data
0	tx_clk_sel	R/W	1b0	In RGMII mode, Enable or disable the internal delay for TXD wrt TX_CLK (use this mode when RGMII_TX_CLK and RGMII_TXD are aligned). The delay magnitude can be configured by programming register 0x430[11:8] 1b0 = clock and data are aligned 1b1 = clock is internally delayed by 90 degrees

7.6.2.58 SGMII_CTRL_1 Register (Address = 0x608) [reset = 0x7B]

SGMII_CTRL_1 is shown in Table 7-81.

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Table 7-81. SGMII_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	sgmii_tx_err_dis	R/W	1b0	1 = Disable SGMII TX Error indication 0 = Enable SGMII TX Error indication 1b0 = Enable SGMII TX Error indication 1b1 = Disable SGMII TX Error indication
14	cfg_align_idx_force	R/W	1b0	Force word boundray index selection
13-10	cfg_align_idx_value	R/W	4b0000	when cfg_align_idx_force = '1' This value set the iword boundray index
9	cfg_sgmii_en	R/W	1b0	SGMII enable bit Default from strap 1b0 = SGMII disable 1b1 = SGMII enable
8	cfg_sgmii_rx_pol_invert	R/W	1b0	SGMII RX bus invert polarity 1b0 = Polarity not inverted 1b1 = SGMII RX bus invert polarity
7	cfg_sgmii_tx_pol_invert	R/W	1b0	SGMII TX bus invert polarity 1b0 = Polarity not inverted 1b1 = SGMII TX bus invert polarity
6-5	serdes_tx_bits_order	R/W	2b11	SERDES TX bits order (input to digital core) : 00 - MSB-first in every SERDES data (10 bits) , 1st SERDES data goes to LSB of comma detect's 20bits bus (default) 01 - LSB-first in every SERDES data (10 bits) , 1st SERDES data goes to LSB of comma detect's 20bits bus 10 - MSB-first in every SERDES data (10 bits) , 1st SERDES data goes to MSB of comma detect's 20bits bus 11 - LSB-first in every SERDES data (10 bits) , 1st SERDES data goes to MSB of comma detect's 20bits bus 2b00 = MSB-first in every SERDES data (10 bits) , 1st SERDES data goes to LSB of comma detect's 20bits bus (default) 2b01 = LSB-first in every SERDES data (10 bits) , 1st SERDES data goes to LSB of comma detect's 20bits bus 2b10 = MSB-first in every SERDES data (10 bits) , 1st SERDES data goes to MSB of comma detect's 20bits bus 2b11 = LSB-first in every SERDES data (10 bits) , 1st SERDES data goes to MSB of comma detect's 20bits bus
4	serdes_rx_bits_order	R/W	1b1	SERDES RX bits order (output of digital core) : 0 - MSB-first 1 - LSB-first (reversed order) 1b0 = MSB-first 1b1 = LSB-first (reversed order)
3	cfg_align_pkt_en	R/W	1b1	For aligning the start of read out TX packet (towards serializer) w/ tx_even pulse. To sync with the Code_Group/OSET FSM code slots. Default is '1', when using '0' we go back to Gemini code

Table 7-81. SGMII_CTRL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-1	sgmii_autoneg_timer	R/W	2b01	Selects duration of SGMII Auto-Negotiation timer: 00: 1.6ms 01: 2us 10: 800us 11: 11ms 2b00 = 1.6ms 2b01 = 2us 2b10 = 800us 2b11 = 11ms
0	mr_an_enable	R/W	1b1	1 = Enable SGMII Auto-Negotaition 0 = Disable SGMII Auto-Negotiation 1b0 = Disable SGMII Auto-Negotiation 1b1 = Enable SGMII Auto-Negotaition

7.6.2.59 SGMII_EEE_CTRL_1 Register (Address = 0x609) [reset = 0x6318]

SGMII_EEE_CTRL_1 is shown in Table 7-82.

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Table 7-82. SGMII_EEE_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	cfg_tx_tr_timer_val	R/W	5b01100	
10-6	cfg_tx_tq_timer_val	R/W	5b01100	
5-1	cfg_tx_ts_timer_val	R/W	5b01100	
0	cfg_support_non_eee_mac_sgmii_en	R/W	1b0	special mode to support non sgmii eee mac in eee mode in the phy

7.6.2.60 SGMII_STATUS Register (Address = 0x60A) [reset = 0x0]

SGMII_STATUS is shown in Table 7-83.

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Table 7-83. SGMII_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	3b000	Reserved
12	sgmii_page_received	R	1b0	Indicates that a new auto neg page was received 1b0 = No new auto neg page received 1b1 = A new auto neg page received
11	link_status_1000bx	R	1b0	sgmii link status 1b0 = SGMII link down 1b1 = SGMII link up
10	mr_an_complete	R	1b0	sgmii autoneg complete indication 1b0 = SGMII autoneg not completed 1b1 = SGMII autoneg completed
9	cfg_align_en	R	1b0	word boundary FSM - align indication
8	cfg_sync_status	R	1b0	word boundary FSM - sync status indication 1b0 = sync not achieved 1b1 = sync achieved
7-4	cfg_align_idx	R	4b0000	word boundary index selection
3-0	cfg_state	R	4b0000	word boundary FSM state

7.6.2.61 SGMII_EEE_CTRL_2 Register (Address = 0x60B) [reset = 0x5]

SGMII_EEE_CTRL_2 is shown in Table 7-84.

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Table 7-84. SGMII_EEE_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	12b000000000000	Reserved
3-0	cfg_rx_quiet_timer_val	R/W	4b0101	

7.6.2.62 SGMII_CTRL_2 Register (Address = 0x60C) [reset = 0x1B]

SGMII_CTRL_2 is shown in Table 7-85.

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Table 7-85. SGMII_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	7b0000000	Reserved
8	sgmii_signal_detect_force_val	R/W	1b0	SGMII cdr lock force value
7	sgmii_signal_detect_force_en	R/W	1b0	SGMII cdr lock force enable
6	mr_restart_an	R/WSC,0	1b0	Restart sgmii autonegotiation
5-3	tx_half_full_th	R/W	3b011	SGMII TX sync FIFO half full threshold
2-0	rx_half_full_th	R/W	3b011	SGMII RX sync FIFO half full threshold

7.6.2.63 SGMII_FIFO_STATUS Register (Address = 0x60D) [reset = 0x0]

SGMII_FIFO_STATUS is shown in Table 7-86.

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Table 7-86. SGMII_FIFO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	12b000000000000	Reserved
3	sgmii_rx_af_full_err	R/W0C	1b0	SGMII RX fifo full error 1b0 = No error indication 1b1 = SGMII RX fifo full error has been indicated
2	sgmii_rx_af_empty_err	R/W0C	1b0	SGMII RX fifo empty error 1b0 = No error indication 1b1 = SGMII RX fifo empty error has been indicated
1	sgmii_tx_af_full_err	R/W0C	1b0	SGMII TX fifo full error 1b0 = No error indication 1b1 = SGMII TX fifo full error has been indicated
0	sgmii_tx_af_empty_err	R/W0C	1b0	SGMII TX fifo empty error 1b0 = No error indication 1b1 = SGMII TX fifo empty error has been indicated

7.6.2.64 PRBS_STATUS_1 Register (Address = 0x618) [reset = 0x0]

PRBS_STATUS_1 is shown in Table 7-87.

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Table 7-87. PRBS_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	8b00000000	Reserved
7-0	prbs_err_ov_cnt	R	8b00000000	Holds number of error counter overflow that received by the PRBS checker. Value in this register is locked when write is done to register prbs_status_6 bit[0] or bit[1]. Counter stops on 0xFF. Note: when PRBS counters work in single mode, overflow counter is not active

7.6.2.65 PRBS_CTRL_1 Register (Address = 0x619) [reset = 0x574]

PRBS_CTRL_1 is shown in Table 7-88.

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Table 7-88. PRBS_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	2b00	Reserved
13	cfg_pkt_gen_64	R/W	1b0	Reserved
12	send_pkt	R/WMC,0	1b0	Enables generating MAC packet with fix/incremental data w CRC (pkt_gen_en has to be set and cfg_pkt_gen_prbs has to be clear) Cleared automatically when pkt_done is set 1b0 = Stop MAC packet 1b1 = Transmit MAC packet w CRC
11	RESERVED	R	1b0	Reserved
10-8	cfg_prbs_chk_sel	R/W	3b101	000 : Checker receives from RGMII TX 001 : Checker receives SGMII TX 101 : Checker receives from Cu RX 3b000 = Checker receives from RGMII TX 3b001 = Checker receives SGMII TX 3b101 = Checker receives from Cu RX
7	RESERVED	R	1b0	Reserved
6-4	cfg_prbs_gen_sel	R/W	3b111	000 : PRBS transmits to RGMII RX 001 : PRBS transmits to SGMII RX 101 : PRBS transmits to Cu TX 3b000 = PRBS transmits to RGMII RX 3b001 = PRBS transmits to SGMII RX 3b101 = PRBS transmits to Cu TX
3	cfg_prbs_cnt_mode	R/W	1b0	1 = Continuous mode, when one of the PRBS counters reaches max value, pulse is generated and counter starts counting from zero again 0 = Single mode, When one of the PRBS counters reaches max value, PRBS checker stops counting. 1b0 = Single mode, When one of the PRBS counters reaches max value, PRBS checker stops counting. 1b1 = Continuous mode, when one of the PRBS counters reaches max value, pulse is generated and counter starts counting from zero again
2	cfg_prbs_chk_enable	R/W	1b1	Enable PRBS checker xbar (to receive data) To be enabled for counters in 0x63C, 0x63D, 0x63E to work 1b0 = Disable PRBS checker 1b1 = Enable PRBS checker
1	cfg_pkt_gen_prbs	R/W	1b0	If set: (1) When pkt_gen_en is set, PRBS packets are generated continuously (3) When pkt_gen_en is cleared, PRBS RX checker is still enabled If cleared: (1) When pkt_gen_en is set, non - PRBS packet is generated (3) When pkt_gen_en is cleared, PRBS RX checker is disabled as well 1b0 = Stop PRBS packet 1b1 = Transmit PRBS packet

Table 7-88. PRBS_CTRL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	pkt_gen_en	R/W	1b0	1 = Enable packet/PRBS generator 0 = Disable packet/PRBS generator 1b0 = Disable packet/PRBS generator 1b1 = Enable packet/PRBS generator

7.6.2.66 PRBS_CTRL_2 Register (Address = 0x61A) [reset = 0x5DC]

PRBS_CTRL_2 is shown in Table 7-89.

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Table 7-89. PRBS_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	cfg_pkt_len_prbs	R/W	16b0000010 111011100	Length (in bytes) of PRBS packets and MAC packets w CRC

7.6.2.67 PRBS_CTRL_3 Register (Address = 0x61B) [reset = 0x7D]

PRBS_CTRL_3 is shown in Table 7-90.

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Table 7-90. PRBS_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	8b00000000	Reserved
7-0	cfg_ipg_len	R/W	8b01111101	Inter-packet gap (in bytes) between packets

7.6.2.68 PRBS_STATUS_2 Register (Address = 0x61C) [reset = 0x0]

PRBS_STATUS_2 is shown in Table 7-91.

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Table 7-91. PRBS_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	prbs_byte_cnt	R	16b0000000000000000	Holds number of total bytes that received by the PRBS checker. Value in this register is locked when write is done to register prbs_status_6 bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFF

7.6.2.69 PRBS_STATUS_3 Register (Address = 0x61D) [reset = 0x0]

PRBS_STATUS_3 is shown in Table 7-92.

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Table 7-92. PRBS_STATUS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	prbs_pkt_cnt_15_0	R	16b0000000 000000000	Bits [15:0] of number of total packets received by the PRBS checker Value in this register is locked when write is done to register prbs_status_6 bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF

7.6.2.70 PRBS_STATUS_4 Register (Address = 0x61E) [reset = 0x0]

PRBS_STATUS_4 is shown in Table 7-93.

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Table 7-93. PRBS_STATUS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	prbs_pkt_cnt_31_16	R	16b0000000000000000	Bits [31:16] of number of total packets received by the PRBS checker Value in this register is locked when write is done to register prbs_status_6 bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF

7.6.2.71 PRBS_STATUS_6 Register (Address = 0x620) [reset = 0x0]

PRBS_STATUS_6 is shown in Table 7-94.

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Table 7-94. PRBS_STATUS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	3b000	Reserved
12	pkt_done	R	1b0	Set when all MAC packets w CRC are transmitted 1b0 = MAC packet transmission in progress 1b1 = MAC packets transmission completed
11	pkt_gen_busy	R	1b0	1 = Packet generator is in process 0 = Packet generator is not in process 1b0 = Packet generator is not in process 1b1 = Packet generator is in process
10	prbs_pkt_ov	R	1b0	If set, packet counter reached overflow Overflow is cleared when PRBS counters are cleared - done by setting bit #1 of prbs_status_6 1b0 = No overflow 1b1 = Packet counter overflow
9	prbs_byte_ov	R	1b0	If set, bytes counter reached overflow Overflow is cleared when PRBS counters are cleared - done by setting bit #1of prbs_status_6 1b0 = No overflow 1b1 = byte counter overflow
8	prbs_lock	R	1b0	1 = PRBS checker is locked sync) on received byte stream 0 = PRBS checker is not locked 1b0 = PRBS checker is not locked 1b1 = PRBS checker is locked sync) on received byte stream
7-0	prbs_err_cnt	R	8b00000000	Holds number of errored bits received by the PRBS checker Value in this register is locked when write is done to bit[0] or bit[1] When PRBS Count Mode set to zero, count stops on 0xFF Notes: Writing bit 0 generates a lock signal for the PRBS counters. Writing bit 1 generates a lock and clear signal for the PRBS counters

7.6.2.72 PRBS_STATUS_8 Register (Address = 0x622) [reset = 0x0]

PRBS_STATUS_8 is shown in Table 7-95.

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Table 7-95. PRBS_STATUS_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pkt_err_cnt_15_0	R	16b0000000000000000	Bits [15:0] of number of total packets with error received by the PRBS checker Value in this register is locked when write is done to register prbs_status_6 bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF

7.6.2.73 PRBS_STATUS_9 Register (Address = 0x623) [reset = 0x0]

PRBS_STATUS_9 is shown in Table 7-96.

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Table 7-96. PRBS_STATUS_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pkt_err_cnt_31_16	R	16b0000000000000000	Bits [31:16] of number of total packets with error received by the PRBS checker Value in this register is locked when write is done to register prbs_status_6 bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF

7.6.2.74 PRBS_CTRL_4 Register (Address = 0x624) [reset = 0x5511]

PRBS_CTRL_4 is shown in Table 7-97.

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Table 7-97. PRBS_CTRL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_pkt_data	R/W	8b01010101	Fixed data to be sent in Fix data mode
7-6	cfg_pkt_mode	R/W	2b00	2'b00 - Incremental 2'b01 - Fixed 2'b1x - PRBS 2b00 = Incremental 2b01 = Fixed
5-3	cfg_pattern_vld_bytes	R/W	3b010	Number of bytes of valid pattern in packet (Max - 6) 3b000 = 0 bytes 3b001 = 1 bytes 3b010 = 2 bytes 3b011 = 3 bytes 3b100 = 4 bytes 3b101 = 5 bytes 3b110 = 6 bytes 3b111 = 6 bytes
2-0	cfg_pkt_cnt	R/W	3b001	000b = 1 packet 001b = 10 packets 010b = 100 packets 011b = 1000 packets 100b = 10000 packets 101b = 100000 packets 110b = 1000000 packets 111b = Continuous packets 3b000 = 1 packet 3b001 = 10 packets 3b010 = 100 packets 3b011 = 1000 packets 3b100 = 10000 packets 3b101 = 100000 packets 3b110 = 1000000 packets 3b111 = Continuous packets

7.6.2.75 PRBS_CTRL_5 Register (Address = 0x625) [reset = 0x0]

PRBS_CTRL_5 is shown in Table 7-98.

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Table 7-98. PRBS_CTRL_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pattern_15_0	R/W	16b0000000 000000000	Bits 15:0 of pattern

7.6.2.76 PRBS_CTRL_6 Register (Address = 0x626) [reset = 0x0]

PRBS_CTRL_6 is shown in Table 7-99.

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Table 7-99. PRBS_CTRL_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pattern_31_16	R/W	16b0000000000000000	Bits 31:16 of pattern

7.6.2.77 PRBS_CTRL_7 Register (Address = 0x627) [reset = 0x0]

PRBS_CTRL_7 is shown in Table 7-100.

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Table 7-100. PRBS_CTRL_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pattern_47_32	R/W	16b0000000000000000	Bits 47:32 of pattern

7.6.2.78 PRBS_CTRL_8 Register (Address = 0x628) [reset = 0x0]

PRBS_CTRL_8 is shown in Table 7-101.

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Table 7-101. PRBS_CTRL_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pmatch_data_15_0	R/W	16b0000000 000000000	Bits 15:0 of Perfect Match Data - used for DA (destination address) match

7.6.2.79 PRBS_CTRL_9 Register (Address = 0x629) [reset = 0x0]

PRBS_CTRL_9 is shown in Table 7-102.

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Table 7-102. PRBS_CTRL_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pmatch_data_31_16	R/W	16b0000000 000000000	Bits 31:16 of Perfect Match Data - used for DA (destination address) match

7.6.2.80 PRBS_CTRL_10 Register (Address = 0x62A) [reset = 0x0]

PRBS_CTRL_10 is shown in Table 7-103.

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Table 7-103. PRBS_CTRL_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pmatch_data_47_32	R/W	16b0000000 000000000	Bits 47:32 of Perfect Match Data - used for DA (destination address) match

7.6.2.81 CRC_STATUS Register (Address = 0x638) [reset = 0x0]

CRC_STATUS is shown in Table 7-104.

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Table 7-104. CRC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	14b00000000000000	Reserved
1	rx_bad_crc	R	1b0	CRC error indication in packet received on Cu RX 1b0 = No CRC error 1b1 = CRC error
0	tx_bad_crc	R	1b0	CRC error indication in packet transmitted on Cu TX 1b0 = No CRC error 1b1 = CRC error

7.6.2.82 PKT_STAT_1 Register (Address = 0x639) [reset = 0x0]

PKT_STAT_1 is shown in Table 7-105.

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Table 7-105. PKT_STAT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	tx_pkt_cnt_15_0		16b0000000000000000	Lower 16 bits of Tx packet counter Note : Register is cleared when 0x39, 0x3A, 0x3B are read in sequence

7.6.2.83 PKT_STAT_2 Register (Address = 0x63A) [reset = 0x0]

PKT_STAT_2 is shown in Table 7-106.

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Table 7-106. PKT_STAT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	tx_pkt_cnt_31_16		16b0000000 000000000	Upper 16 bits of Tx packet counter Note : Register is cleared when 0x39, 0x3A, 0x3B are read in sequence

7.6.2.84 PKT_STAT_3 Register (Address = 0x63B) [reset = 0x0]

PKT_STAT_3 is shown in Table 7-107.

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Table 7-107. PKT_STAT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	tx_err_pkt_cnt		16b0000000 000000000	Tx packet w error (CRC error) counter Note : Register is cleared when 0x39, 0x3A, 0x3B are read in sequence

7.6.2.85 PKT_STAT_4 Register (Address = 0x63C) [reset = 0x0]

PKT_STAT_4 is shown in Table 7-108.

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Table 7-108. PKT_STAT_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rx_pkt_cnt_15_0		16b0000000000000000	Lower 16 bits of Rx packet counter Note : Register is cleared when 0x3C, 0x3D, 0x3E are read in sequence

7.6.2.86 PKT_STAT_5 Register (Address = 0x63D) [reset = 0x0]

PKT_STAT_5 is shown in Table 7-109.

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Table 7-109. PKT_STAT_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rx_pkt_cnt_31_16		16b0000000000000000	Upper 16 bits of Rx packet counter Note : Register is cleared when 0x3C, 0x3D, 0x3E are read in sequence

7.6.2.87 PKT_STAT_6 Register (Address = 0x63E) [reset = 0x0]

PKT_STAT_6 is shown in Table 7-110.

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Table 7-110. PKT_STAT_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rx_err_pkt_cnt		16b0000000 000000000	Rx packet w error (CRC error) counter Note : Register is cleared when 0x3C, 0x3D, 0x3E are read in sequence

7.6.2.88 SQI_1 Register (Address = 0x8AD) [reset = 0x3051]

SQI_1 is shown in Table 7-111.

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Table 7-111. SQI_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	cfg_hist_1_2	R/W	4b0011	Hysteresis between SQI value 1 and 2
11-10	cfg_acc_window_sel	R/W	2b00	Accumulator window select - 00b = 90us 01b = 180us 10b = 360us 11b = 720us
9-0	cfg_sqi_th_1_2	R/W	10b0001010001	Threshold between SQI value 1 and 2

7.6.2.89 SQI_2 Register (Address = 0x8ED) [reset = 0x3041]

SQI_2 is shown in Table 7-112.

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Table 7-112. SQI_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	cfg_hist_2_3	R/W	4b0011	Hysteresis between SQI value 2 and 3
11-10	RESERVED	R	2b00	Reserved
9-0	cfg_sqi_th_2_3	R/W	10b0001000001	Threshold between SQI value 2 and 3

7.6.2.90 SQI_3 Register (Address = 0x8EF) [reset = 0x3033]

SQI_3 is shown in Table 7-113.

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Table 7-113. SQI_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	cfg_hist_3_4	R/W	4b0011	Hysteresis between SQI value 3 and 4
11-10	RESERVED	R	2b00	Reserved
9-0	cfg_sqi_th_3_4	R/W	10b0000110011	Threshold between SQI value 3 and 4

7.6.2.91 SQI_4 Register (Address = 0x8F0) [reset = 0x3029]

SQI_4 is shown in Table 7-114.

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Table 7-114. SQI_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	cfg_hist_4_5	R/W	4b0011	Hysteresis between SQI value 4 and 5
11-10	RESERVED	R	2b00	Reserved
9-0	cfg_sqi_th_4_5	R/W	10b0000101001	Threshold between SQI value 4 and 5

7.6.2.92 SQI_5 Register (Address = 0x8F1) [reset = 0x2020]

SQI_5 is shown in Table 7-115.

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Table 7-115. SQI_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	cfg_hist_5_6	R/W	4b0010	Hysteresis between SQI value 5 and 6
11-10	RESERVED	R	2b00	Reserved
9-0	cfg_sqi_th_5_6	R/W	10b0000100000	Threshold between SQI value 5 and 6

7.6.2.93 SQI_6 Register (Address = 0x8F2) [reset = 0x2019]

SQI_6 is shown in Table 7-116.

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Table 7-116. SQI_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	cfg_hist_6_7	R/W	4b0010	Hysteresis between SQI value 6 and 7
11-10	RESERVED	R	2b00	Reserved
9-0	cfg_sqi_th_6_7	R/W	10b0000011001	Threshold between SQI value 6 and 7

7.6.2.94 DSP_DEBUG2_REG_40 Register (Address = 0xA40) [reset = 0x0]

DSP_DEBUG2_REG_40 is shown in Table 7-117.

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Table 7-117. DSP_DEBUG2_REG_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	16b0000000000000000	Reserved

7.6.2.95 DSP_DEBUG2_REG_41 Register (Address = 0xA41) [reset = 0x0]

DSP_DEBUG2_REG_41 is shown in Table 7-118.

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Table 7-118. DSP_DEBUG2_REG_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	16b0000000000000000	Reserved

7.6.2.96 DSP_DEBUG2_REG_42 Register (Address = 0xA42) [reset = 0x0]

DSP_DEBUG2_REG_42 is shown in Table 7-119.

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Table 7-119. DSP_DEBUG2_REG_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	16b0000000000000000	Reserved

7.6.2.97 DSP_DEBUG2_REG_81 Register (Address = 0xA81) [reset = 0x0]

DSP_DEBUG2_REG_81 is shown in Table 7-120.

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Table 7-120. DSP_DEBUG2_REG_81 Register Field Descriptions

Bit	Field	Type	Reset	Description
12-8	PGA_ATTN_LVL	R	5b00000	Read back value for RX PATH attenuation. Used for cable Emulation. See https://confluence.itg.ti.com/display/DP83720/9.10+Cable+Length+Emulator and document attached to this page.
7-0	RESERVED	R	8b00000000	

7.6.2.98 DSP_DEBUG2_REG_86 Register (Address = 0xA86) [reset = 0x0]

DSP_DEBUG2_REG_86 is shown in Table 7-121.

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Table 7-121. DSP_DEBUG2_REG_86 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MSE	R	16b0000000000000000	Debug read access for the MSE which is an indicator of signal quality. Will increase with increase in cable length. Used for cable Emulation. See https://confluence.itg.ti.com/display/DP83720/9.10+Cable+Length+Emulator and document attached to this page.

7.6.2.99 PMA_PMD_CONTROL_1 Register (Address = 0x1000) [reset = 0x0]

PMA_PMD_CONTROL_1 is shown in Table 7-122.

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Table 7-122. PMA_PMD_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	pma_reset_2	R	1b0	1 = PMA/PMD reset 0 = Normal operation Note - RW bit, self clearing Note - 0x1 added in [15:12] to differentiate 1b0 = Normal operation 1b1 = PMA/PMD reset
14-12	RESERVED	R	3b000	Reserved
11	cfg_low_power_2	R	1b0	1 = Low-power mode 0 = Normal operation Note - RW bit Note - 0x1 added in [15:12] to differentiate 1b0 = Normal operation 1b1 = Low-power mode
10-0	RESERVED	R	11b00000000000	Reserved

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7.6.2.100 PMA_PMD_CONTROL_2 Register (Address = 0x1007) [reset = 0x3D]

PMA_PMD_CONTROL_2 is shown in Table 7-123.

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Table 7-123. PMA_PMD_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	10b0000000000	Reserved
5-0	cfg_pma_type_selection	R/W	6b111101	BASE-T1 type selection for device Note - 0x1 added in [15:12] to differentiate 6b111101 = BASE-T1 type selection for device

7.6.2.101 PMA_PMD_TRANSMIT_DISABLE Register (Address = 0x1009) [reset = 0x0]

PMA_PMD_TRANSMIT_DISABLE is shown in Table 7-124.

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Table 7-124. PMA_PMD_TRANSMIT_DISABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	15b000000000000000	Reserved
0	cfg_transmit_disable_2	R	1b0	1 = Transmit disable 0 = Normal operation Note - RW bit Note - 0x1 added in [15:12] to differentiate 1b0 = Normal operation 1b1 = Transmit disable

7.6.2.102 PMA_PMD_EXTENDED_ABILITY2 Register (Address = 0x100B) [reset = 0x800]

PMA_PMD_EXTENDED_ABILITY2 is shown in Table 7-125.

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Table 7-125. PMA_PMD_EXTENDED_ABILITY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	4b0000	Reserved
11	base_t1_extended_abilities	R	1b1	1 = PMA/PMD has BASE-T1 extended abilities listed in register 1.18 0 = PMA/PMD does not have BASE-T1 extended abilities Note - 0x1 added in [15:12] to differentiate 1b0 = PMA/PMD does not have BASE-T1 extended abilities 1b1 = PMA/PMD has BASE-T1 extended abilities listed in register 1.18
10-0	RESERVED	R	11b00000000000	Reserved

7.6.2.103 PMA_PMD_EXTENDED_ABILITY Register (Address = 0x1012) [reset = 0x2]

PMA_PMD_EXTENDED_ABILITY is shown in Table 7-126.

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Table 7-126. PMA_PMD_EXTENDED_ABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	14b00000000000000	Reserved
1	mr_1000_base_t1_ability	R	1b1	1 = PMA/PMD is able to perform 1000BASE-T1 0 = PMA/PMD is not able to perform 1000BASE-T1 Note - 0x1 added in [15:12] to differentiate 1b0 = PMA/PMD is not able to perform 1000BASE-T1 1b1 = PMA/PMD is able to perform 1000BASE-T1
0	mr_100_base_t1_ability	R	1b0	1 = PMA/PMD is able to perform 100BASE-T1 0 = PMA/PMD is not able to perform 100BASE-T1 Note - 0x1 added in [15:12] to differentiate 1b0 = PMA/PMD is not able to perform 100BASE-T1 1b1 = PMA/PMD is able to perform 100BASE-T1

7.6.2.104 PMA_PMD_CONTROL Register (Address = 0x1834) [reset = 0x8001]

PMA_PMD_CONTROL is shown in Table 7-127.

Return to the Summary Table.

Table 7-127. PMA_PMD_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	1b1	Reserved
14	cfg_master_slave_val	R/W	1b0	1 = Configure PHY as MASTER 0 = Configure PHY as SLAVE Note - 0x1 added in [15:12] to differentiate 1b0 = Configure PHY as SLAVE 1b1 = Configure PHY as MASTER
13-4	RESERVED	R	10b0000000000	Reserved
3-0	cfg_type_selection	R/W	4b0001	0000 = 100BASE-T1 0001 = 1000BASE-T1 Note - 0x1 added in [15:12] to differentiate 4b0000 = 100BASE-T1 4b0001 = 1000BASE-T1

7.6.2.105 PMA_CONTROL Register (Address = 0x1900) [reset = 0x0]

PMA_CONTROL is shown in Table 7-128.

Return to the Summary Table.

Table 7-128. PMA_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	pma_reset	R	1b0	1 = PMA/PMD reset 0 = Normal operation Note - RW bit, self clearing Note - 0x1 added in [15:12] to differentiate 1b0 = Normal operation 1b1 = PMA/PMD reset
14	cfg_transmit_disable	R	1b0	1 = Transmit disable 0 = Normal operation Note - RW bit Note - 0x1 added in [15:12] to differentiate 1b0 = Normal operation 1b1 = Transmit disable
13-12	RESERVED	R	2b00	Reserved
11	cfg_low_power	R	1b0	1 = Low-power mode 0 = Normal operation Note - RW bit Note - 0x1 added in [15:12] to differentiate 1b0 = Normal operation 1b1 = Low-power mode
10-0	RESERVED	R	11b00000000000	Reserved

7.6.2.106 PMA_STATUS Register (Address = 0x1901) [reset = 0x900]

PMA_STATUS is shown in Table 7-129.

Return to the Summary Table.

Table 7-129. PMA_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	4b0000	Reserved
11	oam_ability	R	1b1	1 = PHY has 1000BASE-T1 OAM ability 0 = PHY does not have 1000BASE-T1 OAM ability Note - 0x1 added in [15:12] to differentiate 1b0 = PHY does not have 1000BASE-T1 OAM ability 1b1 = PHY has 1000BASE-T1 OAM ability
10	eee_ability	R	1b0	1 = PHY has EEE ability 0 = PHY does not have EEE ability Note - 0x1 added in [15:12] to differentiate 1b0 = PHY does not have EEE ability 1b1 = PHY has EEE ability
9	receive_fault_ability	R	1b0	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path Note - 0x1 added in [15:12] to differentiate 1b0 = PMA/PMD does not have the ability to detect a fault condition on the receive path 1b1 = PMA/PMD has the ability to detect a fault condition on the receive path
8	low_power_ability	R	1b1	1 = PMA/PMD has low-power ability 0 = PMA/PMD does not have low-power ability Note - 0x1 added in [15:12] to differentiate 1b0 = PMA/PMD does not have low-power ability 1b1 = PMA/PMD has low-power ability
7-3	RESERVED	R	5b00000	Reserved
2	receive_polarity	R	1b0	1 = Receive polarity is reversed 0 = Receive polarity is not reversed Note - 0x1 added in [15:12] to differentiate 1b0 = Receive polarity is not reversed 1b1 = Receive polarity is reversed
1	receive_fault	R	1b0	1 = Fault condition detected 0 = Fault condition not detected Note - 0x1 added in [15:12] to differentiate 1b0 = Fault condition not detected 1b1 = Fault condition detected
0	pma_receive_link_status_ll	R/W0S	1b0	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down Note - 0x1 added in [15:12] to differentiate 1b0 = PMA/PMD receive link down 1b1 = PMA/PMD receive link up

7.6.2.107 TRAINING Register (Address = 0x1902) [reset = 0x2]

TRAINING is shown in Table 7-130.

Return to the Summary Table.

Table 7-130. TRAINING Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	5b00000	Reserved
10-4	cfg_training_user_fld	R/W	7b0000000	7-bit user defined field to send to the link partner Note - 0x1 added in [15:12] to differentiate
3-2	RESERVED	R	2b00	Reserved
1	cfg_oam_en	R/W	1b1	1 = 1000BASE-T1 OAM ability advertised to link partner 0 = 1000BASE-T1 OAM ability not advertised to link partner Note - 0x1 added in [15:12] to differentiate 1b0 = 1000BASE-T1 OAM ability not advertised to link partner 1b1 = 1000BASE-T1 OAM ability advertised to link partner
0	cfg_eee_en	R/W	1b0	1 = EEE ability advertised to link partner 0 = EEE ability not advertised to link partner Note - 0x1 added in [15:12] to differentiate 1b0 = EEE ability not advertised to link partner 1b1 = EEE ability advertised to link partner

7.6.2.108 LP_TRAINING Register (Address = 0x1903) [reset = 0x0]

LP_TRAINING is shown in Table 7-131.

Return to the Summary Table.

Table 7-131. LP_TRAINING Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	5b00000	Reserved
10-4	lp_training_user_fld	R	7b0000000	7-bit user defined field received from the link partner Note - 0x1 added in [15:12] to differentiate
3-2	RESERVED	R	2b00	Reserved
1	lp_oam_adv	R	1b0	1 = Link partner has 1000BASE-T1 OAM ability 0 = Link partner does not have 1000BASE-T1 OAM ability Note - 0x1 added in [15:12] to differentiate 1b0 = Link partner does not have 1000BASE-T1 OAM ability 1b1 = Link partner has 1000BASE-T1 OAM ability
0	lp_eee_adv	R	1b0	1 = Link partner has EEE ability 0 = Link partner does not have EEE ability Note - 0x1 added in [15:12] to differentiate 1b0 = Link partner does not have EEE ability 1b1 = Link partner has EEE ability

7.6.2.109 TEST_MODE_CONTROL Register (Address = 0x1904) [reset = 0x0]

TEST_MODE_CONTROL is shown in Table 7-132.

Return to the Summary Table.

Table 7-132. TEST_MODE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	cfg_test_mode	R/W	3b000	111b = Test mode 7 110b = Test mode 6 101b = Test mode 5 100b = Test mode 4 011b = Reserved 010b = Test mode 2 001b = Test mode 1 000b = Normal (non-test) operation Note - 0x1 added in [15:12] to differentiate 3b000 = Normal (non-test) operation 3b001 = Test mode 1 3b010 = Test mode 2 3b011 = Reserved 3b100 = Test mode 4 3b101 = Test mode 5 3b110 = Test mode 6 3b111 = Test mode 7
12-0	RESERVED	R	13b0000000000000	Reserved

7.6.2.110 PCS_CONTROL_COPY Register (Address = 0x3000) [reset = 0x0]

PCS_CONTROL_COPY is shown in Table 7-133.

Return to the Summary Table.

Table 7-133. PCS_CONTROL_COPY Register Field Descriptions

Bit	Field	Type	Reset	Description
15	pcs_reset_2	R	1b0	1 = PCS reset 0 = Normal operation Note - RW bit, self clear bit Note - 0x3 added in [15:12] to differentiate 1b0 = Normal operation 1b1 = PCS reset
14	mmd3_loopback_2	R	1b0	1 = Enable loopback mode 0 = Disable loopback mode Note - RW bit Note - 0x3 added in [15:12] to differentiate 1b0 = Disable loopback mode 1b1 = Enable loopback mode
13-0	RESERVED	R	14b0000000 0000000	Reserved

7.6.2.111 PCS_CONTROL Register (Address = 0x3900) [reset = 0x0]

PCS_CONTROL is shown in Table 7-134.

Return to the Summary Table.

Table 7-134. PCS_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	pcs_reset	R	1b0	1 = PCS reset 0 = Normal operation Note - RW bit, self clear bit Note - 0x3 added in [15:12] to differentiate 1b0 = Normal operation 1b1 = PCS reset
14	mmd3_loopback	R	1b0	1 = Enable loopback mode 0 = Disable loopback mode Note - RW bit Note - 0x3 added in [15:12] to differentiate 1b0 = Disable loopback mode 1b1 = Enable loopback mode
13-0	RESERVED	R	14b00000000000000	Reserved

7.6.2.112 PCS_STATUS Register (Address = 0x3901) [reset = 0x0]

PCS_STATUS is shown in Table 7-135.

Return to the Summary Table.

Table 7-135. PCS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	4b0000	Reserved
11	tx_lpi_received_lh	R/W0C	1b0	1 = Tx PCS has received LPI 0 = LPI not received Note - 0x3 added in [15:12] to differentiate 1b0 = LPI not received 1b1 = Tx PCS has received LPI
10	rx_lpi_received_lh	R/W0C	1b0	1 = Rx PCS has received LPI 0 = LPI not received Note - 0x3 added in [15:12] to differentiate 1b0 = LPI not received 1b1 = Rx PCS has received LPI
9	tx_lpi_indication	R	1b0	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI Note - 0x3 added in [15:12] to differentiate 1b0 = PCS is not currently receiving LPI 1b1 = Tx PCS is currently receiving LPI
8	rx_lpi_indication	R	1b0	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI Note - 0x3 added in [15:12] to differentiate 1b0 = PCS is not currently receiving LPI 1b1 = Rx PCS is currently receiving LPI
7	pcs_fault	R	1b0	1 = Fault condition detected 0 = No fault condition detected Note - 0x3 added in [15:12] to differentiate 1b0 = No fault condition detected 1b1 = Fault condition detected
6-3	RESERVED	R	4b0000	Reserved
2	pcs_receive_link_status_ll	R/W0S	1b0	1 = PCS receive link up 0 = PCS receive link down Note - 0x3 added in [15:12] to differentiate 1b0 = PCS receive link down 1b1 = PCS receive link up
1-0	RESERVED	R	2b00	Reserved

7.6.2.113 PCS_STATUS_2 Register (Address = 0x3902) [reset = 0x0]

PCS_STATUS_2 is shown in Table 7-136.

Return to the Summary Table.

Table 7-136. PCS_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	5b00000	Reserved
10	pcs_receive_link_status	R	1b0	1 = PCS receive link up 0 = PCS receive link down Note - 0x3 added in [15:12] to differentiate 1b0 = PCS receive link down 1b1 = PCS receive link up
9	hi_rfer	R	1b0	1 = PCS reporting a high BER 0 = PCS not reporting a high BER Note - 0x3 added in [15:12] to differentiate 1b0 = PCS not reporting a high BER 1b1 = PCS reporting a high BER
8	block_lock	R	1b0	1 = PCS locked to received blocks 0 = PCS not locked to received blocks Note - 0x3 added in [15:12] to differentiate 1b0 = PCS not locked to received blocks 1b1 = PCS locked to received blocks
7	hi_rfer_lh	R/W0C	1b0	1 = PCS has reported a high BER 0 = PCS has not reported a high BER Note - 0x3 added in [15:12] to differentiate 1b0 = PCS has not reported a high BER 1b1 = PCS has reported a high BER
6	block_lock_ll	R/W0S	1b0	1 = PCS has block lock 0 = PCS does not have block lock Note - 0x3 added in [15:12] to differentiate 1b0 = PCS does not have block lock 1b1 = PCS has block lock
5-0	ber_count		6b000000	BER counter Note - 0x3 added in [15:12] to differentiate

7.6.2.114 OAM_TRANSMIT Register (Address = 0x3904) [reset = 0x0]

OAM_TRANSMIT is shown in Table 7-137.

Return to the Summary Table.

Table 7-137. OAM_TRANSMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	mr_tx_valid	R/WMC,0	1b0	This bit is used to indicate message data in registers 3.2308.11:8, 3.2309, 3.2310, 3.2311, and 3.2312 are valid and ready to be loaded. This bit shall self-clear when registers are loaded by the state machine. 1 = Message data in registers are valid 0 = Message data in registers are not valid Note - 0x3 added in [15:12] to differentiate 1b0 = Message data in registers are not valid 1b1 = Message data in registers are valid
14	mr_tx_toggle	R	1b0	Toggle value to be transmitted with message. This bit is set by the state machine and cannot be overridden by the user. Note - 0x3 added in [15:12] to differentiate
13	mr_tx_received		1b0	This bit shall self clear on read. 1 = 1000BASE-T1 OAM message received by link partner 0 = 1000BASE-T1 OAM message not received by link partner Note - 0x3 added in [15:12] to differentiate 1b0 = 1000BASE-T1 OAM message not received by link partner 1b1 = 1000BASE-T1 OAM message received by link partner
12	mr_tx_received_toggle	R	1b0	Toggle value of message that was received by link partner Note - 0x3 added in [15:12] to differentiate
11-8	mr_tx_message_num	R/W	4b0000	User-defined message number to send Note - 0x3 added in [15:12] to differentiate
7-4	RESERVED	R	4b0000	Reserved
3	mr_rx_ping	R	1b0	Received PingTx value from latest good 1000BASE-T1 OAM frame received Note - 0x3 added in [15:12] to differentiate
2	mr_tx_ping	R/W	1b0	Ping value to send to link partner Note - 0x3 added in [15:12] to differentiate
1-0	mr_tx_snr	R	2b00	00 = PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame. 01 = LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled). 10 = PHY SNR is marginal. 11 = PHY SNR is good. Note - 0x3 added in [15:12] to differentiate 2b00 = PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame. 2b01 = LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled). 2b10 = PHY SNR is marginal. 2b11 = PHY SNR is good.

7.6.2.115 OAM_TX_MESSAGE_1 Register (Address = 0x3905) [reset = 0x0]

OAM_TX_MESSAGE_1 is shown in Table 7-138.

Return to the Summary Table.

Table 7-138. OAM_TX_MESSAGE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_tx_message_15_0	R/W	16b0000000 000000000	Message octet 1/0. LSB transmitted first. Note - 0x3 added in [15:12] to differentiate

7.6.2.116 OAM_TX_MESSAGE_2 Register (Address = 0x3906) [reset = 0x0]

OAM_TX_MESSAGE_2 is shown in Table 7-139.

Return to the Summary Table.

Table 7-139. OAM_TX_MESSAGE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_tx_message_31_16	R/W	16b0000000 000000000	Message octet 3/2. LSB transmitted first. Note - 0x3 added in [15:12] to differentiate

7.6.2.117 OAM_TX_MESSAGE_3 Register (Address = 0x3907) [reset = 0x0]

OAM_TX_MESSAGE_3 is shown in Table 7-140.

Return to the Summary Table.

Table 7-140. OAM_TX_MESSAGE_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_tx_message_47_32	R/W	16b0000000 000000000	Message octet 5/4. LSB transmitted first. Note - 0x3 added in [15:12] to differentiate

7.6.2.118 OAM_TX_MESSAGE_4 Register (Address = 0x3908) [reset = 0x0]

OAM_TX_MESSAGE_4 is shown in Table 7-141.

Return to the Summary Table.

Table 7-141. OAM_TX_MESSAGE_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_tx_message_63_48	R/W	16b0000000 000000000	Message octet 7/6. LSB transmitted first. Note - 0x3 added in [15:12] to differentiate

7.6.2.119 OAM_RECEIVE Register (Address = 0x3909) [reset = 0x0]

OAM_RECEIVE is shown in Table 7-142.

Return to the Summary Table.

Table 7-142. OAM_RECEIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	mr_rx_lp_valid	R	1b0	This bit is used to indicate message data in registers 3.2313.11:8, 3.2314, 3.2315, 3.2316, and 3.2317 are stored and ready to be read. This bit shall self clear when register 3.2317 is read. 1 = Message data in registers are valid 0 = Message data in registers are not valid Note - 0x3 added in [15:12] to differentiate 1b0 = Message data in registers are not valid 1b1 = Message data in registers are valid
14	mr_rx_lp_toggle	R	1b0	Toggle value received with message Note - 0x3 added in [15:12] to differentiate
13-12	RESERVED	R	2b00	Reserved
11-8	mr_rx_lp_message_num	R	4b0000	Message number from link partner Note - 0x3 added in [15:12] to differentiate
7-2	RESERVED	R	6b000000	Reserved
1-0	mr_rx_lp_SNR	R	2b00	00 = Link partner link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame. 01 = LPI refresh is insufficient to maintain link partner SNR. Link partner requests local device to exit LPI and send idles (used only when EEE is enabled). 10 = Link partner SNR is marginal. 11 = Link partner SNR is good Note - 0x3 added in [15:12] to differentiate 2b00 = Link partner link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame. 2b01 = LPI refresh is insufficient to maintain link partner SNR. Link partner requests local device to exit LPI and send idles (used only when EEE is enabled). 2b10 = Link partner SNR is marginal. 2b11 = Link partner SNR is good

7.6.2.120 OAM_RX_MESSAGE_1 Register (Address = 0x390A) [reset = 0x0]

OAM_RX_MESSAGE_1 is shown in Table 7-143.

Return to the Summary Table.

Table 7-143. OAM_RX_MESSAGE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_rx_lp_message_15_0	R	16b0000000 000000000	Message octet 1/0. LSB transmitted first. Note - 0x3 added in [15:12] to differentiate

7.6.2.121 OAM_RX_MESSAGE_2 Register (Address = 0x390B) [reset = 0x0]

OAM_RX_MESSAGE_2 is shown in Table 7-144.

Return to the Summary Table.

Table 7-144. OAM_RX_MESSAGE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_rx_lp_message_31_16	R	16b0000000 000000000	Message octet 3/2. LSB transmitted first. Note - 0x3 added in [15:12] to differentiate

7.6.2.122 OAM_RX_MESSAGE_3 Register (Address = 0x390C) [reset = 0x0]

OAM_RX_MESSAGE_3 is shown in Table 7-145.

Return to the Summary Table.

Table 7-145. OAM_RX_MESSAGE_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_rx_lp_message_47_32	R	16b0000000 000000000	Message octet 5/4. LSB transmitted first. Note - 0x3 added in [15:12] to differentiate

7.6.2.123 OAM_RX_MESSAGE_4 Register (Address = 0x390D) [reset = 0x0]

OAM_RX_MESSAGE_4 is shown in Table 7-146.

Return to the Summary Table.

Table 7-146. OAM_RX_MESSAGE_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_rx_lp_message_63_48		16b0000000 000000000	Message octet 7/6. LSB transmitted first. Note - 0x3 added in [15:12] to differentiate

7.6.2.124 AN_CFG Register (Address = 0x7200) [reset = 0x0]

AN_CFG is shown in Table 7-147.

Return to the Summary Table.

Table 7-147. AN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	15b000000000000000	Reserved
0	mr_main_reset	R/WSC	1b0	1 = Reset link sync/autoneg Note - RW bit Note - Added 7 to [15:12] to differentiate

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DP83TG720S-Q1 is a single-port 1-Gbps Automotive Ethernet PHY. It supports IEEE 802.3bp and allows for connections to an Ethernet MAC through RGMII or SGMII. When using the device for Ethernet applications, it is necessary to meet certain requirements for normal operation. The following subsections are intended to assist in appropriate component selection and required connections.

8.2 Typical Applications

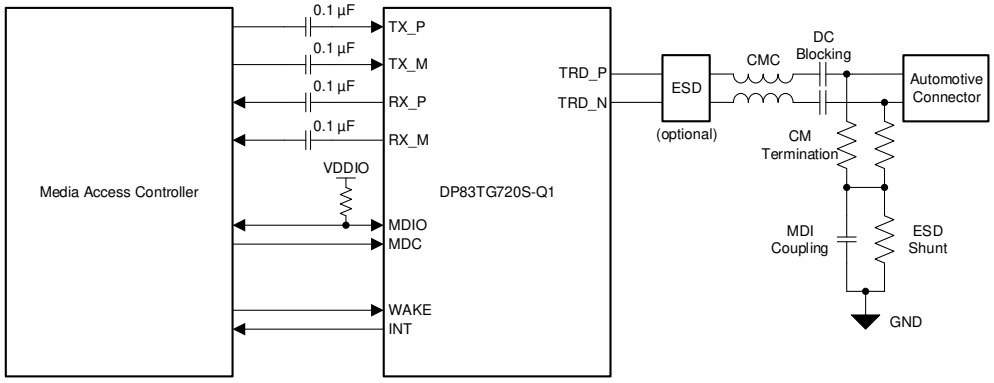

Figure 8-1. Typical Application (SGMII)

9 Power Supply Recommendations

The DP83TG720S-Q1 is capable of operating with a wide range of IO supply voltages (3.3 V, 2.5 V, or 1.8 V). No power supply sequencing is required. The recommended power supply de-coupling network is shown in following figure :

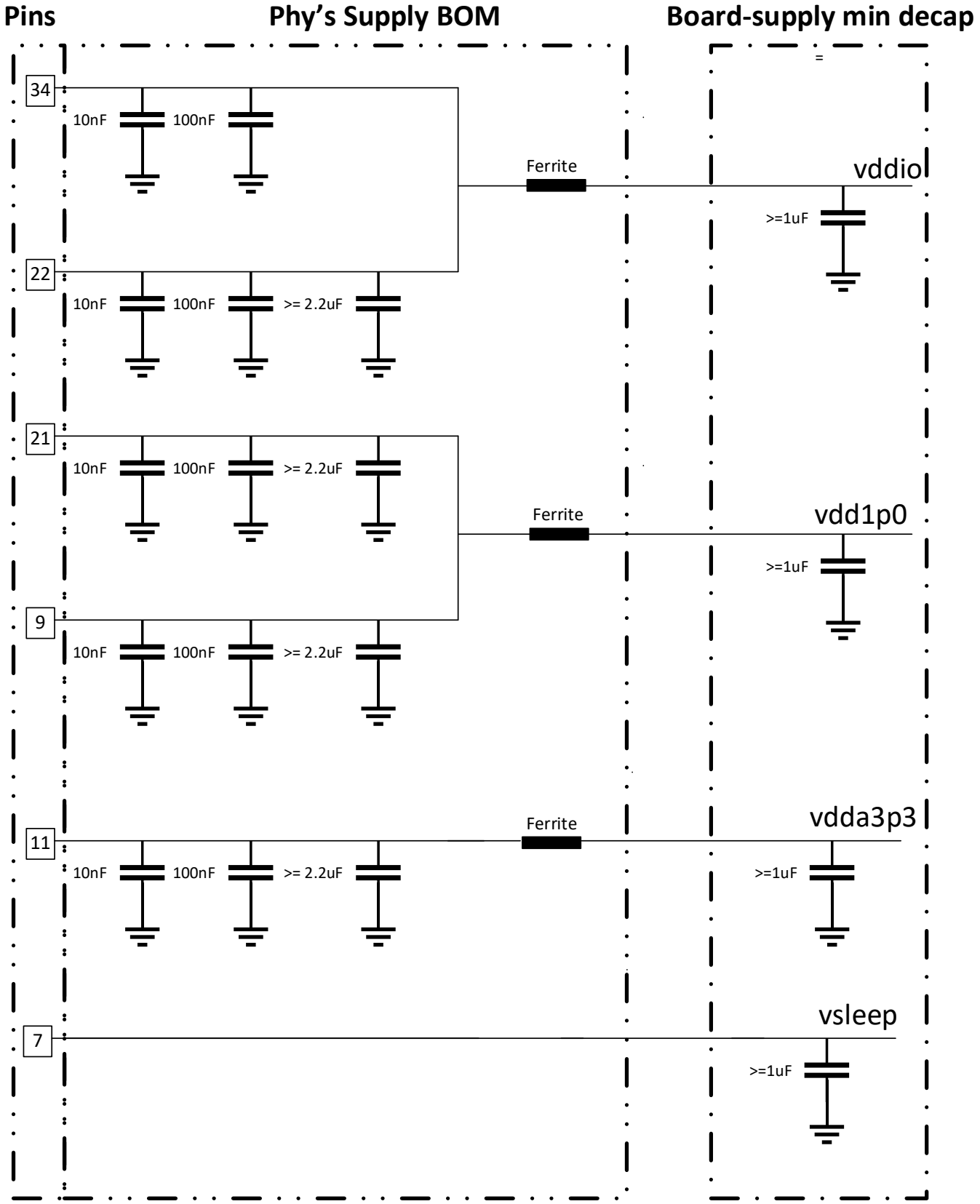

Figure 9-1. Recommended Supply De-Coupling Network

TPS784105QWDRBRQ1 can be used as 1V LDO to supply vdd1p0.

10 Layout

10.1 Layout Guidelines

10.1.1 Signal Traces

PCB traces are lossy and long traces can degrade signal quality. Traces should be kept short as possible. Unless mentioned otherwise, all signal traces should be 50-Ω, single-ended impedance. Differential traces should be 50-Ω single-ended and 100-Ω differential. Take care to ensure impedance is controlled throughout. Impedance discontinuities will cause reflections leading to emissions and signal integrity issues. Stubs should be avoided on all signal traces, especially differential signal pairs.

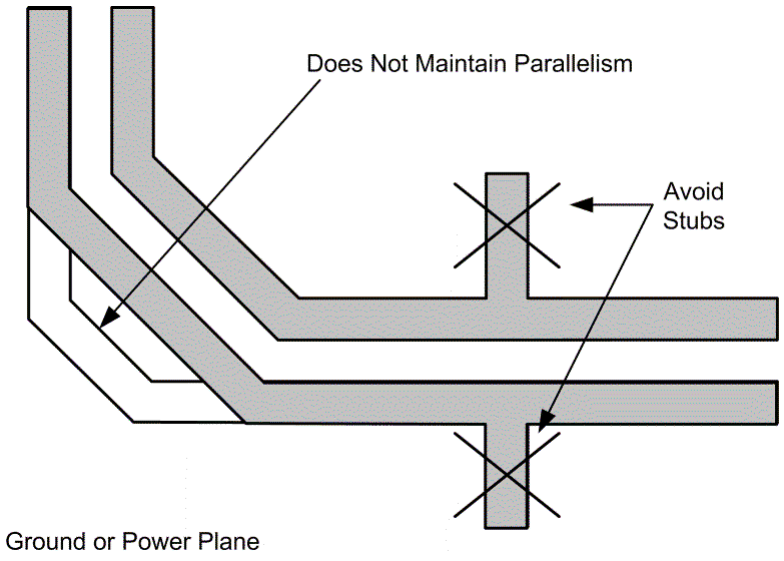

Figure 10-1. Differential Signal Trace Routing

Within the differential pairs, trace lengths should be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and emissions. Length matching is also important for MAC interface connections. All transmit signal traces should be length matched to each other and all receive signal traces should be length matched to each other.

Ideally, there should be no crossover or vias on signal path traces. Vias present impedance discontinuities and should be minimized when possible. Route trace pairs on the same layer. Signals on different layers should not cross each other without at least one return path plane between them. Differential pairs should always have a constant coupling distance between them. For convenience and efficiency, TI recommends routing critical signals first (that is, MDI differential pairs, reference clock, and MAC IF traces).

10.1.2 Return Path

A general best practice is to have a solid return path beneath all signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Breaks in return path between the signal traces should be avoided at all cost. A signal crossing a split plane may cause unpredictable return path currents and could impact signal quality and result in emissions issues.

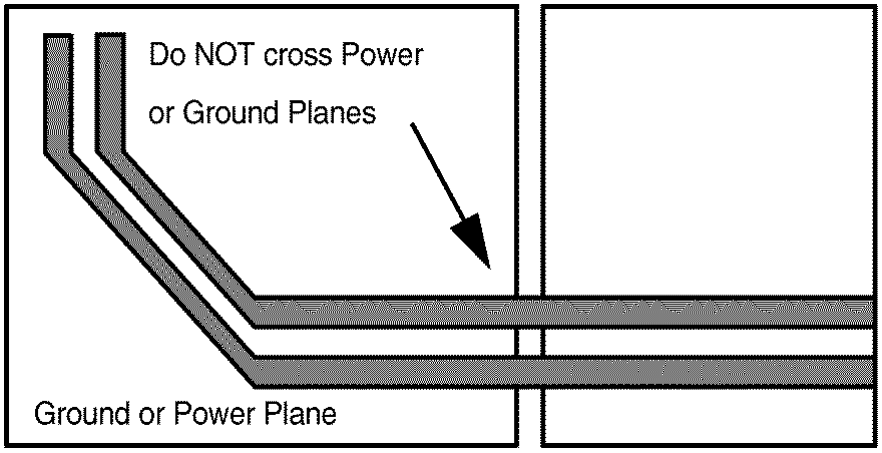

Figure 10-2. Power and Ground Plane Breaks

10.1.3 Physical Medium Attachment

There must be no metal running beneath the common-mode choke. CMCs can inject noise into metal beneath them, which can affect the emissions and immunity performance of the system. Because the DP83TG720S-Q1 is a voltage mode line driver, no external termination resistors are required. The ESD shunt and MDI coupling capacitor should be connected to ground. Ensure that the common mode termination resistors are 1% tolerance or better to improve differential coupling.

10.1.4 Metal Pour

All metal pours that are not signals or power must be tied to ground. There must be no floating metal in the system, and there must be no metal between differential traces.

10.1.5 PCB Layer Stacking

To meet signal integrity and performance requirements, minimum four-layer PCB is recommended. However, a six-layer PCB and above should be used when possible.

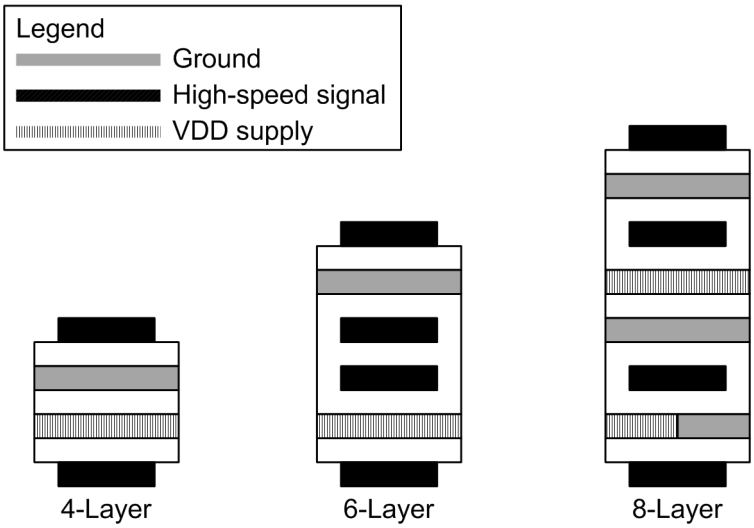

Figure 10-3. Recommended PCB Layer Stack-Up

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.3 Trademarks

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All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
PDP83TG720SWCSTQ1	EARLY SAMPLE	VQFN	RHA	36	250	RoHS	NiPdAu	MSL3-260C	-40 to 125	
DP83TG720SWRHATQ1	PREVIEW	VQFN	RHA	36	250	RoHS	NiPdAu	MSL3-260C	-40 to 125	720S
DP83TG720SWRHARQ1	PREVIEW	VQFN	RHA	36	2000	RoHS	NiPdAu	MSL3-260C	-40 to 125	720S

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

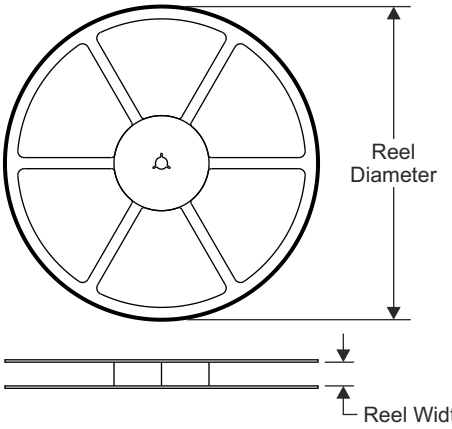
(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

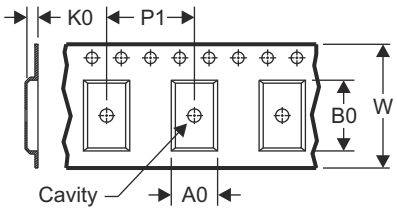
ADVANCE INFORMATION

12.1.2 Tape and Reel Information

REEL DIMENSIONS

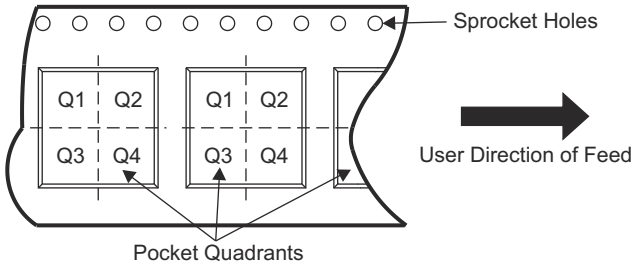


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

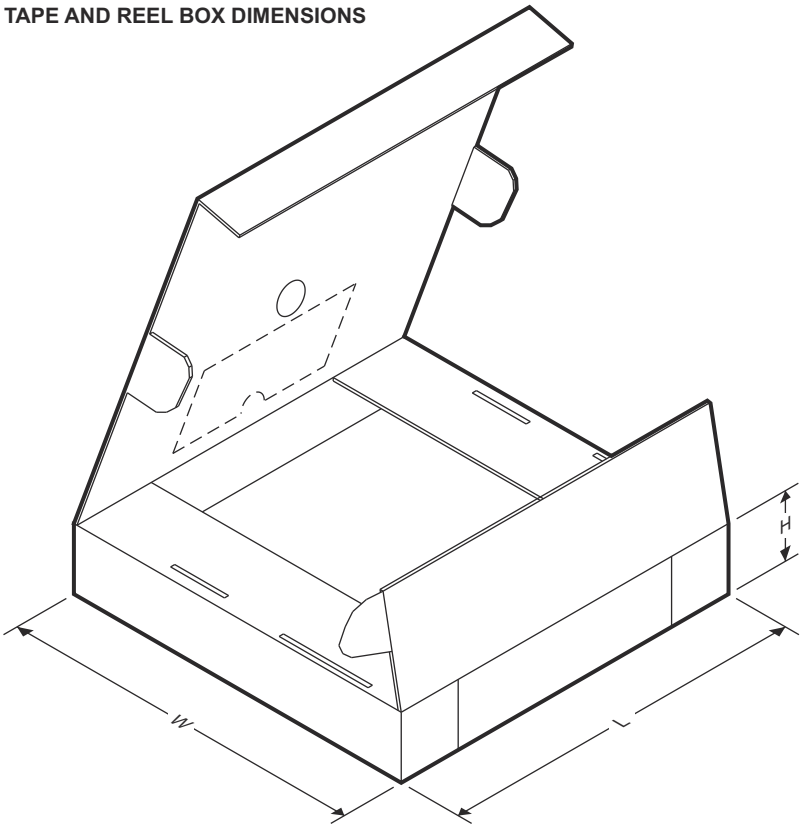
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PDP83TG720SWCSTQ1	VQFN	RHA	36	250	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
DP83TG720SWRHATQ1	VQFN	RHA	36	250	180	16.4	6.3	6.3	1.1	12	16	Q2
DP83TG720SWRHARQ1	VQFN	RHA	36	2000	330	16.4	6.3	6.3	1.1	12	16	Q2

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DP83TG720SWRHATQ1	VQFN	RHA	36	250	210	185	35
DP83TG720SWRHARQ1	VQFN	RHA	36	2000	367	367	38

ADVANCE INFORMATION

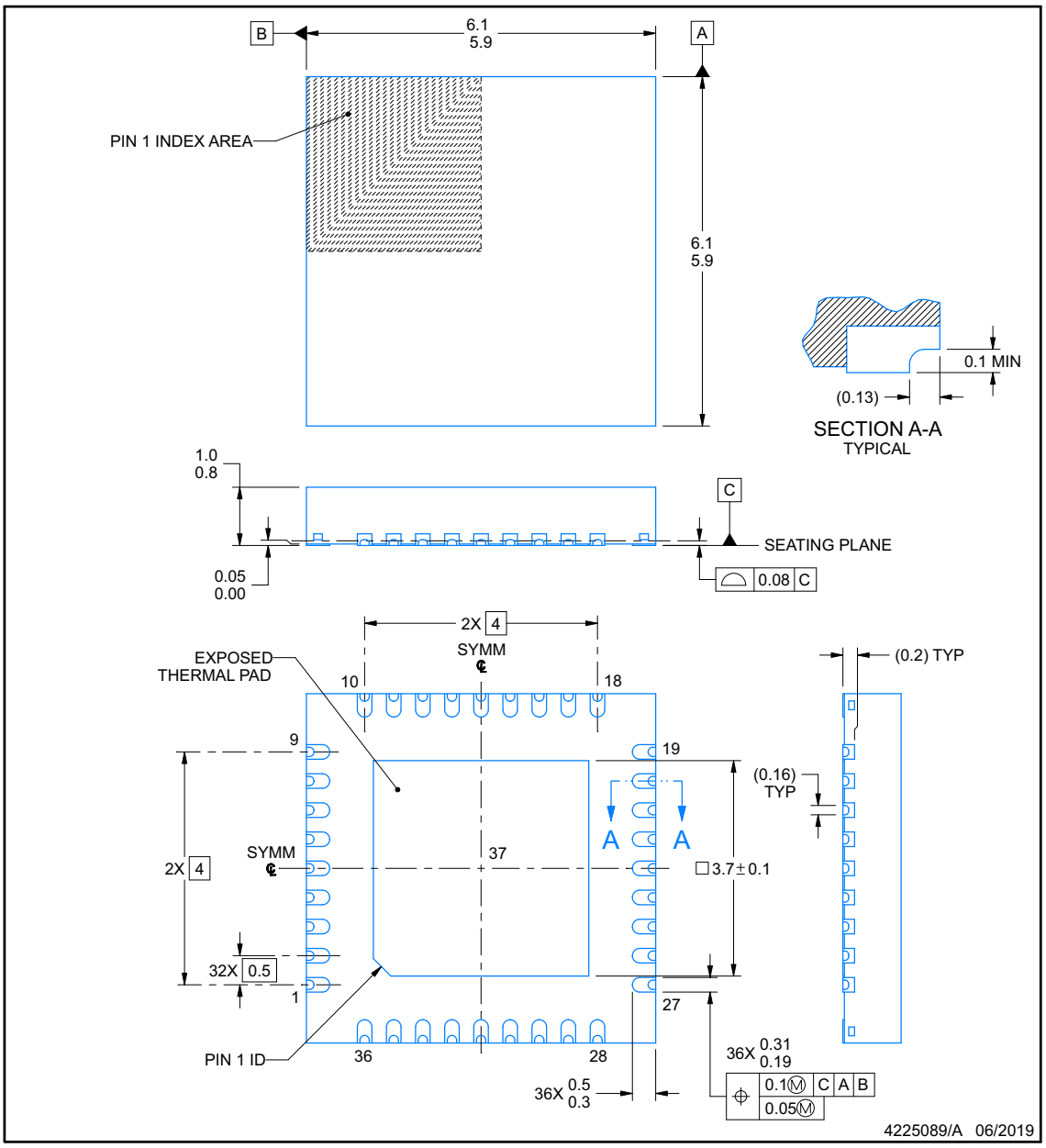
ADVANCE INFORMATION

PACKAGE OUTLINE

RHA0036A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

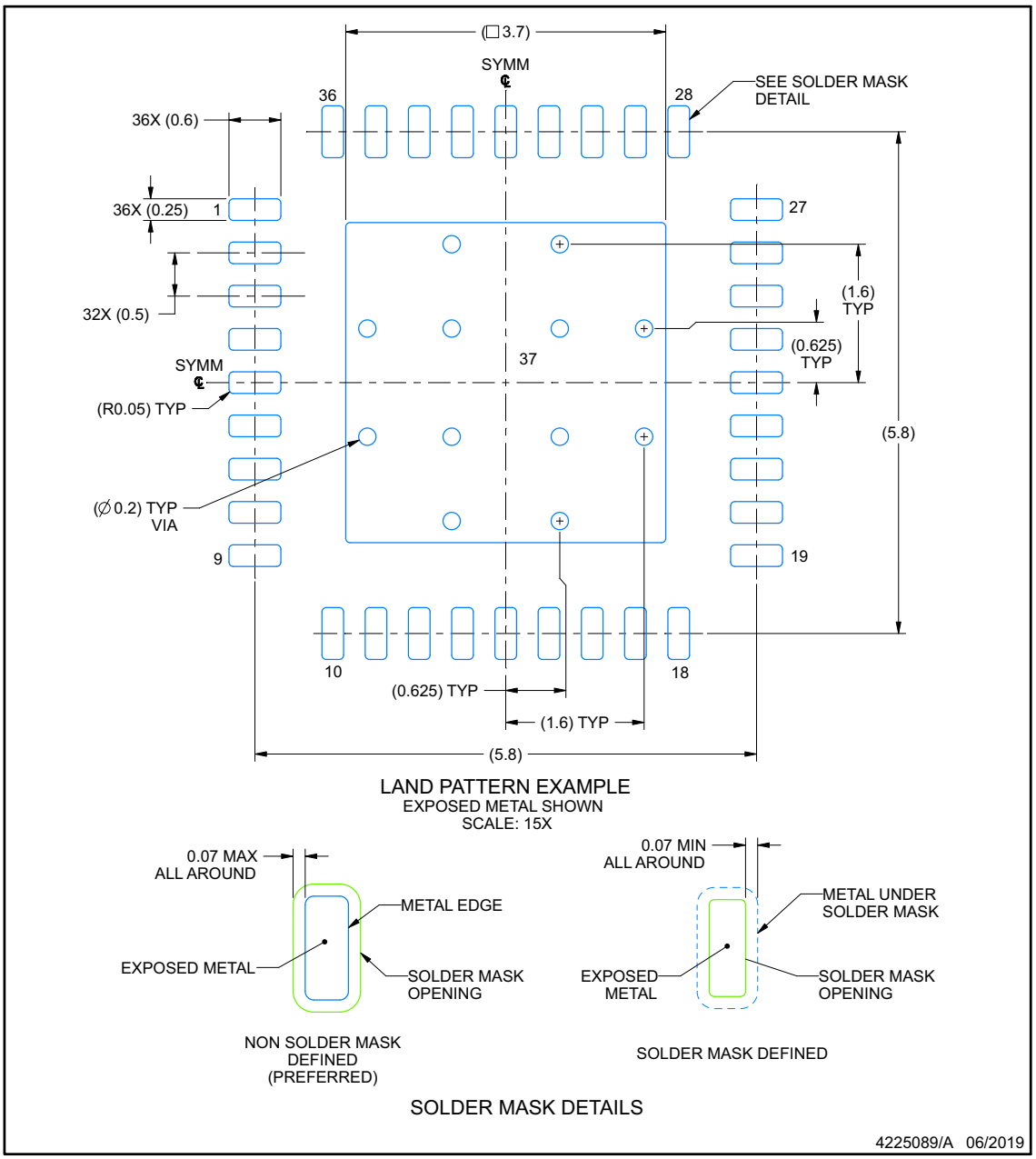
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHA0036A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

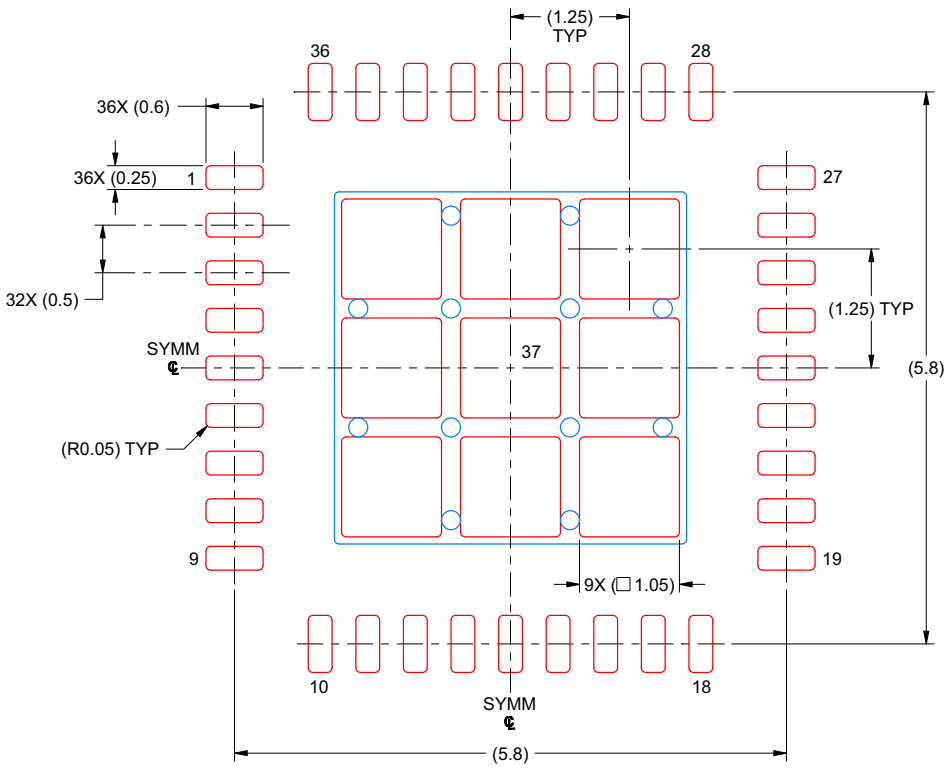
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RHA0036A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225089/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DP83TG720SWRHARQ1	PREVIEW	VQFN	RHA	36	2000	TBD	Call TI	Call TI	-40 to 125		
DP83TG720SWRHATQ1	PREVIEW	VQFN	RHA	36	250	TBD	Call TI	Call TI	-40 to 125		
PDP83TG720SWCSTQ1	ACTIVE	VQFN	RHA	36	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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