

Low Cost 3.3V Spread Aware Zero Delay Buffer

Features

- 10 MHz to 100 and 133 MHz operating range, compatible with CPU and PCI bus frequencies
- Zero input-output propagation delay
- Multiple low skew outputs
 - Output-output skew less than 250 ps
 - Device-device skew less than 700 ps
 - One input drives five outputs (CY23S05)
 - One input drives nine outputs, grouped as 4 + 4 + 1 (CY23S09)
- Less than 200 ps cycle-to-cycle jitter is compatible with Pentium® based systems
- Test mode to bypass PLL (CY23S09 only, see [Select Input Decoding for CY23S09](#) on page 2)
- Available in space saving 16-pin, 150-mil SOIC, 4.4 mm TSSOP, and 150-mil SSOP (CY23S09) or 8-pin, 150-mil SOIC package (CY23S05)
- 3.3V operation, advanced 0.65μ CMOS technology
- Spread Aware

Functional Description

The CY23S09 is a low cost 3.3V zero delay buffer designed to distribute high speed clocks and is available in a 16-pin SOIC package. The CY23S05 is an 8-pin version of the CY23S09. It accepts one reference input, and drives out five low skew clocks. The -1H versions of each device operate at up to 100 and 133

MHz frequencies and have higher drive than the -1 devices. All parts have on-chip PLLs that lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

The CY23S09 has two banks of four outputs each, which can be controlled by the select inputs as shown in the Select Input Decoding table on [Select Input Decoding for CY23S09](#) on page 2. If all output clocks are not required, Bank B can be three-stated. The select inputs also allow the input clock to be directly applied to the outputs for chip and system testing purposes.

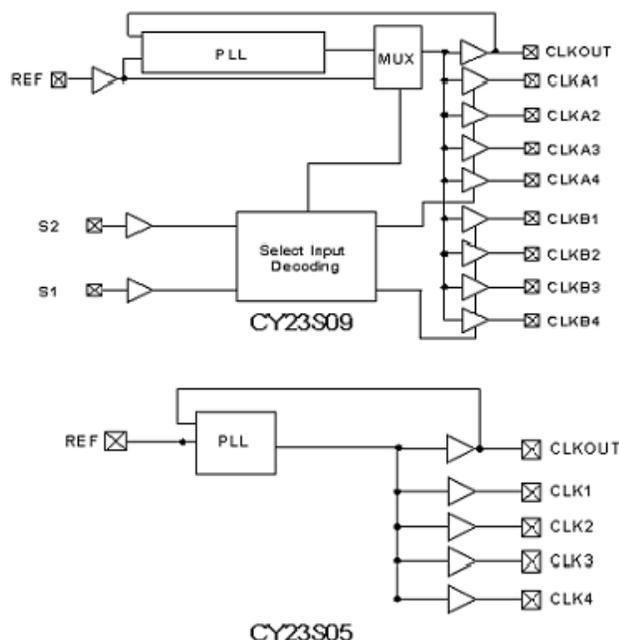
The CY23S09 and CY23S05 PLLs enter a power down mode when there are no rising edges on the REF input. In this state, the outputs are three-stated and the PLL is turned off, resulting in less than 12.0 μA of current draw (for commercial temperature devices) and 25.0 μA (for industrial temperature devices). The CY23S09 PLL shuts down in one additional case, as shown in the [Select Input Decoding for CY23S09](#) on page 2.

Multiple CY23S09 and CY23S05 devices can accept the same input clock and distribute it. In this case, the skew between the outputs of two devices is guaranteed to be less than 700 ps.

All outputs have less than 200 ps of cycle-to-cycle jitter. The input to output propagation delay on both devices is guaranteed to be less than 350 ps; the output to output skew is guaranteed to be less than 250 ps.

The CY23S05 and CY23S09 is available in two different configurations, as shown in the [Ordering Information](#) on page 6. The CY23S05-1 and CY23S09-1 is the base part. The CY23S05-1H and CY23S09-1H is the high drive version of the -1, and its rise and fall times are much faster than -1.

Logic Block Diagram



Select Input Decoding for CY23S09

| S2 | S1 | CLOCK A1–A4 | CLOCK B1–B4 | CLKOUT ^[1] | Output Source | PLL Shut-down |
|----|----|-------------|-------------|-----------------------|---------------|---------------|
| 0 | 0 | Three-state | Three-state | Driven | PLL | N |
| 0 | 1 | Driven | Three-state | Driven | PLL | N |
| 1 | 0 | Driven | Driven | Driven | Reference | Y |
| 1 | 1 | Driven | Driven | Driven | PLL | N |

Zero Delay and Skew Control

All outputs must be uniformly loaded to achieve Zero Delay between the input and output. Because the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay. This is shown in the above graph.

For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs, to obtain zero input-output delay. If input to output delay adjustments are required, use the above graph to calculate loading differences between the CLKOUT pin and other outputs.

For zero output-output skew, be sure to load all outputs equally. For further information, refer to the application note “CY23S05 and CY23S09 as PCI and SDRAM Buffers.”

Spread Aware

Many systems being designed now use a technology called Spread Spectrum Frequency Timing Generation. Cypress is one of the pioneers of SSFTG development and designed this product so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the SS feature through, the result is a significant amount of tracking skew, which may cause problems in systems requiring synchronization.

For more details on Spread Spectrum timing technology, please see the Cypress application note [AN1278, EMI Suppression Techniques with Spread Spectrum Frequency Timing Generator \(SSFTG\) ICs](#).

Pin Configurations

Figure 1. Pin Diagram - CY23S09

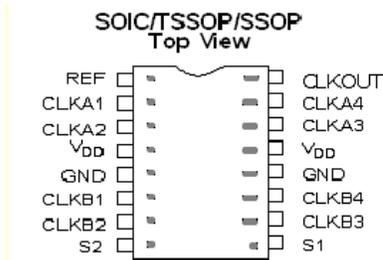
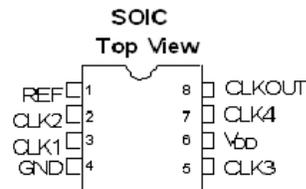


Figure 2. Pin Diagram - CY23S05



Note

1. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

Pin Description for CY23S09

| Pin | Signal | Description |
|-----|-----------------------|--|
| 1 | REF ^[2] | Input reference frequency, 5V tolerant input |
| 2 | CLKA1 ^[3] | Buffered clock output, bank A |
| 3 | CLKA2 ^[3] | Buffered clock output, bank A |
| 4 | V _{DD} | 3.3V supply |
| 5 | GND | Ground |
| 6 | CLKB1 ^[3] | Buffered clock output, bank B |
| 7 | CLKB2 ^[3] | Buffered clock output, bank B |
| 8 | S2 ^[4] | Select input, bit 2 |
| 9 | S1 ^[4] | Select input, bit 1 |
| 10 | CLKB3 ^[3] | Buffered clock output, bank B |
| 11 | CLKB4 ^[3] | Buffered clock output, bank B |
| 12 | GND | Ground |
| 13 | V _{DD} | 3.3V supply |
| 14 | CLKA3 ^[3] | Buffered clock output, bank A |
| 15 | CLKA4 ^[3] | Buffered clock output, bank A |
| 16 | CLKOUT ^[3] | Buffered output, internal feedback on this pin |

Pin Description for CY23S05

| Pin | Signal | Description |
|-----|-----------------------|--|
| 1 | REF ^[2] | Input reference frequency, 5V tolerant input |
| 2 | CLK2 ^[3] | Buffered clock output |
| 3 | CLK1 ^[3] | Buffered clock output |
| 4 | GND | Ground |
| 5 | CLK3 ^[3] | Buffered clock output |
| 6 | V _{DD} | 3.3V supply |
| 7 | CLK4 ^[3] | Buffered clock output |
| 8 | CLKOUT ^[3] | Buffered clock output, internal feedback on this pin |

Notes

2. Weak pull-down.
3. Weak pull-down on all outputs.
4. Weak pull-up on these inputs.

Maximum Ratings

Supply Voltage to Ground Potential.....-0.5V to +7.0V
 DC Input Voltage (Except REF)-0.5V to $V_{DD} + 0.5V$
 DC Input Voltage REF-0.5V to 7V

Storage Temperature-65°C to +150°C
 Maximum Soldering Temperature (10 seconds)..... 260°C
 Junction Temperature 150°C
 Static Discharge Voltage
 (per MIL-STD-883, Method 3015) > 2,000V

Operating Conditions for CY23S05SC-XX and CY23S09SC-XX Commercial Temperature Devices^[5]

| Parameter | Description | Min | Max | Unit |
|-----------|---|-----|-----|------|
| V_{DD} | Supply Voltage | 3.0 | 3.6 | V |
| T_A | Operating Temperature (Ambient Temperature) | 0 | 70 | °C |
| C_L | Load Capacitance, below 100 MHz | | 30 | pF |
| C_L | Load Capacitance, from 100 MHz to 133 MHz | | 10 | pF |
| C_{IN} | Input Capacitance | | 7 | pF |

Electrical Characteristics for CY23S05SC-XX and CY23S09SC-XX Commercial Temperature Devices

| Parameter | Description | Test Conditions | Min | Max | Unit |
|--------------------|------------------------------------|--|-----|-------|------|
| V_{IL} | Input LOW Voltage ^[6] | | | 0.8 | V |
| V_{IH} | Input HIGH Voltage ^[6] | | 2.0 | | V |
| I_{IL} | Input LOW Current | $V_{IN} = 0V$ | | 50.0 | μA |
| I_{IH} | Input HIGH Current | $V_{IN} = V_{DD}$ | | 100.0 | μA |
| V_{OL} | Output LOW Voltage ^[7] | $I_{OL} = 8\text{ mA} (-1)$ $I_{OH} = 12\text{ mA} (-1H)$ | | 0.4 | V |
| V_{OH} | Output HIGH Voltage ^[7] | $I_{OH} = -8\text{ mA} (-1)$ $I_{OL} = -12\text{ mA} (-1H)$ | 2.4 | | V |
| I_{DD} (PD mode) | Power Down Supply Current | REF = 0 MHz | | 12.0 | μA |
| I_{DD} | Supply Current | Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD} | | 32.0 | mA |

Switching Characteristics for CY23S05SC-1 and CY23S09SC-1 Commercial Temperature Devices^[8]

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|------------|---|---|----------|------|---------------|------------|
| t_1 | Output Frequency | 30 pF load 10 pF load | 10 10 | | 100 133.33 | MHz MHz |
| | Duty Cycle ^[7] = $t_2 \div t_1$ | Measured at 1.4V, $F_{out} = 66.67\text{ MHz}$ | 40.0 | 50.0 | 60.0 | % |
| t_3 | Rise Time ^[7] | Measured between 0.8V and 2.0V | | | 2.50 | ns |
| t_4 | Fall Time ^[7] | Measured between 0.8V and 2.0V | | | 2.50 | ns |
| t_5 | Output-to-Output Skew ^[7] | All outputs equally loaded | | | 250 | ps |
| t_6 | Delay, REF Rising Edge to CLKOUT Rising Edge ^[7] | Measured at $V_{DD}/2$ | | 0 | ±350 | ps |
| t_7 | Device-to-Device Skew ^[7] | Measured at $V_{DD}/2$ on the CLKOUT pins of devices | | 0 | 700 | ps |
| t_J | Cycle-to-Cycle Jitter ^[7] | Measured at 66.67 MHz, loaded outputs | | | 200 | ps |
| t_{LOCK} | PLL Lock Time ^[7] | Stable power supply, valid clock presented on REF pin | | | 1.0 | ms |

Notes

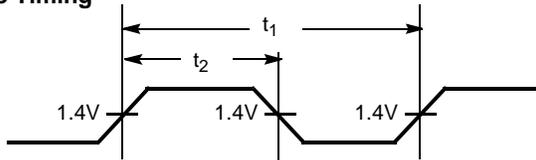
5. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power up. Power supply sequencing is NOT required.
6. REF input has a threshold voltage of $V_{DD}/2$.
7. Parameter is guaranteed by design and characterization. Not 100% tested in production.
8. All parameters specified with loaded outputs.

Switching Characteristics for CY23S05SI-1H and CY23S09SI-1H Industrial Temperature Devices^[8]

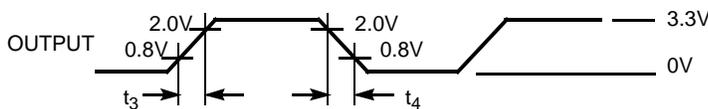
| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|-------------------|---|---|----------|------|---------------|------------|
| t1 | Output Frequency | 30 pF load 10 pF load | 10 10 | | 100 133.33 | MHz MHz |
| | Duty Cycle ^[7] = $t_2 \div t_1$ | Measured at 1.4V, $F_{out} = 66.67$ MHz | 40.0 | 50.0 | 60.0 | % |
| | Duty Cycle ^[7] = $t_2 \div t_1$ | Measured at 1.4V, $F_{out} < 50.0$ MHz | 45.0 | 50.0 | 55.0 | % |
| t3 | Rise Time ^[7] | Measured between 0.8V and 2.0V | | | 1.50 | ns |
| t4 | Fall Time ^[7] | Measured between 0.8V and 2.0V | | | 1.50 | ns |
| t5 | Output-to-Output Skew ^[7] | All outputs equally loaded | | | 250 | ps |
| t6 | Delay, REF Rising Edge to CLKOUT Rising Edge ^[7] | Measured at $V_{DD}/2$ | | 0 | ± 350 | ps |
| t7 | Device-to-Device Skew ^[7] | Measured at $V_{DD}/2$ on the CLKOUT pins of devices | | 0 | 700 | ps |
| t8 | Output Slew Rate ^[7] | Measured between 0.8V and 2.0V using Test Circuit #2 | 1 | | | V/ns |
| tj | Cycle-to-Cycle Jitter ^[7] | Measured at 66.67 MHz, loaded outputs | | | 200 | ps |
| t _{LOCK} | PLL Lock Time ^[7] | Stable power supply, valid clock presented on REF pin | | | 1.0 | ms |

Switching Waveforms

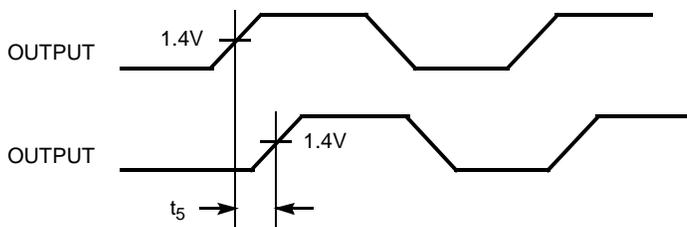
Duty Cycle Timing



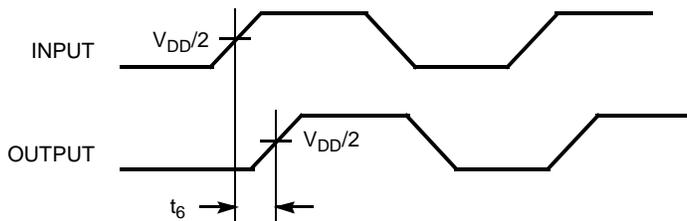
All Outputs Rise/Fall Time



Output-Output Skew

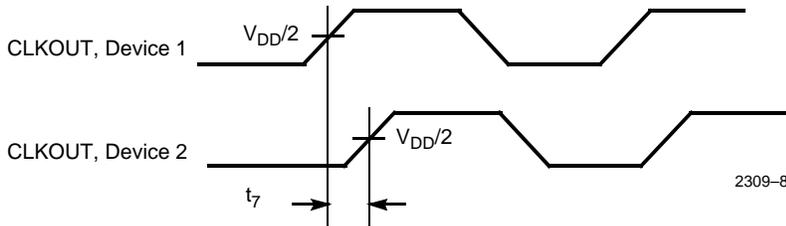


Input-Output Propagation Delay

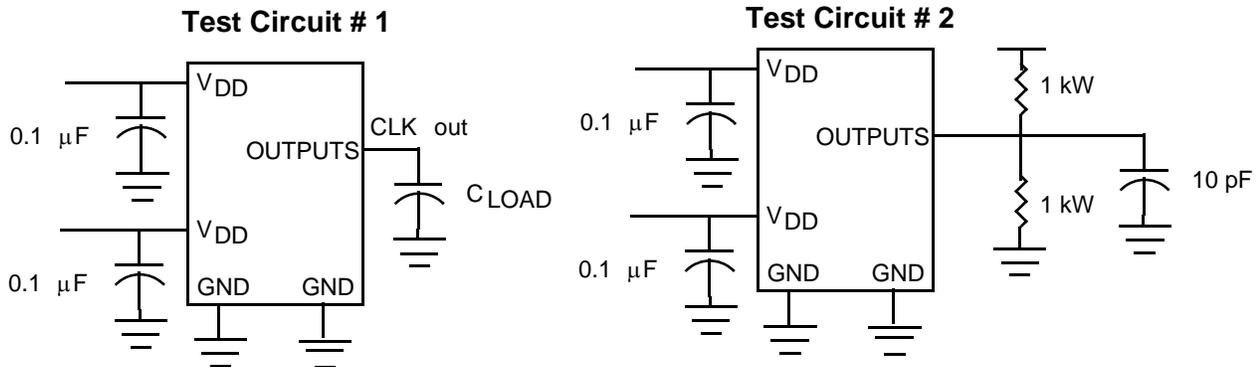


Switching Waveforms continued

Device-Device Skew



Test Circuits



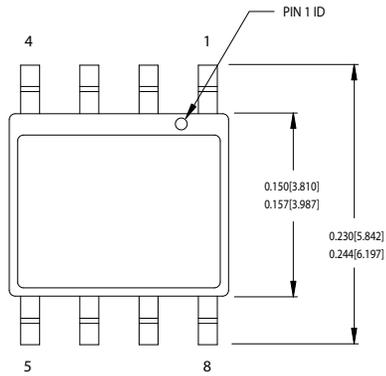
For parameter t8 (output slew rate) on -1H devices

Ordering Information

| Ordering Code | Package Name | Package Type | Operating Range | Status |
|----------------|--------------|---------------------|-----------------|----------|
| CY23S05SC-1 | S8 | 8-pin 150-mil SOIC | Commercial | Active |
| CY23S05SC-1H | S8 | 8-pin 150-mil SOIC | Commercial | Obsolete |
| CY23S09SC-1 | S16 | 16-pin 150-mil SOIC | Commercial | Obsolete |
| CY23S09SC-1H | S16 | 16-pin 150-mil SOIC | Commercial | Obsolete |
| CY23S09ZC-1 | Z16 | 16-pin 4.4 mm TSSOP | Commercial | Obsolete |
| CY23S09ZC-1H | Z16 | 16-pin 4.4 mm TSSOP | Commercial | Obsolete |
| CY23S09OC-1 | O16 | 16-pin 150-mil SSOP | Commercial | Obsolete |
| CY23S09OC-1H | O16 | 16-pin 150-mil SSOP | Commercial | Obsolete |
| Pb-Free | | | | |
| CY23S05SXC-1 | S8 | 8-pin 150-mil SOIC | Commercial | Active |
| CY23S05SXC-1H | S8 | 8-pin 150-mil SOIC | Commercial | Active |
| CY23S09SXC-1 | S16 | 16-pin 150-mil SOIC | Commercial | Active |
| CY23S09SXC-1H | S16 | 16-pin 150-mil SOIC | Commercial | Active |
| CY23S09ZXC-1 | Z16 | 16-pin 4.4 mm TSSOP | Commercial | Obsolete |
| CY23S09ZXC-1H | Z16 | 16-pin 4.4 mm TSSOP | Commercial | Active |
| CY23S09OXC-1 | O16 | 16-pin 150-mil SSOP | Commercial | Obsolete |
| CY23S09OXC-1H | O16 | 16-pin 150-mil SSOP | Commercial | Obsolete |

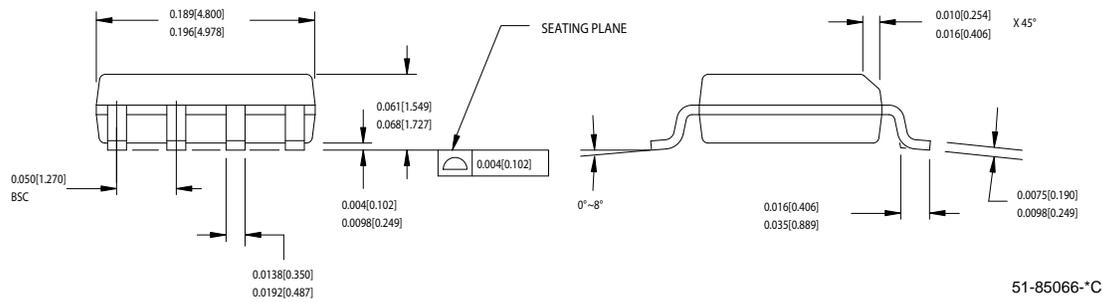
Package Diagrams

Figure 3. 8-Pin (150-Mil) SOIC S8



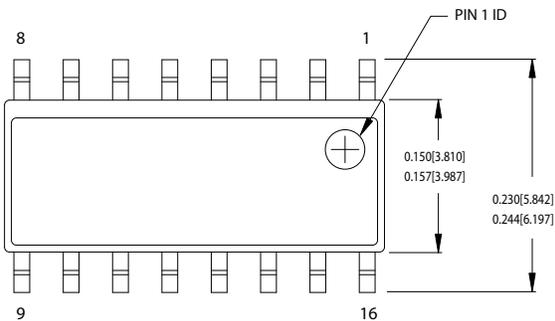
1. DIMENSIONS IN INCHES[MM] MIN. MAX.
2. PIN 1 ID IS OPTIONAL, ROUND ON SINGLE LEADFRAME RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

| PART # |
|------------------------|
| S08.15 STANDARD PKG. |
| SZ08.15 LEAD FREE PKG. |



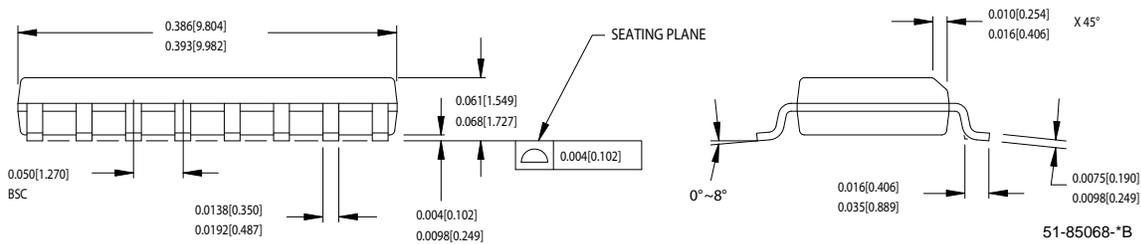
51-85066-°C

Figure 4. 16-Pin (150-Mil) SOIC S16.15



- DIMENSIONS IN INCHES[MM] MIN. MAX.
- REFERENCE JEDEC MS-012
- PACKAGE WEIGHT 0.15gms

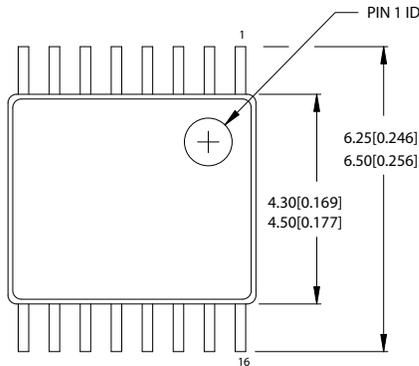
| PART # |
|------------------------|
| S16.15 STANDARD PKG. |
| SZ16.15 LEAD FREE PKG. |



51-85068-°B

Package Diagrams continued

Figure 5. 16-Pin TSSOP 4.40 mm Body Z16.173

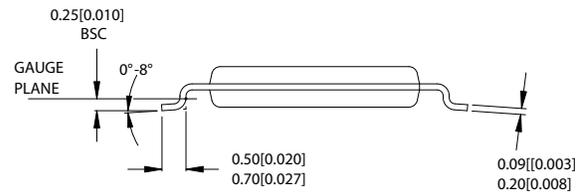
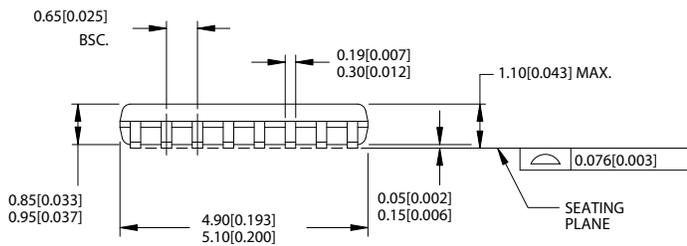


DIMENSIONS IN MM [INCHES] MIN.
MAX.

REFERENCE JEDEC MO-153

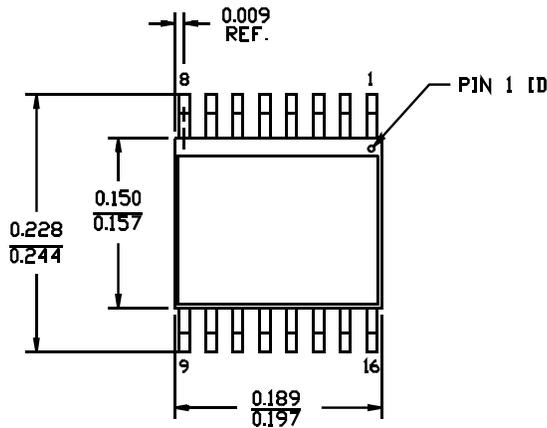
PACKAGE WEIGHT 0.05 gms

| PART # | |
|----------|----------------|
| Z16.173 | STANDARD PKG. |
| ZZ16.173 | LEAD FREE PKG. |

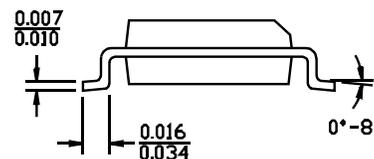
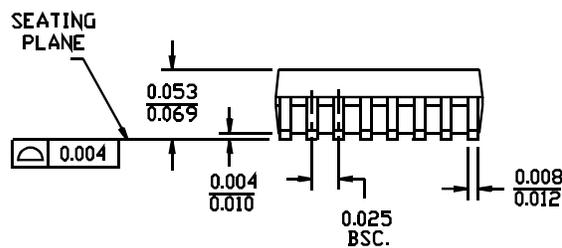


51-85091-*A

Figure 6. 16-Pin (150-Mil) QSOP Q1



DIMENSIONS IN INCHES MIN.
MAX.



51-85053-*B

Document History Page

| Document Title: CY23S09/CY23S05 Low Cost 3.3V Spread Aware Zero Delay Buffer | | | | |
|--|---------|-----------------|-----------------|---|
| Document Number: 38-07296 | | | | |
| Rev. | ECN No. | Submission Date | Orig. of Change | Description of Change |
| ** | 111147 | 11/14/01 | DSG | Changed from spec number 38-01094 to 38-07296 |
| *A | 111773 | 02/20/02 | CTK | Added 150-mil SSOP option |
| *B | 122885 | 12/22/02 | RBI | Added power-up requirements to Operating Conditions |
| *C | 267849 | See ECN | RGL | Added Lead-Free devices |
| *D | 2595524 | 10/23/08 | CXQ/PYRS | Added device "Status" to Ordering Information |

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