Two LVPECL Output, High-Performance Clock Buffer

Check for Samples: CDCLVP1102

FEATURES

- **1:2 Differential Buffer**
- **Single Clock Input**
- **Universal Inputs Can Accept LVPECL, LVDS, LVCMOS/LVTTL**
- **Two LVPECL Outputs**
- **Maximum Clock Frequency: 2 GHz**
- **Maximum Core Current Consumption: 33 mA**
- **Very Low Additive Jitter: <100 fs,rms in 10-kHz to 20-MHz Offset Range**
- **2.375 V to 3.6 V Device Power Supply**
- **Maximum Propagation Delay: 450 ps**
- **Maximum Output Skew: 10 ps**
- **LVPECL Reference Voltage, V_{AC_REF}, Available for Capacitive-Coupled Inputs**
- **Industrial Temperature Range: –40°C to +85°C**
- **Available in 3-mm × 3-mm QFN-16 (RGT) Package**
- **ESD Protection Exceeds 2 kV (HBM)**

APPLICATIONS

- **Wireless Communications**
- **Telecommunications/Networking**
- **Medical Imaging**
- **Test and Measurement Equipment**

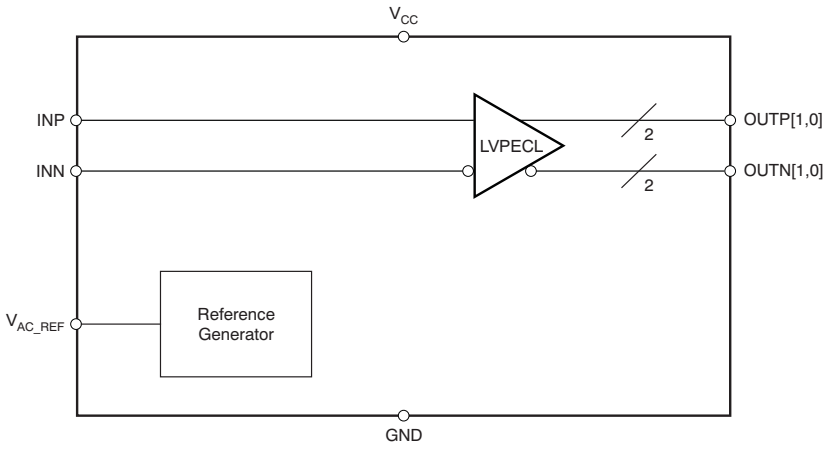
DESCRIPTION

The CDCLVP1102 is a highly versatile, low additive jitter buffer that can generate two copies of LVPECL clock outputs from one LVPECL, LVDS, or LVCMOS input for a variety of communication applications. It has a maximum clock frequency up to 2 GHz. The overall additive jitter performance is less than 0.1 ps, RMS from 10 kHz to 20 MHz, and overall output skew is as low as 10 ps, making the device a perfect choice for use in demanding applications.

The CDCLVP1102 clock buffer distributes a single clock input (IN) to two pairs of differential LVPECL clock outputs (OUT0, OUT1) with minimum skew for clock distribution. The inputs can be LVPECL, LVDS, or LVCMOS/LVTTL.

The CDCLVP1102 is specifically designed for driving 50-Ω transmission lines. When driving the inputs in single-ended mode, the LVPECL bias voltage (V_{AC_REF}) should be applied to the unused negative input pin. However, for high-speed performance up to 2 GHz, differential mode is strongly recommended.

The CDCLVP1102 is characterized for operation from –40°C to +85°C and is available in a QFN-16, 3-mm × 3-mm package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS(1)

T_A	PACKAGED DEVICES	FEATURES
–40°C to +85°C	CDCLVP1102RGTT	16-pin QFN (RGT) package, small tape and reel
	CDCLVP1102RGTR	16-pin QFN (RGT) package, tape and reel

(1) For the most current specifications and package information, see the Package Option Addendum located at the end of this data sheet or refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted).(1)

		CDCLVP1102	UNIT
V_{CC}	Supply voltage range(2)	–0.5 to 4.6	V
V_{IN}	Input voltage range (3)	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Output voltage range (3)	–0.5 to V_{CC} + 0.5	V
I_{IN}	Input current	20	mA
I_{OUT}	Output current	50	mA
T_A	Specified free-air temperature range (no airflow)	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+125	°C
ESD	Electrostatic discharge (HBM)	2	kV

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All supply voltages must be supplied simultaneously.
(3) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		CDCLVP1102 MIN	CDCLVP1102 TYP	CDCLVP1102 MAX	UNIT
V_{CC}	Supply voltage	2.375	2.50/3.30	3.60	V
T_A	Ambient temperature	–40		+85	°C

PACKAGE DISSIPATION RATINGS(1) (2)

PARAMETER		TEST CONDITIONS	VALUE 2 × 2 VIAS ON PAD	UNIT
θ_{JA}	Thermal resistance, junction-to-ambient	0 LFM	51.8	°C/W
		150 LFM	45	°C/W
		400 LFM	40.8	°C/W
θ_{JP} (3)	Thermal resistance, junction-to-pad		6.12	°C/W

(1) The package thermal resistance is calculated in accordance with JESD 51 and JEDEC 2S2P (high-K board).
(2) Connected to GND with four thermal vias (0.3-mm diameter).
(3) θ_{JP} (junction-to-pad) is used for the QFN package, because the primary heat flow is from the junction to the GND pad of the QFN package.

ELECTRICAL CHARACTERISTICS: LVCMOS Input(1)

At V_{CC} = 2.375 V to 3.6 V and T_A = –40°C to +85°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	CDCLVP1102			UNIT
			MIN	TYP	MAX	
f_{IN}	Input frequency				200	MHz
V_{th}	Input threshold voltage	External threshold voltage applied to complementary input	1.1		1.8	V
V_{IH}	Input high voltage		V_{th} + 0.1		V_{CC}	V
V_{IL}	Input low voltage		0		V_{th} – 0.1	V
I_{IH}	Input high current	V_{CC} = 3.6 V, V_{IH} = 3.6 V			40	µA
I_{IL}	Input low current	V_{CC} = 3.6 V, V_{IL} = 0 V			–40	µA
ΔV/ΔT	Input edge rate	20% to 80%	1.5			V/ns
I_{CAP}	Input capacitance			5		pF

(1) Figure 3 and Figure 4 show dc test setup.

ELECTRICAL CHARACTERISTICS: Differential Input(1)

At V_{CC} = 2.375 V to 3.6 V and T_A = –40°C to +85°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	CDCLVP1102			UNIT
			MIN	TYP	MAX	
f_{IN}	Input frequency	Clock input			2000	MHz
$V_{IN, DIFF, PP}$	Differential input peak-peak voltage	f_{IN} ≤ 1.5 GHz	0.1		1.5	V
		1.5 GHz ≤ f_{IN} ≤ 2 GHz	0.2		1.5	V
V_{ICM}	Input common-mode level		1.0		V_{CC} – 0.3	V
I_{IH}	Input high current	V_{CC} = 3.6 V, V_{IH} = 3.6 V			40	µA
I_{IL}	Input low current	V_{CC} = 3.6 V, V_{IL} = 0 V			–40	µA
ΔV/ΔT	Input edge rate	20% to 80%	1.5			V/ns
I_{CAP}	Input capacitance			5		pF

(1) Figure 5 and Figure 6 show dc test setup. Figure 7 shows ac test setup.

ELECTRICAL CHARACTERISTICS: LVPECL Output[1]

At V_{CC} = 2.375 V to 2.625 V and T_A = –40°C to +85°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	CDCLVP1102			UNIT
			MIN	TYP	MAX	
V_{OH}	Output high voltage		V_{CC} – 1.26		V_{CC} – 0.9	V
V_{OL}	Output low voltage		V_{CC} – 1.7		V_{CC} – 1.3	V
$V_{OUT, DIFF, PP}$	Differential output peak-peak voltage	f_{IN} ≤ 2 GHz	0.5		1.35	V
V_{AC_REF}	Input bias voltage[2]	I_{AC_REF} = 2 mA	V_{CC} – 1.6		V_{CC} – 1.1	V
t_{PD}	Propagation delay	$V_{IN, DIFF, PP}$ = 0.1V			450	ps
		$V_{IN, DIFF, PP}$ = 0.3V			450	ps
$t_{SK,PP}$	Part-to-part skew				100	ps
$t_{SK,O}$	Output skew				10	ps
$t_{SK,P}$	Pulse skew (with 50% duty cycle input)	Crossing-point-to-crossing-point distortion, f_{OUT} = 100 MHz	–50		50	ps
t_{RJIT}	Random additive jitter (with 50% duty cycle input)	f_{OUT} = 100 MHz, $V_{IN,SE}$ = V_{CC}, V_{th} = 1.25 V, 10 kHz to 20 MHz		0.089		ps, RMS
		f_{OUT} = 100 MHz, $V_{IN,SE}$ = 0.9 V, V_{th} = 1.1 V, 10 kHz to 20 MHz		0.093		ps, RMS
		f_{OUT} = 2 GHz, $V_{IN,DIFF,PP}$ = 0.2 V, V_{ICM} = 1 V, 10 kHz to 20 MHz		0.037		ps, RMS
		f_{OUT} = 100 MHz, $V_{IN,DIFF,PP}$ = 0.15 V, V_{ICM} = 1 V, 10 kHz to 20 MHz		0.094		ps, RMS
		f_{OUT} = 100 MHz, $V_{IN,DIFF,PP}$ = 1 V, V_{ICM} = 1 V, 10 kHz to 20 MHz		0.091		ps, RMS
t_R/t_F	Output rise/fall time	20% to 80%			200	ps
I_{EE}	Supply internal current	Outputs unterminated			33	mA
I_{CC}	Output and internal supply current	All outputs terminated, 50 Ω to V_{CC} – 2			100	mA

(1) Figure 8 and Figure 9 show dc and ac test setup.
(2) Internally generated bias voltage (V_{AC_REF}) is for 3.3-V operation only. It is recommended to apply externally generated bias voltage for V_{CC} < 3.0 V.

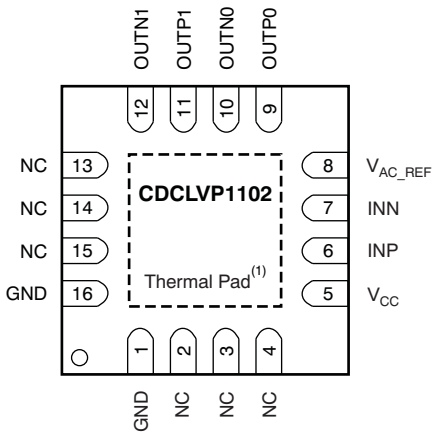
ELECTRICAL CHARACTERISTICS: LVPECL Output(1)

At V_{CC} = 3.0 V to 3.6 V and T_A = –40°C to +85°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	CDCLVP1102			UNIT
			MIN	TYP	MAX	
V_{OH}	Output high voltage		V_{CC} – 1.26		V_{CC} – 0.9	V
V_{OL}	Output low voltage		V_{CC} – 1.7		V_{CC} – 1.3	V
$V_{OUT, DIFF, PP}$	Differential output peak-peak voltage	f_{IN} ≤ 2 GHz	0.65		1.35	V
V_{AC_REF}	Input bias voltage	I_{AC_REF} = 2 mA	V_{CC} – 1.6		V_{CC} – 1.1	V
t_{PD}	Propagation delay	$V_{IN, DIFF, PP}$ = 0.1V			450	ps
		$V_{IN, DIFF, PP}$ = 0.3V			450	ps
$t_{SK,PP}$	Part-to-part skew				100	ps
$t_{SK,O}$	Output skew				10	ps
$t_{SK,P}$	Pulse skew (with 50% duty cycle input)	Crossing-point-to-crossing-point distortion, f_{OUT} = 100 MHz	–50		50	ps
t_{RJIT}	Random additive jitter (with 50% duty cycle input)	f_{OUT} = 100 MHz, $V_{IN,SE}$ = V_{CC}, V_{th} = 1.65 V, 10 kHz to 20 MHz		0.081		ps, RMS
		f_{OUT} = 100 MHz, $V_{IN,SE}$ = 0.9 V, V_{th} = 1.1 V, 10 kHz to 20 MHz		0.097		ps, RMS
		f_{OUT} = 2 GHz, $V_{IN,DIFF,PP}$ = 0.2 V, V_{ICM} = 1 V, 10 kHz to 20 MHz		0.050		ps, RMS
		f_{OUT} = 100 MHz, $V_{IN,DIFF,PP}$ = 0.15 V, V_{ICM} = 1 V, 10 kHz to 20 MHz		0.098		ps, RMS
		f_{OUT} = 100 MHz, $V_{IN,DIFF,PP}$ = 1 V, V_{ICM} = 1 V, 10 kHz to 20 MHz		0.095		ps, RMS
t_R/t_F	Output rise/fall time	20% to 80%			200	ps
I_{EE}	Supply internal current	Outputs unterminated			33	mA
I_{CC}	Output and internal supply current	All outputs terminated, 50 Ω to V_{CC} – 2			100	mA

(1) Figure 8 and Figure 9 show dc and ac test setup.

RGT PACKAGE
QFN-16
(TOP VIEW)



(1) Thermal pad must be soldered to ground.

PIN DESCRIPTIONS

CDCLVP1102 Pin Descriptions

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
V_{CC}	5	Power	2.5-V/3.3-V supply for the device
GND	1, 16	Ground	Device ground
INP, INN	6, 7	Input	Differential input pair or single-ended input
OUTP1, OUTN1	11, 12	Output	Differential LVPECL output pair no. 1. Unused output pair can be left floating.
OUTP0 OUTN0	9, 10	Output	Differential LVPECL output pair no. 0. Unused output pair can be left floating.
V_{AC_REF}	8	Output	Bias voltage output for capacitive-coupled input pair no. 0. Do not use V_{AC_REF} at V_{CC} < 3.0 V. If used, it is recommended to use a 0.1-µF capacitor to GND on this pin. The output current is limited to 2 mA.
NC	2, 3, 4, 13, 14, 15	—	Do not connect

TYPICAL CHARACTERISTICS

At T_A = –40°C to +85°C (unless otherwise noted).

DIFFERENTIAL OUTPUT PEAK-TO-PEAK VOLTAGE vs FREQUENCY

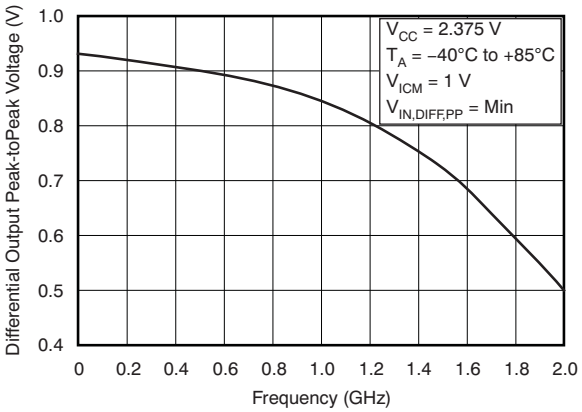


Figure 1.

DIFFERENTIAL OUTPUT PEAK-TO-PEAK VOLTAGE vs FREQUENCY

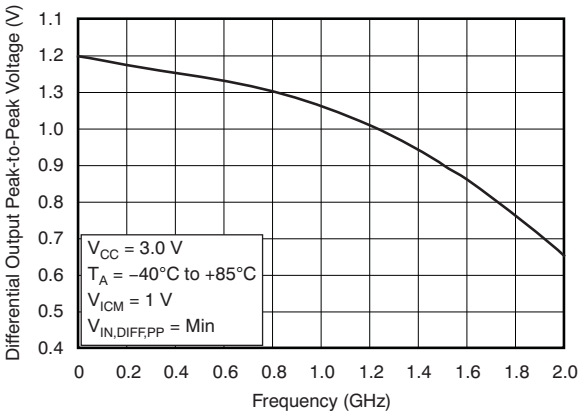


Figure 2.

TEST CONFIGURATIONS

This section describes the function of each block for the CDCLVP1102. Figure 3 through Figure 9 illustrate how the device should be setup for a variety of test configurations.

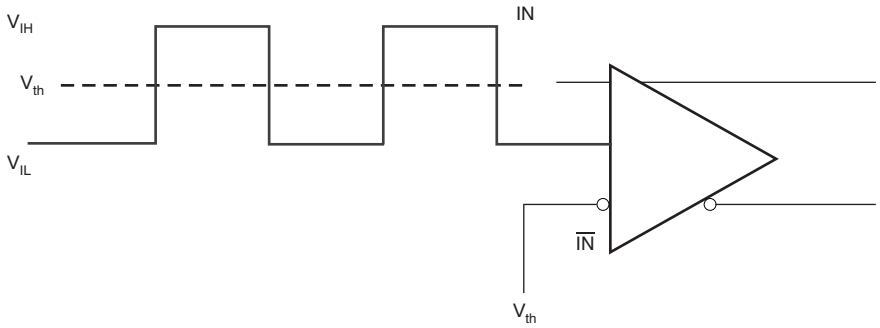


Figure 3. DC-Coupled LVCMOS Input During Device Test

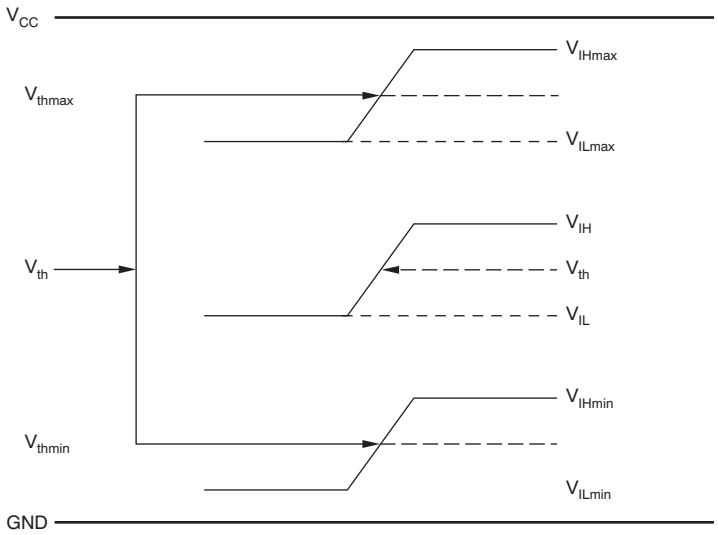


Figure 4. V_{th} Variation over LVCMOS Levels

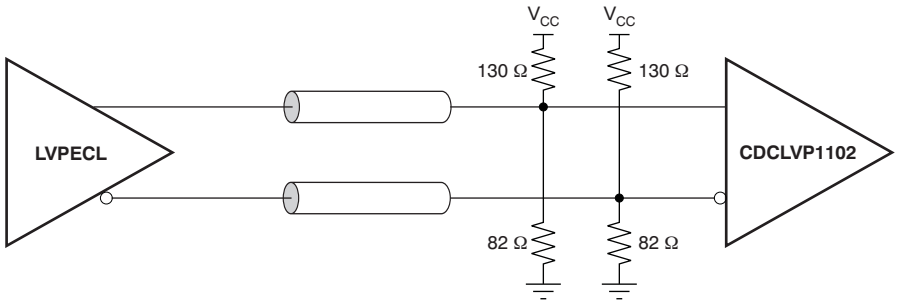


Figure 5. DC-Coupled LVPECL Input During Device Test

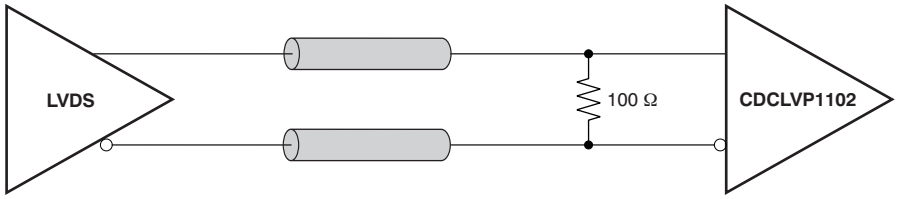


Figure 6. DC-Coupled LVDS Input During Device Test

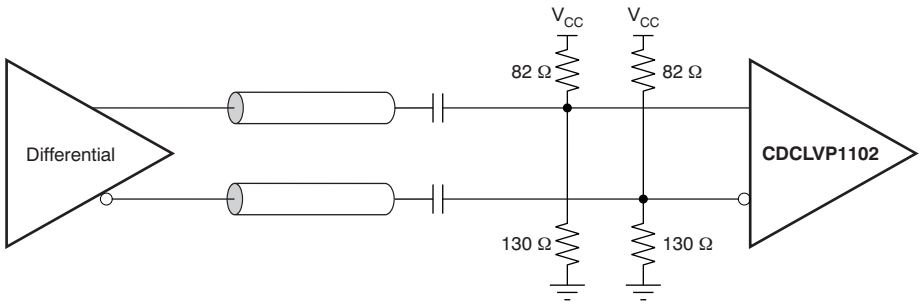


Figure 7. AC-Coupled Differential Input to Device

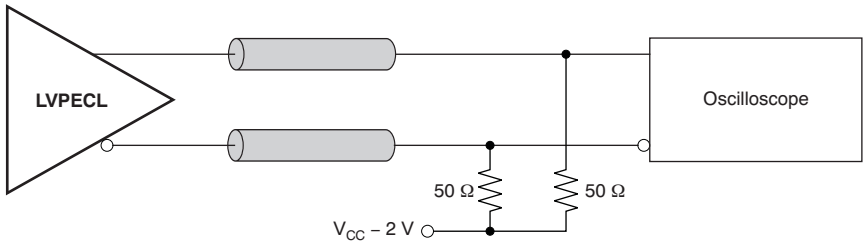


Figure 8. LVPECL Output DC Configuration During Device Test

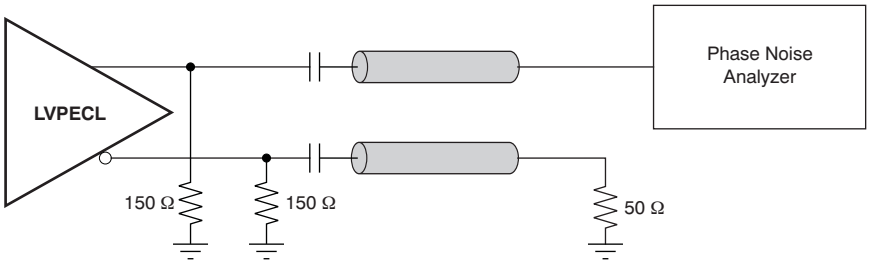


Figure 9. LVPECL Output AC Configuration During Device Test

Figure 10 shows the output voltage and rise/fall time. Output and part-to-part skew are shown in Figure 11.

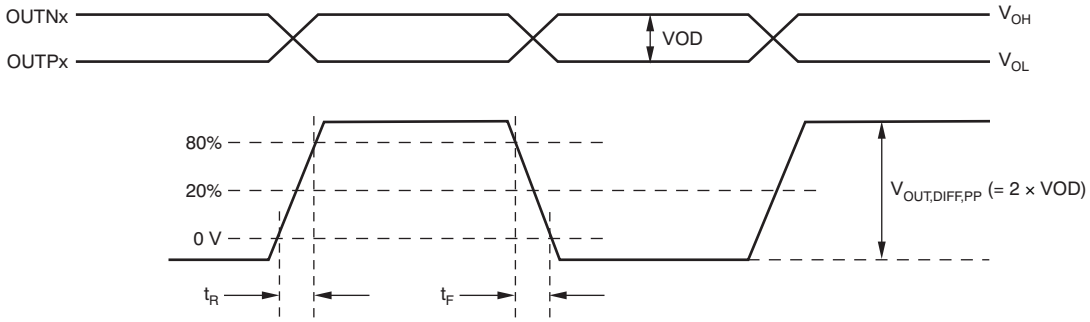
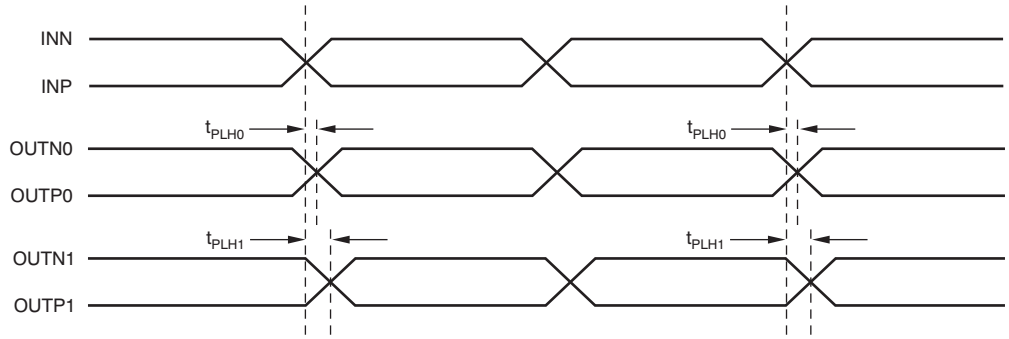


Figure 10. Output Voltage and Rise/Fall Time



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest t_{PLHn} (n = 0, 1), or as the difference between the fastest and the slowest t_{PHLn} (n = 0, 1).

(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest t_{PLHn} (n = 0, 1) across multiple devices, or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1) across multiple devices.

Figure 11. Output and Part-to-Part Skew

APPLICATION INFORMATION

Thermal Management

Power consumption of the CDCLVP1102 can be high enough to require attention to thermal management. For reliability and performance reasons, the die temperature should be limited to a maximum of +125°C. That is, as an estimate, ambient temperature (T_A) plus device power consumption times θ_{JA} should not exceed +125°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. Figure 12 shows a recommended land and via pattern.

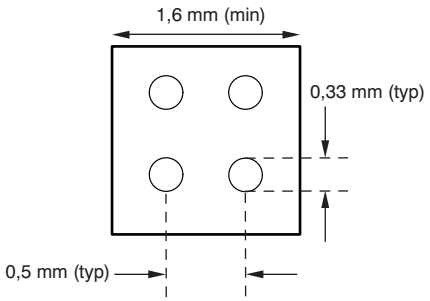


Figure 12. Recommended PCB Layout

Power-Supply Filtering

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is very critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply pins and laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1-µF) bypass capacitors as there are supply pins in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with very low dc resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

Figure 13 illustrates this recommended power-supply decoupling method.

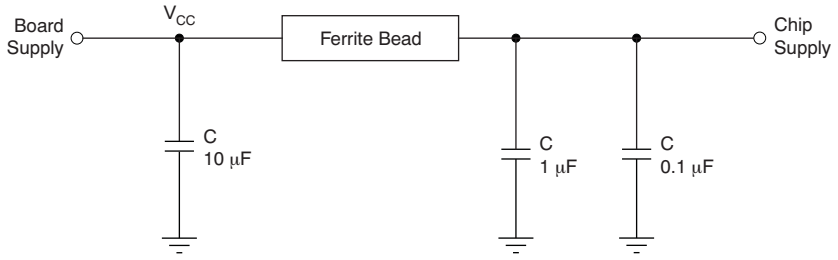
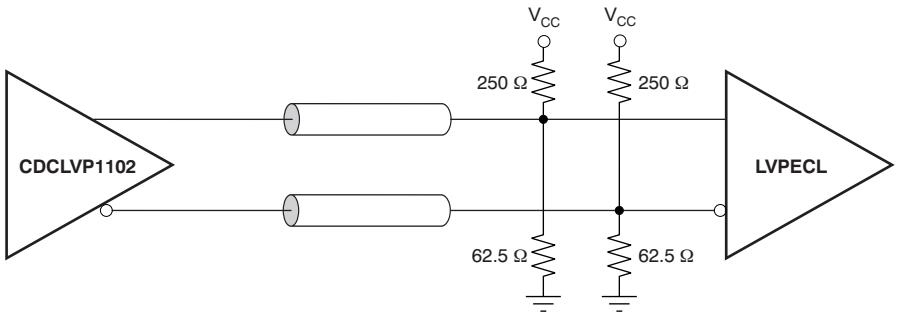


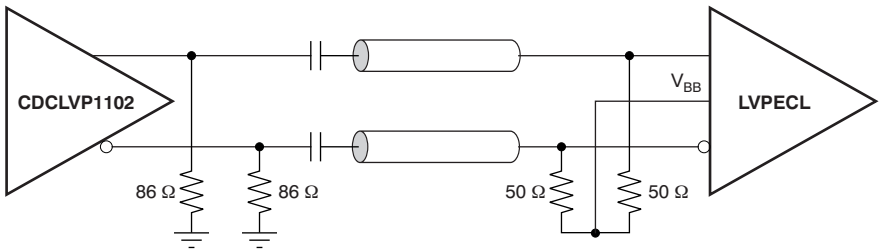
Figure 13. Power-Supply Decoupling

LVPECL Output Termination

The CDCLVP1102 is an open emitter for LVPECL outputs. Therefore, proper biasing and termination are required to ensure correct operation of the device and to minimize signal integrity. The proper termination for LVPECL outputs is a 50 Ω to (V_{CC} –2) V, but this dc voltage is not readily available on PCB. Therefore, a Thevenin equivalent circuit is worked out for the LVPECL termination in both direct-coupled (dc) and ac-coupled configurations. These configurations are shown in Figure 14a and b for V_{CC} = 2.5 V and Figure 15a and b for V_{CC} = 3.3 V, respectively. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltage for the driver and receiver is different, ac coupling is required.

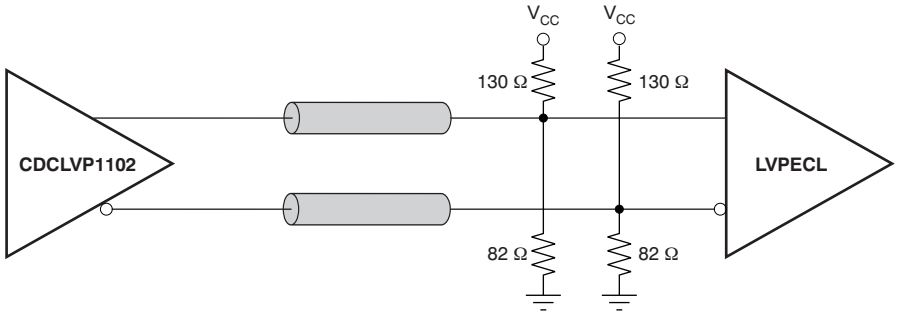


(a) Output DC Termination

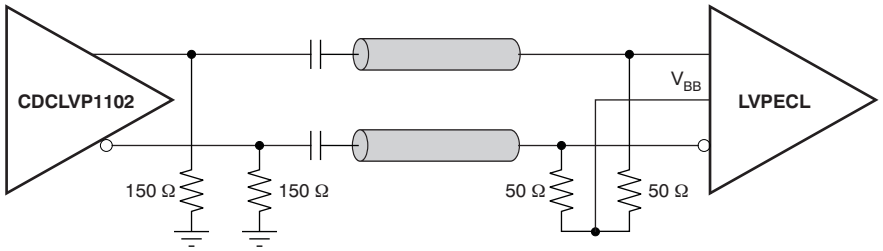


(b) Output AC Termination

Figure 14. LVPECL Output DC and AC Termination for V_{CC} = 2.5 V



(a) Output DC Termination



(b) Output AC Termination

Figure 15. LVPECL Output DC and AC Termination for V_{CC} = 3.3 V

Input Termination

The CDCLVP1102 inputs can be interfaced with LVPECL, LVDS, or LVCMOS drivers. Figure 16 illustrates how to dc couple an LVCMOS input to the CDCLVP1102. The series resistance (R_S) should be placed close to the LVCMOS driver; its value is calculated as the difference between the transmission line impedance and the driver output impedance.

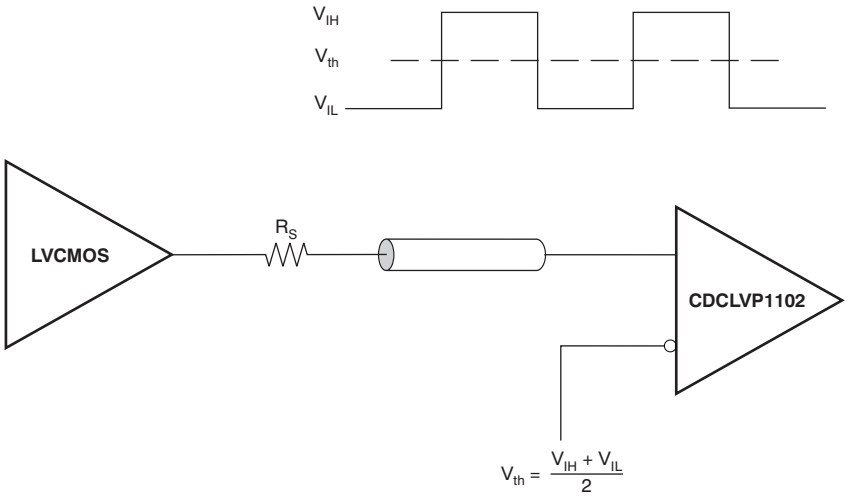


Figure 16. DC-Coupled LVCMOS Input to CDCLVP1102

Figure 17 shows how to dc couple LVDS inputs to the CDCLVP1102. Figure 18 and Figure 19 describe the method of dc coupling LVPECL inputs to the CDCLVP1102 for V_{CC} = 2.5 V and V_{CC} = 3.3 V, respectively.

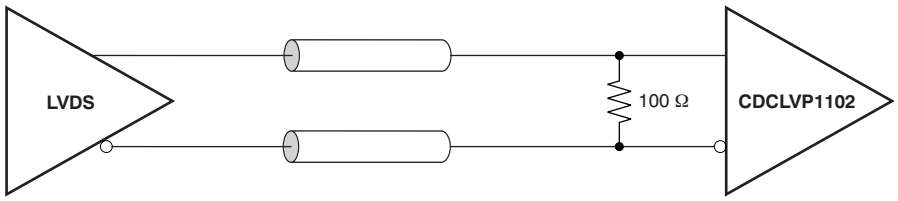


Figure 17. DC-Coupled LVDS Inputs to CDCLVP1102

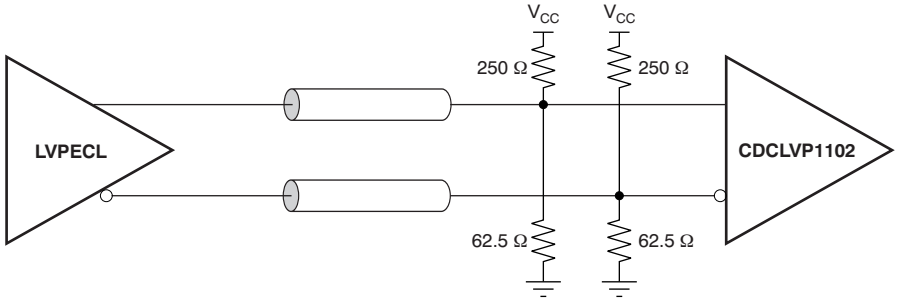


Figure 18. DC-Coupled LVPECL Inputs to CDCLVP1102 (V_{CC} = 2.5 V)

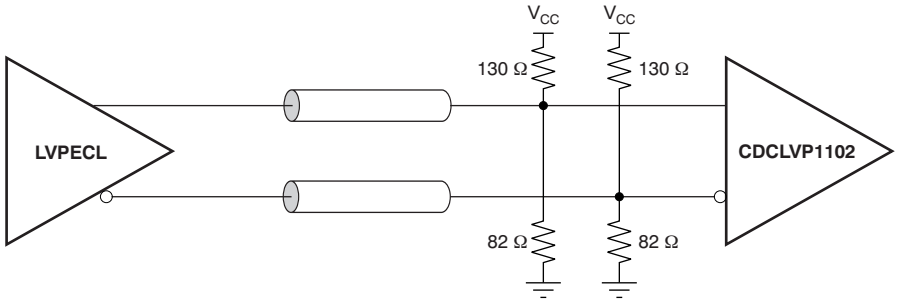


Figure 19. DC-Coupled LVPECL Inputs to CDCLVP1102 (V_{CC} = 3.3 V)

Figure 20 and Figure 21 show the technique of ac coupling differential inputs to the CDCLVP1102 for V_{CC} = 2.5 V and V_{CC} = 3.3 V, respectively. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltages of the driver and receiver are different, ac coupling is required.

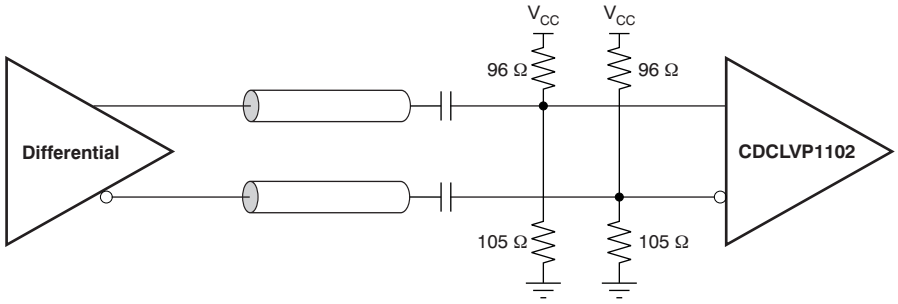


Figure 20. AC-Coupled Differential Inputs to CDCLVP1102 (V_{CC} = 2.5 V)

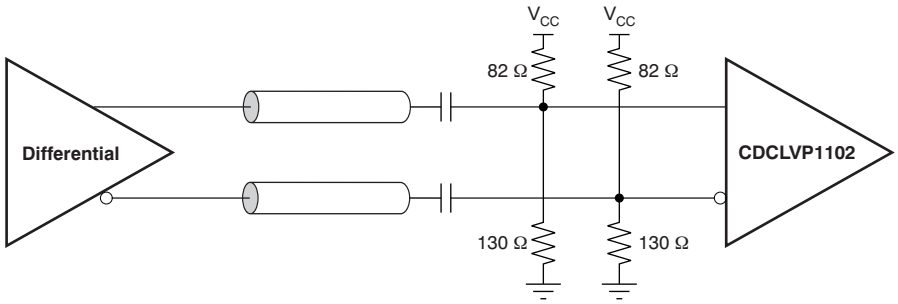


Figure 21. AC-Coupled Differential Inputs to CDCLVP1102 (V_{CC} = 3.3 V)

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May, 2010) to Revision C **Page**

- Corrected V_{IL} parameter description in *Electrical Characteristics* table for LVCMOS inputs 3
- Added footnote (2) to *Electrical Characteristics* table for LVPECL Output, V_{CC} = 2.375 V to 2.625 V 4
- Revised description of pin 8 6
- Changed recommended resistor values in Figure 14(a) 12
- Changed resistor values in Figure 18 14
- Changed resistor values in Figure 19 14

Changes from Revision A (October, 2009) to Revision B **Page**

- Changed description of OUTN1 and OUTN0 pins in *Pin Descriptions* table 6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
CDCLVP1102RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CDCLVP1102RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

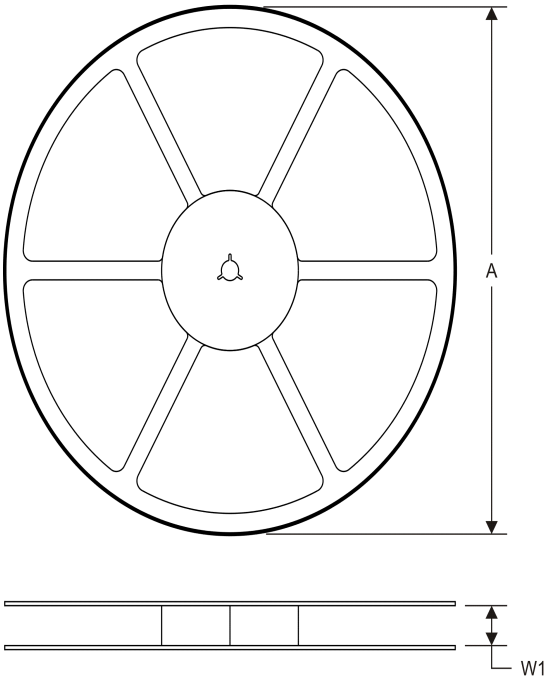
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

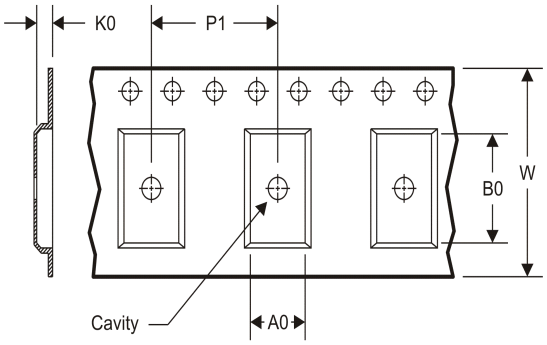
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



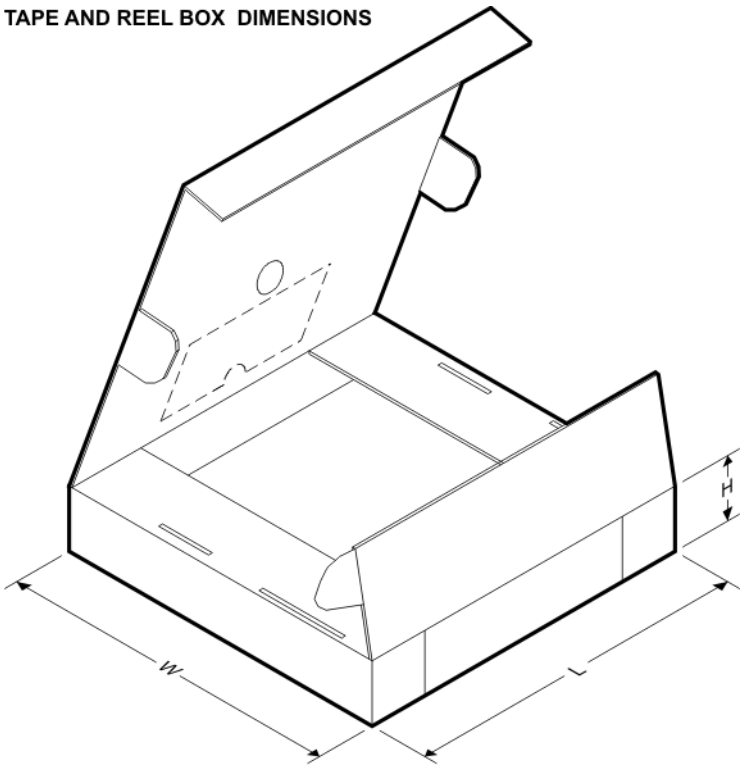
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVP1102RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
CDCLVP1102RGTT	QFN	RGT	16	250	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

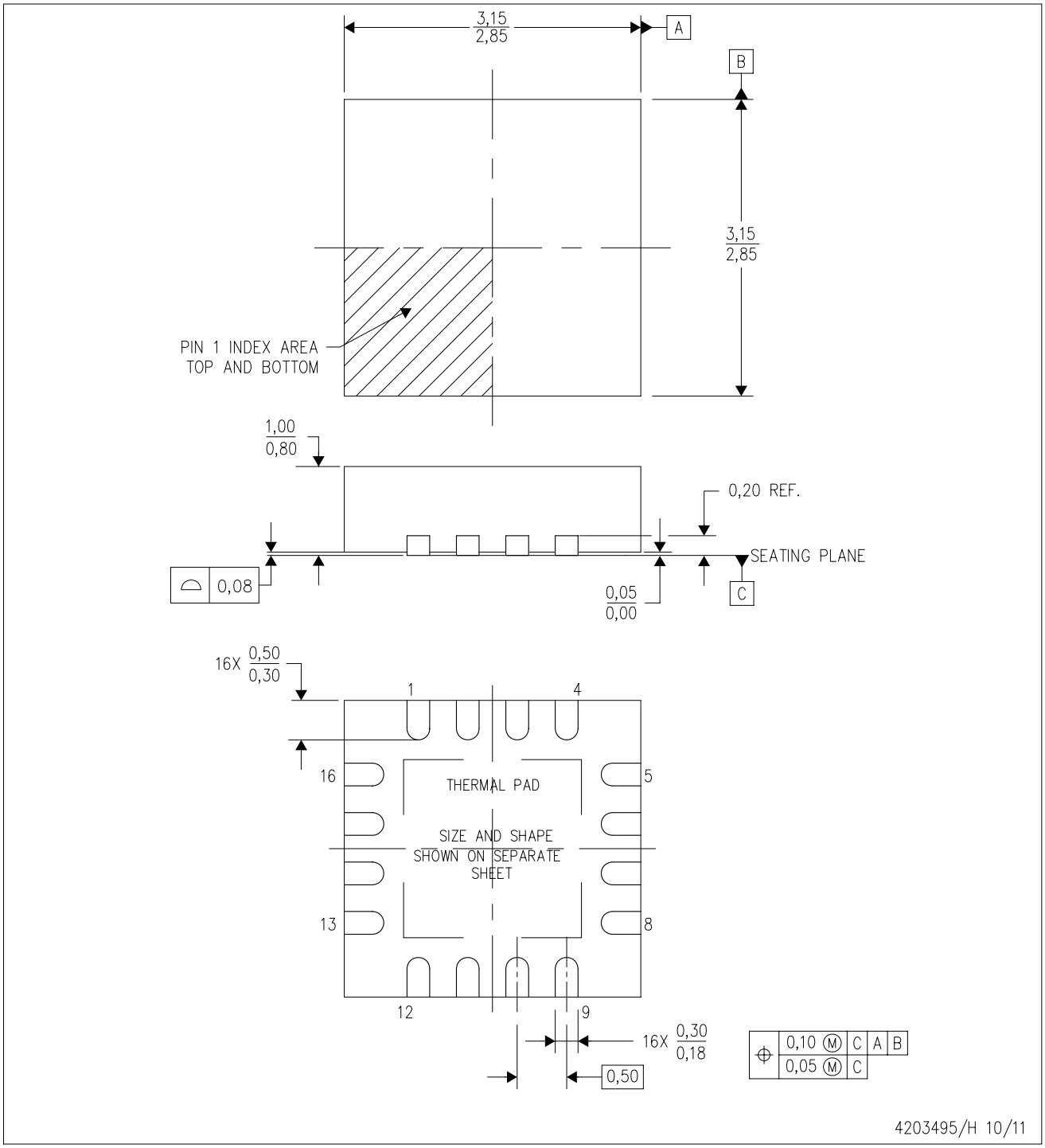
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVP1102RGTR	QFN	RGT	16	3000	338.1	338.1	20.6
CDCLVP1102RGTT	QFN	RGT	16	250	338.1	338.1	20.6

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

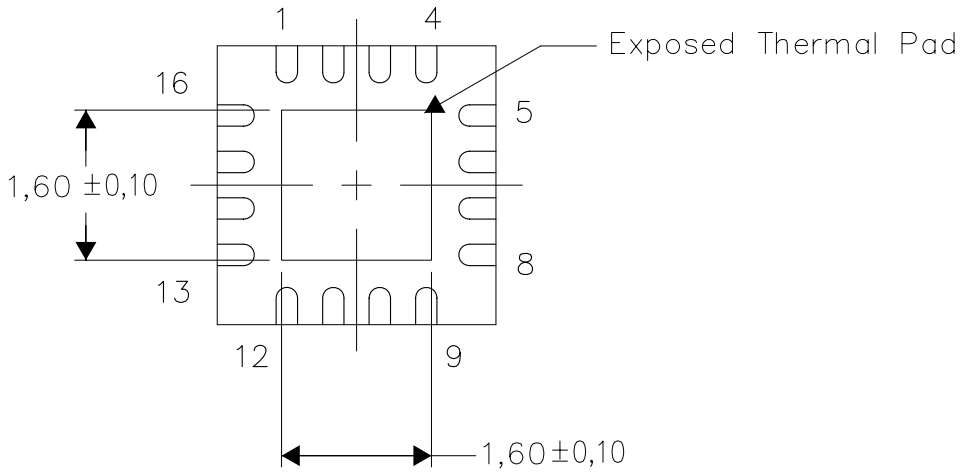
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



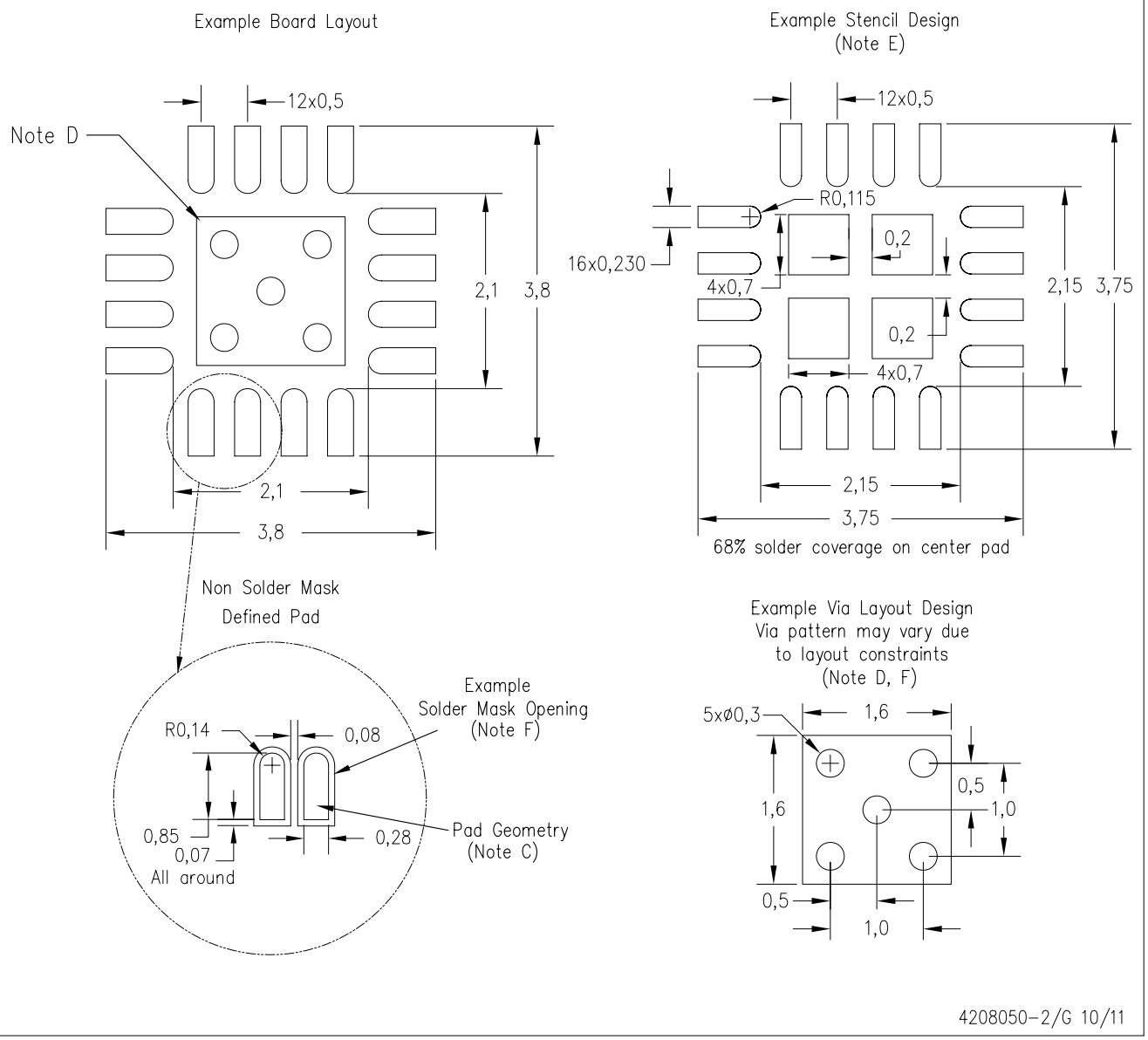
Bottom View

Exposed Thermal Pad Dimensions

4206349–3/Q 10/11

NOTE: All linear dimensions are in millimeters

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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