BUJ100LR

Silicon diffused power transistor

Rev. 01 — 12 August 2009

Product data sheet

1. Product profile

1.1 General description

High voltage, high speed, planar passivated NPN power switching transistor in a SOT54 (TO-92) 3 leads plastic package.

1.2 Features and benefits

Fast switching

■ High voltage capability of 700 V

1.3 Applications

- Compact fluorescent lamps (CFL)
- Electronic lighting ballasts
- Inverters
- Off-line self-oscillating power supplies

1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$I_{\mathbb{C}}$	collector current	DC; see Figure 1	-	-	1	Α
P _{tot}	total power dissipation	T _{lead} ≤ 25 °C; see <u>Figure 2</u>	-	-	2.1	W
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0 \text{ V}$	-	-	700	V
Static ch	naracteristics					
h _{FE}	DC current gain	$V_{CE} = 5 \text{ V; } I_{C} = 0.8 \text{ A;}$ $T_{lead} = 25 ^{\circ}\text{C;}$ see Figure 8 and 9	5	7.5	20	



2. Pinning information

Table 2. Pinning information

	_			
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	В	base		
2	С	collector		C
3			B	
			SOT54 (TO-92)	

3. Ordering information

Table 3. Ordering information

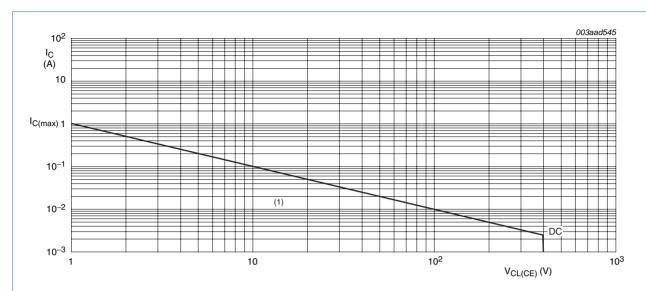
Type number	Package		
	Name	Description	Version
BUJ100LR	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

4. Limiting values

Table 4. Limiting values

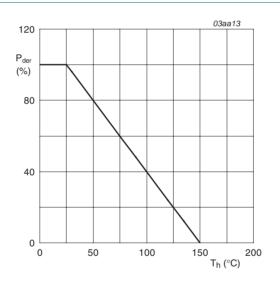
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0 \text{ V}$	-	700	V
V_{CBO}	collector-base voltage	I _E = 0 A	-	700	V
V _{CEO}	collector-emitter voltage	$I_B = 0 A$	-	400	V
I _C	collector current	DC; see Figure 1	-	1	Α
I _{CM}	peak collector current		-	2	Α
I _B	base current		-	0.5	Α
I _{BM}	peak base current		-	1	Α
P _{tot}	total power dissipation	T _{lead} ≤ 25 °C; see <u>Figure 2</u>	-	2.1	W
T _{stg}	storage temperature		-65	150	°C
T _j	junction temperature		-	150	°C
V_{EBO}	emitter-base voltage	I _C = 0 A; I(Emitter) = 10 mA	-	9	V



 $T_{lead} \le 25$ °C(1)Region of permissible DC operation

Fig 1. Forward bias safe operating area



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

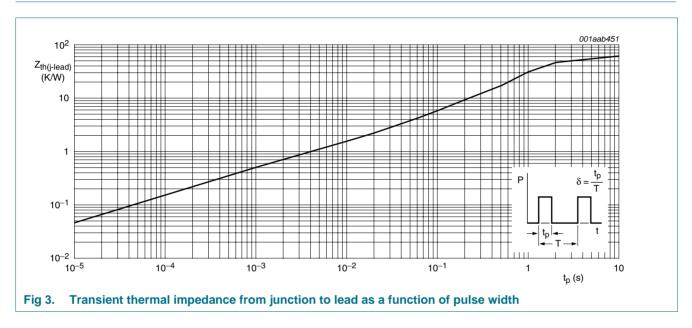
Fig 2. Normalized total power dissipation as a function of heatsink temperature



5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j\text{-lead})}$	thermal resistance from junction to lead	see Figure 3	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	150	-	K/W



6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics					
I _{CES}	collector-emitter cut-off	$V_{BE} = 0 \text{ V}; V_{CE} = 700 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	mΑ
	current	V _{BE} = 0 V; V _{CE} = 700 V; T _j = 125 °C	-	-	5	mΑ
I _{EBO}	emitter-base cut-off current	$V_{EB} = 9 \text{ V}; I_{C} = 0 \text{ A}; T_{lead} = 25 \text{ °C}$	-	-	1	mA
V_{CEOsus}	collector-emitter sustaining voltage	$I_B = 0 \text{ A}$; $I_C = 1 \text{ mA}$; $L_C = 25 \text{ mH}$; $T_{lead} = 25 ^{\circ}\text{C}$; see Figure 4 and 5	400	-	-	V
OLSat	collector-emitter saturation voltage	I_C = 0.25 A; I_B = 50 mA; T_{lead} = 25 °C; see Figure 6	-	0.2	0.5	V
		I_C = 0.5 A; I_B = 125 mA; T_{lead} = 25 °C; see Figure 6	-	0.3	1	V
		I_C = 0.75 A; I_B = 250 mA; T_{lead} = 25 °C; see Figure 6	-	0.4	1.5	V
V _{BEsat}	base-emitter saturation voltage	I_C = 0.25 A; I_B = 50 mA; T_{lead} = 25 °C; see Figure 7	-	-	1	V
		I_C = 0.5 A; I_B = 125 mA; T_{lead} = 25 °C; see Figure 7	-	-	1.2	V
h _{FE}	DC current gain	I_C = 0.5 mA; V_{CE} = 2 V; T_{lead} = 25 °C	12	-	-	
		$I_C = 0.4 \text{ A}$; $V_{CE} = 5 \text{ V}$; $T_{lead} = 25 \text{ °C}$; see Figure 8 and 9	10	-	30	
		I_C = 0.8 A; V_{CE} = 5 V; T_{lead} = 25 °C; see Figure 8 and 9	5	7.5	20	
Dynamic c	haracteristics					
t _f	fall time	I_C = 1 A; I_{Bon} = 200 mA; V_{BB} = -5 V; L_B = 1 μ H; T_{lead} = 25 °C; inductive load; see Figure 10 and 11	-	80	-	ns

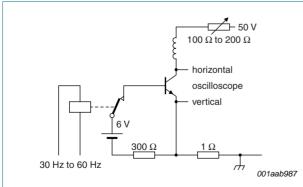


Fig 4. Test circuit for collector-emitter sustaining voltage

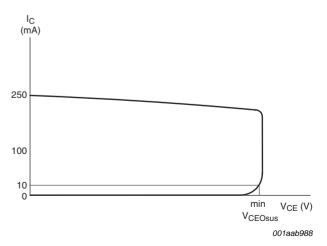


Fig 5. Oscilloscope display for collector-emitter sustaining voltage test waveform

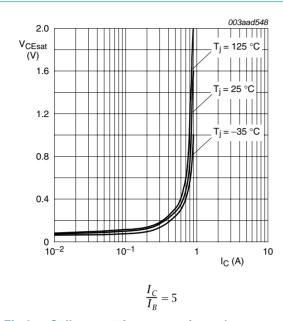


Fig 6. Collector-emitter saturation voltage as a function of collector current; typical values

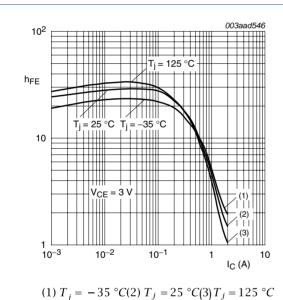


Fig 8. DC current gain as a function of collector current; typical values

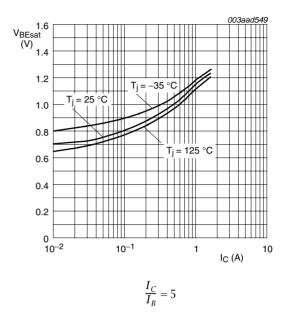
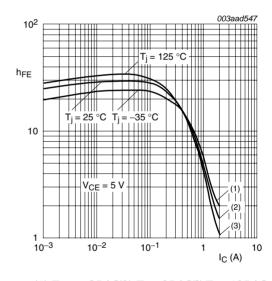


Fig 7. Base-emitter saturation voltage as a function of collector current; typical values

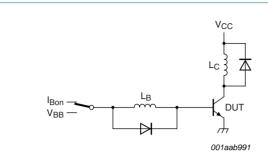


(1) $T_j = -35 \, ^{\circ}C(2) \, T_j = 25 \, ^{\circ}C(3) \, T_j = 125 \, ^{\circ}C$

Fig 9. DC current gain as a function of collector current; typical values

6 of 11





 $V_{CC} = 300 \ V; V_{BB} = -5 \ V; L_C = 200 \ \mu H; L_B = 1 \ \mu H$

Fig 10. Test circuit for inductive load switching

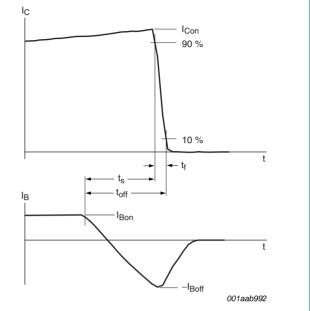
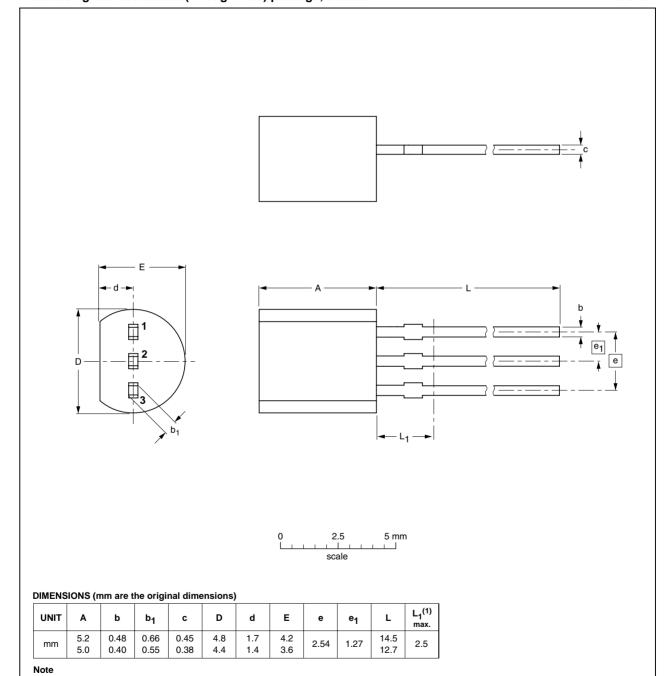


Fig 11. Switching times waveforms for inductive load

7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE		REFER	ENCES		EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC JEITA		PROJECTION	ISSUE DATE		
SOT54		TO-92	SC-43A			-04-06-28 04-11-16	

Fig 12. Package outline SOT54 (TO-92)



8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUJ100LR_1	20090812	Product data sheet	-	-



9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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