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HF/VHF power MOS transistor

BLF175

FEATURES

- High power gain
- Low intermodulation distortion
- Easy power control
- Good thermal stability
- Withstands full load mismatch
- Gold metallization ensures excellent reliability.

PIN CONFIGURATION

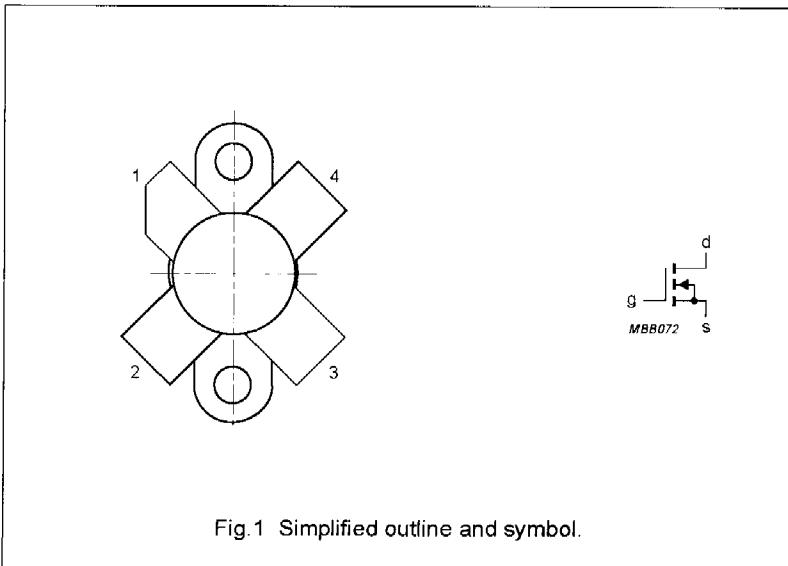


Fig.1 Simplified outline and symbol.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the HF/VHF frequency range.

The transistor has a 4-lead, SOT123A flange package, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the handbook 'General' section for further information.

PINNING - SOT123A

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

QUICK REFERENCE DATA

RF performance at $T_h = 25^\circ\text{C}$ in a common source test circuit.

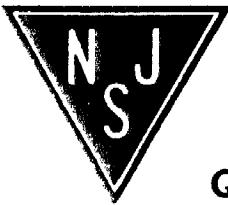
MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB)
class-A	28	50	800	8 (PEP)	>24	-	<-40
class-AB	28	50	150	30 (PEP)	typ. 24	typ. 40 ⁽¹⁾	typ. -35
CW, class-B	108	50	30	30	typ. 20	typ. 65	-

Note

1. 2-tone efficiency.

NJ Semi-Conductors reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However, NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.

Quality Semi-Conductors



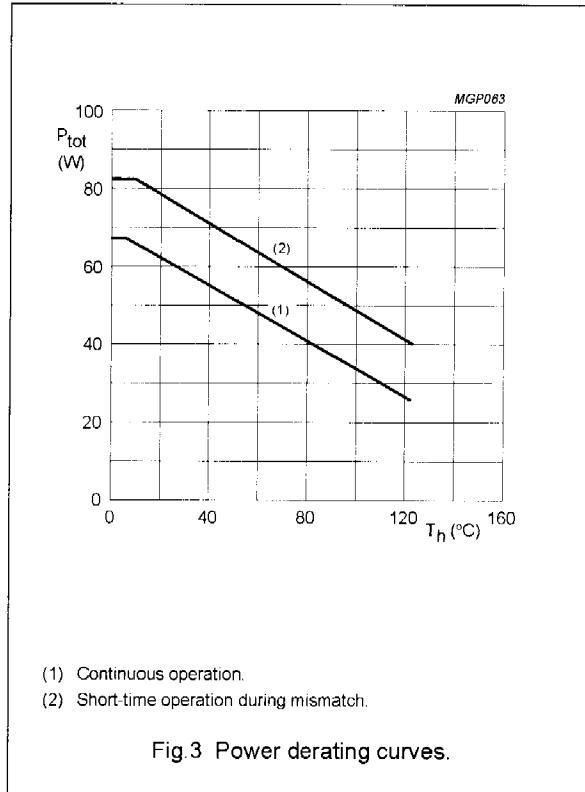
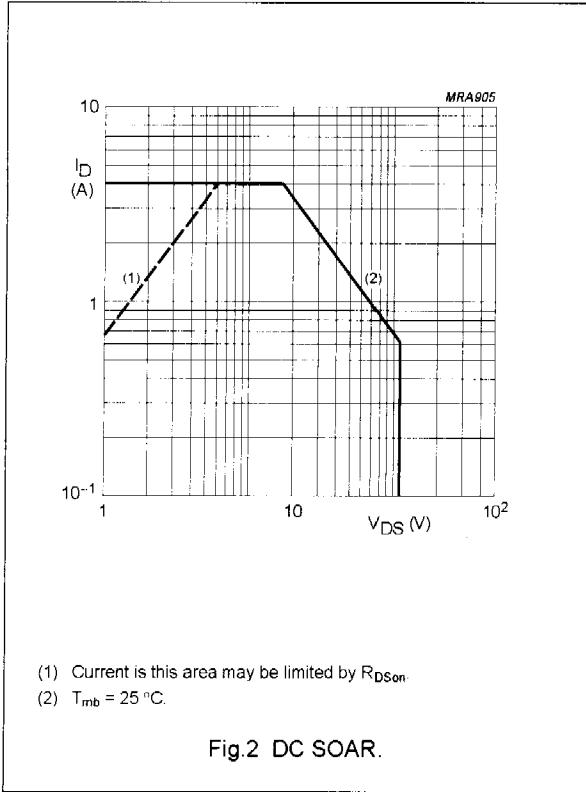
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	125	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	4	A
P_{tot}	total power dissipation	$T_{mb} \leq 25^\circ\text{C}$	–	68	W
T_{stg}	storage temperature		–65	+150	$^\circ\text{C}$
T_J	junction temperature		–	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th J-mb}$	thermal resistance from junction to mounting base	$T_{mb} = 25^\circ\text{C}; P_{tot} = 68 \text{ W}$	2.6	K/W
$R_{th mb-h}$	thermal resistance from mounting base to heatsink	$T_{mb} = 25^\circ\text{C}; P_{tot} = 68 \text{ W}$	0.3	K/W



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CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(\text{BR})\text{DSS}}$	drain-source breakdown voltage	$I_D = 100 \text{ mA}; V_{GS} = 0$	125	—	—	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0; V_{DS} = 50 \text{ V}$	—	—	100	μA
I_{GSS}	gate-source leakage current	$\pm V_{GS} = 20 \text{ V}; V_{DS} = 0$	—	—	1	μA
V_{GSt}	gate-source threshold voltage	$I_D = 10 \text{ mA}; V_{DS} = 10 \text{ V}$	2	—	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	$I_D = 10 \text{ mA}; V_{DS} = 10 \text{ V}$	—	—	100	mV
g_{fs}	forward transconductance	$I_D = 1 \text{ A}; V_{DS} = 10 \text{ V}$	1.1	1.6	—	S
R_{DSon}	drain-source on-state resistance	$I_D = 1 \text{ A}; V_{GS} = 10 \text{ V}$	—	0.75	1.5	Ω
I_{DSX}	on-state drain current	$V_{GS} = 10 \text{ V}; V_{DS} = 10 \text{ V}$	—	5.5	—	A
C_{is}	input capacitance	$V_{GS} = 0; V_{DS} = 50 \text{ V}; f = 1 \text{ MHz}$	—	130	—	pF
C_{os}	output capacitance	$V_{GS} = 0; V_{DS} = 50 \text{ V}; f = 1 \text{ MHz}$	—	36	—	pF
C_{rs}	feedback capacitance	$V_{GS} = 0; V_{DS} = 50 \text{ V}; f = 1 \text{ MHz}$	—	3.7	—	pF

V_{GS} group indication

GROUP	LIMITS (V)		GROUP	LIMITS (V)	
	MIN.	MAX.		MIN.	MAX.
A	2.0	2.1	O	3.3	3.4
B	2.1	2.2	P	3.4	3.5
C	2.2	2.3	Q	3.5	3.6
D	2.3	2.4	R	3.6	3.7
E	2.4	2.5	S	3.7	3.8
F	2.5	2.6	T	3.8	3.9
G	2.6	2.7	U	3.9	4.0
H	2.7	2.8	V	4.0	4.1
J	2.8	2.9	W	4.1	4.2
K	2.9	3.0	X	4.2	4.3
L	3.0	3.1	Y	4.3	4.4
M	3.1	3.2	Z	4.4	4.5
N	3.2	3.3			

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PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 4 leads

SOT123A

