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EDGE/GPRS/GSM SINGLE-CHIP MULTIMEDIA BASEBAND PROCESSOR

FEATURES

- Single mixed-signal package options:
 - 256 pin FBGA @ 14 x 14 mm
 - 276 pin FBGA @ 12 x 12 mm
- GSM voice handset capabilities: FR/EFR/HR/AMR
- GSM850, E-GSM900, GSM1800, and GSM1900 bands
- EDGE/GPRS Mobile Class B (multi-slot Class 10)
- All data modes for EDGE, HSCSD, and GPRS
- Incremental redundancy function
- 8PSK MAP equalizer
- ARM926EJ with support for Jazelle KVM acceleration
- Standard CCIR-656 video port/camera interface
- Color LCD parallel interface with graphics accelerator and video postprocessor
- MultiMedia Card (MMC) and Secure Digital (SD) I/F
- High resolution stereo audio DAC I/F
- USB 1.1 interface
- Low-power design: 3V I/O and 2.5V core
- Flexible audio circuitry
 - Noise suppression and echo cancellation for car/speaker phone
 - Sidetone/microphone amplification control
- High output speaker driver
- Real-time clock and alarm
- DMA controller (2-channel)
- NOR Flash and SRAM, or NAND Flash and SDRAM I/F

SUMMARY OF BENEFITS

Comprehensive EDGE/GPRS/GSM system design

- Release 99 EDGE/GPRS/GSM protocol stack
- Proven reference designs for bar-type and flip-type handsets
- Color display support (up to 262K colors) for two panels
- Interface to MIDI-based polyphonic ringers with wave table synthesis
- MP3 player
- Bluetooth[™] interface (with GAP, SDAP, HP, PAN, SPP, DNP, OBEX profiles, and others optional)
- Multicolored LED notifications/backlight
- Fully functional GSM handset user interface
- Foreign language fonts, including Chinese
- Startup animations, songs, games, and ring tones
 Unicode SMS and full EMS messaging
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- SIM Application Toolkit (SATK)
- Fully integrated Layer 1, including device drivers for peripherals
- AT commands (GSM 07.05 and 07.07) with 07.10 mux
- Phase 2+ supplemental services
- Transparent Class 2 and 2.0 fax (Group 3)
- Error correction:
- V.42, MNP2-4
- Radio Link Protocol (RLP)
- Compression: IP header for GPRS and V.42bis in all modes (greater than 200 kbps receive throughput)
- Rapid prototyping development system available

APPLICATIONS

- GSM and GPRS always-on multimedia handsets
- Wireless Internet (high-speed multislot EDGE)
- Modems for wireless mobile computing





OVERVIEW



The **BCM2132** EDGE/GPRS/GSM baseband processor offers a high level of system integration, performance, and features for next-generation wireless multimedia handsets and data modules. For low-power consumption, accelerators are extensively used for certain necessary computation-intensive functions.

The **BCM2132** contains all analog and digital EDGE/GPRS/GSM baseband processing functions on a single CMOS chip. Interface functions and drivers are integrated to enable auxiliary components such as microphone, speaker, and SIM to connect directly to the chip.

The Broadcom reference design is based on the industry-proven ARM9 RISC and TeakLite DSP cores, and Type Approved protocol stack software. The platform is well suited for support of multimedia handset features, such as MMS, WAP2.0 browser, and Java applications.

To accelerate the product development cycle, Broadcom can support the design of handset system solutions, including complete handset or modem software, evaluation boards, and reference designs. Extensive integration support through GSM Certification Forum (GCF), Inter-Operability Testing (IOT), and worldwide network testing can also be provided.

Processors

- ARM926EJ embedded RISC core, up to 78 MHz
 - Memory Management Unit (MMU)
 - 8 KB/8 KB instruction/data cache
 - 48 KB tightly coupled data memory
 - Page mode Flash memory interface
- TeakLite embedded DSP core, up to 78 MHz
- JTAG debug and ETM trace ports

Interfaces

- Three UART serial ports for data/testing/Bluetooth
- USB (version 1.1)
- Analog interface to speaker, microphone, and headset
- Keypad
- MMC/SD Flash card I/F
- Color LCD parallel I/F
- Camera I/F via CCIR-656 video port
- Multi-voltage SIM, PCMCIA, and IrDA compliant I/Fs
- Control interface to Power Management Unit
- Four-channel ADC for system monitoring
- Flexible RF transceiver control interface:
 - PA ramping RAM and DAC
 - Programmable schedule-based control
 - Supports straight or multiplexed I and Q interface
 - AFC DAC, APC DAC, and serial control

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