# 24-Bit Analog-to-Digital Converter with One- and Two-Channel Differential Inputs and Internal Oscillator

## FEATURES

- **100SPS Data Rate (High-Speed Mode)**
- **Single-Cycle Settling**
- **Easy Conversion Control with START Pin**
- **Automatic Shutdown**
- **Low Noise: 4μ$V_{RMS}$ Noise (High-Resolution Mode)**
- **Input Multiplexer with Two Differential Channels (ADS1226)**
- **Voltage Reference Supports Ratiometric Measurements**
- **Self-Calibrating**
- **Simple Read-Only 2-Wire Serial Interface**
- **Internal High-Impedance Input Buffer**
- **Internal Temperature Sensor**
- **Internal Oscillator**
- **Low-Power: 1mW While Operating, < 1μA During Shutdown**
- **Analog and Digital Supplies: 2.7V to 5.5V**

## APPLICATIONS

- **Hand-Held Instrumentation**
- **Portable Medical Equipment**
- **Industrial Process Control**

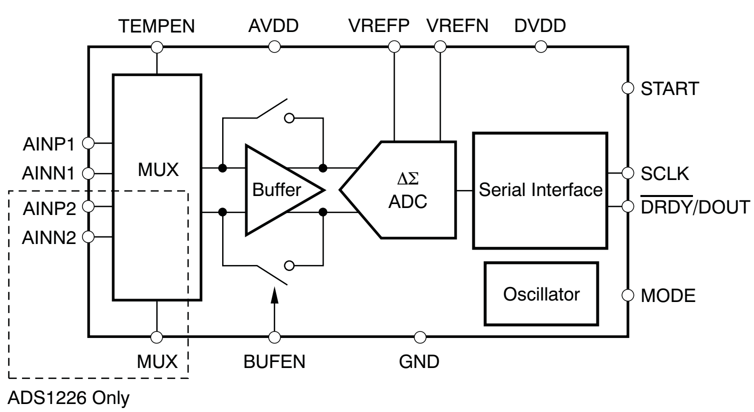
## DESCRIPTION

The ADS1225 and ADS1226 are 24-bit delta-sigma analog-to-digital (A/D) converters. They offer excellent performance, ease-of-use, and low power in a small 4mm × 4mm QFN package and are well-suited for demanding high-resolution measurements, especially in portable and other space-saving and power-constrained applications.

The ADS1225 and ADS1226 convert on command using a dedicated START pin. Simply pulse this pin to initiate a conversion. Data is read in a single cycle for retrieval over a 2-wire serial interface that easily connects to popular microcontrollers like the MSP430. After the conversion completes, the ADS1225 and ADS1226 automatically shuts down all circuitry.

Internal features include a two-channel multiplexer (ADS1226), selectable input buffer, temperature sensor, and oscillator. The full-scale range is defined by the external voltage reference with support provided for up to a 5V differential input signal. Two operating modes allow for speed (100SPS data rate, 15μ$V_{RMS}$ noise) or resolution (4μ$V_{RMS}$ noise, 16SPS data rate).

The ADS1225/6 supports 2.7 to 5.5V analog and digital supplies. Power consumption is 1mW while converting with 3V supplies. The ADS1225 and ADS1226 are fully specified over an extended industrial temperature range of –40°C to +105°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet or see the TI web site at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

| | ADS1225, ADS1226 | UNIT |
|---|---|---|
| AVDD to GND | –0.3 to +6 | V |
| DVDD to GND | –0.3 to +6 | V |
| Input current | 100, momentary | mA |
| | 10, continuous | mA |
| Analog input voltage to GND | –0.3 to AVDD +0.3 | V |
| Digital input voltage to GND | –0.3 to to AVDD +0.3 | V |
| Maximum junction temperature | +150 | °C |
| Operating temperature range | –55 to +125 | °C |
| Storage temperature range | –50 to +150 | °C |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

## ELECTRICAL CHARACTERISTICS

All specifications at $T_A$ = –40°C to +105°C, AVDD = +5V, DVDD = +3V, and $V_{REF}$ = +5V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | ADS1225, ADS1226 MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Analog Input** | | | | | |
| Full-scale input voltage | AINP – AINN | | $\pm V_{REF}$ | | V |
| Absolute input voltage | Buffer off; AINP, AINN with respect to GND | GND – 0.1 | | AVDD + 0.1 | V |
| | Buffer on; AINP, AINN with respect to GND | GND + 0.05 | | AVDD – 1.5 | V |
| Differential input impedance | Buffer off | | 2 | | MΩ |
| | Buffer on | | 1 | | GΩ |
| Common-mode input impedance | Buffer off | | 4 | | MΩ |
| **System Performance** | | | | | |
| Resolution | | 24 | | | Bits |
| Data rate | High-Speed mode | 75 | 100 | 125 | SPS(1) |
| | High-Resolution mode | 12 | 16 | 22 | SPS(1) |
| Integral nonlinearity (INL) | End-point fit | | 0.0005 | 0.0020 | % of FSR(2) |
| Offset error | | | 60 | 200 | µV |
| Offset error drift | | | 0.3 | | µV/°C |
| Gain error | | | 0.004 | 0.025 | % |
| Gain error drift | | | 0.3 | | ppm/°C |
| Common-mode rejection | At DC | 85 | 95 | | dB |
| Analog power-supply rejection | At DC, ± 10% Δ in AVDD | | 95 | | dB |
| Digital power-supply rejection | At DC, DVDD = 2.7V to 5.5V | | 80 | | dB |
| Noise | High-Speed mode | | 1.5 | | ppm of FSR, rms |
| | High-Resolution mode | | 0.4 | | ppm of FSR, rms |
| **Temperature Sensor** | | | | | |
| Temperature sensor voltage | $T_A$ = +25°C | | 106 | | mV |
| Temperature sensor coefficient | | | 360 | | µV/°C |
| **Voltage Reference Input** | | | | | |
| Reference input voltage | $V_{REF}$ = VREFP – VREFN | 0.5 | 5 | AVDD | V |
| Negative reference input | | GND - 0.1 | | VREFP – 0.5 | V |
| Positive reference input | | VREFN + 0.5 | | AVDD + 0.1 | V |
| Voltage reference impedance | | | 1.5 | | MΩ |

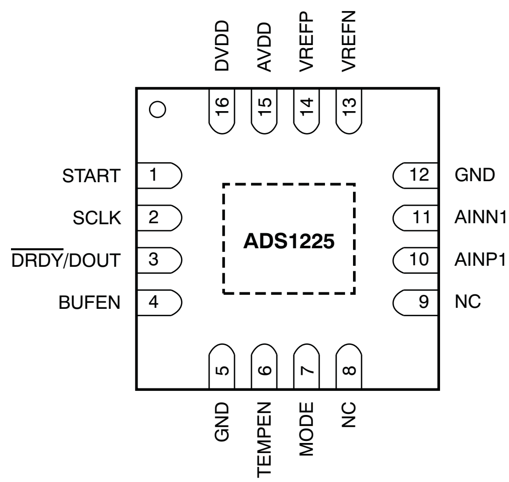
(1) SPS = samples per second.
(2) FSR = full-scale range = 2 × $V_{REF}$.

## ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A$ = –40°C to +105°C, AVDD = +5V, DVDD = +3V, and $V_{REF}$ = +5V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | ADS1225, ADS1226 MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Digital Input/Output** | | | | | | |
| Logic levels | $V_{IH}$ | | 0.8 DVDD | | DVDD + 0.1 | V |
| | $V_{IL}$ | | GND – 0.1 | | 0.2 DVDD | V |
| | $V_{OH}$ | $I_{OH}$ = 1mA | 0.8 DVDD | | | V |
| | $V_{OL}$ | $I_{OL}$ = 1mA | | | 0.2 DVDD | V |
| Input leakage | | | | | ±10 | µA |
| **Power Supply** | | | | | | |
| AVDD | | | 2.7 | | 5.5 | V |
| DVDD | | | 2.7 | | 5.5 | V |
| AVDD current | | Shutdown | | < 1 | | µA |
| | | AVDD = 5V, converting, buffer off | | 285 | | µA |
| | | AVDD = 5V, converting, buffer on | | 405 | | µA |
| | | AVDD = 3V, converting, buffer off | | 265 | | µA |
| | | AVDD = 3V, converting, buffer on | | 385 | | µA |
| DVDD current | | Shutdown | | < 1 | | µA |
| | | DVDD = 5V, converting | | 90 | | µA |
| | | DVDD = 3V, converting | | 55 | | µA |
| Total power dissipation | | AVDD = 5V, DVDD = 3V, buffer off | | 1.6 | 2.5 | mW |
| | | AVDD = DVDD = 3V, buffer off | | 1 | | mW |
| **Temperature Range** | | | | | | |
| Specified | | | –40 | | +105 | °C |
| Operating | | | –55 | | +125 | °C |
| Storage | | | –60 | | +150 | °C |

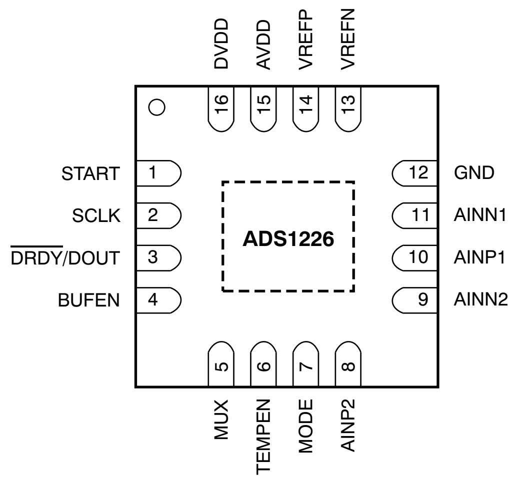
## PIN CONFIGURATION




## PIN DESCRIPTIONS – ADS1225

| TERMINAL | | ANALOG/DIGITAL INPUT/OUTPUT | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| START | 1 | Digital Input | High: Start conversions; Low: Shutdown |
| SCLK | 2 | Digital Input | Serial clock input |
| DRDY/DOUT | 3 | Digital Output | Dual-purpose output:<br>Data ready: indicates valid data by going low.<br>Data output: outputs data, MSB first, on the rising edge of SCLK. |
| BUFEN | 4 | Digital Input | Enables buffer after MUX |
| GND | 5 | Ground | Ground |
| TEMPEN | 6 | Digital Input | Selects temperature sensor input from MUX |
| MODE | 7 | Digital Input | Selects between High-Speed and High-Resolution modes |
| NC | 8 | | No connect |
| NC | 9 | | No connect |
| AINP1 | 10 | Analog Input | Analog channel 1 positive input |
| AINN1 | 11 | Analog Input | Analog channel 1 negative input |
| GND | 12 | Ground | Analog and digital ground |
| VREFN | 13 | Analog Input | Negative reference input |
| VREFP | 14 | Analog Input | Positive reference input |
| AVDD | 15 | Analog | Analog power supply |
| DVDD | 16 | Digital | Digital power supply |

**RGV PACKAGE**
**QFN-16 4.0mm x 4.0mm**
**(TOP VIEW)**




## PIN DESCRIPTIONS – ADS1226

| TERMINAL | | ANALOG/DIGITAL INPUT/OUTPUT | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| START | 1 | Digital Input | High: Start conversions; Low: Shutdown |
| SCLK | 2 | Digital Input | Serial clock input |
| $\overline{\text{DRDY}}$/DOUT | 3 | Digital Output | Dual-purpose output:<br>Data ready: indicates valid data by going low.<br>Data output: outputs data, MSB first, on the rising edge of SCLK. |
| BUFEN | 4 | Digital Input | Enables buffer after MUX |
| MUX | 5 | Digital Input | Selects analog input from MUX |
| TEMPEN | 6 | Digital Input | Selects temperature sensor input from MUX |
| MODE | 7 | Digital Input | Selects between High-Speed and High-Resolution modes |
| AINP2 | 8 | Analog Input | Analog channel 2 positive input |
| AINN2 | 9 | Analog Input | Analog channel 2 negative input |
| AINP1 | 10 | Analog Input | Analog channel 1 positive input |
| AINN1 | 11 | Analog Input | Analog channel 1 negative input |
| GND | 12 | Ground | Analog and digital ground |
| VREFN | 13 | Analog Input | Negative reference input |
| VREFP | 14 | Analog Input | Positive reference input |
| AVDD | 15 | Analog | Analog power supply |
| DVDD | 16 | Digital | Digital power supply |

# TYPICAL CHARACTERISTICS

At $T_A$ = –40°C to +85°C, AVDD = +5V, DVDD = +3V, and $V_{REF}$ = +5V, unless otherwise noted.

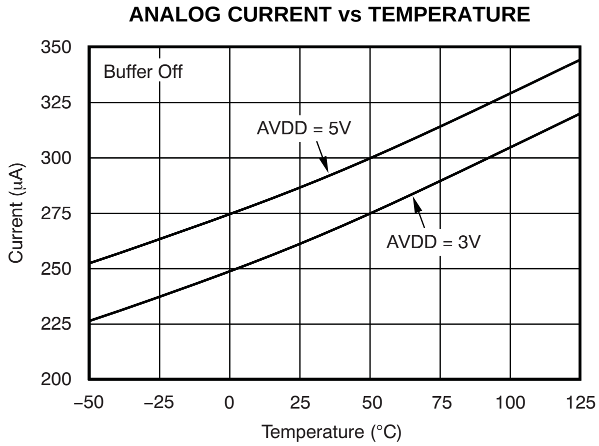



Figure 1.

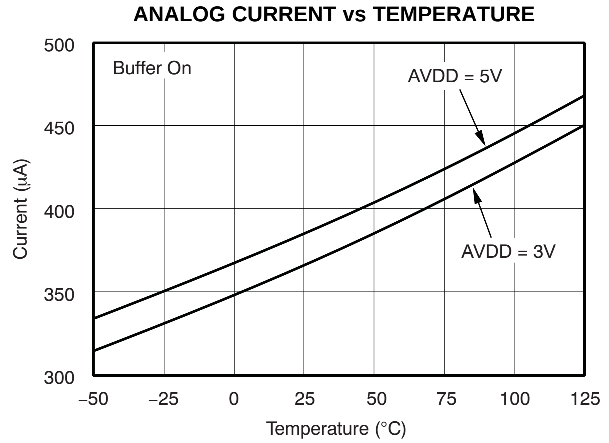



Figure 2.

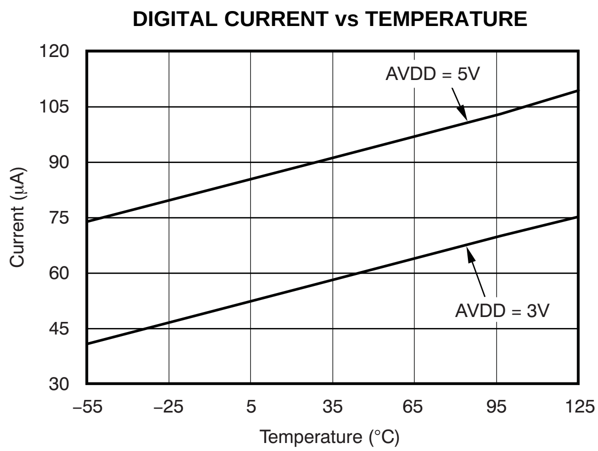



Figure 3.

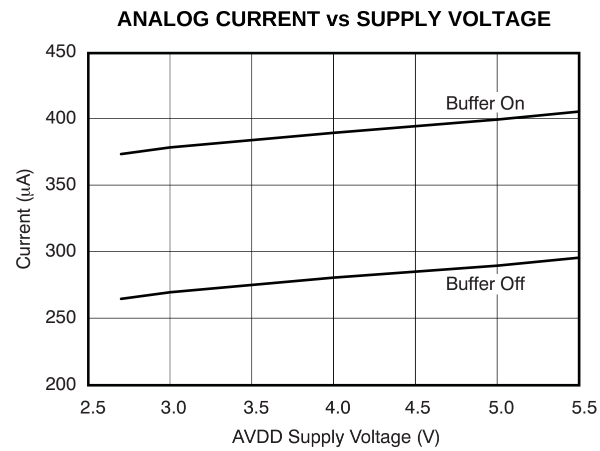



Figure 4.

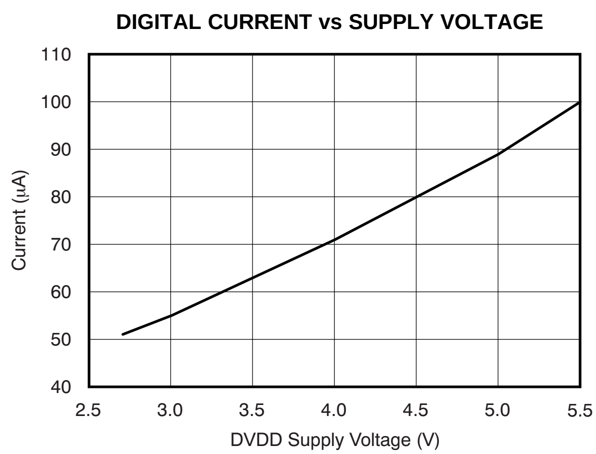



Figure 5.

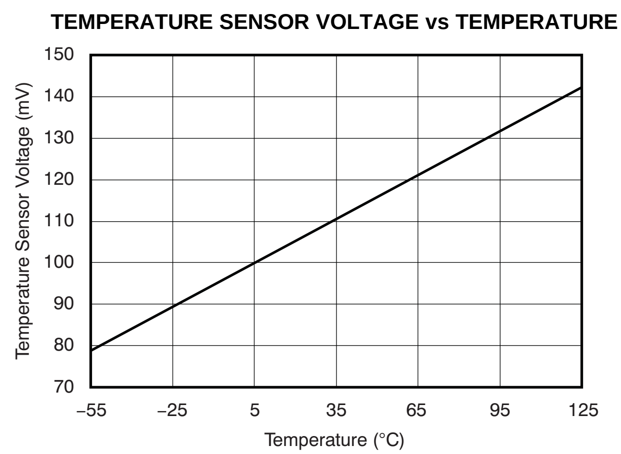



Figure 6.

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = –40°C to +85°C, AVDD = +5V, DVDD = +3V, and $V_{REF}$ = +5V, unless otherwise noted.

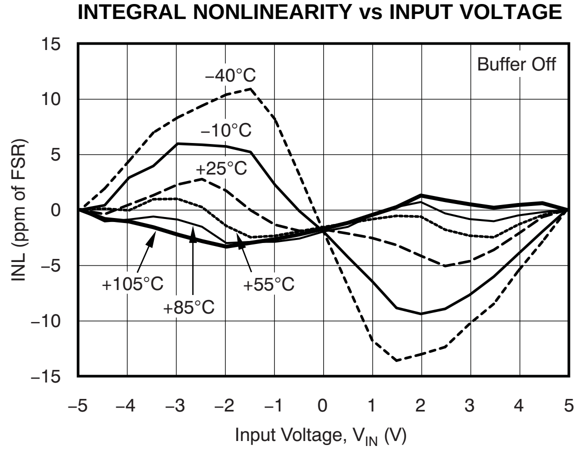



**Figure 7.**

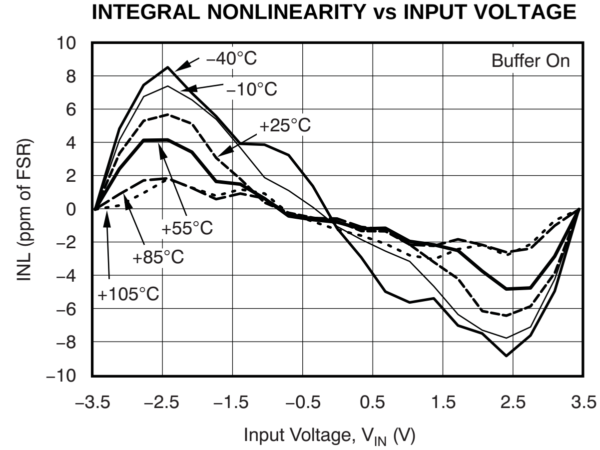



**Figure 8.**

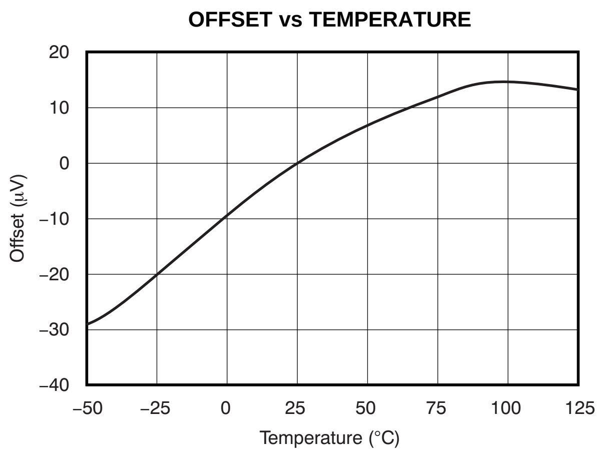



**Figure 9.**

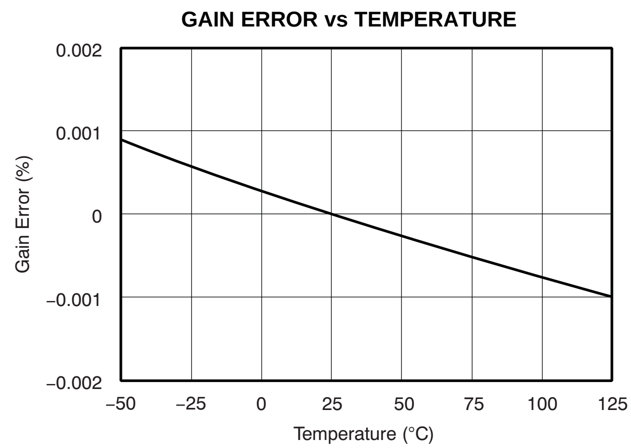



**Figure 10.**

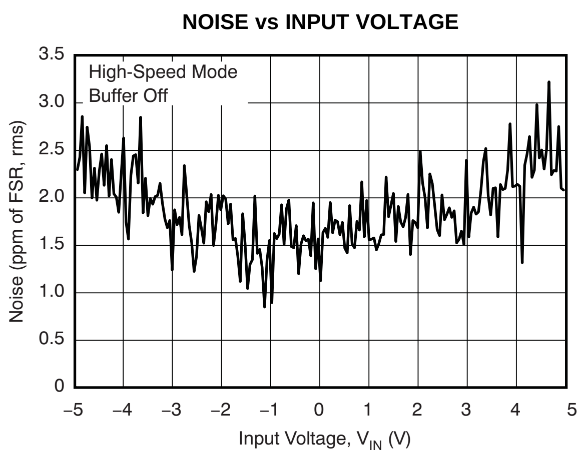



**Figure 11.**

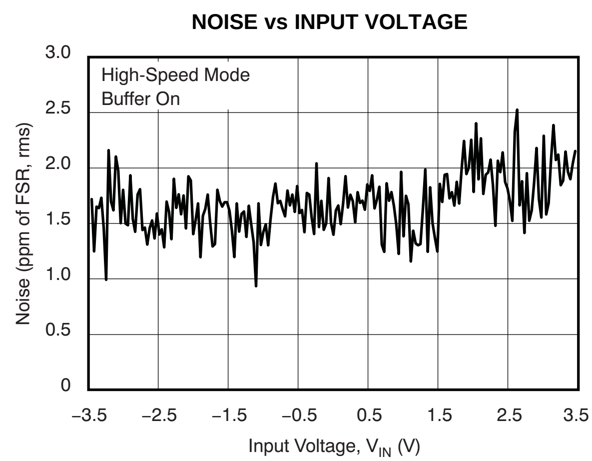



**Figure 12.**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = –40°C to +85°C, AVDD = +5V, DVDD = +3V, and $V_{REF}$ = +5V, unless otherwise noted.

**NOISE vs INPUT VOLTAGE**

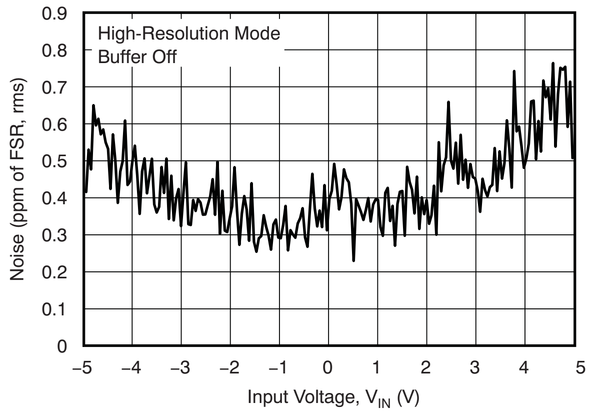



**Figure 13.**

**NOISE vs INPUT VOLTAGE**

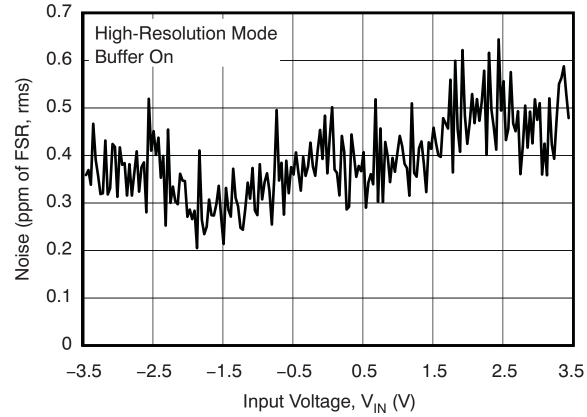



**Figure 14.**

**NOISE HISTOGRAM**

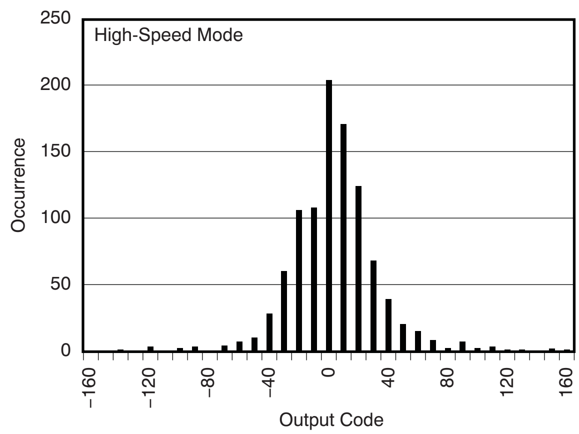



**Figure 15.**

**NOISE HISTOGRAM**

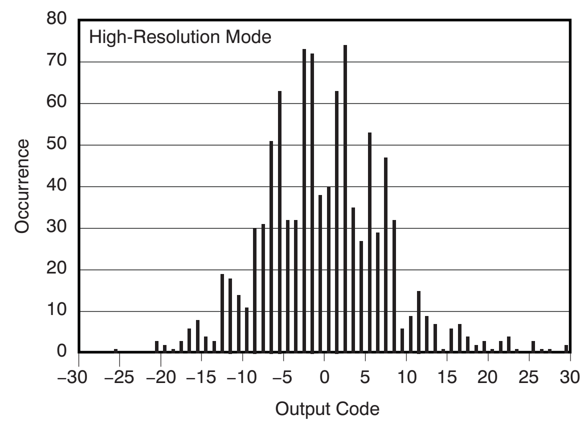



**Figure 16.**

**HIGH-SPEED MODE DATA RATE vs TEMPERATURE**

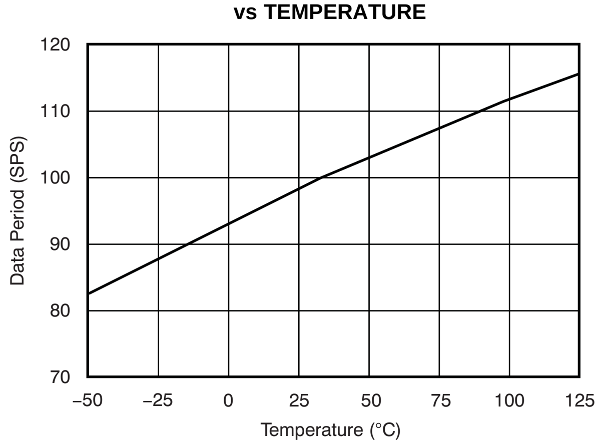



**Figure 17.**

**HIGH-RESOLUTION MODE DATA RATE vs TEMPERATURE**

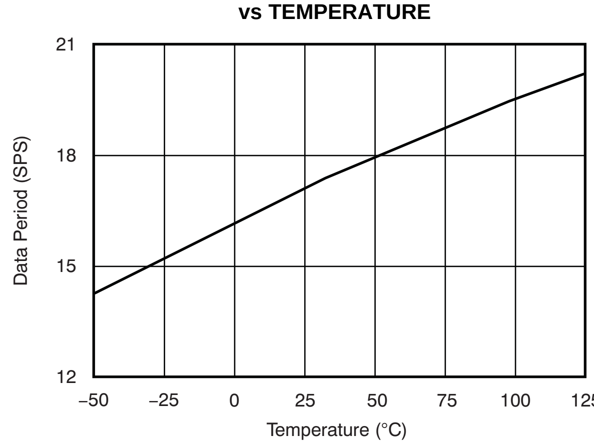



**Figure 18.**

## OVERVIEW

The ADS1225 and ADS1226 are 24-bit delta-sigma A/D converters. Figure 19 shows a conceptual diagram of the device. The ADS1225 has a single channel, while the ADS1226 allows for one of two input channels to be selected through a multiplexer. A buffer can also be selected to increase the input impedance. The modulator measures the differential input signal $V_{IN}$ = (AINP – AINN) against the differential reference $V_{REF}$ = (VREFP – VREFN). The full-scale input range is $\pm V_{REF}$. A 2-wire serial interface indicates conversion completion and provides the user with the output data. An internal oscillator allows for free-running of the ADS1225 and ADS1226.

Two other pins are used to control the operation of the ADS1225 and ADS1226. The START pin initiates conversions. The MODE pin puts the device into one of two modes. In High-Speed mode, the device gives data at 100 samples per second (SPS). In High-Resolution mode, data comes out at 16SPS with lower noise. In both modes, the device has single-cycle settling, reducing the latency of the output data.

## ANALOG INPUTS (AINx+, AINx–)

The input signal to be measured is applied to the input pins AINPx and AINNx. The positive internal input is generalized as AINP, and the negative internal input is generalized as AINN. The signal is selected though the input MUX, which is controlled by MUX, as shown in Table 1. The ADS1225 and ADS1226 accept differential input signals, but can also measure unipolar signals. When measuring unipolar (or single-ended) signals with respect to ground, connect the negative input (AINN) to ground and connect the input signal to the positive input (AINP). Note that when the ADS1225 and ADS1226 are configured this way, only half of the converter full-scale range is used since only positive digital output codes are produced. An input buffer can be selected to increase the input impedance of the A/D converter with the BUFEN pin.

**Table 1. Input Channel Selection with MUX**

| DIGITAL PIN | SELECTED ANALOG INPUTS | |
|---|---|---|
| MUX | POSITIVE INPUT | NEGATIVE INPUT |
| 0 | AINP1 | AINN1 |
| 1 | AINP2 | AINN2 |

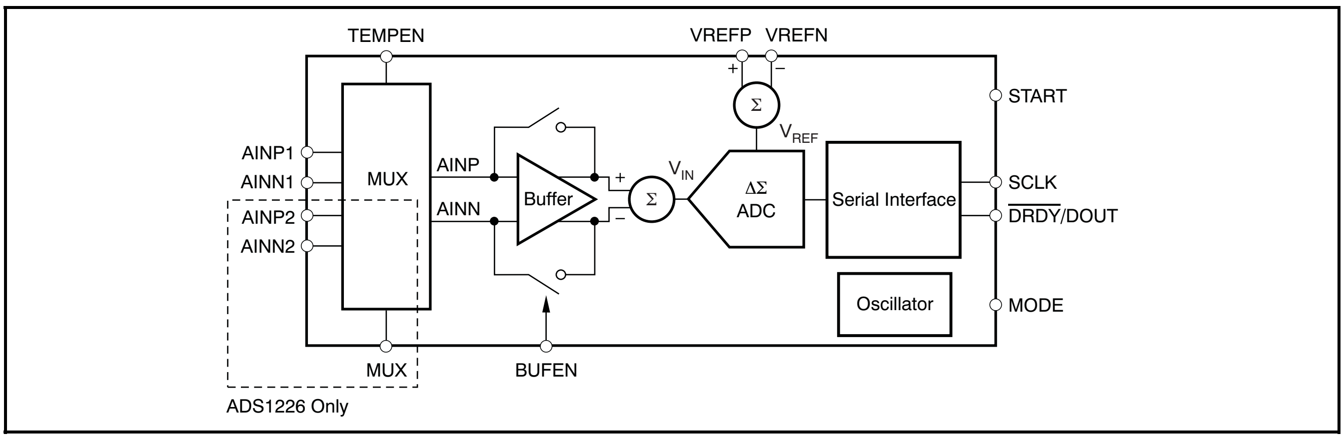



**Figure 19. Conceptual Diagram of the ADS1225 and ADS1226**

### Analog Input Measurement Without the Input Buffer

With the buffer disabled by setting the BUFEN pin low, the ADS1225 and ADS1226 measure the input signal using internal capacitors that are continuously charged and discharged. Figure 20 shows a simplified schematic of the ADS1225/6 input circuitry, with Figure 21 showing the on/off timings of the switches. The $S_1$ switches close during the input sampling phase. With $S_1$ closed, $C_{A1}$ charges to AINP, $C_{A2}$ charges to AINN, and $C_B$ charges to (AINP – AINN). For the discharge phase, $S_1$ opens first and then $S_2$ closes. $C_{A1}$ and $C_{A2}$ discharge to approximately VDD/2 and $C_B$ discharges to 0V. The constant charging of the input capacitors presents a load on the inputs that can be represented by effective impedances. Figure 22 shows the input circuitry with the capacitors and switches of Figure 20 by their effective impedances.

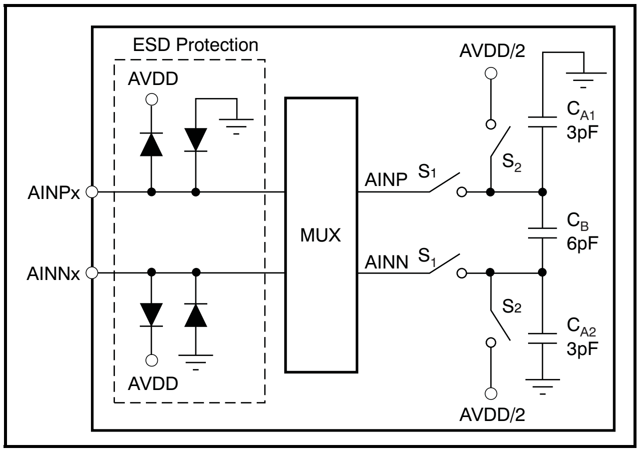



**Figure 20. Simplified Input Structure with the Buffer Turned Off**

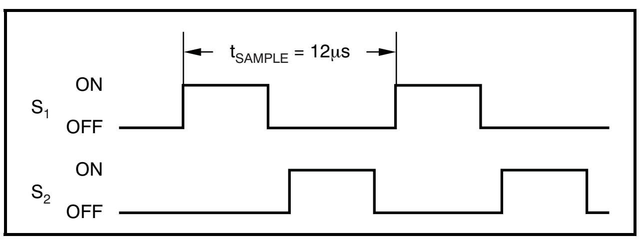



**Figure 21. $S_1$ and $S_2$ Switch Timing for Figure 20**

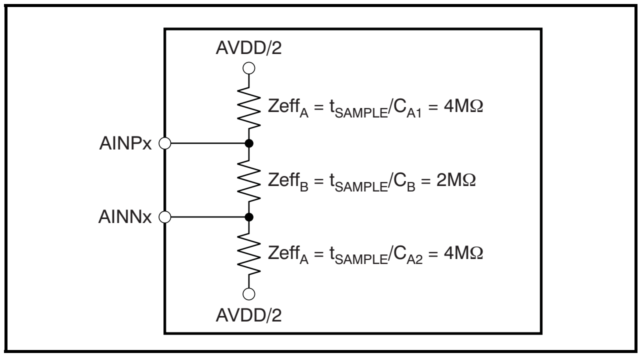



**Figure 22. Effective Analog Input Impedances with the Buffer Off**

ESD silicon diodes protect the inputs. To keep these diodes from turning on, make sure the voltages on the input pins do not go below GND by more than 100mV, and likewise do not exceed VDD by 100mV. This limitation is shown in Equation 1:

$$\text{GND} - 100\text{mV} < (\text{AINP, AINN}) < \text{VDD} + 100\text{mV} \quad (1)$$

### Analog Input Measurement with the Input Buffer

When the buffer is enabled by setting the BUFEN pin high, a low-drift, chopper-stabilized input buffer is used to achieve very high input impedance. The buffer charges the input sampling capacitors, thus removing the load from the measurement. Because the input buffer is chopper-stabilized, the charging of parasitic capacitances causes the charge to be carried away, as if by resistance. The input impedance can be modeled by a single resistor, as shown in Figure 23.

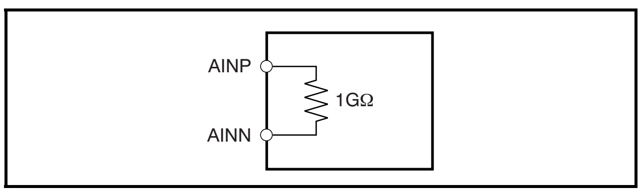



**Figure 23. Effective Analog Input Impedances with the Buffer On**

Note that the analog inputs (listed in the Electrical Characteristics table as *Absolute Input Range*) must remain between GND + 0.05V to AVDD – 1.5V. Exceeding this range degrades linearity and results in performance outside the specified limits.

## TEMPERATURE SENSOR

Internal diodes provide temperature-sensing capability. By setting the TEMPEN pin high, the selected analog inputs are disconnected and the inputs to the A/D converter are connected to the anodes of two diodes scaled to 1x and 64x in current and size inside the MUX, as shown in Figure 24. By measuring the difference in voltage of these diodes, temperature changes can be inferred from a baseline temperature. Typically, the difference in diode voltages is 106mV at +25°C, with a temperature coefficient of 360µV/°C. A similar structure is used in the MSC1210 for temperature measurement. For more information, see TI application report SBAA100, Using the MSC121x as a High-Precision Intelligent Temperature Sensor, available for download at www.ti.com.

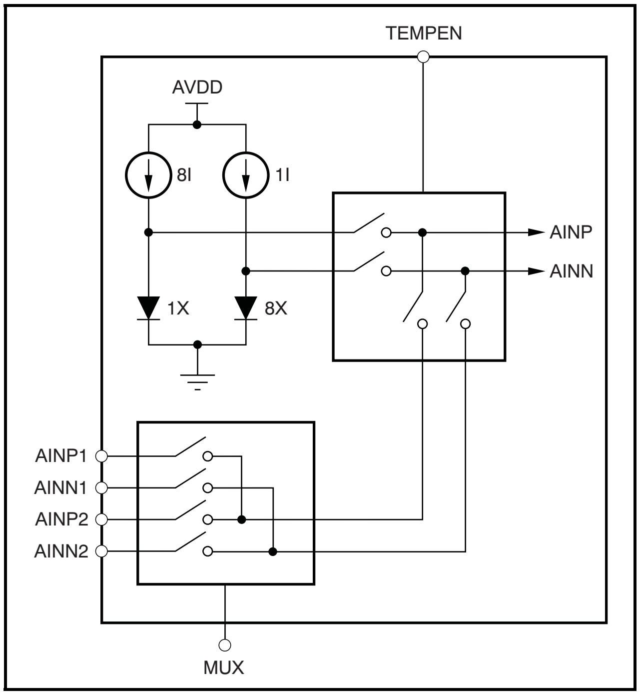



**Figure 24. Measurement of the Temperature Sensor in the Input**

## VOLTAGE REFERENCE INPUTS (VREFP, VREFN)

The voltage reference used by the modulator is generated from the voltage difference between VREFP and VREFN: $V_{REF}$ = VREFP – VREFN. The reference inputs use a structure similar to that of the analog inputs. A simplified diagram of the circuitry on the reference inputs is shown in Figure 25. The switches and capacitors can be modeled with an effective impedance of 250kΩ.

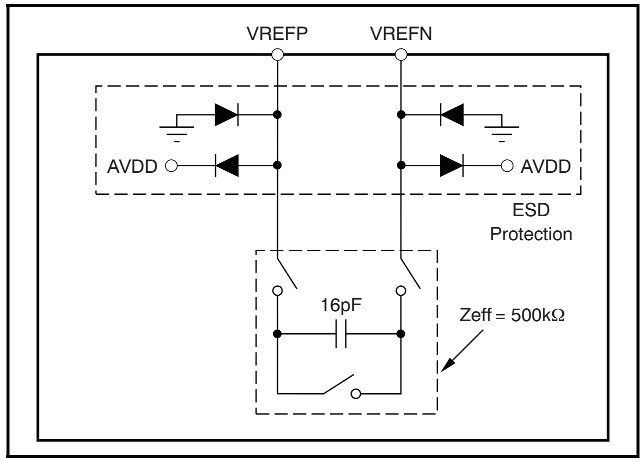



**Figure 25. Simplified Reference Input Circuitry**

ESD diodes protect the reference inputs. To prevent these diodes from turning on, make sure the voltages on the reference pins do not go below GND by more than 100mV, and likewise, do not exceed VDD by 100mV. This limitation is shown in Equation 2:

$$GND - 100mV < (VREFP, VREFN) < VDD + 100mV \quad (2)$$

For best performance, bypass the voltage reference inputs with a 0.1µF capacitor between VREFP and VREFN. Place the capacitor as close as possible to the pins.

The differential voltage reference inputs and the wide range of operation ($V_{REF}$ can support up to AVDD) make ratiometric measurements easy to implement.

## INTERNAL OSCILLATOR

The ADS1225 and ADS1226 have an internal oscillator and run without an external crystal or oscillator.

## DATA READY/DATA OUTPUT ($\overline{DRDY}$/DOUT)

This digital output pin serves two purposes. First, it indicates when new data is ready by going LOW. Afterwards, on the first rising edge of SCLK, the $\overline{DRDY}$/DOUT pin changes function and begins to output the conversion data, most significant bit (MSB) first. Data is shifted out on each subsequent SCLK rising edge. After all 24 bits have been retrieved, the pin can be forced high with an additional SCLK. It then stays high until new data is ready. This configuration is useful when polling on the status of $\overline{DRDY}$/DOUT to determine when to begin data retrieval.

## SERIAL CLOCK INPUT (SCLK)

This digital input shifts serial data out with each rising edge. As with CLK, this input may be driven with 5V logic regardless of the DVDD voltage. There is hysteresis built into this input, but care should still be taken to ensure a clean signal. Glitches or slow-rising signals can cause unwanted additional shifting. For this reason, it is best to make sure the rise-and-fall times of SCLK are less than 50ns.

## MODE

The ADS1225 and ADS1226 have two modes of operation, allowing for High-Speed or High-Resolution. By taking the MODE pin high, the data rate is approximately 100Hz with an rms noise of 15µV. When the MODE pin is low, the ADS1225 and ADS1226 average multiple samples to increase the noise performance to 4µV of rms noise with a data rate of 16Hz. Table 2 shows the MODE pin operation.

**Table 2. MODE Pin Operation for the ADS1225 and ADS1226**

| MODE PIN | MODE | DATA RATE | NOISE |
|---|---|---|---|
| 0 | High-Resolution | 16SPS | 4µVrms |
| 1 | High-Speed | 100SPS | 15µVrms |

## START

The START pin provides easy and precise control of conversions. Pulse the START pin high to begin a conversion as shown in Figure 26 and Table 3. The completion of the conversion is indicated by the $\overline{DRDY}$/DOUT pin going low. Once the conversion completes, the ADS1225 and ADS1226 automatically shut down to save power. They stay shut down until START is once again taken high to begin a new conversion.

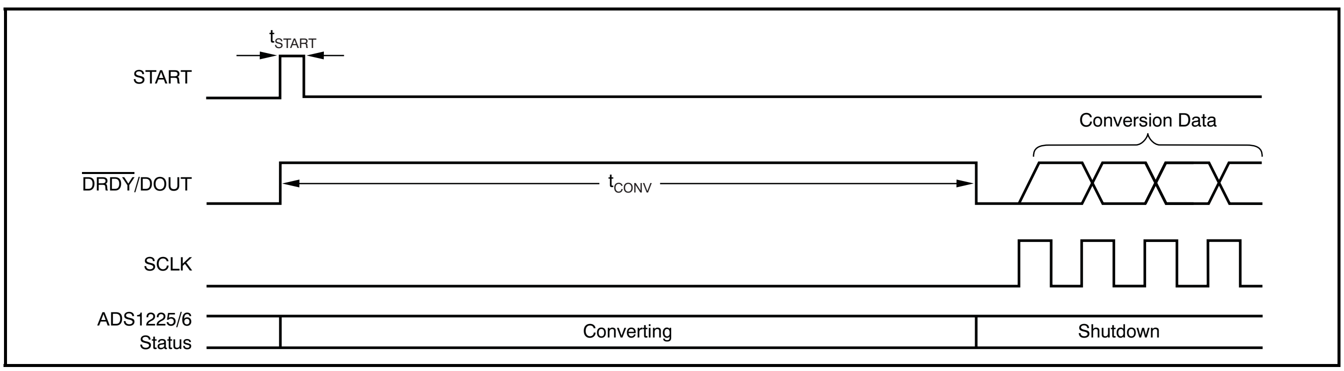



**Figure 26. Controlling Conversion with the START Pin**

**Table 3. START Pin Conversion Times for Figure 26**

| SYMBOL | DESCRIPTION | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{START}$ | Minimum START pulse to initiate a conversion | 17 | | µs |
| $t_{CONV}$ | Conversion time High-Speed mode | 8.0 | 13.3 | ms |
| | Conversion time High-Resolution mode | 45.5 | 83.3 | ms |

The ADS1225 and ADS1226 can be configured to continuously convert by holding the START pin high as shown in Figure 27. With START held high, a new conversion starts immediately after the previous conversion completes. This configuration continues until the START pin is taken low.

## DATA FORMAT

The ADS1225 and ADS1226 output 24 bits of data in binary two's complement format. The least significant bit (LSB) has a weight of $(V_{REF})/(2^{23} - 1)$. The positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 4 summarizes the ideal output codes for different input signals.

**Table 4. Ideal Output Code vs Input Signal**

| Input Signal $V_{IN}$ (AINP - AINN) | IDEAL OUTPUT CODE(1) |
|---|---|
| $\geq +V_{REF}$ | 7FFFFFh |
| $\frac{+V_{REF}}{2^{23} - 1}$ | 000001h |
| 0 | 000000h |
| $\frac{-V_{REF}}{2^{23} - 1}$ | FFFFFFh |
| $\leq -V_{REF}\left(\frac{2^{23}}{2^{23} - 1}\right)$ | 800000h |

(1) Excludes effects of noise, INL, offset, and gain errors.

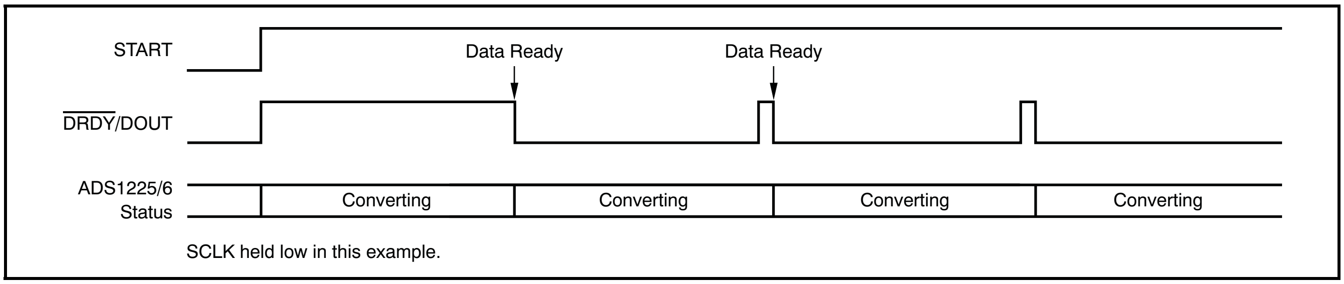



**Figure 27. Conversion with the START Pin Tied High**

## DATA RETRIEVAL

With the START pin high, the ADS1225 and ADS1226 continuously convert the analog input signal. To retrieve data, wait until DRDY/DOUT goes low, as illustrated in Figure 28 and Table 5. After this occurs, begin shifting out the data by applying SCLKs. Data is shifted out MSB first. It is not required to shift out all 24 bits of data, but the data must be retrieved before the new data is updated (see $t_2$) or else it will be overwritten.

Avoid data retrieval during the update period. DRDY/DOUT remain at the state of the last bit shifted out until it is taken high (see $t_6$), indicating that new data is being updated. To avoid having DRDY/DOUT remain in the state of the last bit, shift a 25th SCLK to force DRDY/DOUT high (refer to Figure 29). This technique is useful when a host controlling the ADS1225 and ADS1226 is polling DRDY/DOUT to determine when data is ready.

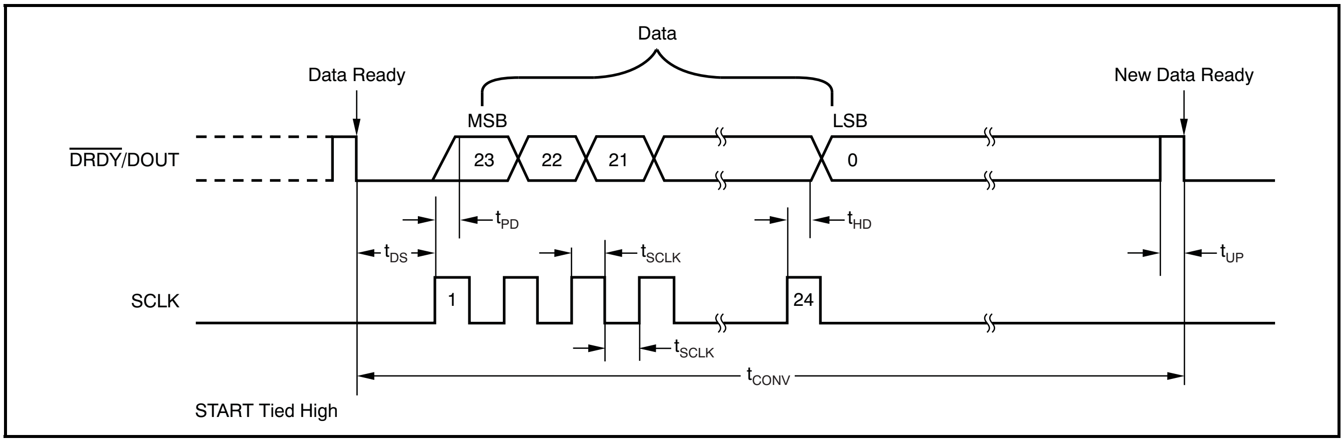



**Figure 28. Data Retrieval Timing**

**Table 5. Data Retrieval Times for Figure 28**

| SYMBOL | DESCRIPTION | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{DS}$ | DRDY/DOUT low to first SCLK rising edge | 0 | | ns |
| $t_{SCLK}$ | SCLK positive or negative pulse width | 100 | | ns |
| $t_{PD}$ | SCLK rising edge to new data bit valid: propagation delay | | 50 | ns |
| $t_{HD}$ | SCLK rising edge to old data bit valid: hold time | 0 | | ns |
| $t_{UP}$ | Data updating: no readback allowed | 29.5 | 49.2 | µs |
| $t_{CONV}$ | Conversion time (1/data rate), High-Speed mode | 8.0 | 13.3 | ms |
| | Conversion time (1/data rate), High-Resolution mode | 45.5 | 83.3 | ms |

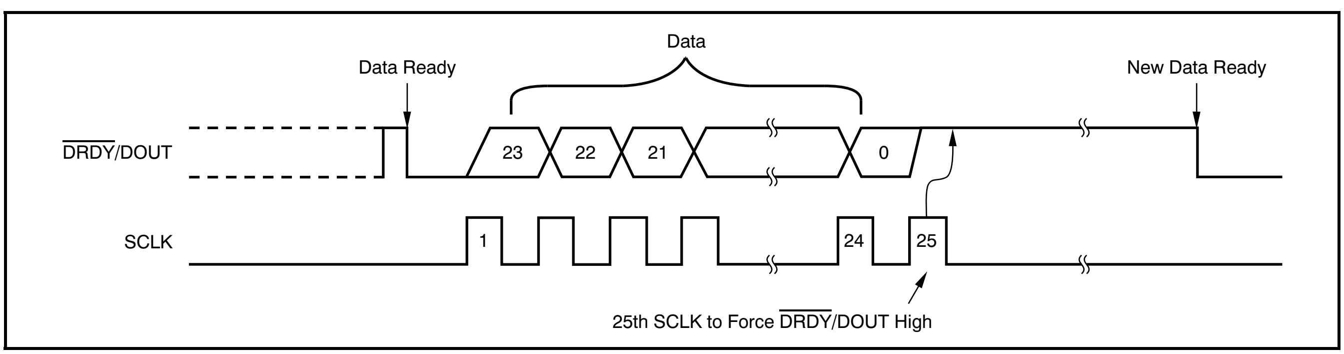



**Figure 29. Data Retrieval with DRDY/DOUT Forced High Afterwards**

## SELF-CALIBRATION

Self-calibration can be initiated at any time, although in many applications the ADS1225 and ADS1226 drift performance is so good that the self-calibration performed automatically at power-up is all that is needed. To initiate self-calibration, apply at least two additional SCLKs after retrieving 24 bits of data. Figure 30 and Table 6 illustrate the timing pattern. The 25th SCLK will send $\overline{DRDY}$/DOUT high. The falling edge of the 26th SCLK will begin the calibration cycle. Additional SCLK pulses may be sent after the 26th SCLK; however, activity on SCLK should be minimized during calibration for best results.

When the calibration is complete, $\overline{DRDY}$/DOUT goes low, indicating that new data is ready. There is no need to alter the analog input signal applied to the ADS1225 and ADS1226 during calibration; the input pins are disconnected within the A/D converter and the appropriate signals are applied internally and automatically. The first conversion after a calibration is fully settled and valid for use. The time required for a calibration depends on two independent signals: the falling edge of SCLK and an internal clock derived from CLK. Variations in the internal calibration values change the time required for calibration ($t_8$) within the range given by the min/max specs. $t_{11}$ and $t_{12}$ described in the next section are affected likewise.

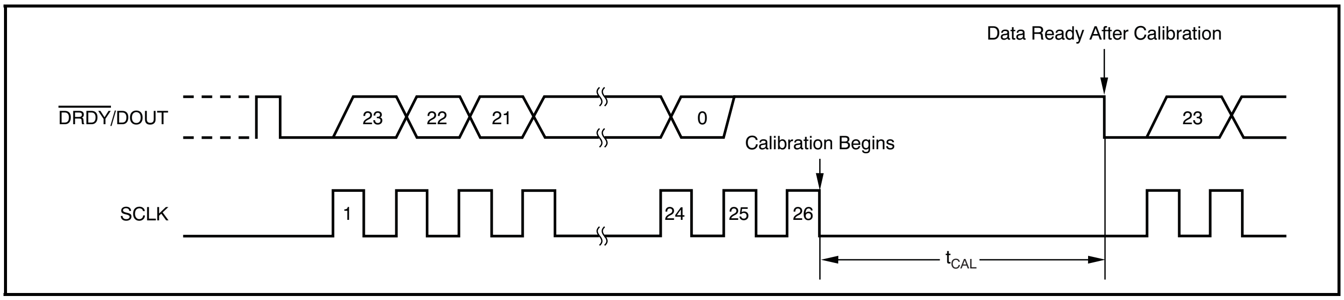



**Figure 30. Self-Calibration Timing**

**Table 6. Self-Calibration Time for Figure 30**

| SYMBOL | DESCRIPTION | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{CAL}$ | First data ready after calibration | 187 | 313 | ms |

## APPLICATION INFORMATION

### GENERAL RECOMMENDATIONS

The ADS1225 and ADS1226 are high-resolution A/D converters. Achieving optimal device performance requires careful attention to the support circuitry and printed circuit board (PCB) design. Figure 31 shows the basic connections for the ADS1225 and ADS1226. As with any precision circuit, be sure to use good supply bypassing capacitor techniques. A smaller value ceramic capacitor in parallel with a larger value tantalum capacitor works well. Place the capacitors, in particular the ceramic ones, close to the supply pins. Use a ground plane and tie the ADS1225 and ADS1226 GND pin and bypass capacitors directly to it. Avoid ringing on the digital inputs. Small resistors (≈100Ω) in series with the digital pins can help by controlling the trace impedance. Place these resistors at the source end.

Pay special attention to the reference and analog inputs. These inputs are critical to performance. Bypass the voltage reference using similar techniques to the supply voltages. The quality of the reference directly affects the overall accuracy of the device. Make sure to use a low noise and low drift reference such as the REF1004. Often, only a simple RC filter is needed on the inputs. The circuit limits the higher frequency noise. Avoid low-grade dielectrics for the capacitors and place them as close as possible to the input pins. Keep the traces to the input pins short, and carefully watch how they are routed on the PCB.

After the power supplies and reference voltage have stabilized, issue a self-calibration command to minimize offset and gain errors.

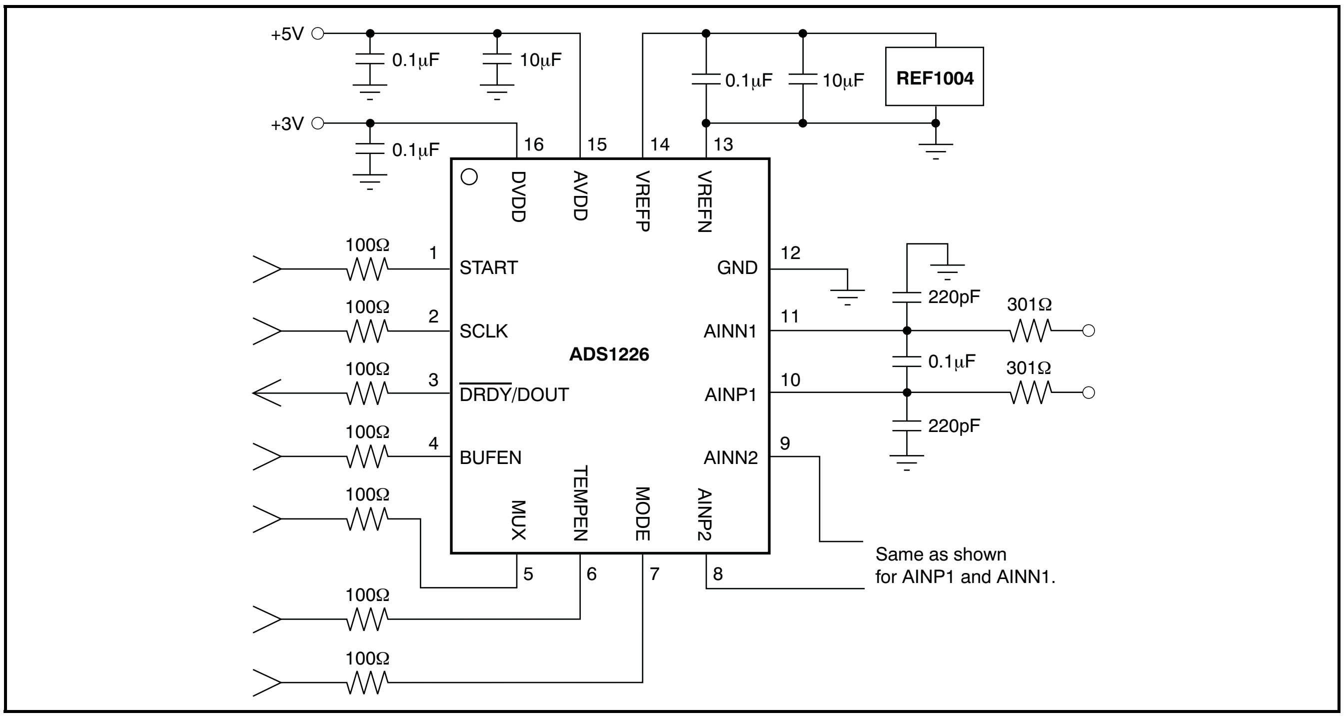



**Figure 31. Basic Connections**

## SMALL INPUT SIGNALS

Figure 32 shows the schematic of the ADS1225 for measuring small output signals such as the output of a bridge sensor or load cell. In this application, the load cell is combined with the ADS1225 and an MSP430 microcontroller. An OPA2333 is used to buffer the inputs and to provide the gain of the load cell signal. A 5V source is used as the reference and the excitation, although any clean source can create a proper ratiometric signal for the reference.

A typical load cell with a bridge sensitivity of 2mV/V using a 5V source would have a full-scale output of 10mV. The recommended gain of the OPA2333, for this load cell using low-drift resistors, would be $1 + 2R_F/R_G = 100.8V/V$. This value gives a full-scale measurement of approximately 1V while keeping the noise contribution of the OPA2333 low. The noise is low enough compared to full-scale to create a several-thousand count weigh scale, even in High-Speed mode. For better accuracy, this noise could be lowered through either additional filtering or using the High-Resolution mode.

It is important to make sure that the reference and inputs are clean from clocks or other periodic signals to prevent coupling. Isolate the analog from the digital supplies and grounds whenever possible.

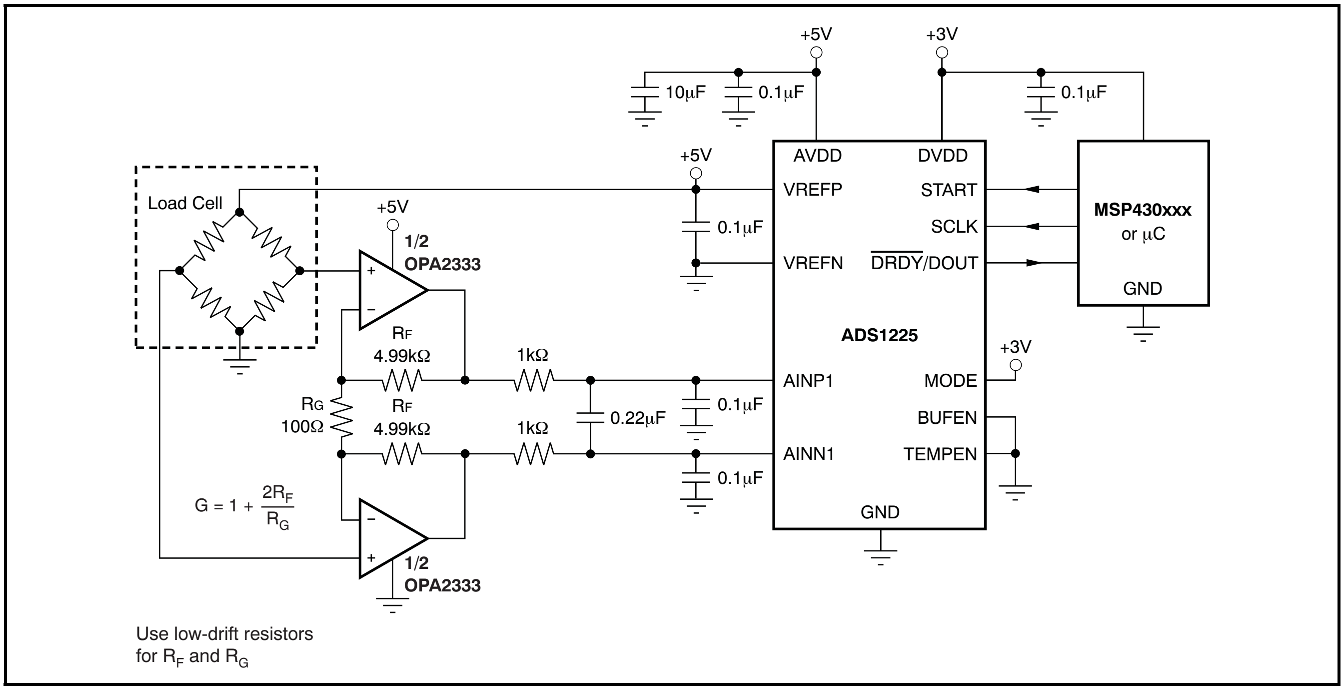



**Figure 32. Using the OPA2333 as a Gain Stage in Front of the ADS1225**

## LARGE INPUT SIGNALS

Many industrial applications require measurement of signals that go beyond 5V. The ADS1225 can be used to measure large input signals with the help of an INA159. The precision, level translation differential amplifier converts a ±10V input to a 5V input scale. This design allows systems to be run from a single 5V supply without the need for higher voltage supplies for signal conditioning.

Figure 33 shows a basic schematic. The negative input of the INA159 is grounded while the positive input is allowed to swing from –10V to +10V. Similarly, the negative input of the ADS1225 is grounded while the positive input swings from 0.5V to +4.5V given the useful $V_{OUT}$ swing of the INA159. The larger signal is easily measured without the need for extra ±10V supplies. See the INA159 data sheet for additional details.

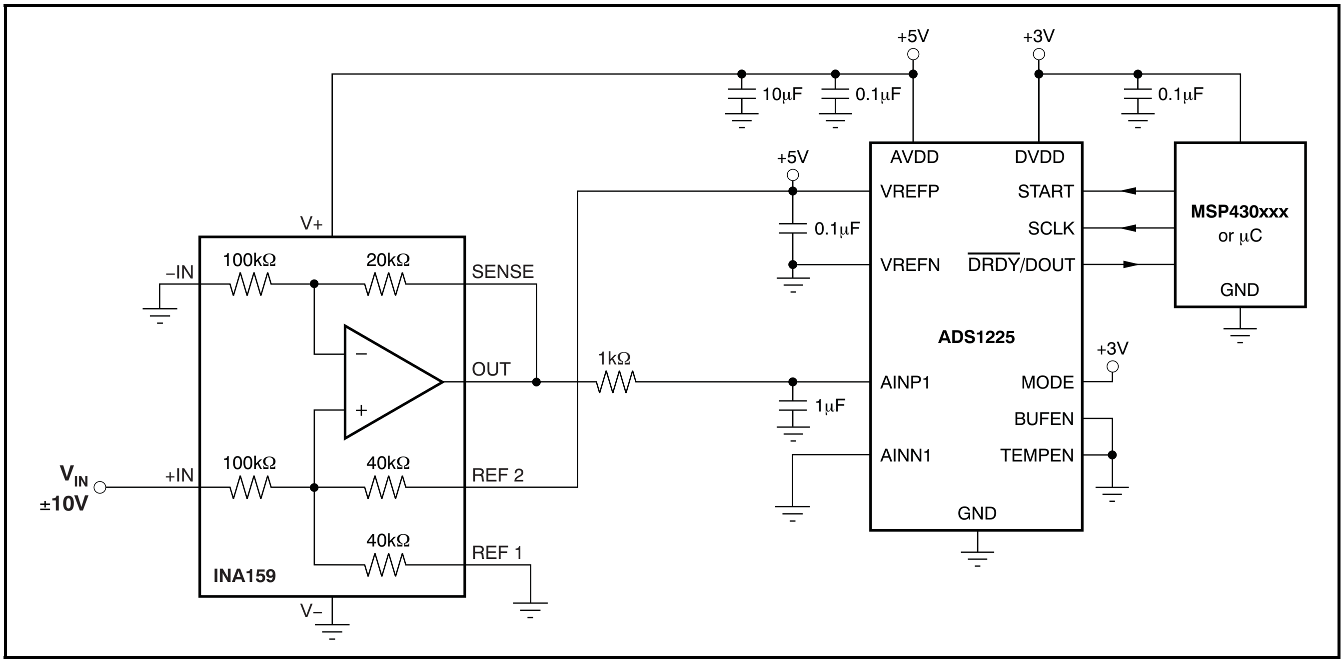



Figure 33. With the Help of an INA159, the ADS1225 Measures ±10V Signals

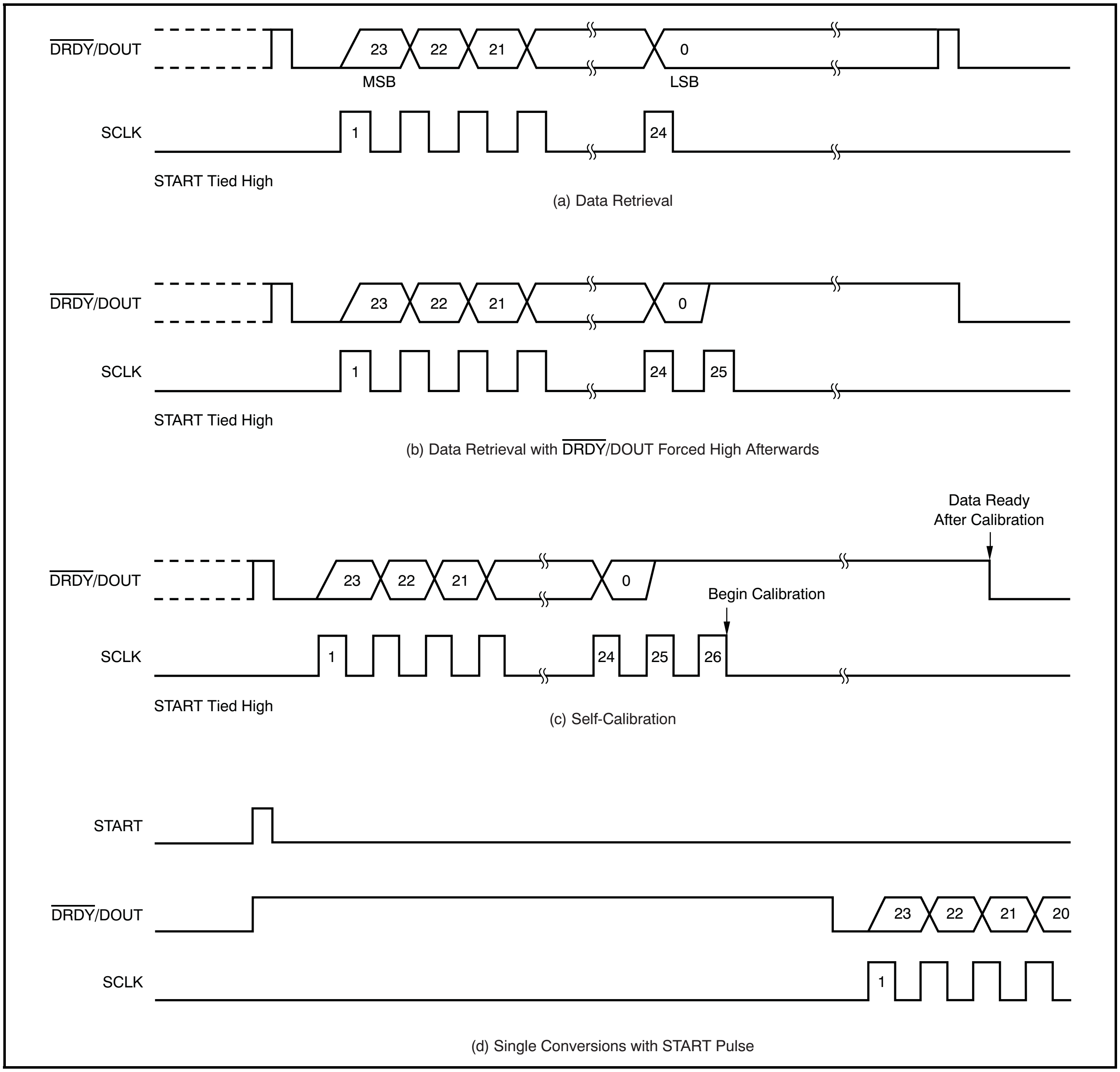



**Figure 34. Summary of Serial Interface Waveforms**

**Table 7. Digital Pin Operations**

| DIGITAL PIN | PIN NO. | INPUT | |
|---|---|---|---|
| | | **0** | **1** |
| START | 1 | Shutdown Mode | Start Conversion |
| BUFEN | 4 | Buffer Off | Buffer On |
| MUX (ADS1226 only) | 5 | AINP1 – AINN1 Input | AINP2 – AINN2 Input |
| TEMPEN | 6 | Temperature Sensor Off | Temperature Sensor On |
| MODE | 7 | High-Resolution Mode | High-Speed Mode |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| ADS1225IRGVR | ACTIVE | QFN | RGV | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1225IRGVRG4 | ACTIVE | QFN | RGV | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1225IRGVT | ACTIVE | QFN | RGV | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1225IRGVTG4 | ACTIVE | QFN | RGV | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1226IRGVR | ACTIVE | QFN | RGV | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1226IRGVRG4 | ACTIVE | QFN | RGV | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1226IRGVT | ACTIVE | QFN | RGV | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1226IRGVTG4 | ACTIVE | QFN | RGV | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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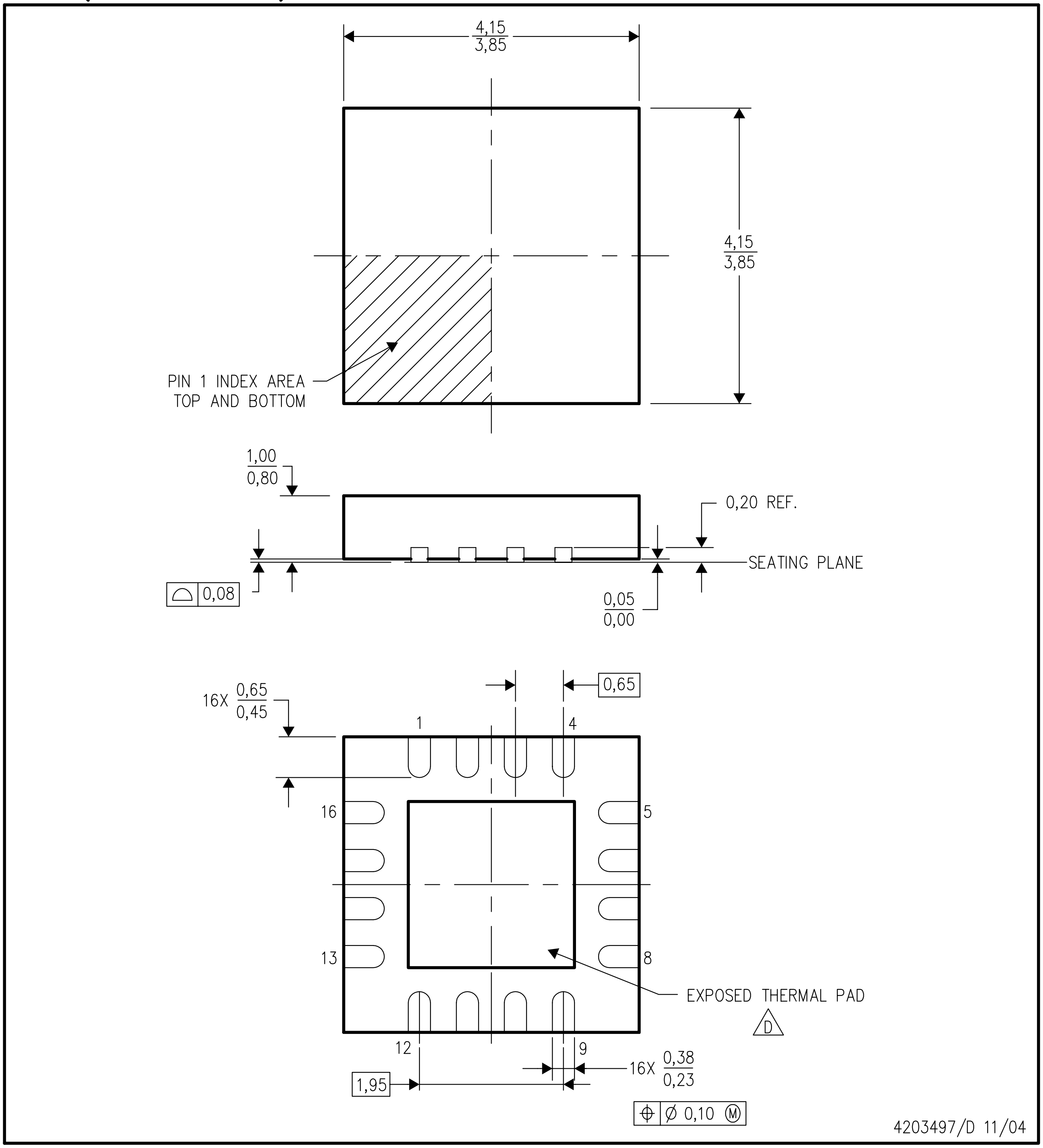
RGV (S-PQFP-N16) PLASTIC QUAD FLATPACK




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO-220.

# THERMAL PAD MECHANICAL DATA

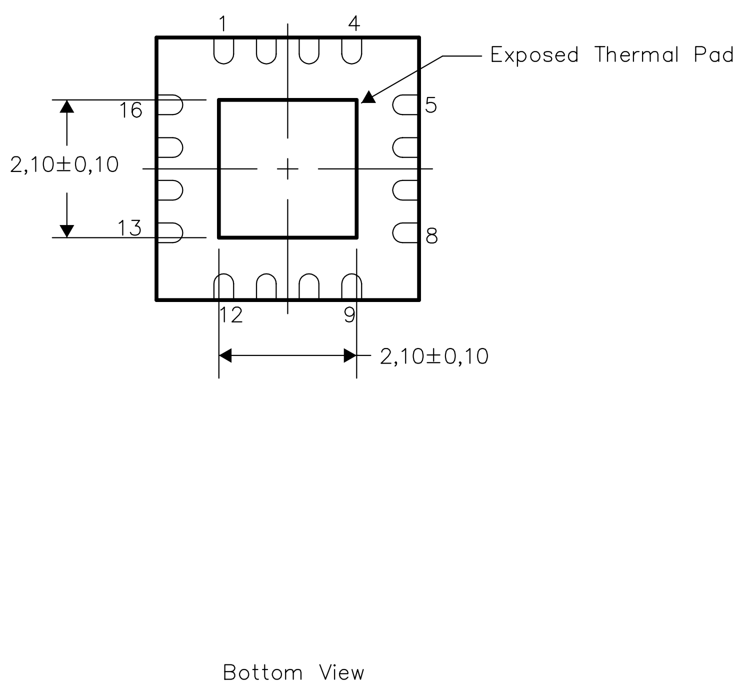
## RGV (S–PQFP–N16)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265