Buck or Boost, PWM Controller for Battery Test Solutions

Data Sheet **ADP1972**

FEATURES

- Input voltage range: 6 V to 60 V
- On-board 5 V low dropout regulator
- Selective buck or boost mode
- Excellent PWM linearity with high amplitude PWM sawtooth
  - 4.0 V p-p
- FAULT input compatible with AD8450
- COMP input compatible with AD8450
- Adjustable frequency from 50 kHz to 300 kHz
- Synchronization output or input with adjustable phase shift
- Programmable maximum duty cycle
- Maximum internal duty cycle: 98%
- Programmable soft start
- Peak hiccup current limit protection
- Input voltage UVLO protection
- TSD protection
- 16-lead TSSOP

APPLICATIONS

- PWM battery test systems with recycle capability including hybrid vehicles, PCs, and camera batteries
- Compatible with AD8450 constant voltage (CV) and constant current (CC) monitors

GENERAL DESCRIPTION

The ADP1972 is a constant frequency, voltage mode, pulse-width modulation (PWM) controller for buck or boost, dc-to-dc, asynchronous applications. The ADP1972 is designed for use in asynchronous battery testing applications with an external, high voltage field effect transistor (FET), half bridge driver, and an external control device, such as the AD8450. The asynchronous device operates as a buck converter in battery charge mode and operates as a boost converter in recycle mode to recycle energy to the input bus.

The ADP1972 high voltage, VIN supply pin can withstand a maximum operating voltage of 60 V and reduces the need for additional system supply voltages. The ADP1972 has integrated features such as precision enable, pin selective buck or boost mode operation, internal and external synchronization control with programmable phase shift, programmable maximum duty cycle, and programmable peak hiccup current limit. Additional protection features include soft start to limit input inrush current during startup, input voltage undervoltage lockout (UVLO), and thermal shutdown (TSD). The ADP1972 also has a COMP pin to provide external control of the PWM operation and a FAULT pin that can be signaled to disable the DH and DL outputs if a fault condition occurs externally to the ADP1972.

The ADP1972 is available in a 16-lead TSSOP package.

TYPICAL APPLICATION CIRCUIT

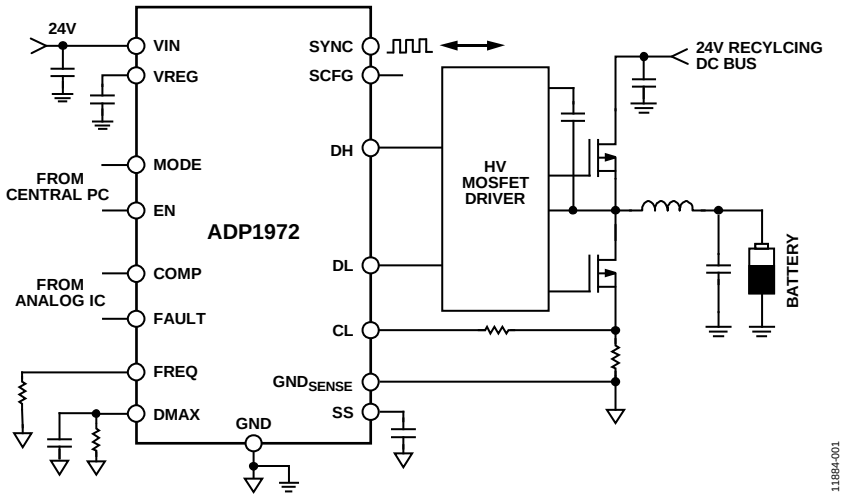

Figure 1.

Rev. B

Document Feedback

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6/14—Rev. 0 to Rev. A

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1/14—Revision 0: Initial Version

SPECIFICATIONS

VIN = 24 V and the specifications are valid for T_J = −40°C to +125°C, unless otherwise specified. Typical values are at T_A = 25°C. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE (VIN)						
Voltage Range	V_{IN}		6		60	V
VIN Supply Current	I_{VIN}	R_{FREQ} = 100 kΩ, V_{SS} = 0 V, SYNC floating		1.5	2.5	mA
VIN Shutdown Current	I_{SHDN}	V_{EN} = 0 V		15	70	µA
UVLO Threshold Rising		V_{IN} rising		5.71	6	V
UVLO Threshold Falling		V_{IN} falling	5.1	5.34		V
SOFT START (SS)						
SS Pin Current	I_{SS}	V_{SS} = 0 V	4	5	6	µA
SS Threshold Rising				0.52	0.65	V
SS Threshold Falling			0.4	0.5		V
PWM CONTROL						
FREQ						
Frequency Range	f_{SET}		50		300	kHz
Oscillator Frequency	f_{OSC}	R_{FREQ} = 100 kΩ	90	100	110	kHz
FREQ Pin Voltage	V_{FREQ}	R_{FREQ} = 100 kΩ	1.2	1.252	1.3	V
SYNC						
Maximum SYNC Pin Voltage					5.5	V
SYNC Pull-Down Resistor			0.5	1	1.5	MΩ
SYNC Output (Internal Frequency Control)		V_{SCFG} ≥ 4.53 V or SCFG pin floating				
Internal SYNC Range	f_{SET}	For SYNC output	50		300	kHz
SYNC Output Clock Duty Cycle		V_{SCFG} = V_{VREG}, R_{FREQ} = 100 kΩ	40	50	60	%
SYNC Sink Resistance	R_{SYNC}	V_{SCFG} = 5 V, I_{SYNC} = 10 mA		10	20	Ω
SYNC Input (External Frequency Control)		V_{SCFG} < 4.25 V				
External SYNC Range	f_{SYNC}	For SYNC input clock	50		300	kHz
SYNC Threshold Rising				1.2	1.5	V
SYNC Threshold Falling			0.7	1.05		V
R_{FREQ} Slave to Master Ratio for Synchronization		For example, $R_{FREQ\ (SLAVE)}$ = 1.11 × $R_{FREQ\ (MASTER)}$		1.11		
SCFG	V_{SCFG}					
SCFG High Threshold Rising				4.53	4.7	V
SCFG High Threshold Falling			4.25	4.51		V
SCFG Low Threshold Rising				0.52	0.65	V
SCFG Low Threshold Falling			0.4	0.5		V
SCFG Current	I_{ISCFG}	R_{FREQ} = 100 kΩ	9.5	11	12.5	µA
DMAX						
Maximum Internal Duty Cycle		V_{COMP}, V_{DMAX}, V_{SS}, and V_{SCFG} = 5 V		97.37		%
DMAX Setting Current	I_{DMAX}	V_{DMAX} = 0 V, R_{FREQ} = 100 kΩ	9.5	11	12.5	µA
DMAX and SCFG Current Matching[1]					10	%
COMP						
Maximum COMP Pin Voltage	V_{COMP}				5	V
Internal Peak-to-Peak Ramp Voltage	V p-p			4		V
COMP Maximum Internal Ramp Voltage				4.5		V
COMP Minimum Internal Ramp Voltage		Internal oscillator is disabled	0.45	0.5	0.55	V
DH and DL Shutdown Range[2]	V_{COMP}	COMP not regulated			0.45	V
Maximum Duty Cycle Range[2]	V_{COMP}			4.4		V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
PRECISION ENABLE LOGIC (EN)						
Maximum EN Pin Voltage					60	V
EN Threshold Rising				1.25	1.4	V
EN Threshold Falling			1.1	1.22		V
EN Pin Current		V_{EN} = 5 V		0.32	2	µA
MODE LOGIC						
Maximum MODE Pin Voltage					5.5	V
MODE Threshold Rising				1.20	1.5	V
MODE Threshold Falling			0.7	1.05		V
CURRENT LIMIT (CL)						
Set Current	I_{CL}	V_{CL} = 0 V	18	20	21	µA
Buck Internal Reference	$V_{REF (BUCK)}$		250	300	350	mV
Boost Internal Reference	$V_{REF (BOOST)}$		450	500	550	mV
Hiccup Detect Time		R_{FREQ} = 100 kΩ	4.4	5.2	6.1	ms
Hiccup Off-Time		R_{FREQ} = 100 kΩ	4.4	5.2	6.1	ms
VREG						
LDO Regulator Output Voltage	V_{VREG}	V_{IN} = 6 V to 60 V	4.9	5	5.1	V
Guaranteed Output Current	$I_{OUT (MAX)}$	V_{IN} = 6 V			5	mA
Line Regulation		V_{IN} = 6 V to 60 V		5	5.1	V
Load Regulation		V_{IN} = 6 V, I_{OUT} = 0 mA to 5 mA		5	5.1	V
FAULT						
Maximum FAULT Pin Voltage					60	V
FAULT Threshold Rising				1.2	1.5	V
FAULT Threshold Falling			0.7	1.05		V
FAULT Pin Current		V_{FAULT} = 5 V		0.49	2	µA
PWM DRIVE LOGIC SIGNALS (DH/DL)						
DL Drive Voltage	V_{DL}	No load		VREG		V
DH Drive Voltage	V_{DH}	No load		VREG		V
DL and DH Sink Resistance		I_{DL} = 10 mA		1.2	2.4	Ω
DL and DH Source Resistance		I_{DL} = 10 mA		1.4	2.6	Ω
DL and DH Pull-Down Resistor			0.5	1	1.5	MΩ
THERMAL SHUTDOWN (TSD)						
TSD Threshold Rising				150		°C
TSD Threshold Falling				135		°C

[1] The DMAX and SCFG current matching specification is calculated by taking the absolute value of the difference between the measured I_{SCFG} and I_{DMAX} currents, dividing them by the 11 µA typical value, and multiplying this answer by 100.

$$DMAX\ and\ SCFG\ Current\ Matching\,(\%) = \left[\frac{I_{SCFG} - I_{DMAX}}{11\,\mu A}\right] \times 100$$

[2] See Figure 11 for a graph of the duty cycle vs. the applied COMP pin voltage.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, EN, FAULT to GND	−0.3 V to +61 V
SYNC, COMP, MODE to GND	−0.3 V to +5.5 V
DH, DL, SS, DMAX, SCFG, CL to GND	−0.3 V to VREG + 0.3 V
GND_{SENSE} to GND	−0.3 V to +0.3 V
Operating Ambient Temperature Range	−40°C to +85°C
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Absolute maximum ratings apply individually only, not in combination.

THERMAL OPERATING RANGES

The ADP1972 can be damaged when the junction temperature limits are exceeded. The maximum operating junction temperature ($T_{J\ MAX}$) takes precedence over the maximum operating ambient temperature ($T_{A\ MAX}$). Monitoring ambient temperature does not guarantee that the junction temperature (T_J) is within the specified temperature limits.

In applications with high power dissipation and poor printed circuit board (PCB) thermal resistance, the maximum ambient temperature may need to be derated. In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit when the junction temperature is within specification limits.

The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction to ambient thermal resistance of the package (θ_{JA}). Use the following equation to calculate the maximum junction temperature (T_J) from the ambient temperature (T_A) and power dissipation (P_D):

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

For additional information on thermal resistance, refer to Application Note AN-000, *Thermal Characteristics of IC Assembly*.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

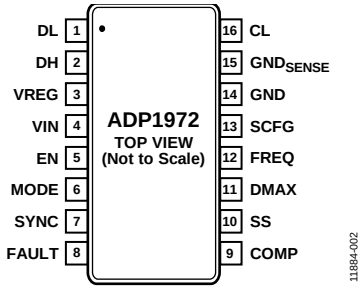

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DL	Logic Drive Low Output for External Low-Side MOSFET Driver.
2	DH	Logic Drive High Output for External High-Side MOSFET Driver.
3	VREG	Internal Low Dropout (LDO) Voltage Regulator Output and Internal Bias Supply. A bypass capacitance of 1 µF or greater from this pin to ground is required.
4	VIN	High Input Voltage Supply Pin. Bypass this pin with a 4.7 µF capacitor to ground.
5	EN	Logic Enable Input. Drive EN logic low to shut down the device. Drive EN logic high to turn on the device.
6	MODE	Mode Select. Drive MODE logic low to place the device in boost/recycle mode. Drive MODE logic high to place the device in buck/charge mode of operation.
7	SYNC	Synchronization Pin. This pin is used as an input and synchronized to an external clock or used as an output clock to synchronize with other channels.
8	FAULT	Fault Input Pin. Signaled by an overcurrent protection (OCP) or overvoltage protection (OVP) fault condition on the companion ASIC, AD8450. The ADP1972 is disabled until this pin is logic high.
9	COMP	Output Error Amplifier Signal from the companion ASIC, AD8450. This pin is the error input to the ADP1972 and is compared internally to the linear ramp to produce the PWM signal. Do not leave this pin floating.
10	SS	Soft Start Control Pin. A capacitor connected from SS to ground brings the output up slowly during power-up and reduces the inrush current.
11	DMAX	Maximum Duty Cycle Input. Connect an external resistor to ground to set the maximum duty cycle. If the 98% internal maximum duty cycle is sufficient for the application, tie this pin to VREG. If DMAX is left floating, this pin is internally tied to VREG.
12	FREQ	Frequency Set Pin. Connect an external resistor between this pin and ground to set the frequency between 50 kHz and 300 kHz.
13	SCFG	Synchronization Configuration Input. Drive $V_{SCFG} \geq 4.53$ V to configure SYNC as an output clock signal. Drive $V_{SCFG} < 4.25$ V to configure SYNC as an input. Connect a resistor to ground with $0.65 \text{ V} < V_{SCFG} < 4.25$ V to introduce a phase shift to the synchronized clock. Drive $V_{SCFG} \leq 0.5$ V to configure SYNC as an input with no phase shift so that it synchronizes the device to an external clock source. If SCFG is left floating, the SYNC pin is internally tied to VREG, and SYNC is configured as an output.
14	GND	Power and Analog Ground Pin.
15	GND_{SENSE}	Ground Sense for the Current-Limit Setting Resistor.
16	CL	Current-Limit Programming Pin. Connect a current-limit sense resistor in series with the FET source to set the peak current limit.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{VIN} = V_{EN} = V_{FAULT} = 24$ V, $V_{MODE} = V_{CL} = V_{SS} = V_{COMP} = 0$ V, $T_A = 25°C$, unless otherwise noted.

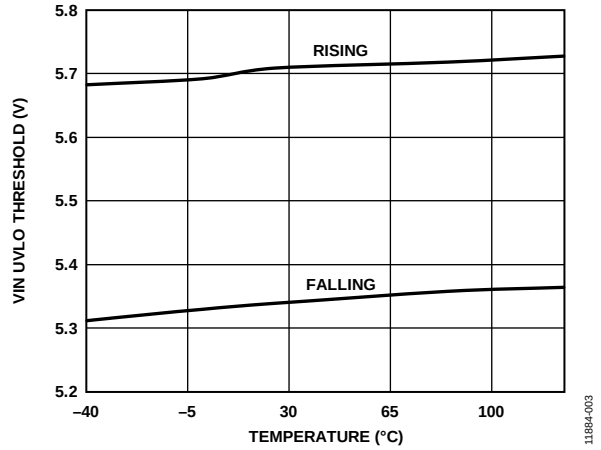

Figure 3. Input Voltage UVLO Threshold vs. Temperature, $V_{FAULT} = 0$ V

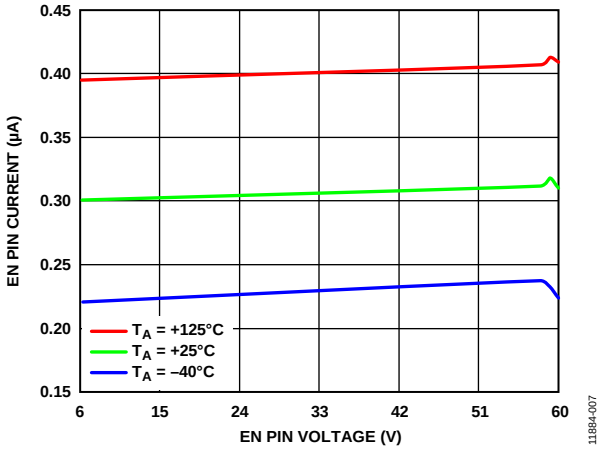

Figure 6. EN Pin Current vs. EN Pin Voltage, $V_{EN} = 5$ V and $V_{FAULT} = 0$ V

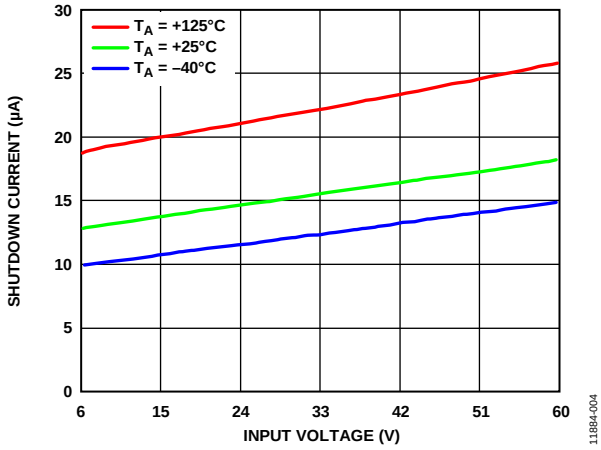

Figure 4. Shutdown Current vs. Input Voltage, $V_{EN} = 0$ V and $V_{FAULT} = 0$ V

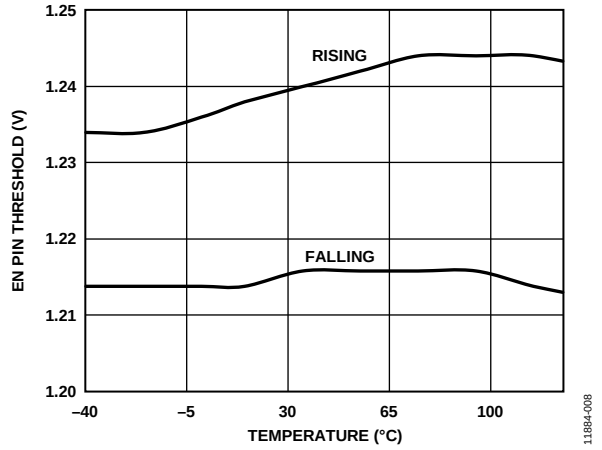

Figure 7. EN Pin Threshold vs. Temperature, $V_{FAULT} = 0$ V

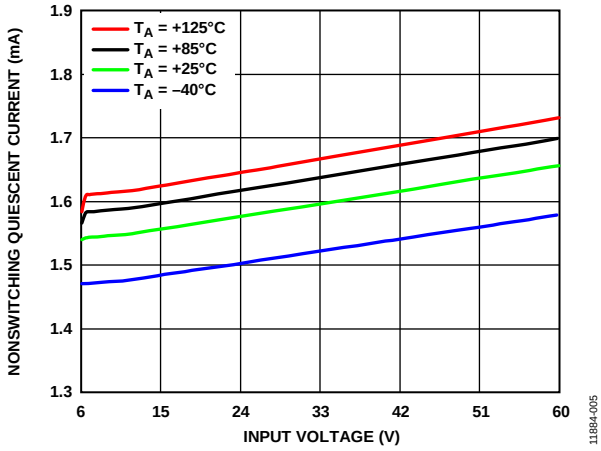

Figure 5. Nonswitching Quiescent Current vs. Input Voltage (SYNC = Floating)

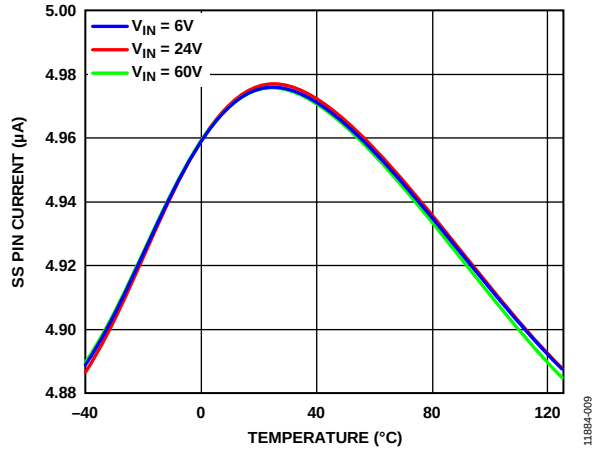

Figure 8. SS Pin Current vs. Temperature

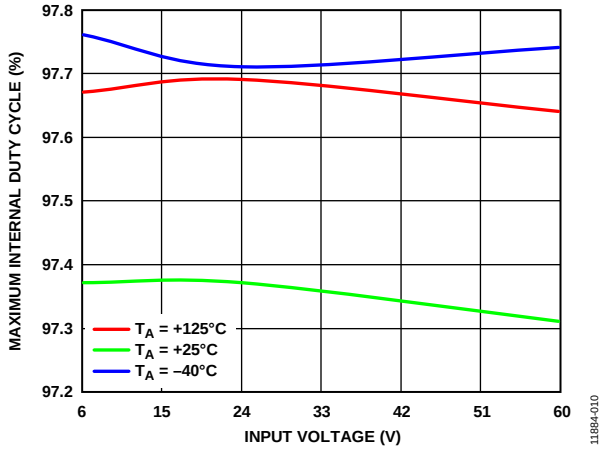

Figure 9. Maximum Internal Duty Cycle vs. Input Voltage, R_{FREQ} = 100 kΩ, V_{COMP} = 5 V, and No Load on DL, DH, or DMAX

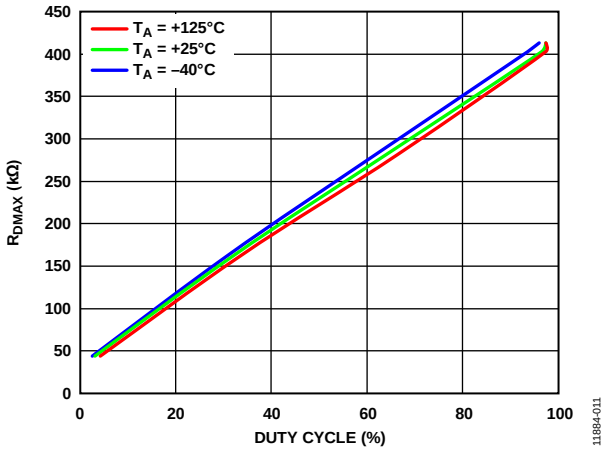

Figure 10. R_{DMAX} vs. Duty Cycle, R_{FREQ} = 100 kΩ, V_{COMP} = 5 V, and No Load on DL or DH

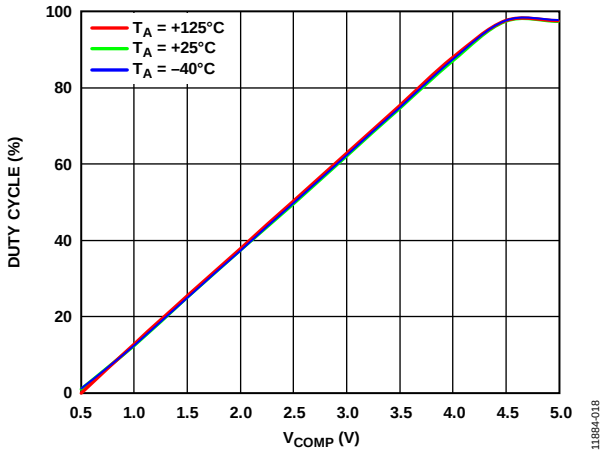

Figure 11. Duty Cycle vs. V_{COMP}, R_{FREQ} = 100 kΩ, and No Load on DL, DH, or DMAX

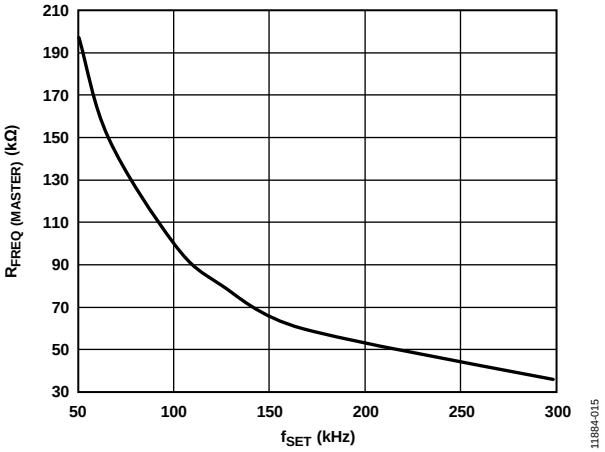

Figure 12. $R_{FREQ\ (MASTER)}$ vs. Switching Frequency (f_{SET})

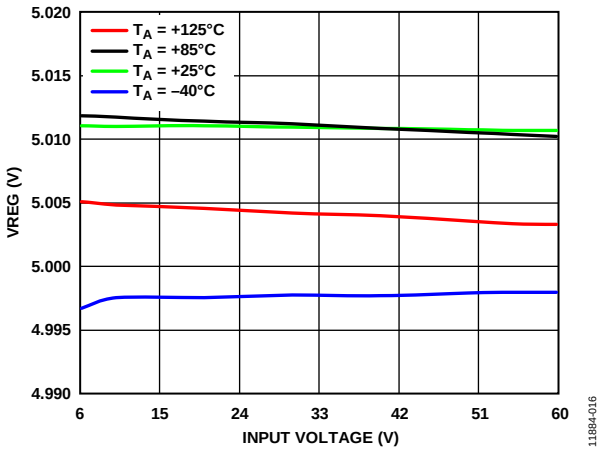

Figure 13. VREG vs. Input Voltage, No Load

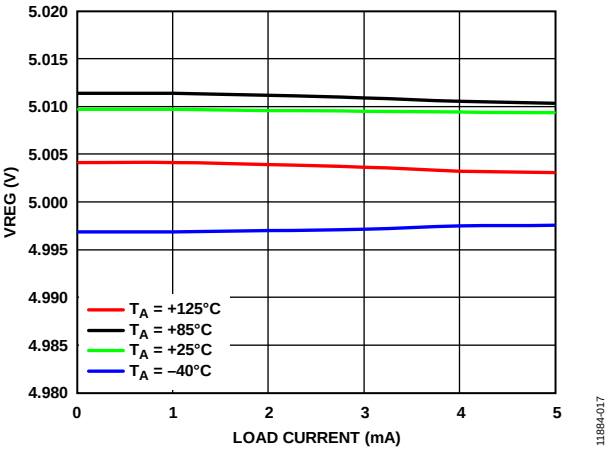

Figure 14. VREG vs. Load Current

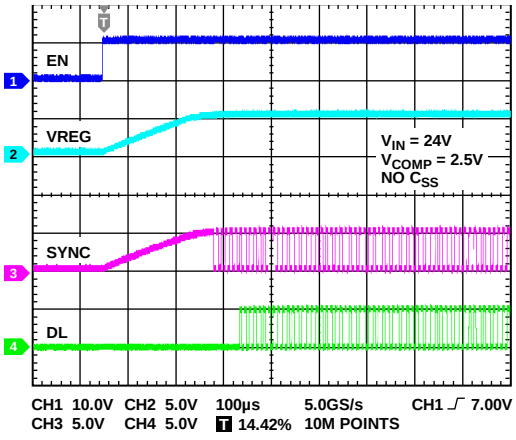

Figure 15. Startup

THEORY OF OPERATION

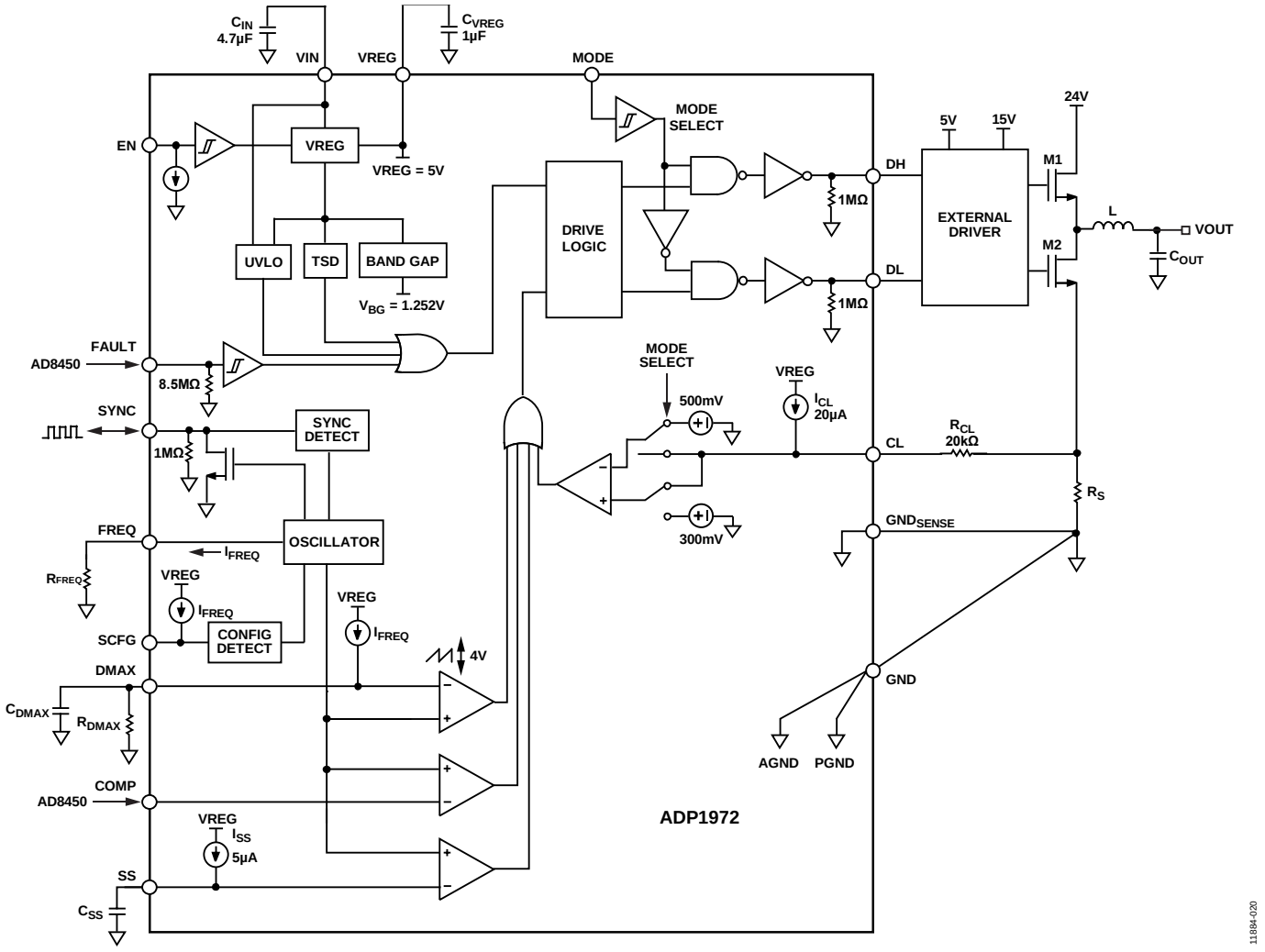

Figure 16. Block Diagram

The ADP1972 is a constant frequency, voltage mode, PWM controller for buck or boost, dc-to-dc, asynchronous applications with an external, high voltage FET, half bridge driver, and an external error signal generating device, such as the AD8450. The ADP1972 has a high input voltage range, multiple externally programmed control pins, and integrated safety features.

SUPPLY PINS

The ADP1972 has two voltage supply pins, VIN and VREG. The VIN pin operates from an external supply that ranges from 6 V to 60 V and is the supply voltage for the internal LDO regulator of the ADP1972. Bypass the VIN pin to ground with a 4.7 µF or greater ceramic capacitor.

The VREG pin is the output of the internal LDO regulator. The internal LDO regulator generates the 5 V (typical) rail that is used internally to bias the control circuitry and can be used externally as a pull-up voltage for the MODE, SYNC, DMAX, and FAULT pins. Bypass the VREG pin to ground with a 1 µF ceramic capacitor.

When operating with an input voltage above 50 V, additional input filtering is necessary. Figure 17 shows the recommended filter configuration.

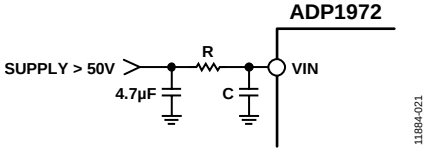

Figure 17. Recommended Filter Configuration for Input Voltages Greater than 50 V

EN/SHUTDOWN

The EN input turns the ADP1972 on or off. The EN pin of the ADP1972 can operate from voltages up to 60 V and is designed with stable ±20% thresholds for precision enable control. When the EN voltage is less than 1.22 V (typical), the ADP1972 shuts down, driving both DL and DH low. When the ADP1972 is shut down, the VIN supply current is 15 µA (typical). When the EN voltage is greater than 1.25 V (typical), the ADP1972 is enabled.

The device can be disabled via the EN pin, a fault condition indicated by a TSD event, a UVLO condition, or an external fault condition signaled via the FAULT pin.

UNDERVOLTAGE LOCKOUT (UVLO)

There is internal UVLO for the VIN pin. When VIN rises, the UVLO does not allow the ADP1972 to turn on unless VIN is greater than 5.71 V (typical). When VIN falls, the UVLO disables the device when VIN drops below 5.34 V (typical). The UVLO prevents potentially erratic operation of the application at low input voltages that may damage the ADP1972 and the external circuitry. The UVLO levels have ~370 mV of hysteresis to ensure glitch free startup.

SOFT START

The ADP1972 is equipped with a programmable soft start that prevents output voltage overshoot during startup. When the ADP1972 is enabled with the EN pin, the VREG voltage begins rising to 5 V. When VREG reaches 90% of its 5 V (typical) value, the 5 µA (typical) internal soft start current (I_{SS}) begins charging the soft start capacitor (C_{SS}), causing the voltage on the SS pin (V_{SS}) to rise. While V_{SS} is less than 0.52 V (typical), the ADP1972 switching control remains disabled.

When V_{SS} reaches 0.52 V (typical), switching is enabled, and regulation of the ADP1972 control loop begins. As C_{SS} continues to charge and V_{SS} rises, the PWM duty cycle gradually increases, allowing the output voltage to rise linearly with little to no overshoot during startup. C_{SS} charges and V_{SS} rises until V_{SS} reaches the internal VREG voltage (5 V typical). When the internal system duty cycle is less than the soft start duty cycle, the internal control loop takes control of the ADP1972. See Figure 18 for a soft start diagram.

There is an active, internal, pull-down resistor on the SS pin that discharges C_{SS} when the device shuts down to prevent a fault from occurring.

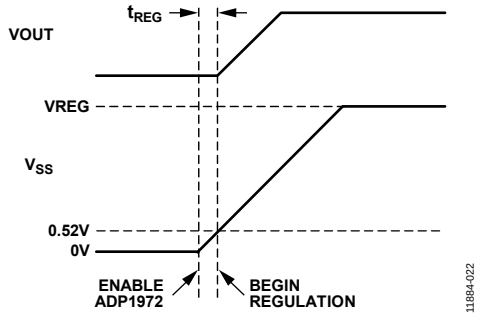

Figure 18. Soft Start Diagram

OPERATING MODES

The ADP1972 can be programmed to operate as an asynchronous boost or as an asynchronous buck. If the MODE pin is driven low by less than 1.05 V (typical), then the ADP1972 operates in a boost configuration. A boost configuration is ideal for power recycling and discharging in battery charging applications. When the MODE pin is driven high by greater than 1.20 V (typical), the ADP1972 operates in a buck configuration for battery charging. See Figure 19 and Figure 20 for the ADP1972 behavior in each mode. When the ADP1972 is enabled, the internal LDO regulator connected to the VREG pin also powers up. On the rising edge of VREG, the state of the MODE pin is latched, preventing the mode of operation from being changed while the device is enabled. To change between boost and buck modes of operation, shutdown or disable the ADP1972, adjust the MODE pin to change the operating mode, and restart the system.

The operating mode can be changed when the EN pin is driven low, the FAULT pin is driven low, or the ADP1972 is disabled via a TSD event or UVLO condition. On the rising edge of the FAULT control signal, the state of the MODE pin is latched, preventing the mode of operation from being changed while the device is enabled.

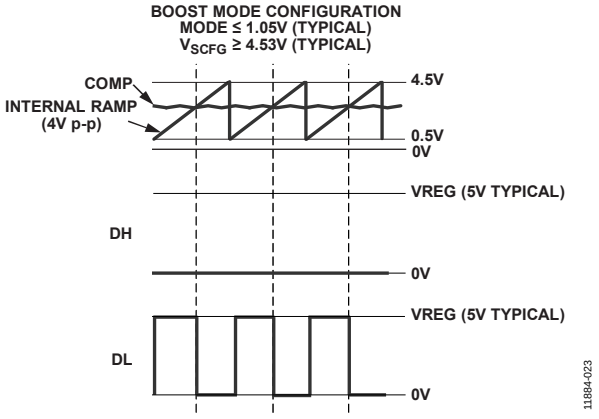

Figure 19. Signal Diagram for Boost Configuration

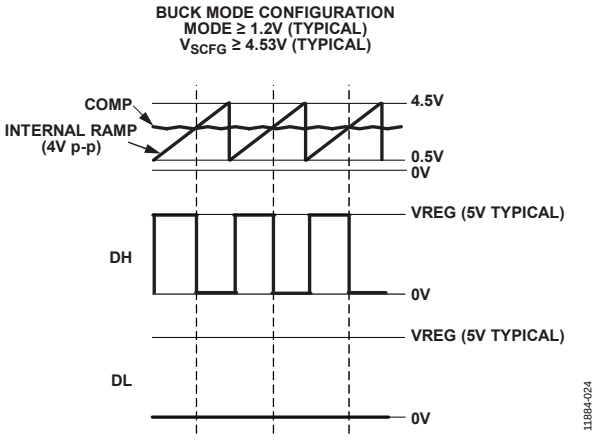

Figure 20. Signal Diagram for Buck Configuration

PWM DRIVE SIGNALS

The ADP1972 has two output drive signals, DH and DL, that are compatible with drivers similar to the IR2110S.

The drive signal DL is active when the MODE pin is logic low and the ADP1972 is configured in the boost/recycle mode. The DL drive signal turns on and off the low-side switch driven from the external driver. While in the boost/recycle mode, the DH signal is driven low to prevent the high-side switch from turning on and only allows the body diode to conduct.

The drive signal DH is active when the MODE pin is logic high and the ADP1972 is configured in the buck/charge mode. The DH drive signal turns on and off the high-side switch driven from the external driver. While in the buck/charge mode, the DL signal is driven low to prevent the low-side switch from turning on, and it only allows the body diode to conduct.

When driving capacitive loads with the DH and DL pins, a 20 Ω resistor must be placed in series with the capacitive load to reduce ground noise and ensure signal integrity.

EXTERNAL COMP CONTROL

The ADP1972 COMP pin is the input to the error amplifier that controls the PWM output on the DH pin or DL pin. The ADP1972 uses voltage mode control that compares an error signal, applied to the COMP pin by an external device, such as the AD8450, to an internal 4 V p-p triangle waveform. As the load changes, the error signal increases or decreases. The internal PWM comparator determines the appropriate duty cycle drive signal by monitoring the error signal at the COMP pin and the internal 4 V p-p ramp signal. The internal PWM comparator subsequently drives the external gate driver at the determined duty cycle through the DH and DL drive control pins.

The functional voltage range of the COMP pin is from 0 V to 5.0 V. If V_{COMP} is less than 0.5 V (typical), the DH and DL outputs are disabled. If V_{COMP} is between 0.5 V and 4.5 V, the ADP1972 regulates the DH and DL outputs accordingly. If V_{COMP} is greater than 4.5 V, the ADP1972 operates the DH and DL outputs at the maximum programmed duty cycle (98% default). The input to the COMP pin must never exceed the 5.5 V absolute maximum rating.

The DL and DH signals swing from VREG (5 V typical) to ground. The external FET driver used must have input control pins compatible with a 5 V logic signal.

CURRENT LIMIT

The ADP1972 features a peak hiccup current limit implementation. When the peak inductor current exceeds the programmed current limit for more than 500 consecutive clock cycles, 5.2 ms (typical) for a 100 kHz programmed frequency, the peak hiccup current limit condition occurs. PWM regulation of the output voltage then disables for 500 clock cycles, which is enough time for the output to discharge, and the average power dissipation to reduce. When the 500 clock cycles have expired, the ADP1972 restarts. When the SS pin exceeds 0.52 V (typical), the ADP1972 resumes PWM regulation.

Figure 21 shows the current limit block diagram for peak current limit protection.

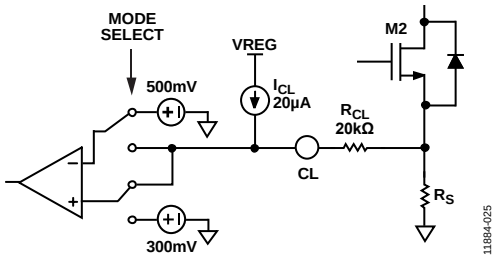

Figure 21. Current Limit Block Diagram

PWM FREQUENCY CONTROL

The FREQ, SYNC, and SCFG pins are all used to determine the source, frequency, and synchronization of the clock signal that operates the PWM control of the ADP1972.

Internal Frequency Control

The ADP1972 frequency can be programmed with an external resistor connected between FREQ and ground. The range of frequency can be set from a minimum of 50 kHz to a maximum of 300 kHz. If the SCFG pin is tied to VREG, forcing $V_{SCFG} \geq 4.53$ V, or if the SCFG pin is left floating, the SYNC pin is configured as an output, and the ADP1972 operates at the frequency set by R_{FREQ}, which outputs from the SYNC pin through the open drain device. The output clock of the SYNC pin operates with a 50% (typical) duty cycle. In this configuration, the SYNC pin can be used to synchronize other switching regulators in the system to the ADP1972. When the SYNC pin is configured as an output, an external pull-up resistor is needed from the SYNC pin to an external supply. The VREG pin of the ADP1972 is used as the external supply rail for the pull-up resistor.

External Frequency Control

When $V_{SCFG} \leq 0.5$ V, the SYNC pin is configured as an input, and the ADP1972 synchronizes to the external clock applied to the SYNC pin and operates as a slave device. This synchronization allows the ADP1972 to operate at the same switching frequency with the same phase as other switching regulators or devices in the system. When operating the ADP1972 with an external clock, select R_{FREQ} to provide a frequency that approximates but is not equal to the external clock frequency, which is further explained in the Applications Information section.

Operating Frequency Phase Shift

When the voltage applied to the SCFG pin is $0.65 \text{ V} < V_{SCFG} < 4.25$ V, the SYNC pin is configured as an input, and the ADP1972 synchronizes to a phase shifted version of the external clock applied to the SYNC pin. To adjust the phase shift, place a resistor (R_{SCFG}) from SCFG to ground. The phase shift reduces the input supply ripple for systems containing multiple switching power supplies.

MAXIMUM DUTY CYCLE

The maximum duty cycle of the ADP1972 can be externally programmed to any value between 0% and 98% via an external resistor on the DMAX pin connected from DMAX to ground. The maximum duty cycle defaults to 98% if DMAX is left floating, is tied to VREG, or is programmed to a value greater than 98%.

EXTERNAL FAULT SIGNALING

The ADP1972 is equipped with a FAULT pin that signals the ADP1972 when an external fault condition occurs. The external fault signal stops PWM operation of the system to avoid damage to the application and components. When a voltage less than 1.05 V (typical) is applied to the FAULT pin, the ADP1972 disables. In this state, the DL and DH PWM drive signals are both driven low to prevent switching of the system dc-to-dc converter, and the soft start is reset. When a voltage greater than 1.20 V (typical) is applied to the FAULT pin, the ADP1972 begins switching. A voltage ranging from 0 V to 60 V can be applied to the FAULT pin of the ADP1972.

THERMAL SHUTDOWN (TSD)

The ADP1972 has a TSD protection circuit. The thermal shutdown triggers and disables switching when the junction temperature of the ADP1972 reaches 150°C (typical). While in TSD, the DL and DH signals are driven low and the C_{SS} capacitor discharges to ground. VREG remains high. When the junction temperature decreases to 135°C (typical), the ADP1972 restarts the application control loop.

APPLICATIONS INFORMATION

The ADP1972 has many programmable features that are optimized and controlled for a given application. The ADP1972 provides pins for selecting the operating mode, controlling the current limit, selecting an internal or external clock, setting the operating frequency, phase shifting the operating frequency, programming the maximum duty cycle, and adjusting the soft start.

BUCK OR BOOST SELECTION

To operate the ADP1972 in boost/recycle mode, apply a voltage less than 1.05 V (typical) to the MODE pin. To operate the ADP1972 in buck/discharge mode, drive the MODE pin high, greater than 1.2 V (typical). The state of the MODE pin can only be changed when the ADP1972 is shutdown via the EN pin, or disabled via an external fault condition signaled on the FAULT pin, a TSD event, or a UVLO condition.

SELECTING R_S TO SET THE CURRENT LIMIT

See Figure 21 for the current-limit block diagram for peak current-limit control. Use using the following equation to set the current limit:

$$I_{PK}(\text{mA}) = \frac{100\ \text{mV}}{R_S} \quad (1)$$

where:
I_{PK} is the desired peak current-limit in mA.
R_S is the sense resistor used to set the peak current limit in Ω.

When the ADP1972 is configured to operate in buck/charge mode, the internal current-limit reference is set to 300 mV (typical). When the ADP1972 is configured to operate in boost/recycle mode, the internal current-limit reference is set to 500 mV (typical). The external resistor, R_{CL}, is needed to offset the current properly to detect the peak in both buck and boost operation. Set the value of R_{CL} to 20 kΩ. In operation, the equation for setting the peak current follows:

For buck/charge mode, it is

$$V_{REF\,(BUCK)} = (I_{CL}) \times (R_{CL}) - (I_{PK}) \times (R_S) \quad (2)$$

For boost/recycle mode, it is

$$V_{REF\,(BOOST)} = (I_{CL}) \times (R_{CL}) + (I_{PK}) \times (R_S) \quad (3)$$

where:
$V_{REF\,(BUCK)}$ = 300 mV, typical.
$V_{REF\,(BOOST)}$ = 500 mV, typical.
I_{CL} = 20 µA, typical.
R_{CL} = 20 kΩ.

The ADP1972 is designed so that the peak current limit is the same in both the buck mode and boost mode of operation. A 1% or better tolerance for the R_{CL} and R_S resistors is recommended.

ADJUSTING THE OPERATING FREQUENCY

If the SCFG pin is tied to VREG, forcing $V_{SCFG} \geq 4.53$ V, or if SCFG is left floating and internally tied to VREG, the ADP1972 operates at the frequency set by R_{FREQ}, and the SYNC pin outputs a clock at the programmed frequency. When $V_{SCFG} \geq 4.53$ V, the output clock on the SYNC pin can be used as a master clock in applications that require synchronization.

If $V_{SCFG} \leq 0.5$ V, the SYNC pin is configured as an input, and the ADP1972 operates as a slave device. As a slave device, the ADP1972 synchronizes to the external clock applied to the SYNC pin. If the voltage applied to the SCFG pin is $0.65\ \text{V} < V_{SCFG} < 4.25$ V, and a resistor is connected between SCFG and ground, the SYNC pin is configured as an input, and the ADP1972 synchronizes to a phase shifted version of the external clock applied to the SYNC pin.

Whether operating the ADP1972 as a master or as a slave device, R_{FREQ} must be carefully selected using the equations in the following sections.

Selecting R_{FREQ} for a Master Device

When V_{SCFG} is ≥ 4.53 V, the ADP1972 operates as a master device. When functioning as a master device, the ADP1972 operates at the frequency set by the external R_{FREQ} resistor connected between FREQ and ground, and the ADP1972 outputs a clock at the programmed frequency on the SYNC pin.

Figure 22 shows the relationship between the programmed switching frequency (f_{SET}) and the value of R_{FREQ}.

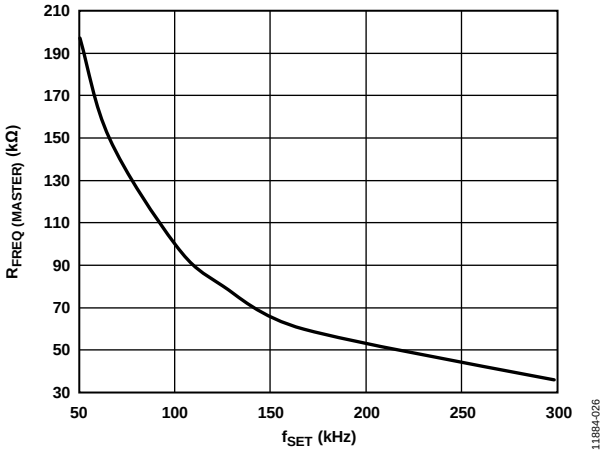

Figure 22. R_{FREQ} vs. Switching Frequency (f_{SET})

Use the following equation to calculate the R_{FREQ} value for a desired master clock synchronization frequency:

$$R_{FREQ\,(MASTER)}(\text{k}\Omega) = \frac{10^4}{f_{SET}(\text{kHz})} \quad (4)$$

where:
f_{SET} is the switching frequency in kHz.
$R_{FREQ\,(MASTER)}$ is the resistor in kΩ to set the frequency for master devices.

Selecting R_{FREQ} for a Slave Device

To configure the ADP1972 as a slave device, drive V_{SCFG} < 4.53 V. When functioning as a slave device, the ADP1972 operates at the frequency of the external clock applied to the SYNC pin. To ensure proper synchronization, select R_{FREQ} to set the frequency to a value slightly slower than that of the master clock by using the following equation:

$$R_{FREQ\ (SLAVE)} = 1.11 \times R_{FREQ\ (MASTER)} \quad (5)$$

where:
$R_{FREQ\ (MASTER)}$ is the resistor value that corresponds to the frequency of the master clock applied to the SYNC pin.
$R_{FREQ\ (SLAVE)}$ is the resistor value that appropriately scales the frequency for the slave device, and 1.11 is the R_{FREQ} slave to master ratio for synchronization.

The frequency of the slave device is set to a frequency slightly lower than that of the master device to allow the digital synchronization loop of the ADP1972 to synchronize to the master clock period. The slave device has approximately a 30% range capability to adjust to match the master clock value. Setting $R_{FREQ\ (SLAVE)}$ to 1.11× larger than $R_{FREQ\ (MASTER)}$ runs the synchronization loop in approximately the center of the adjustment range.

Programming the External Clock Phase Shift

If a phase shift is not required for slave devices, connect SCFG of each slave device to ground. For devices that require a phase shifted version of the synchronization clock that is applied to the SYNC pin of the slave devices, connect a resistor (R_{SCFG}) from SCFG to ground to program the desired phase shift. To determine the R_{SCFG} for a desired phase shift (φ_{SHIFT}), start by calculating the frequency of the slave clock (f_{SLAVE}).

$$f_{SLAVE}(\text{kHz}) = \frac{10^4}{R_{FREQ(SLAVE)}} \quad (6)$$

Next, calculate the period of the slave clock.

$$T_{SLAVE}(\mu\text{s}) = \frac{1}{f_{SLAVE}(\text{kHz})} \times 10^3 \quad (7)$$

where:
T_{SLAVE} is the period of the master clock in µs.
f_{SLAVE} is the frequency of the master clock in kHz.

Next, determine the phase time delay (T_{DELAY}) for the desired phase shift (φ_{SHIFT}) using the following equation:

$$T_{DELAY}(\mu\text{s}) = \frac{\varphi_{SHIFT} \times T_{SLAVE}(\mu\text{s})}{360} \quad (8)$$

where:
T_{DELAY} is the phase delay in µs.
φ_{SHIFT} is the desired phase shift.

Lastly, to calculate the phase delay (T_{DELAY}), use the following equation:

$$R_{SCFG}\ (\text{k}\Omega) = 0.45 \times R_{FREQ\ (SLAVE)}\ (\text{k}\Omega) + 50 \times T_{DELAY}\ (\mu\text{s}) \quad (9)$$

where:
R_{SCFG} is the corresponding resistor for the desired phase shift in kHz.

When using the phase shift feature, connect a capacitor of 47 pF or greater in parallel with R_{SCFG}.

Alternatively, the SCFG pin can be controlled with a voltage source. When using an independent voltage source, ensure $V_{SCFG} \le$ VREG under all conditions. When the ADP1972 is disabled via the EN pin or UVLO, VREG = 0 V, and the voltage source must adjust accordingly to ensure $V_{SCFG} \le$ VREG.

Figure 23 shows the internal voltage ramp of the ADP1972. The voltage ramp has a well controlled 4 V p-p.

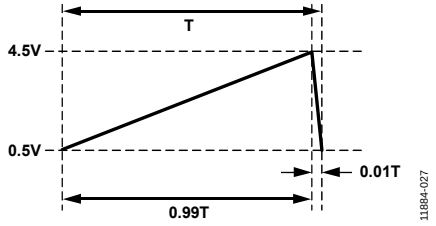

Figure 23. Internal Voltage Ramp

PROGRAMMING THE MAXIMUM DUTY CYCLE

The ADP1972 is designed with a 98% (typical) internal maximum duty cycle. By connecting a resistor from DMAX to ground, the maximum duty cycle can be programmed at any value from 0% to 98%, using the following equation:

$$D_{MAX}(\%) = \frac{21.5 \times V_{FREQ} \times R_{DMAX}}{R_{FREQ}} - 10.5 \quad (10)$$

where:
D_{MAX} is the programmed maximum duty cycle.
V_{FREQ} is 1.252 V (typical).
R_{DMAX} is the value of the resistance used to program the maximum duty cycle.
R_{FREQ} is the frequency set resistor used in the application.

The current source of DMAX is equivalent to the programmed current of the FREQ pin:

$$I_{DMAX} = I_{FREQ} = \frac{V_{FREQ}}{R_{FREQ}} \quad (11)$$

where $I_{DMAX} = I_{FREQ}$ = the current programmed on the FREQ pin.

The maximum allowable duty cycle of the ADP1972 is 98% (typical). If the resistor on DMAX sets a maximum duty cycle larger than 98%, the ADP1972 defaults to its internal maximum. If the 98% internal maximum duty cycle is sufficient for the application, tie the DMAX pin to VREG or leave it floating.

The C_{DMAX} capacitor connected from the DMAX pin to GND must be 47 pF or greater.

ADJUSTING THE SOFT START PERIOD

The ADP1972 has a programmable soft start feature that prevents output voltage overshoot during startup. Refer to Figure 18 for a soft start diagram. Use the following equation to calculate the delay time before switching is enabled (t_{REG}):

$$t_{REG} = \frac{0.52}{I_{SS}} \times C_{SS} \quad (12)$$

where I_{SS} = 5 µA, typical.

A C_{SS} capacitor is not required for the ADP1972. When the C_{SS} capacitor is not used, the internal 5 µA (typical) current source immediately pulls the SS pin voltage to VREG. When a C_{SS} capacitor is not used, there is no soft start control internal to the ADP1972, and the system could produce a large output overshoot and a large peak inductor spike during startup. When a C_{SS} is not used, ensure that the output overshoot is not large enough to trip the hiccup current limit during startup.

PCB LAYOUT GUIDELINES

For high efficiency, good regulation, and stability, a well designed PCB layout is required.

Use the following guidelines when designing the PCB (see Figure 16 for the block diagram and Figure 2 for the pin configuration).

- Keep the low effective series resistance (ESR) input supply capacitor for VIN (C_{IN}) as close as possible to the VIN and GND pins to minimize noise being injected into the device from board parasitic inductance.
- Keep the low ESR input supply capacitor for VREG (C_{VREG}) as close as possible to the VREG and GND pins to minimize noise being injected into the device from board parasitic inductance.
- Place the components for the SCFG, FREQ, DMAX, and SS pins close to the corresponding pins. Tie these components collectively to an AGND plane that makes a Kelvin connection to the GND pin.
- Keep the trace from the COMP pin to the accompanying device (for example, AD8450) as short as possible. Avoid routing this trace near switching signals and shield the trace if possible.
- Place any trace or components for the SYNC pin away from sensitive analog nodes. When using an external pull-up, it is best to use a local 0.1 µF bypass capacitor from the supply of the pull-up resistor to GND.
- Keep the traces from the DH and DL pins to the external components as short as possible to minimize parasitic inductance and capacitance, which affect the control signal. The DH and DL pins are switching nodes; do not route them near any sensitive analog circuitry.
- Keep high current traces as short and as wide as possible.
- Connect the ground connection of the ADP1972 directly to the ground connection of the current sense, R_S, resistor.
- Connect CL through a 20 kΩ resistor directly to R_S.
- Use a Kelvin connection shown in Figure 24 and Figure 25 from the following:
  - The GND pin to the ground point for R_S
  - The GND_{SENSE} pin to the ground point for R_S
  - The system power ground to the ground point of R_S

  Extra resistance due to PCB routing introduces a voltage difference between the GND pin and the GND_{SENSE} pin. This voltage difference must not exceed ±0.3 V.
- When building a system with a master and multiple slave devices, the capacitance of the trace attached to the SYNC pin must be minimized.
  - For small systems with only a few slave devices, a resistor connected in series between the master SYNC signal and the slave SYNC input pins limits the capacitance of the trace and reduces the fast ground currents that can inject noise into the master device.
  - For larger applications, the series resistance is not enough to isolate the master SYNC clock. In larger systems, use an external buffer to reduce the capacitance of the trace. The external buffer has the drive capability to support a large number of slave devices.

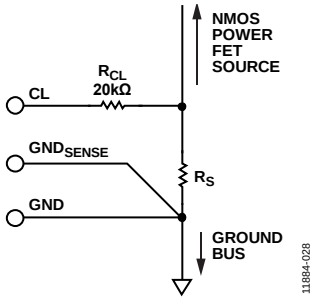

Figure 24. Recommended R_S Kelvin Ground Connection

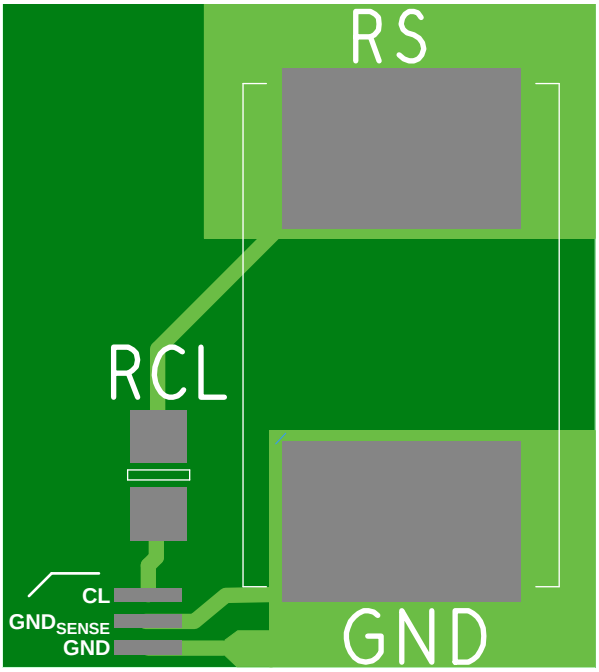

Figure 25. Recommended R_S Kelvin Ground Connection on PCB Layout

OUTLINE DIMENSIONS

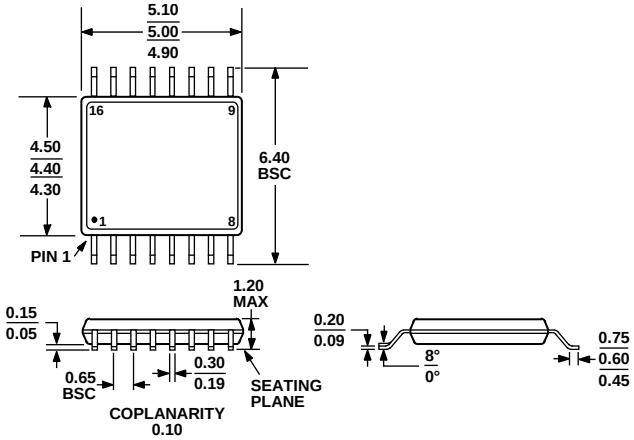

Figure 26. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADP1972ARUZ-R7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP], 7″ Tape and Reel	RU-16	1,000
ADP1972ARUZ-RL	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP], 13″ Tape and Reel	RU-16	2,500
ADP1972-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

D11884-0-11/14(B)