![ANALOG DEVICES]

Hot Swap Controller and I^2C® Power Monitor with Convert Pin

ADM1176

FEATURES

Allows safe board insertion and removal from a live backplane
Controls supply voltages from 3.15 V to 16.5 V
Precision current sense amplifier
Precision voltage input
12-bit ADC for current and voltage readback
Charge pumped gate drive for external N-channel FET
Adjustable analog current limit with circuit breaker
±3% accurate hot swap current limit level
Fast response limits peak fault current
Automatic retry or latch-off on current fault
Programmable hot swap timing via TIMER pin
Active-high ON pin
I^2C® fast mode-compliant interface (400 kHz maximum)
Two address pins allow 16 devices on the same bus
10-lead MSOP

APPLICATIONS

Power monitoring/power budgeting
Central office equipment
Telecommunication and data communication equipment
PCs/servers

GENERAL DESCRIPTION

The ADM1176 is an integrated hot swap controller that offers digital current and voltage monitoring via an on-chip, 12-bit analog-to-digital converter (ADC), communicated through an I^2C interface.

An internal current sense amplifier senses voltage across the sense resistor in the power path via the VCC pin and the SENSE pin.

The ADM1176 limits the current through this resistor by controlling the gate voltage of an external N-channel FET in the power path, via the GATE pin. The sense voltage (and, therefore, the inrush current) is kept below a preset maximum.

The ADM1176 protects the external FET by limiting the time that it spends with maximum current running through it. This current limit period is set by the choice of capacitor attached to the TIMER pin. Additionally, the device provides protection from overcurrent events that may occur once the hot swap event is complete. In the case of a short-circuit event, the current in the sense resistor exceeds an overcurrent trip threshold, and the FET is switched off immediately by pulling down the GATE pin.

FUNCTIONAL BLOCK DIAGRAM

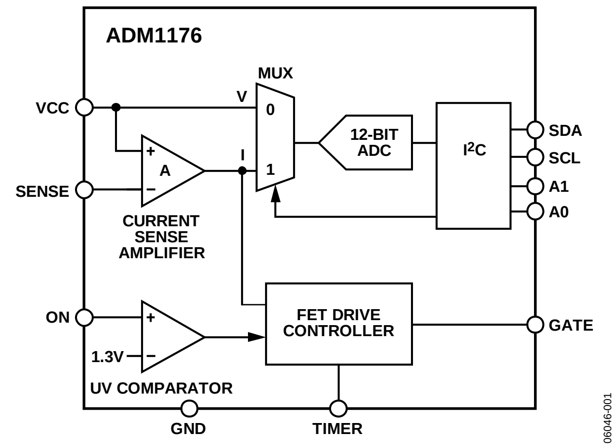

Figure 1.

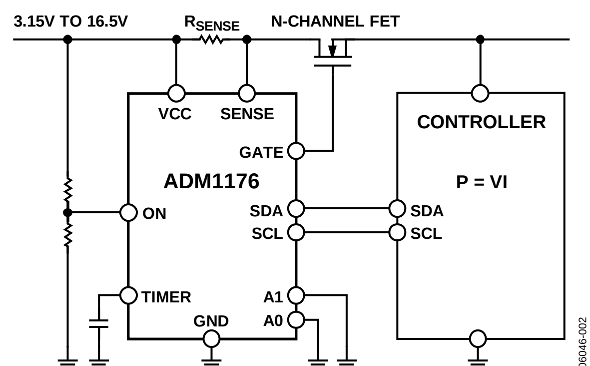

Figure 2. Applications Diagram

A 12-bit ADC can measure the current seen in the sense resistor, as well as the supply voltage on the VCC pin. An industry-standard I^2C interface allows a controller to read current and voltage data from the ADC. Measurements can be initiated by an I^2C command. Alternatively, the ADC can run continuously, and the user can read the latest conversion data whenever it is required. Up to 16 unique I^2C addresses can be created, depending on the way the A0 and A1 pins are connected.

The ADM1176 is packaged in a 10-lead MSOP.

Rev. 0

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REVISION HISTORY

9/06—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.15 V to 16.5 V; T_A = −40°C to +85°C; typical values at T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions
VCC PIN					
Operating Voltage Range, V_{VCC}	3.15		16.5	V	
Supply Current, I_{CC}		1.7	2.5	mA	
Undervoltage Lockout, V_{UVLO}		2.8		V	V_{CC} rising
Undervoltage Lockout Hysteresis, $V_{UVLOHYST}$		80		mV	
ON PIN					
Input Current, I_{INON}	−100		+100	nA	ON < 1.5 V
	−2		+2	µA	
Rising Threshold, V_{ONTH}	1.26	1.3	1.34	V	ON rising
Trip Threshold Hysteresis, V_{ONHYST}	35	50	65	mV	
Glitch Filter Time		3		µs	
SENSE PIN					
Input Leakage, I_{SENSE}	−1		+1	µA	$V_{SENSE} = V_{VCC}$
Overcurrent Fault Timing Threshold, V_{OCTIM}	92			mV	$V_{OCTRIM} = (V_{VCC} - V_{SENSE})$, fault timing starts on the TIMER pin
Overcurrent Limit Threshold, V_{LIM}	97	100	103	mV	$V_{LIM} = (V_{VCC} - V_{SENSE})$, closed-loop regulation to a current limit
Fast Overcurrent Trip Threshold, V_{OCFAST}			115	mV	$V_{OCFAST} = (V_{VCC} - V_{SENSE})$, gate pull-down current turned on
GATE PIN					
Drive Voltage, V_{GATE}	3	6	9	V	$V_{GATE} - V_{VCC}$, V_{VCC} = 3.15 V
	9	11	13	V	$V_{GATE} - V_{VCC}$, V_{VCC} = 5 V
	7	10	13	V	$V_{GATE} - V_{VCC}$, V_{VCC} = 16.5 V
Pull-Up Current	8	12.5	17	µA	V_{GATE} = 0 V
Pull-Down Current		1.5		mA	V_{GATE} = 3 V, V_{VCC} = 3.15 V
		5		mA	V_{GATE} = 3 V, V_{VCC} = 5 V
		7		mA	V_{GATE} = 3 V, V_{VCC} = 16.5 V
TIMER PIN					
Pull-Up Current (Power On Reset), $I_{TIMERUPPOR}$	−3.5	−5	−6.5	µA	Initial cycle, V_{TIMER} = 1 V
Pull-Up Current (Fault Mode), $I_{TIMERUPFAULT}$	−40	−60	−80	µA	During current fault, V_{TIMER} = 1 V
Pull-Down Current (Retry Mode), $I_{TIMERDNRETRY}$		2	3	µA	After current fault and during a cool-down period on a retry device, V_{TIMER} = 1 V
Pull-Down Current, $I_{TIMERDN}$		100		µA	Normal operation, V_{TIMER} = 1 V
Trip Threshold High, V_{TIMERH}	1.26	1.3	1.34	V	TIMER rising
Trip Threshold Low, V_{TIMERL}	0.175	0.2	0.225	V	TIMER falling
A0 PIN, A1 PIN					
Set Address to 00, $V_{ADRLOWV}$	0		0.8	V	Low state
Set Address to 01, $R_{ADRLOWZ}$	135	150	165	kΩ	Resistor to ground state, load pin with specified resistance for 01 decode
Set Address to 10, $I_{ADRHIGHZ}$	−1		+1	µA	Open state, maximum load allowed on the A0 pin and the A1 pin for 10 decode
Set Address to 11, $V_{ADRHIGHV}$	2		5.5	V	High state
Input Current for 11 Decode, I_{ADRLOW}		3	10	µA	V_{ADR} = 2.0 V to 5.5 V
Input Current for 00 Decode, $I_{ADRHIGH}$	−40	−22		µA	V_{ADR} = 0 V to 0.8 V

Parameter	Min	Typ	Max	Unit	Conditions	
MONITORING ACCURACY[1]						
Current Sense Absolute Accuracy	−1.45		+1.45	%	V_{SENSE} = 75 mV	0°C to +70°C
	−1.8		+1.8	%	V_{SENSE} = 50 mV	0°C to +70°C
	−2.8		+2.8	%	V_{SENSE} = 25 mV	0°C to +70°C
	−5.7		+5.7	%	V_{SENSE} = 12.5 mV	0°C to +70°C
	−1.5		+1.5	%	V_{SENSE} = 75 mV	0°C to +85°C
	−1.8		+1.8	%	V_{SENSE} = 50 mV	0°C to +85°C
	−2.95		+2.95	%	V_{SENSE} = 25 mV	0°C to +85°C
	−6.1		+6.1	%	V_{SENSE} = 12.5 mV	0°C to +85°C
	−1.95		+1.95	%	V_{SENSE} = 75 mV	−40°C to +85°C
	−2.45		+2.45	%	V_{SENSE} = 50 mV	−40°C to +85°C
	−3.85		+3.85	%	V_{SENSE} = 25 mV	−40°C to +85°C
	−6.7		+6.7	%	V_{SENSE} = 12.5 mV	−40°C to +85°C
V_{SENSE} for ADC Full Scale		105.84		mV	This is an absolute value to be used when converting ADC codes to current readings; any inaccuracy in this value is factored into absolute current accuracy values (see specs for Current Sense Absolute Accuracy)	
Voltage Sense Accuracy	−0.85		+0.85	%	V_{VCC} = 3.0 V to 5.5 V (low range)	0°C to +70°C
	−0.9		+0.9	%	V_{VCC} = 10.8 V to 16.5 V (high range)	0°C to +70°C
	−0.85		+0.85	%	V_{VCC} = 3.0 V to 5.5 V (low range)	0°C to +85°C
	−0.9		+0.9	%	V_{VCC} = 10.8 V to 16.5 V (high range)	0°C to +85°C
	−0.9		+0.9	%	V_{VCC} = 3.0 V to 5.5 V (low range)	−40°C to +85°C
	−1.15		+1.15	%	V_{VCC} = 10.8 V to 16.5 V (high range)	−40°C to +85°C
V_{CC} for ADC Full Scale, Low Range (VRANGE = 1)		6.65		V	These are absolute values to be used when converting ADC codes to current readings; any inaccuracy in these values is factored into voltage accuracy values (see specs for Current Sense Absolute Accuracy)	
V_{CC} for ADC Full Scale, High Range (VRANGE = 0)		26.52		V		
I^2C TIMING						
Low Level Input Voltage, V_{IL}			0.3 V_{BUS}	V		
High Level Input Voltage, V_{IH}	0.7 V_{BUS}			V		
Low Level Output Voltage on SDA, V_{OL}			0.4	V	I_{OL} = 3 mA	
Output Fall Time on SDA from V_{IHMIN} to V_{ILMAX}	20 + 0.1 C_B		250	ns	C_B = bus capacitance from SDA to GND	
Maximum Width of Spikes Suppressed by Input Filtering on SDA and SCL Pins	50		250	ns		
Input Current, I_I, on SDA/SCL When Not Driving Out a Logic Low	−10		+10	µA		
Input Capacitance on SDA/SCL		5		pF		
SCL Clock Frequency, f_{SCL}			400	kHz		
Low Period of the SCL Clock	600			ns		
High Period of the SCL Clock	1300			ns		

Parameter	Min	Typ	Max	Unit	Conditions
Setup Time for a Repeated Start Condition, $t_{SU;STA}$	600			ns	
SDA Output Data Hold Time, $t_{HD;DAT}$	100		900	ns	
Setup Time for a Stop Condition, $t_{SU;STO}$	600			ns	
Bus Free Time Between a Stop and a Start Condition, t_{BUF}	1300			ns	
Capacitive Load for Each Bus Line			400	pF	

[1] Monitoring accuracy is a measure of the error in a code that is read back for a particular voltage/current. This is a combination of amplifier error, reference error, ADC error, and error in ADC full-scale code conversion factor.

ABSOLUTE MAXIMUM RATINGS

Table 2.

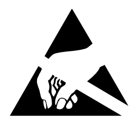
Parameter	Rating
VCC Pin	20 V
SENSE Pin	20 V
TIMER Pin	−0.3 V to +6 V
ON Pin	−0.3 V to +20 V
GATE Pin	30 V
SDA Pin, SCL Pin	−0.3 V to +7 V
A0 Pin, A1 Pin	−0.3 V to +6 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
10-Lead MSOP	137.5	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

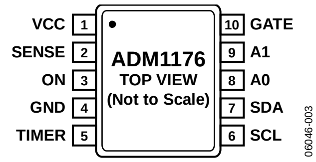


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCC	Positive Supply Input Pin. The operating supply voltage range is from 3.15 V to 16.5 V. An undervoltage lockout (UVLO) circuit resets the ADM1176 when a low supply voltage is detected.
2	SENSE	Current Sense Input Pin. A sense resistor between the VCC pin and the SENSE pin sets the analog current limit. The hot swap operation of the ADM1176 controls the external FET gate to maintain the ($V_{VCC} − V_{SENSE}$) voltage at 100 mV or below.
3	ON	Undervoltage Input Pin. Active-high pin. An internal ON comparator has a trip threshold of 1.3 V, and the output of this comparator is used as an enable for the hot swap operation. With an external resistor divider from VCC to GND, this pin can be used to enable the hot swap operation on a specific voltage on VCC, giving an undervoltage function.
4	GND	Chip Ground Pin.
5	TIMER	Timer Pin. An external capacitor, C_{TIMER}, sets a 270 ms/μF initial timing cycle delay and a 21.7 ms/μF fault delay. The GATE pin turns off when the TIMER pin is pulled beyond the upper threshold. An overvoltage detection with an external Zener can be used to force this pin high.
6	SCL	I^2C Clock Pin. Open-drain input requires an external resistive pull-up.
7	SDA	I^2C Data I/O Pin. Open-drain input/output. Requires an external resistive pull-up.
8	A0	I^2C Address Pin. This pin can be tied low, tied high, left floating, or tied low through a resistor. Sixteen different I^2C address options are available, depending on the external configuration of the A0 pin and A1 pin.
9	A1	I^2C Address Pin. This pin can be tied low, tied high, left floating or tied low through a resistor. Sixteen different I^2C address options are available, depending on the external configuration of the A0 pin and the A1 pin.
10	GATE	GATE Output Pin. This pin is the high-side gate drive of an external N-channel FET. This pin is driven by the FET drive controller, which utilizes a charge pump to provide a 12.5 μA pull-up current to charge the FET GATE pin. The FET drive controller regulates to a maximum load current (100 mV through the sense resistor) by modulating the GATE pin.

TYPICAL PERFORMANCE CHARACTERISTICS

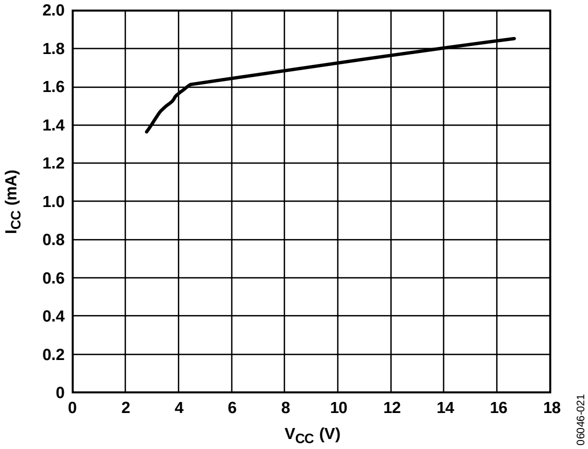


Figure 4. Supply Current vs. Supply Voltage

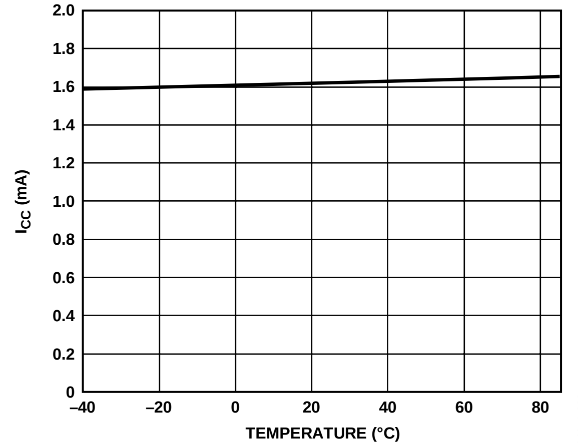


Figure 7. Supply Current vs. Temperature (Gate On)

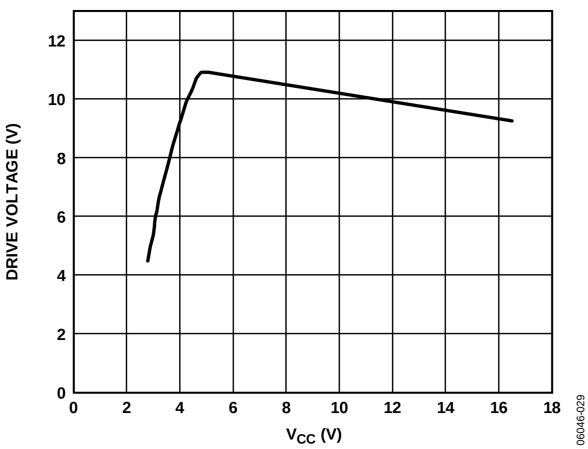


Figure 5. Drive Voltage (V_{GATE} – V_{CC}) vs. Supply Voltage

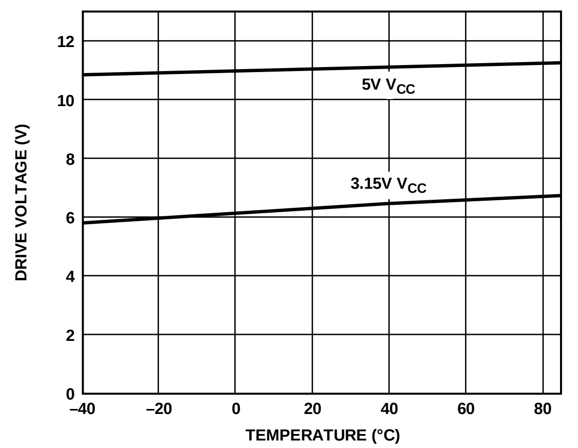


Figure 8. Drive Voltage (V_{GATE} – V_{CC}) vs. Temperature

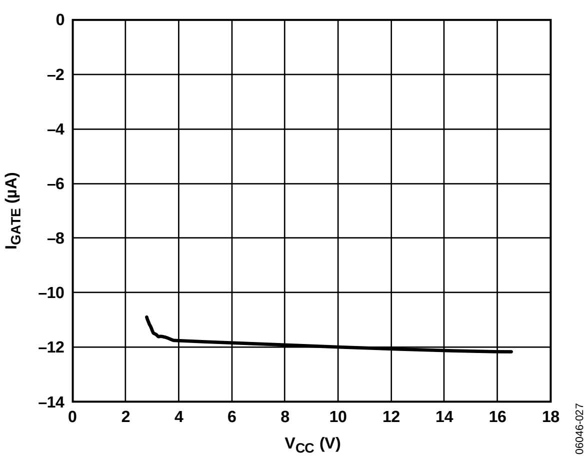


Figure 6. Gate Pull-Up Current vs. Supply Voltage

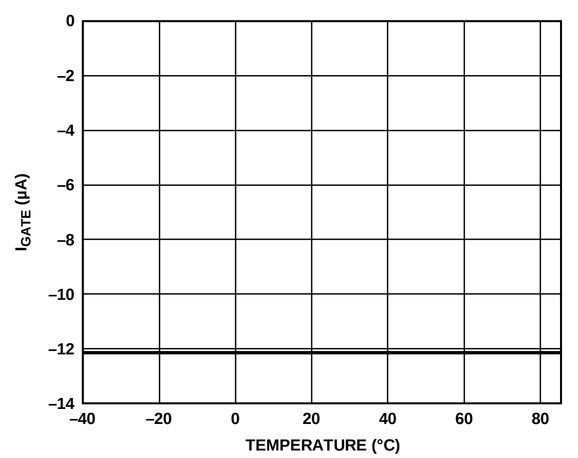


Figure 9. Gate Pull-Up Current vs. Temperature

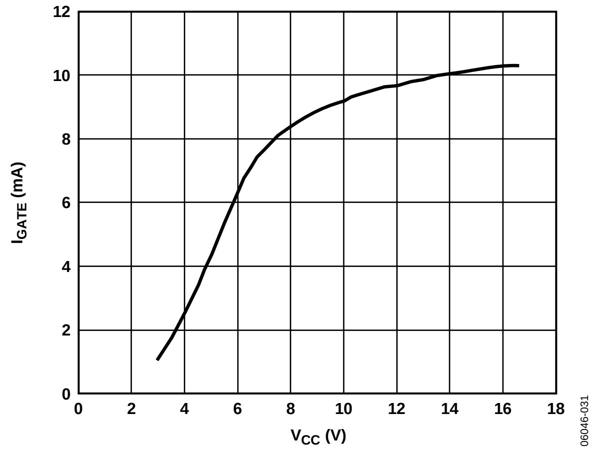


Figure 10. Gate Pull-Down Current vs. V_{CC} at V_{GATE} = 5 V

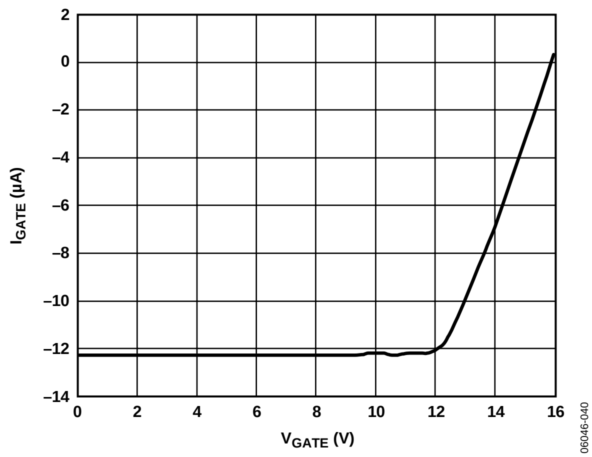


Figure 11. Gate Pull-Up Current vs. Gate Voltage at V_{CC} = 5 V

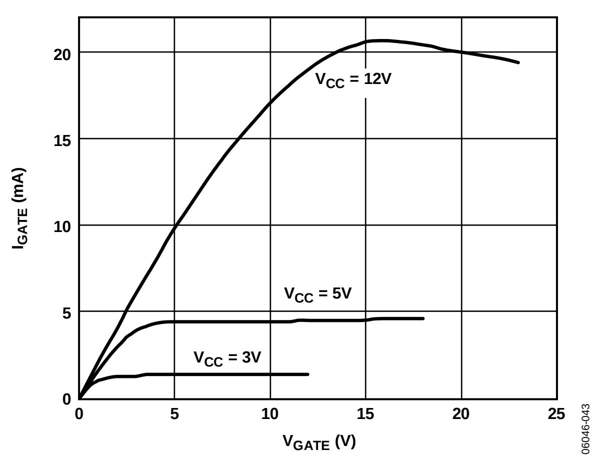


Figure 12. Gate Pull-Down Current vs. Gate Voltage

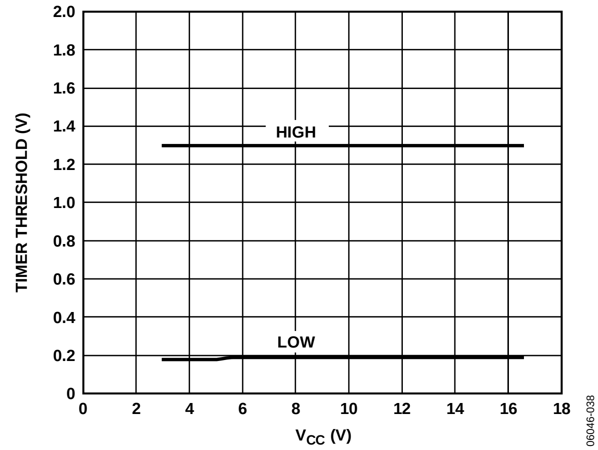


Figure 13. Timer Threshold vs. Supply Voltage

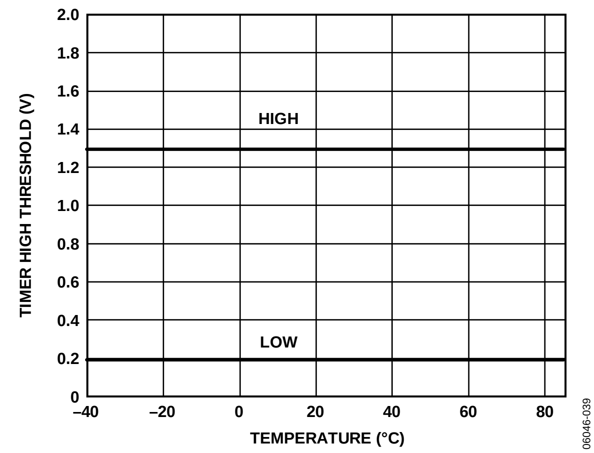


Figure 14. Timer Threshold vs. Temperature

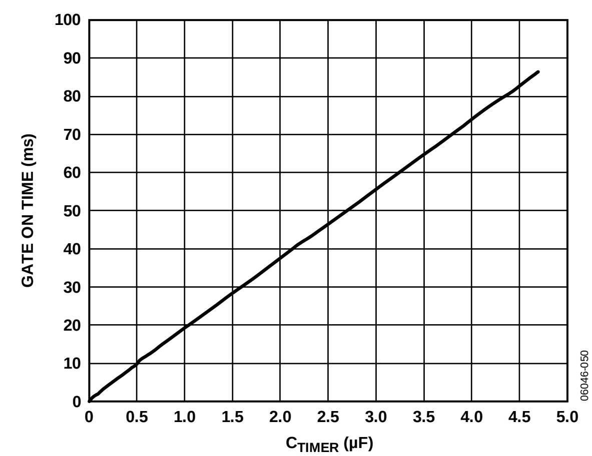


Figure 15. Current Limit On Time vs. Timer Capacitance

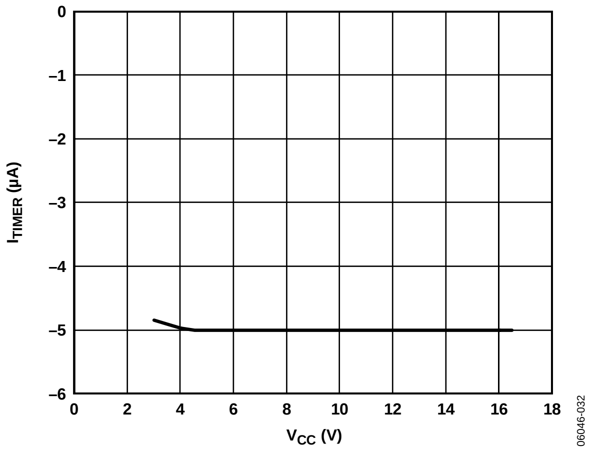


Figure 16.Timer Pull-Up Current (Initial Cycle) vs. Supply Voltage

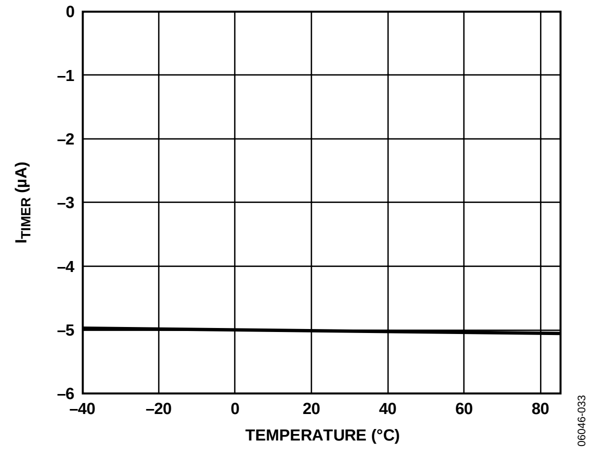


Figure 19. Timer Pull-Up Current (Initial Cycle) vs. Temperature

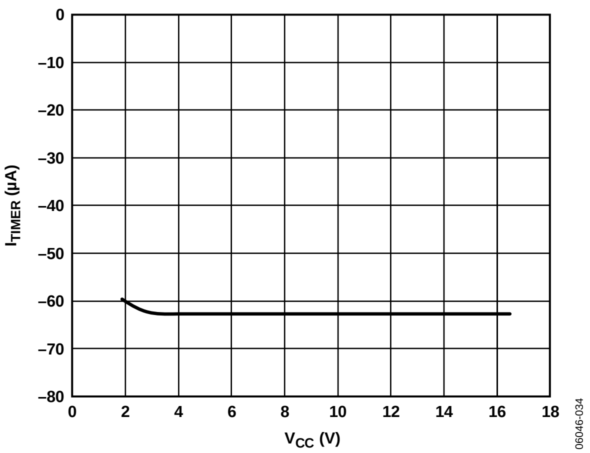


Figure 17. Timer Pull-Up Current (C. B. Delay) vs. Supply Voltage

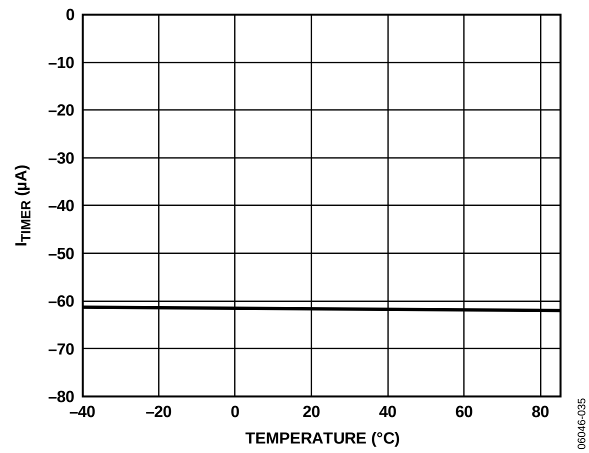


Figure 20. Timer Pull-Up Current (C. B. Delay) vs. Temperature

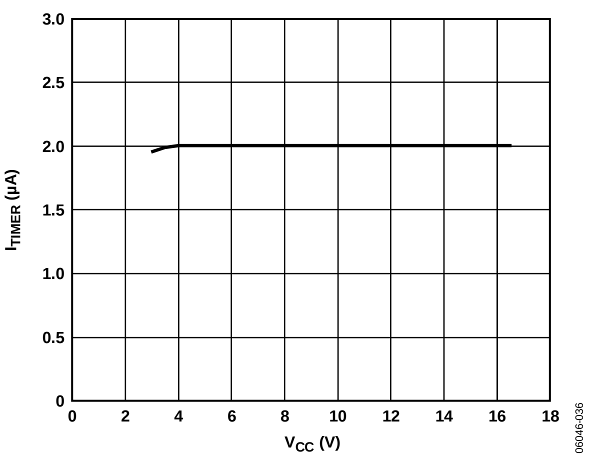


Figure 18. Timer Pull-Down Current (Cool-Off Cycle) vs. Supply Voltage

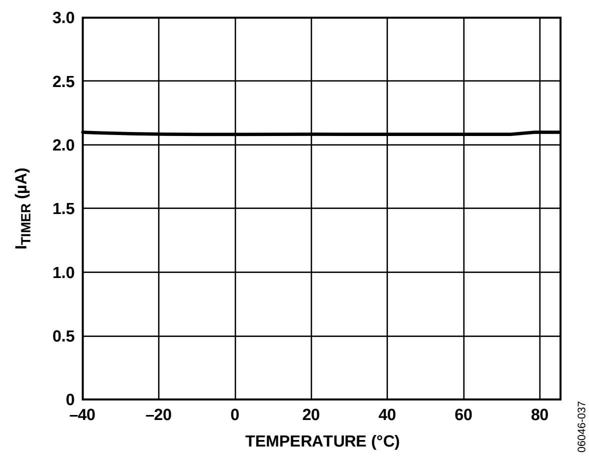


Figure 21. Timer Pull-Down Current (Cool-Off Cycle) vs. Temperature

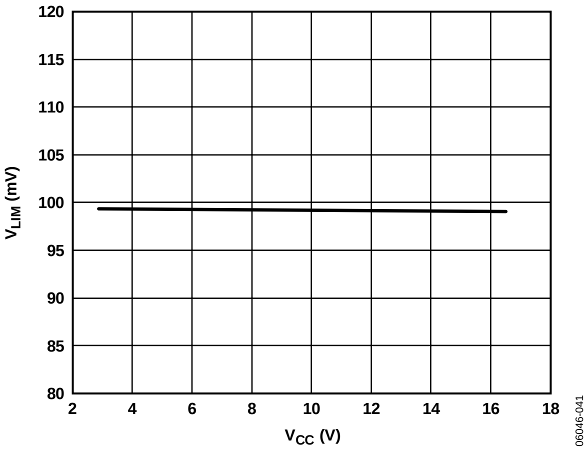


Figure 22. Circuit Breaker Limit Voltage vs. Supply Voltage

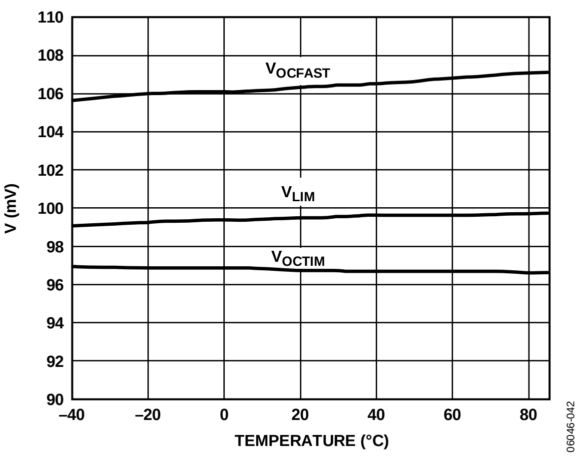


Figure 23. V_{OCTIM}, V_{LIM}, V_{OCFAST} vs. Temperature

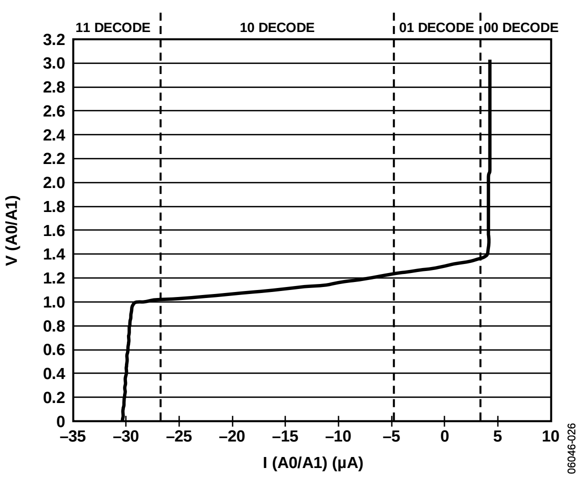


Figure 24. Address Pin Voltage vs. Address Pin Current for Four Addressing Options

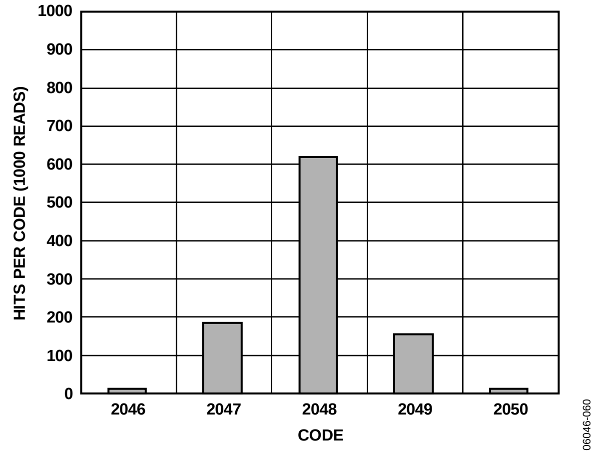


Figure 25. ADC Noise, Current Channel, Midcode Input, 1000 Reads

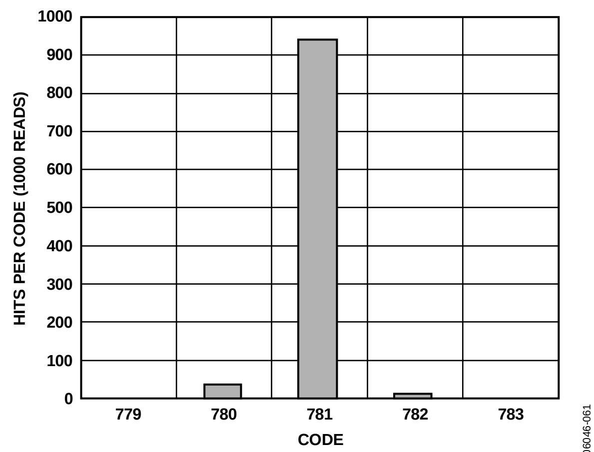


Figure 26. ADC Noise, 14:1 Voltage Channel, 5 V Input, 1000 Reads

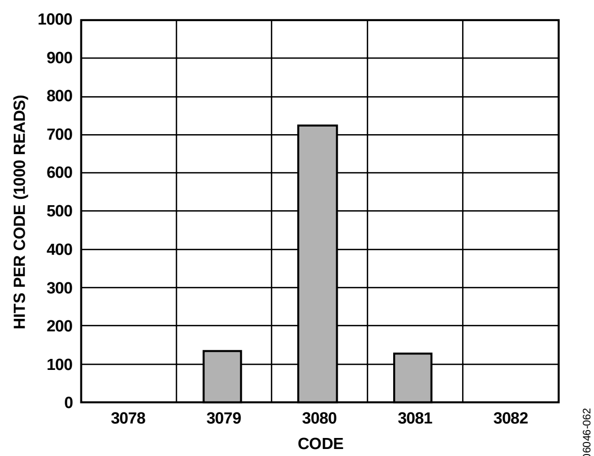


Figure 27. ADC Noise, 7:1 Voltage Channel, 5 V Input, 1000 Reads

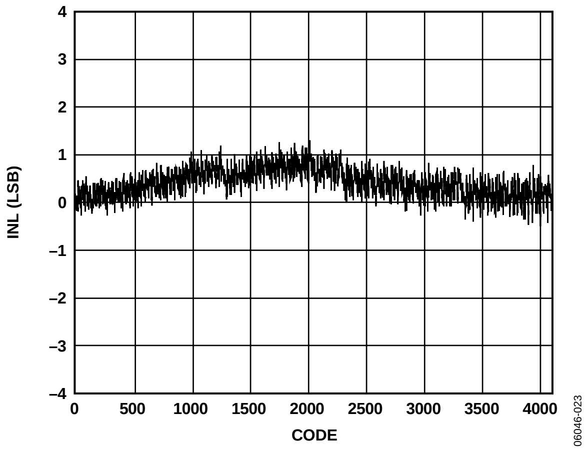


Figure 28. INL for ADC

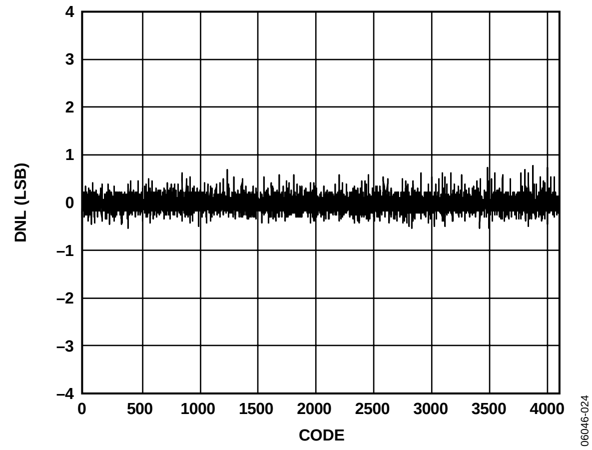


Figure 29. DNL for ADC

OVERVIEW OF THE HOT SWAP FUNCTION

When circuit boards are inserted into a live backplane, discharged supply bypass capacitors draw large transient currents from the backplane power bus as they charge. Such transient currents can cause permanent damage to connector pins, as well as dips on the backplane supply that can reset other boards in the system. The ADM1176 is designed to turn a circuit board supply voltage on and off in a controlled manner, allowing the circuit board to be safely inserted into or removed from a live backplane. The ADM1176 can reside either on the backplane or on the circuit board itself.

The ADM1176 controls the inrush current to a fixed maximum level by modulating the gate of an external N-channel FET placed between the live supply rail and the load. This hot swap function protects the card connectors and the FET itself from damage and limits any problems that can be caused by high current loads on the live supply rail.

The ADM1176 holds the GATE pin down (and, thus, the FET is held off) until a number of conditions are met. An undervoltage lockout circuit ensures that the device is provided with an adequate input supply voltage. Once the input supply voltage has been successfully detected, the device goes through an initial timing cycle to provide a delay before it attempts to hot swap. This delay ensures that the board is fully seated in the backplane before the board is powered up.

Once the initial timing cycle is complete, the hot swap function is switched on under control of the ON pin. When the ON pin is asserted high, the hot swap operation starts.

The ADM1176 charges up the gate of the FET to turn on the load. It continues to charge up the GATE pin until the linear current limit (set to 100 mV/R_{SENSE}) is reached. For some combinations of low load capacitance and high current limit, this limit may not be reached before the load is fully charged up. If current limit is reached, the ADM1176 regulates the GATE pin to keep the current at this limit. For currents above the overcurrent fault timing threshold, nominally 100 mV/R_{SENSE}, the current fault is timed by sourcing a current out to the TIMER pin. If the load becomes fully charged before the fault current limit time is reached (when the TIMER pin reaches 1.3 V), the current drops below the overcurrent fault timing threshold. The ADM1176 then charges the GATE pin higher to fully enhance the FET for lowest R_{ON}, and the TIMER pin is pulled down again.

If the fault current limit time is reached before the load drops below the current limit, a fault has been detected, and the hot swap operation is aborted by pulling down on the GATE pin to turn off the FET. The ADM1176-2 latches off at this point and attempts to hot swap again only when the ON pin is deasserted and then asserted again.

The ADM1176-1 retries the hot swap operation indefinitely, keeping the FET in its safe operating area (SOA) by using the TIMER pin to time a cool-down period in between hot swap attempts. The current and voltage threshold combinations on the TIMER pin set the retry duty cycle to 3.8%.

The ADM1176 is designed to operate over a range of supplies from 3.15 V to 16.5 V.

UNDERVOLTAGE LOCKOUT

An internal undervoltage lockout (UVLO) circuit resets the ADM1176 if the VCC supply is too low for normal operation. The UVLO has a low-to-high threshold of 2.8 V, with 80 mV hysteresis. Above 2.8 V supply voltage, the ADM1176 starts the initial timing cycle.

ON FUNCTION

The ADM1176-1 has an active-high ON pin. The ON pin is the input to a comparator that has a low-to-high threshold of 1.3 V, a 50 mV hysteresis, and a glitch filter of 3 μs. A low input on the ON pin turns off the hot swap operation by pulling the GATE pin to ground, turning off the external FET. The TIMER pin is also reset by turning on a pull-down current on this pin. A low-to-high transition on the ON pin starts the hot swap operation. A 10 kΩ pull-up resistor connecting the ON pin to the supply is recommended.

Alternatively, an external resistor divider at the ON pin can be used to program an undervoltage lockout value higher than the internal UVLO circuit, thereby setting a voltage level at the VCC supply where the hot swap operation is to start. An RC filter can be added at the ON pin to increase the delay time at card insertion if the initial timing cycle delay is insufficient.

TIMER FUNCTION

The TIMER pin handles several timing functions with an external capacitor, C_{TIMER}. There are two comparator thresholds: V_{TIMERH} (0.2 V) and V_{TIMERL} (1.3 V). The four timing current sources are a 5 μA pull-up, a 60 μA pull-up, a 2 μA pull-down, and a 100 μA pull-down. The 100 μA pull-down is a non-ideal current source approximating a 7 kΩ resistor below 0.4 V.

These current and voltage levels, together with the value of C_{TIMER} chosen by the user, determine the initial timing cycle time, the fault current limit time, and the hot swap retry duty cycle.

GATE AND TIMER FUNCTIONS DURING A HOT SWAP

During hot insertion of a board onto a live supply rail at VCC, the abrupt application of supply voltage charges the external FET drain/gate capacitance, which can cause an unwanted gate voltage spike. An internal circuit holds GATE low before the internal circuitry wakes up. This reduces the FET current surges substantially at insertion. The GATE pin is also held low during the initial timing cycle and until the ON pin has been taken high to start the hot swap operation.

During hot swap operation, the GATE pin is first pulled up by a 12 μA current source. If the current through the sense resistor reaches the overcurrent fault timing threshold, V_{OCTIM}, a pull-up current of 60 μA on the TIMER pin, is turned on; and this pin starts charging up. At a slightly higher voltage in the sense resistor, the error amplifier servos the GATE pin to maintain a constant current to the load by controlling the voltage across the sense resistor to the linear current limit, V_{LIM}.

A normal hot swap is complete when the board supply capacitors near full charge and the current through the sense resistor drops to eventually reach the level of the board load current. As soon as the current drops below the overcurrent fault timing threshold, the current into the TIMER pin switches from being a 60 μA pull-up to a 100 μA pull-down. The ADM1176 then drives the GATE voltage as high as it can to fully enhance the FET and reduce R_{ON} losses to a minimum.

A hot swap fails if the load current does not drop below the over-current fault timing threshold, V_{OCTIM}, before the TIMER pin has charged up to 1.3 V. In this case the GATE pin is then pulled down with a 2 mA current sink. The GATE pull-down stays on until a hot swap retry starts, which can be forced by deasserting and then reasserting the ON pin. On the ADM1176-1, the device retries automatically after a cool-down period.

The ADM1176 also features a method of protection from sudden load current surges, such as a low impedance fault, when the current seen across the sense resistor may go well beyond the linear current limit. If the fast overcurrent trip threshold, V_{OCFAST}, is exceeded, the 2 mA GATE pull-down is turned on immediately. This pulls the GATE voltage down quickly to enable the ADM1176 to limit the length of the current spike that gets through and also to bring the current through the sense resistor back into linear regulation as quickly as possible. This process protects the backplane supply from sustained overcurrent conditions that can otherwise cause the backplane supply to droop during the overcurrent event.

CALCULATING CURRENT LIMITS AND FAULT CURRENT LIMIT TIME

The nominal linear current limit is determined by a sense resistor connected between the VCC pin and the SENSE pin as given by Equation 1.

$$I_{LIMIT(NOM)} = V_{LIM(NOM)}/R_{SENSE} = 100\ \text{mV}/R_{SENSE} \quad (1)$$

The minimum linear fault current is given by Equation 2.

$$I_{LIMIT(MIN)} = V_{LIM(MIN)}/R_{SENSE(MAX)} = 90\ \text{mV}/R_{SENSE(MAX)} \quad (2)$$

The maximum linear fault current is given by Equation 3.

$$I_{LIMIT(MAX)} = V_{LIM(MAX)}/R_{SENSE(MIN)} = 110\ \text{mV}/R_{SENSE(MIN)} \quad (3)$$

The power rating of the sense resistor should be rated at the maximum linear fault current level.

The minimum overcurrent fault timing threshold current is given by Equation 4.

$$I_{OCTIM(MIN)} = V_{OCTIM(MIN)}/R_{SENSE(MAX)} = 85\ \text{mV}/R_{SENSE(MAX)} \quad (4)$$

The maximum fast overcurrent trip threshold current is given by Equation 5.

$$I_{OCFAST(MAX)} = V_{OCFAST(MAX)}/R_{SENSE(MIN)} = 115\ \text{mV}/R_{SENSE(MIN)} \quad (5)$$

The fault current limit time is the time that a device spends timing an overcurrent fault, and is given by Equation 6.

$$t_{FAULT} \approx 21.7 \times C_{TIMER}\ \text{ms}/\mu\text{F} \quad (6)$$

INITIAL TIMING CYCLE

When VCC is first connected to the backplane supply, the internal supply (Time Point (1) in Figure 30) of the ADM1176 must be charged up. A very short time later (significantly less than 1 ms), the internal supply is fully up and, because the undervoltage lockout voltage has been exceeded at VCC, the device comes out of reset. During this first short reset period, the GATE pin is held down with a 25 mA pull-down current, and the TIMER pin is pulled down with a 100 μA current sink.

The ADM1176 then goes through an initial timing cycle. At Time Point (2), the TIMER pin is pulled high with 5 μA. At Time Point (3), the TIMER reaches the V_{TIMERL} threshold, and the first portion of the initial cycle ends. The 100 μA current source then pulls down the TIMER pin until it reaches 0.2 V at Time Point (4). The initial cycle delay (Time Point (2) to Time Point (4)) is related to C_{TIMER} by Equation 7.

$$t_{INITIAL} \approx 270 \times C_{TIMER}\ \text{ms}/\mu\text{F} \quad (7)$$

When the initial timing cycle terminates, the device is ready to start a hot swap operation (assuming ON pin is asserted). In the example shown in Figure 30, the ON pin is asserted at the same time that V_{CC} is applied, so the hot swap operation starts immediately after Time Point (4). At this point, the FET gate is charged up with a 12 µA current source.

At Time Point (5), the threshold voltage of the FET is reached, and the load current begins to flow. The FET is controlled to keep the sense voltage at 100 mV (this corresponds to a maximum load current level defined by the value of R_{SENSE}).

At Time Point (6), V_{GATE} and V_{OUT} have reached their full potential, and the load current has settled to its nominal level. Figure 31 illustrates the situation where the ON pin is asserted after V_{CC} is applied.

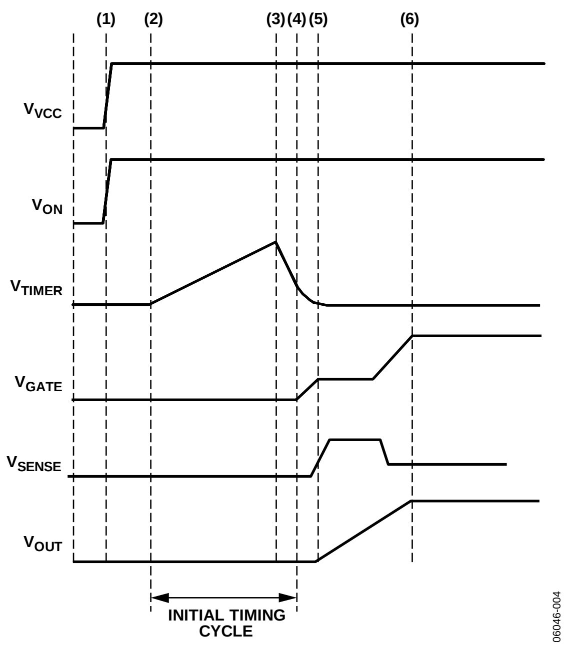


Figure 30. Startup (ON Asserts as Power Is Applied)

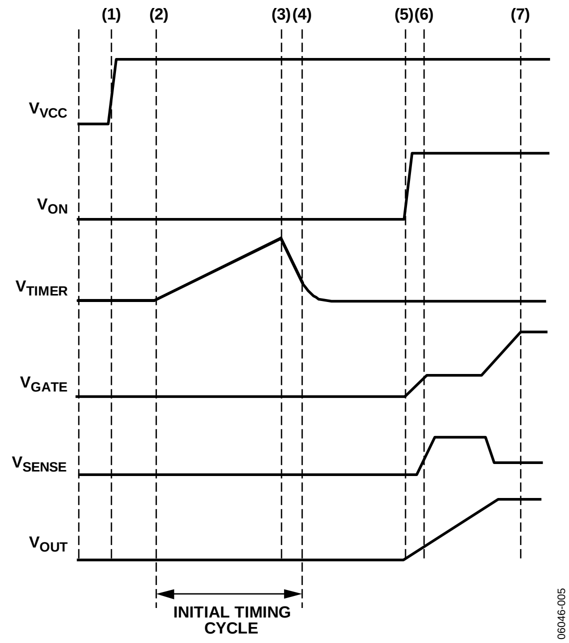


Figure 31. Startup (ON Asserts After Power Is Applied)

HOT SWAP RETRY ON THE ADM1176-1

With the ADM1176-1, the device turns off the FET after an overcurrent fault and then uses the TIMER pin to time a delay before automatically retrying to hot swap.

As with all ADM1176 devices, on overcurrent fault is timed by charging the TIMER cap with a 60 µA pull-up current. When the TIMER pin reaches 1.3 V, the fault current limit time has been reached, and the GATE pin is pulled down. On the ADM1176-1, the TIMER pin is then pulled down with a 2 µA current sink. When the TIMER pin reaches 0.2 V, it automatically restarts the hot swap operation.

The cool-down period is related to C_{TIMER} by Equation 8.

$$t_{COOL} \approx 550 \times C_{TIMER} \text{ ms/µF} \quad (8)$$

Thus, the retry duty cycle is given by Equation 9.

$$t_{FAULT}/(t_{COOL} + t_{FAULT}) \times 100\% = 3.8\% \quad (9)$$

VOLTAGE AND CURRENT READBACK

In addition to providing hot swap functionality, the ADM1176 contains the components to allow voltage and current readback over an Inter-IC (I^2C) bus. The voltage output of the current sense amplifier and the voltage on the VCC pin are fed into a 12-bit ADC via a multiplexer. The device can be instructed to convert voltage and/or current at any time during operation via an I^2C command. When all conversions are complete, the voltage and/or current values can be read out to 12-bit accuracy in two or three bytes.

SERIAL BUS INTERFACE

Control of the ADM1176 is carried out via the I^2C bus. This interface is compatible with fast mode I^2C (400 kHz maximum). The ADM1176 is connected to this bus as a slave device under the control of a master device.

IDENTIFYING THE ADM1176 ON THE I²C BUS

The ADM1176 has a 7-bit serial bus slave address. When the device powers up, it does so with a default serial bus address. The three MSBs of the address are set to 100, and the four LSBs are determined by the state of the A0 pin and the A1 pin. There are 16 different configurations available on the A0 pin and the A1 pin that correspond to 16 different I^2C addresses for the four LSBs (see Table 5). This scheme allows sixteen ADM1176 devices to operate on a single I^2C bus.

Table 5. Setting I²C Addresses via the A0 Pin and the A1 Pin

A0 Configuration	A1 Configuration	Address
Low state	Low state	0x80
Low state	Resistor to GND	0x88
Low state	Floating	0x90
Low state	High state	0x98
Resistor to GND	Low state	0x82
Resistor to GND	Resistor to GND	0x8A
Resistor to GND	Floating	0x92
Resistor to GND	High state	0x9A
Floating	Low state	0x84
Floating	Resistor to GND	0x8C
Floating	Floating	0x94
Floating	High state	0x9C
High state	Low state	0x86
High state	Resistor to GND	0x8E
High state	Floating	0x96
High state	High state	0x9E

GENERAL I²C TIMING

Figure 32 and Figure 33 show timing diagrams for general read and write operations using the I^2C. The I^2C specification defines conditions for different types of read and write operations, which are discussed later. The general I^2C protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line, SDA, while the serial clock line SCL remains high. This indicates that a data stream follows. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit slave address (MSB first) plus an $R/\overline{W}$ bit that determines the direction of the data transfer; that is, whether data is to be written to or read from the slave device (0 = write, 1 = read).

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit, and holding it low during the high period of this clock pulse. All other devices on the bus now remain idle while the selected device waits for data to be read from it or written to it. If the $R/\overline{W}$ bit is 0, the master writes to the slave device. If the $R/\overline{W}$ bit is 1, the master reads from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high can be interpreted as a stop signal.

   If the operation is a write operation, the first data byte after the slave address is a command byte. This tells the slave device what to expect next. It can be an instruction, such as telling the slave device to expect a block write; or it can be a register address that tells the slave where subsequent data is to be written.

   Because data can flow in only one direction, as defined by the $R/\overline{W}$ bit, it is not possible to send a command to a slave device during a read operation. Before doing a read operation, it may first be necessary to do a write operation to tell the slave what sort of read operation to expect and/or the address from which data is to be read.

3. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device releases the SDA line during the low period before the ninth clock pulse, but the slave device does not pull it low. This is known as a no acknowledge. The master then takes the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a stop condition.

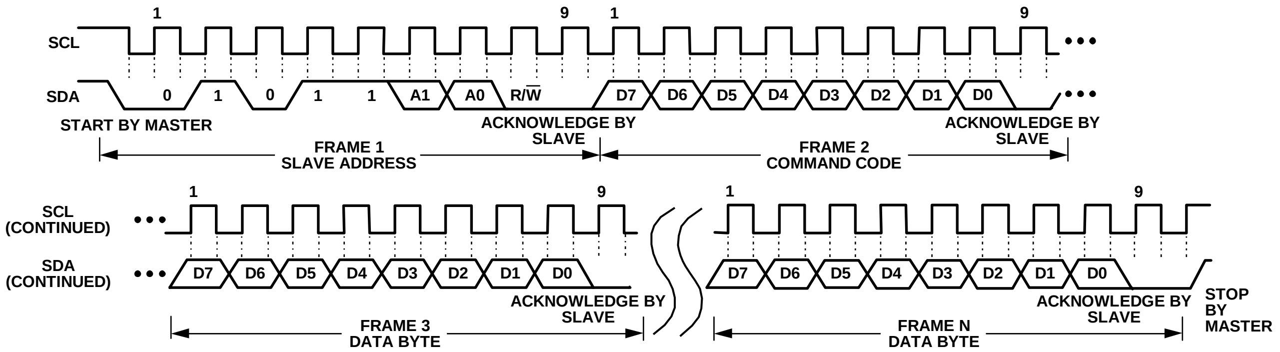


Figure 32. General I²C Write Timing Diagram

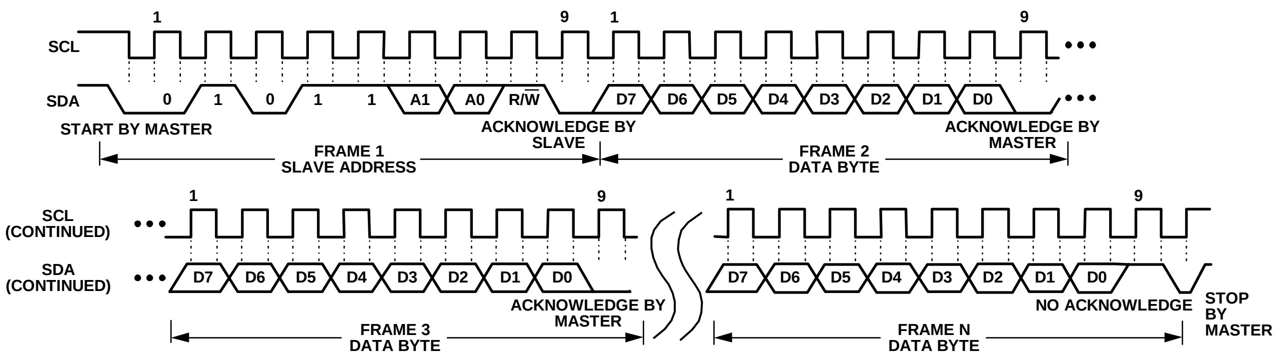


Figure 33. General I²C Read Timing Diagram

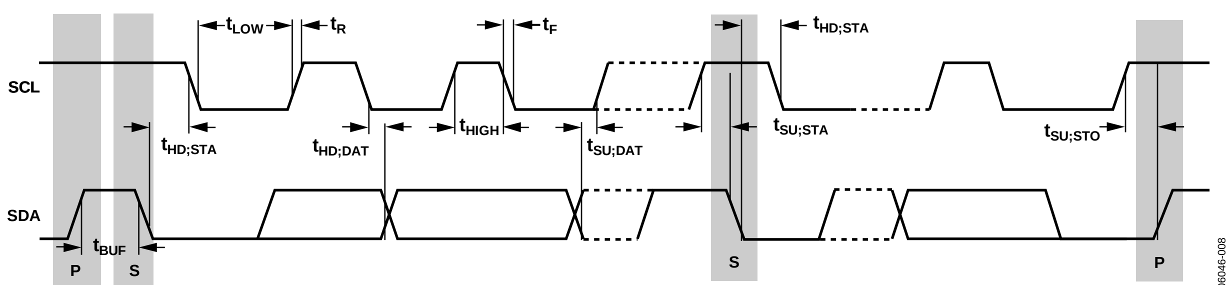


Figure 34. Serial Bus Timing Diagram

WRITE AND READ OPERATIONS

The I^2C specification defines several protocols for different types of read and write operations. The operations used in the ADM1176 are discussed in the sections that follow. Table 6 shows the abbreviations used in the command diagrams.

Table 6. I^2C Abbreviations

Abbreviation	Condition
S	Start
P	Stop
R	Read
W	Write
A	Acknowledge
N	No acknowledge

QUICK COMMAND

The quick command operation allows the master to check if the slave is present on the bus, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address, followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.

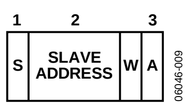


Figure 35. Quick Command

WRITE COMMAND BYTE

In the write command byte operation, the master device sends a command byte to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address, followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends the command byte. The command byte is identified by an MSB = 0. An MSB = 1 indicates an extended register write (see the Write Extended Byte section).
5. The slave asserts an acknowledge on SDA.
6. The master asserts a stop condition on SDA to end the transaction.

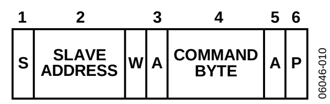


Figure 36. Write Command Byte

The seven LSBs of the command byte are used to configure and control the ADM1176. Table 7 provides details of the function of each bit.

Table 7. Command Byte Operations

Bit	Default	Name	Function
C0	0	V_CONT	Set to convert voltage continuously. If readback is attempted before the first conversion is complete, the ADM1176 asserts an acknowledge and returns all 0s in the returned data.
C1	0	V_ONCE	Set to convert voltage once. Self-clears. I^2C asserts a no acknowledge on attempted reads until the ADC conversion is complete.
C2	0	I_CONT	Set to convert voltage continuously. If readback is attempted before the first conversion is complete, the ADM1176 asserts an acknowledge and returns all 0s in the returned data.
C3	0	I_ONCE	Set to convert current once. Self-clears. I^2C asserts a no acknowledge on attempted reads until the ADC conversion is complete.
C4	0	VRANGE	Selects different internal attenuation resistor networks for voltage readback. A 0 in C4 selects a 14:1 voltage divider. A 1 in C4 selects a 7:2 voltage divider. With an ADC full scale of 1.902 V, the voltage at the VCC pin for an ADC full-scale result is 26.35 V for VRANGE = 0 and 6.65 V for VRANGE = 1.
C5	0	N/A	Unused.
C6	0	STATUS_RD	Status read. When this bit is set, the data byte read back from the ADM1176 is the STATUS byte. This contains the status of the device alerts. See Table 15 for full details of the STATUS byte.

WRITE EXTENDED BYTE

In the write extended byte operation, the master device writes to one of the three extended registers of the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address, followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends the register address byte. The MSB of this byte is set to 1 to indicate an extended register write. The two LSBs indicate which of the three extended registers are to be written to (see Table 8). All other bits should be set to 0.
5. The slave asserts an acknowledge on SDA.
6. The master sends the command byte. The command byte is identified by MSB = 0. MSB = 1 indicates an extended register write.
7. The slave asserts an acknowledge on SDA.
8. The master asserts a stop condition on SDA to end the transaction.

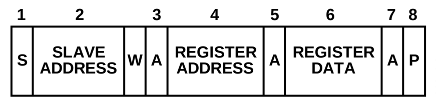


Figure 37. Write Extended Byte

Table 9, Table 10, and Table 11 give details of each extended register.

Table 8. Extended Register Addresses

A6	A5	A4	A3	A2	A1	A0	Extended Register
0	0	0	0	0	0	1	ALERT_EN
0	0	0	0	0	1	0	ALERT_TH
0	0	0	0	0	1	1	CONTROL

Table 9. ALERT_EN Register Operations

Bit	Default	Name	Function
0	0	EN_ADC_OC1	Enabled if a single ADC conversion on the I channel has exceeded the threshold set in the ALERT_TH register.
1	0	EN_ADC_OC4	Enabled if four consecutive ADC conversions on the I channel have exceeded the threshold set in the ALERT_TH register.
2	1	EN_HS_ALERT	Enabled if the hot swap has either latched off or entered a cool down cycle because of an overcurrent event.
3	0	EN_OFF_ALERT	Enables an alert if the HS operation is turned off by a transition that deasserts the ON pin or by an operation that writes the SWOFF bit high.
4	0	CLEAR	Clears the ON_ALERT, HS_ALERT and ADC_ALERT status bits in the STATUS register. These may immediately reset if the source of the alert has not been cleared or disabled with the other bits in this register. This bit self-clears to 0 after the STATUS register bits have been cleared.

Table 10. ALERT_TH Register Operations

Bit	Default	Function
7:0	FF	The ALERT_TH register sets the current level at which an alert occurs. Defaults to ADC full scale. The ALERT_TH 8-bit number corresponds to the top eight bits of the current channel data.

Table 11. CONTROL Register Operations

Bit	Default	Name	Function
0	0	SWOFF	Forces hot swap off. Equivalent to deasserting the ON pin.

READ VOLTAGE AND/OR CURRENT DATA BYTES

The ADM1176 can be set up to provide information in three different ways (see the Write Command Byte section). Depending on how the device is configured, the following data can be read out of the device after a conversion (or conversions).

Voltage and Current Readback

The ADM1176 digitizes both voltage and current. Three bytes are read out of the device in the format shown in Table 12.

Table 12. Voltage and Current Readback Format

Byte	Contents	B7	B6	B5	B4	B3	B2	B1	B0
1	Voltage MSBs	V11	V10	V9	V8	V7	V6	V5	V4
2	Current MSBs	I11	I10	I9	I8	I7	I6	I5	I4
3	LSBs	V3	V2	V1	V0	I3	I2	I1	I0

Voltage Readback

The ADM1176 digitizes voltage only. Two bytes are read out of the device in the format shown in Table 13.

Table 13. Voltage Only Readback Format

Byte	Contents	B7	B6	B5	B4	B3	B2	B1	B0
1	Voltage MSBs	V11	V10	V9	V8	V7	V6	V5	V4
2	Voltage LSBs	V3	V2	V1	V0	0	0	0	0

Current Readback

The ADM1176 digitizes current only. Two bytes are read out of the device in the format shown in Table 14.

Table 14. Current Only Readback Format

Byte	Contents	B7	B6	B5	B4	B3	B2	B1	B0
1	Current MSBs	I11	I10	I9	I8	I7	I6	I5	I4
2	Current LSBs	I3	I2	I1	I0	0	0	0	0

The following series of events occur when the master receives three bytes (voltage and current data) from the slave device:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address, followed by the read bit (high).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master receives the first data byte.
5. The master asserts an acknowledge on SDA.
6. The master receives the second data byte.
7. The master asserts an acknowledge on SDA.
8. The master receives the third data byte.
9. The master asserts a no acknowledge on SDA.
10. The master asserts a stop condition on SDA, and the transaction ends.

For cases where the master is reading voltage only or current only, only two data bytes are read. Step 7 and Step 8 are not required.

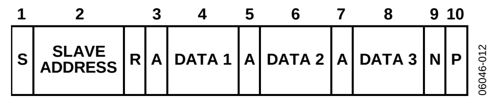


Figure 38. Three-Byte Read from ADM1176

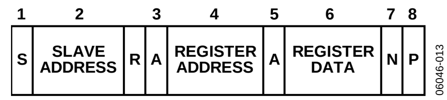


Figure 39. Two-Byte Read from ADM1176

Converting ADC Codes to Voltage and Current Readings

The following equations can be used to convert ADC codes representing voltage and current from the ADM1175 12-bit ADC into actual voltage and current values.

$$Voltage = (V_{FULLSCALE}/4096) \times Code$$

where:
$V_{FULLSCALE}$ = 6.65 (7:2 range) or 26.35 (14:1 range).
Code is the ADC voltage code read from the device (Bit V0 to V11).

$$Current = ((I_{FULLSCALE}/4096) \times Code)/Sense\ Resistor$$

where:
$I_{FULLSCALE}$ = 105.84 mV.
Code is the ADC current code read from the device (Bit I0 to Bit I11).

Read Status Register

A single register of status data can also be read from the ADM1176.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address, followed by the read bit (high).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master receives the status byte.
5. The master asserts an acknowledge on SDA.

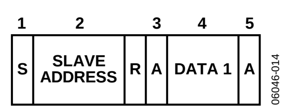


Figure 40. Status Read from ADM1176

Table 15 shows the ADM1176 status registers in detail. Note that Bit 1, Bit 3, and Bit 5 are cleared by writing to Bit 4 of the ALERT_EN register (CLEAR).

Table 15. Status Byte Operations

Bit	Name	Function
0	ADC_OC	An ADC-based overcurrent comparison has been detected on the last three conversions
1	ADC_ALERT	An ADC-based overcurrent trip has happened, which has caused the alert. Cleared by writing to Bit 4 of the ALERT_EN register.
2	HS_OC	The hot swap is off due to an analog overcurrent event. On parts that latch off, this is the same as the HS_ALERT status bit (if EN_HS_ALERT = 1). On the retry parts, this indicates the current state: a 0 may indicate that the data was read during a period when the device was retrying, or that it has successfully hot swapped by retrying after at least one overcurrent timeout.
3	HS_ALERT	The hot swap has failed since the last time this was reset. Cleared by writing to Bit 4 of the ALERT_EN register.
4	OFF_STATUS	The state of the ON pin. Set to 1 if the input pin is deasserted. Can also be set to 1 by writing to the SWOFF bit of the CONTROL register.
5	OFF_ALERT	An alert has been caused by either the ON pin or the SWOFF bit. Cleared by writing to Bit 4 of the ALERT_EN register.

APPLICATIONS WAVEFORMS

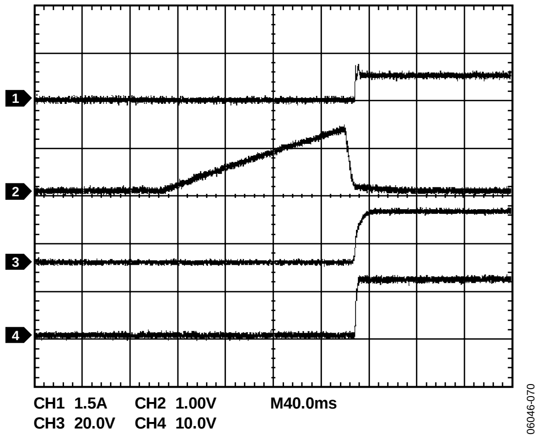


Figure 41. Inrush Current Control into 220 µF Load
(CH1 = I_{LOAD}, CH2 = V_{TIMER}, CH3 = V_{GATE}, CH4 = V_{OUT})

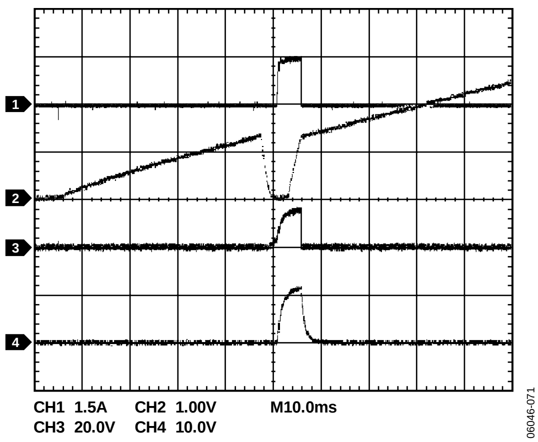


Figure 42. Overcurrent Condition at Startup (ADM1176-1 Model)
(CH1 = I_{LOAD}, CH2 = V_{TIMER}, CH3 = V_{GATE}, CH4 = V_{OUT})

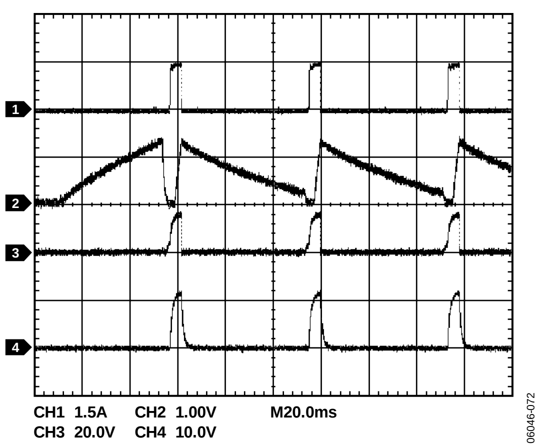


Figure 43. Overcurrent Condition at Startup (ADM1176-2 Model)
(CH1 = I_{LOAD}, CH2 = V_{TIMER}, CH3 = V_{GATE}, CH4 = V_{OUT})

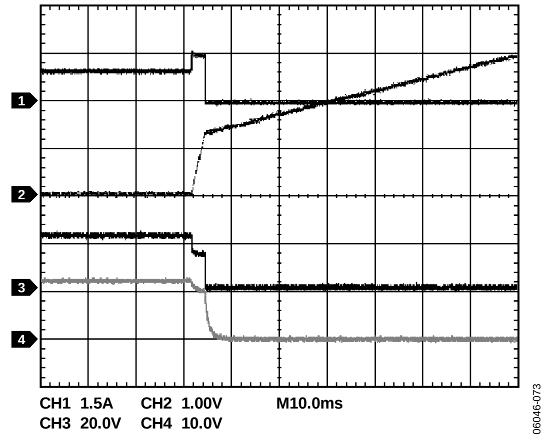


Figure 44. Overcurrent Condition During Operation (ADM1176-1 Model)
(CH1 = I_{LOAD}, CH2 = V_{TIMER}, CH3 = V_{GATE}, CH4 = V_{OUT})

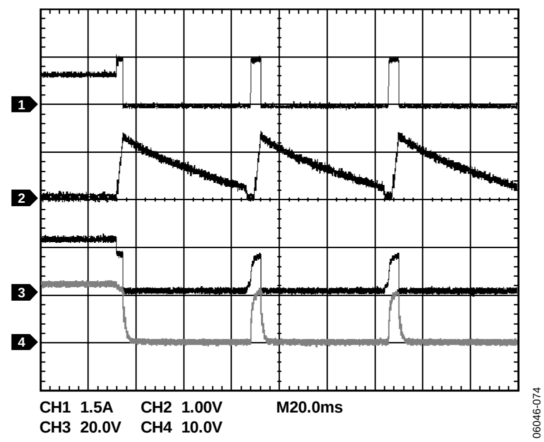


Figure 45. Overcurrent Condition During Operation (ADM1176-2 Model)
(CH1 = I_{LOAD}, CH2 = V_{TIMER}, CH3 = V_{GATE}, CH4 = V_{OUT})

KELVIN SENSE RESISTOR CONNECTION

When using a low value sense resistor for high current measurement, the problem of parasitic series resistance may arise. The lead resistance can be a substantial fraction of the rated resistance, making the total resistance a function of lead length. This problem can be avoided by using a Kelvin sense connection. This type of connection separates the current path through the resistor and the voltage drop across the resistor. Figure 46 shows the correct way to connect the sense resistor between the VCC pin and the SENSE pin of the ADM1176.

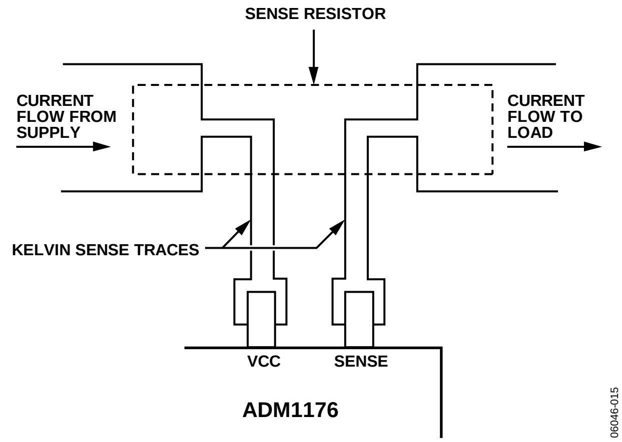
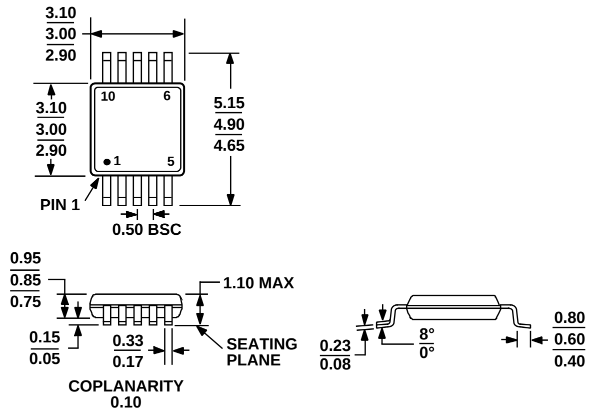


Figure 46. Kelvin Sense Connections

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 47. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Hot Swap Retry Option	Temperature Range	Package Description	Package Option	Branding
ADM1176-1ARMZ-R7[1]	Automatic Retry Version	−40°C to +85°C	10-Lead MSOP	RM-10	M5U
ADM1176-2ARMZ-R7[1]	Latched Off Version	−40°C to +85°C	10-Lead MSOP	RM-10	M5V
EVAL-ADM1176EBZ[1]			Evaluation Board		

[1] Z = Pb-free part.

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