450 MHz to 6000 MHz Crest Factor Detector

ADL5502

FEATURES

- True rms response detector
- Envelope peak hold output
- Excellent temperature stability
- ±0.25 dB rms detection accuracy vs. temperature
- ±0.25 dB envelope detection accuracy vs. temperature; over the top 25 dB of the input range
- Over 35 dB input power dynamic range, inclusive of crest factor
- RF bandwidths from 450 MHz to 6 GHz
- Envelope bandwidths of 10 MHz
- 500 Ω input impedance
- Single-supply operation: 2.5 V to 3.3 V
- Low power: 3 mA at 3 V supply
- RoHS-compliant part

APPLICATIONS

- Power and envelope measurement of W-CDMA, CDMA2000, and QPSK-/QAM-based OFDM, and other complex modulation waveforms
- RF transmitter or receiver power and envelope measurement

FUNCTIONAL BLOCK DIAGRAM

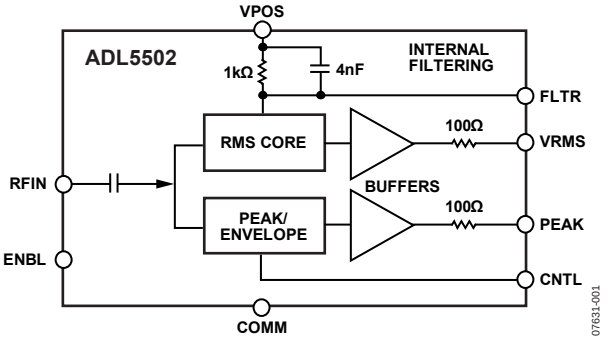

Figure 1.

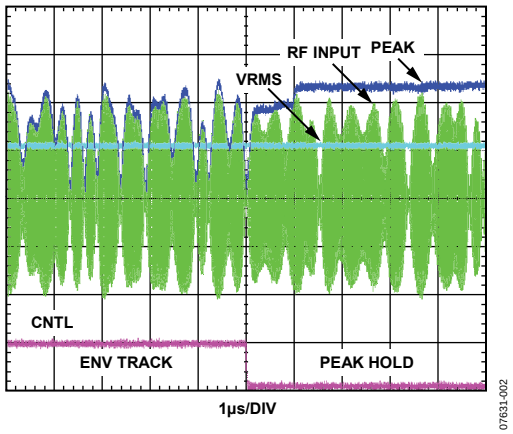

Figure 2.

GENERAL DESCRIPTION

The ADL5502 is a mean-responding (true rms) power detector in combination with an envelope detector to accurately determine the crest factor of a modulated signal. It can be used in high frequency receiver and transmitter signal chains from 450 MHz to 6 GHz with envelope bandwidths over 10 MHz. Requiring only a single supply between 2.5 V and 3.3 V, the detector draws less than 3 mA. The input is internally ac-coupled and has a nominal input impedance of 500 Ω.

The rms output is a linear-responding dc voltage with a conversion gain of 1.8 V/V rms at 900 MHz. The peak envelope output with a conversion gain of 1.2 V/V is toggled for peak hold with less than 1% output voltage droop in over 1 ms.

The ADL5502 is a highly accurate, easy to use means of determining the rms and peak to the average value of complex waveforms. It can be used for crest factor measurements of both simple and complex waveforms but is particularly useful for measuring high crest factor (high peak-to-rms ratio) signals, such as W-CDMA, CDMA2000, and QPSK-/QAM-based OFDM waveforms. The peak hold function allows the capture of short peaks in the envelope with lower sampling rate ADCs.

The crest factor detector operates from −40°C to +85°C and is available in an 8-ball, 1.5 mm × 1.5 mm wafer-level chip scale package. It is fabricated on a high f_T silicon BiCMOS process.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

1/11—Rev. 0 to Rev. A

Changes to Output Intercept Parameters, Table 1 ... 3
Changes to Figure 34 ... 13

10/08—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 3.0 V, C_{FLTR} = 10 nF, C_{OUT} = open, light condition ≤ 600 lux, 75 Ω input termination resistor, unless otherwise noted.

Table 1.

Parameter	Test Conditions	Min	Typ	Max	Unit
FREQUENCY RANGE	Input RFIN	450		6000	MHz
RF INPUT (f = 900 MHz)	Input RFIN to output VRMS and PEAK				
Input Impedance	No termination		330||1.04		Ω||pF
RMS CONVERSION	Input RFIN to output VRMS				
Dynamic Range	CW input, −40°C < T_A < +85°C				
±0.25 dB Error [1]			27		dB
±1 dB Error[1]			33		dB
±2 dB Error[2]			29		dB
Maximum Input Level	±0.25 dB error[2]		12		dBm
Minimum Input Level	±1 dB error[2]		−15		dBm
Conversion Gain	VRMS = (Gain × V_{IN}) + Intercept		1.89		V/V rms
Output Intercept[3]			0.014		V
Output Voltage, High Power In	P_{IN} = 5 dBm, 400 mV rms		0.762		V
Output Voltage, Low Power In	P_{IN} = −15 dBm, 40 mV rms		0.086		V
ENVELOPE CONVERSION	Input RFIN to output PEAK				
Dynamic Range	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[1]			27		dB
±1 dB Error[1]			33		dB
±2 dB Error[2]			30		dB
Maximum Input Level	±0.25 dB error[2]		12		dBm
Minimum Input Level	±1 dB error[2]		−15		dBm
Conversion Gain	PEAK = (Gain × V_{IN}) + Intercept		1.27		V/V rms
Output Intercept[3]			0.014		V
Output Voltage, High Power In	P_{IN} = 5 dBm, 400 mV rms		0.516		V
Output Voltage, Low Power In	P_{IN} = −15 dBm, 40 mV rms		0.062		V

Parameter	Test Conditions	Min	Typ	Max	Unit
RF INPUT (f = 1900 MHz)	Input RFIN to output VRMS and PEAK				
Input Impedance	No termination		238||0.90		Ω||pF
RMS CONVERSION	Input RFIN to output VRMS				
Dynamic Range	CW input, −40°C < T_A < +85°C				
±0.25 dB Error [1]			27		dB
±1 dB Error[1]			32		dB
±2 dB Error[2]			30		dB
Maximum Input Level	±0.25 dB error[2]		12		dBm
Minimum Input Level	±1 dB error[2]		−15		dBm
Conversion Gain	VRMS = (Gain × V_{IN}) + Intercept		1.75		V/V rms
Output Intercept[3]			0.010		V
Output Voltage, High Power In	P_{IN} = 5 dBm, 400 mV rms		0.700		V
Output Voltage, Low Power In	P_{IN} = −15 dBm, 40 mV rms		0.079		V
ENVELOPE CONVERSION	Input RFIN to output PEAK				
Dynamic Range	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[1]			26		dB
±1 dB Error[1]			32		dB
±2 dB Error[2]			30		dB
Maximum Input Level	±0.25 dB error[2]		12		dBm
Minimum Input Level	±1 dB error[2]		−16		dBm
Conversion Gain	PEAK = (Gain × V_{IN}) + Intercept		1.17		V/V rms
Output Intercept[3]			0.011		V
Output Voltage, High Power In	P_{IN} = 5 dBm, 400 mV rms		0.472		V
Output Voltage, Low Power In	P_{IN} = −15 dBm, 40 mV rms		0.057		V
RF INPUT (f = 3500 MHz)	Input RFIN to output VRMS and PEAK				
Input Impedance	No termination		232||0.39		Ω||pF
RMS CONVERSION	Input RFIN to output VRMS				
Dynamic Range	CW input, −40°C < T_A < +85°C				
±1 dB Error[1]			32		dB
±2 dB Error[2]			30		dB
Maximum Input Level	±0.25 dB error[2]		7		dBm
Minimum Input Level	±1 dB error[2]		−16		dBm
Conversion Gain	VRMS = (Gain × V_{IN}) + Intercept		1.52		V/V rms
Output Intercept[3]			0.002		V
Output Voltage, High Power In	P_{IN} = 5 dBm, 400 mV rms		0.594		V
Output Voltage, Low Power In	P_{IN} = −15 dBm, 40 mV rms		0.065		V
ENVELOPE CONVERSION	Input RFIN to output PEAK				
Dynamic Range	CW input, −40°C < T_A < +85°C				
±1 dB Error[1]			32		dB
±2 dB Error[2]			31		dB
Maximum Input Level	±0.25 dB error[2]		7		dBm
Minimum Input Level	±1 dB error[2]		−16		dBm
Conversion Gain	PEAK = (Gain × V_{IN}) + Intercept		1.02		V/V rms
Output Intercept[3]			0.005		V
Output Voltage, High Power In	P_{IN} = 5 dBm, 400 mV rms		0.403		V
Output Voltage, Low Power In	P_{IN} = −15 dBm, 40 mV rms		0.049		V

Parameter	Test Conditions	Min	Typ	Max	Unit
VRMS OUTPUT	Pin VRMS				
Maximum Output Voltage	V_S = 3.0 V, R_{LOAD} ≥ 10 kΩ		2.4		V
Output Offset	No signal at RFIN		15	100	mV
Pulse Response Time	10 dB step, 10% to 90% of settling level, no filter capacitor		15		µs
Available Output Current			3		mA
PEAK OUTPUT	Pin PEAK				
Maximum Output Voltage	V_S = 3.0 V, R_{LOAD} ≥ 10 kΩ		1.5		V
Output Offset	No signal at RFIN		14	100	mV
Available Output Current			3		mA
Envelope Modulation Bandwidth		5	10		MHz
Peak Hold Time	1% voltage drop from last peak, CNTL = high		600		µs
CONTROL INTERFACE					
Logic Level to Track Envelope, High	2.5 V ≤ V_S ≤ 3.3 V, −40°C < T_A < +85°C	1.8		V_{POS}	V
Input Current when High	2.5 V at CNTL, −40°C ≤ T_A ≤ +85°C		0.05	0.1	µA
Logic Level for Peak Hold Condition, Low	2.5 V ≤ V_S ≤ 3.3 V, −40°C < T_A < +85°C	−0.5		+0.5	V
Enable Time	0 dBm at RFIN, CNTL held high for >1 µs		<0.1		µs
ENABLE INTERFACE	Pin ENBL				
Logic Level to Enable Power, High Condition	2.5 V ≤ V_S ≤ 3.3 V, −40°C < T_A < +85°C	1.8		V_{POS}	V
Input Current when High	2.5 V at ENBL, −40°C ≤ T_A ≤ +85°C		0.05	0.1	µA
Logic Level to Disable Power, Low Condition	2.5 V ≤ V_S ≤ 3.3 V, −40°C < T_A < +85°C	−0.5		+0.5	V
Power-Up Response Time[4]	C_{FLTR} = open, 0 dBm at RFIN		12		µs
	C_{FLTR} = 10 nF, 0 dBm at RFIN		10		µs
POWER SUPPLIES					
Operating Range	−40°C < T_A < +85°C	2.5		3.3	V
Quiescent Current	No signal at RFIN,[5] ENBL high input condition		3.0		mA
Disable Current[6]	ENBL input low condition, CNTL in high condition		<1	1	µA

[1] Error referred to delta from 25°C response, see Figure 10, Figure 11, and Figure 12 for VRMS and Figure 16, Figure 17, and Figure 18 for PEAK.
[2] Error referred to best-fit line at 25°C, see Figure 13, Figure 14, and Figure 15 for VRMS and Figure 19, Figure 20, and Figure 21 for PEAK.
[3] Calculated using linear regression.
[4] The response time is measured from 10% to 90% of settling level, see Figure 41, Figure 42, and Figure 43.
[5] Supply current is input level dependant, see Figure 37.
[6] Guaranteed but not tested; limits are specified at six sigma levels.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, V_S	3.5 V
VRMS, PEAK, ENBL, CNTL	0 V, V_S
RFIN	1.25 V rms
Equivalent Power, re: 50 Ω	15 dBm
Internal Power Dissipation	200 mW
θ_{JA} (WLCSP)	200°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

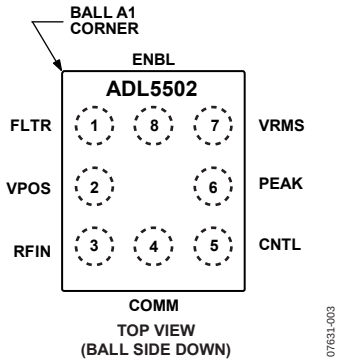

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FLTR	Modulation Filter Pin. Connection for an external capacitor to lower the corner frequency of the modulation filter.
2	VPOS	Supply Voltage Pin. Operational range 2.5 V to 3.3 V.
3	RFIN	Signal Input Pin. Internally ac-coupled after internal termination resistance. Nominal 500 Ω input impedance.
4	COMM	Device Ground Pin.
5	CNTL	Control Pin. Connect pin to ground for peak-hold mode. Connect pin to V_S for reset mode (tracking envelope). To measure the peak of a waveform, the control pin must be briefly set to high (reset mode for >1 µs) to start at a known state.
6	PEAK	Envelope Peak Output. Voltage output for peak-hold function, with limited current drive capability. The output has an internal 100 Ω series resistance. Low capacitance loads are recommended to allow for envelope tracking and fast response time.
7	VRMS	RMS Output Pin. Rail-to-rail voltage output with limited current drive capability. The output has an internal 100 Ω series resistance. High resistive loads and low capacitance loads are recommended to preserve output swing and allow fast response.
8	ENBL	Enable Pin. Connect pin to V_S for normal operation. Connect pin to ground for disable mode.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = 3.0 V, C_{FLTR} = 10 nF, C_{OUT} = open, light condition ≤ 600 lux, 75 Ω input termination resistor, colors: black = +25°C, blue = −40°C, red = +85°C, unless otherwise noted.

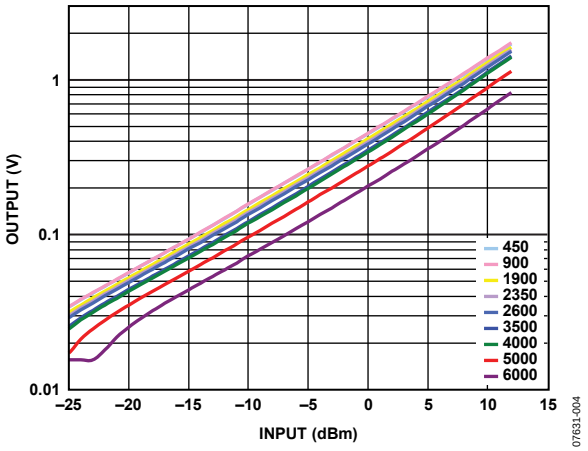

Figure 4. VRMS Output vs. Input Level, 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2600 MHz, 3500 MHz, 4000 MHz, 5000 MHz, 6000 MHz, Supply 3.0 V

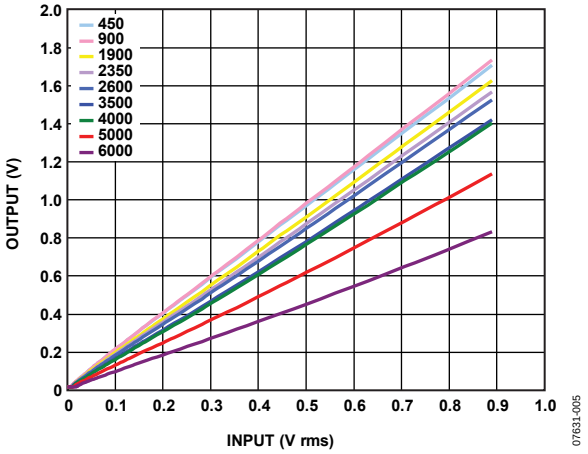

Figure 5. VRMS Output vs. Input Level (Linear Scale), 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2600 MHz, 3500 MHz, 4000 MHz, 5000 MHz, 6000 MHz, Supply 3.0 V

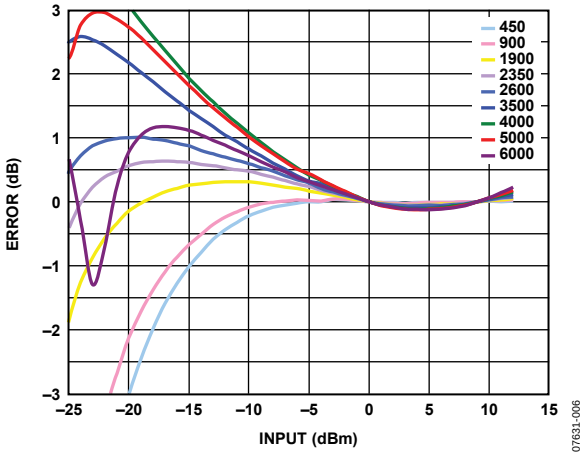

Figure 6. VRMS Linearity Error vs. Input Level, 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2600 MHz, 3500 MHz, 4000 MHz, 5000 MHz, 6000 MHz, Supply 3.0 V

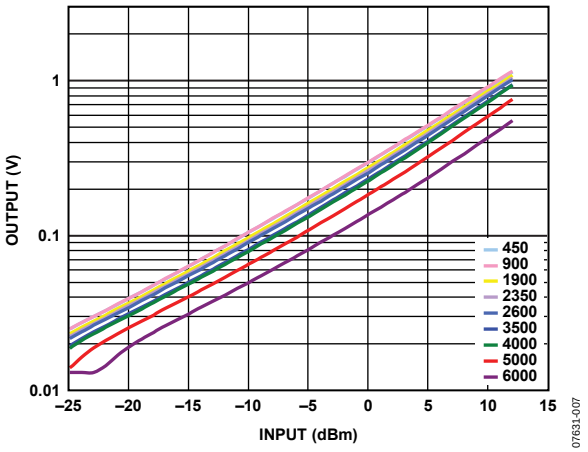

Figure 7. PEAK Output vs. Input Level, 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2600 MHz, 3500 MHz, 4000 MHz, 5000 MHz, 6000 MHz, Supply 3.0 V

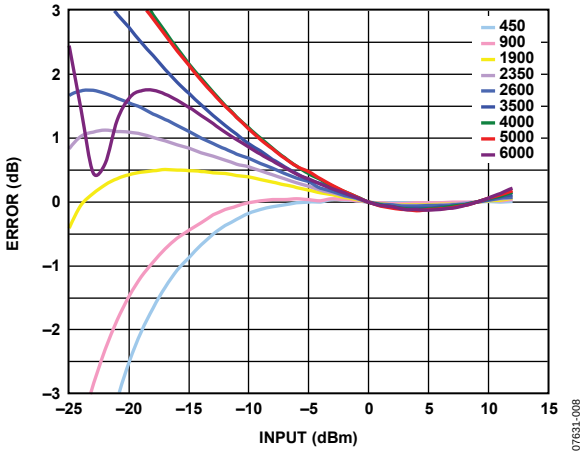

Figure 8. PEAK Linearity Error vs. Input Level, 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2600 MHz, 3500 MHz, 4000 MHz, 5000 MHz, 6000 MHz, Supply 3.0 V

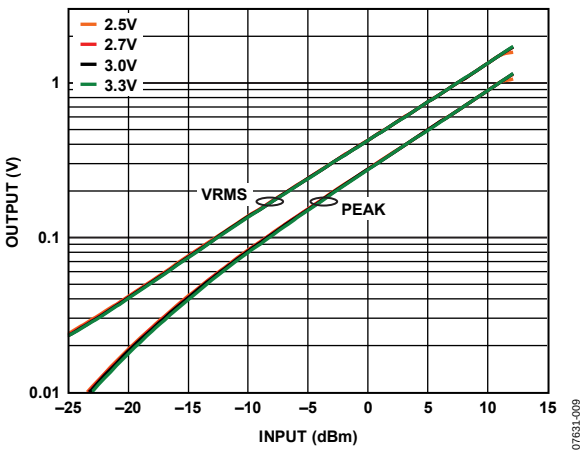

Figure 9. VRMS and PEAK Outputs vs. Input Level, 2.5 V, 2.7 V, 3.0 V, 3.3 V, and 3.5 V Supplies, 900 MHz Frequency

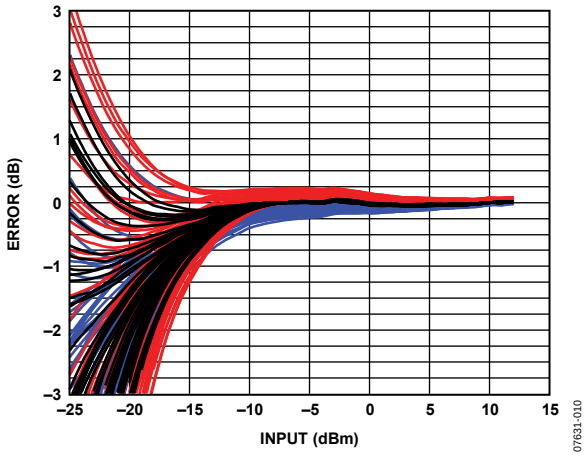

Figure 10. VRMS Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C, 900 MHz Frequency

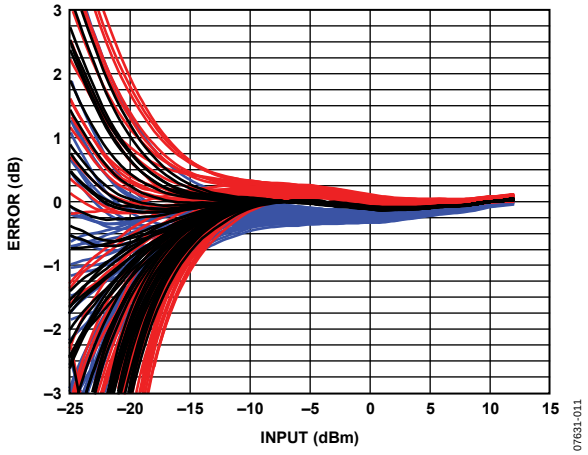

Figure 11. VRMS Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C, 1900 MHz Frequency

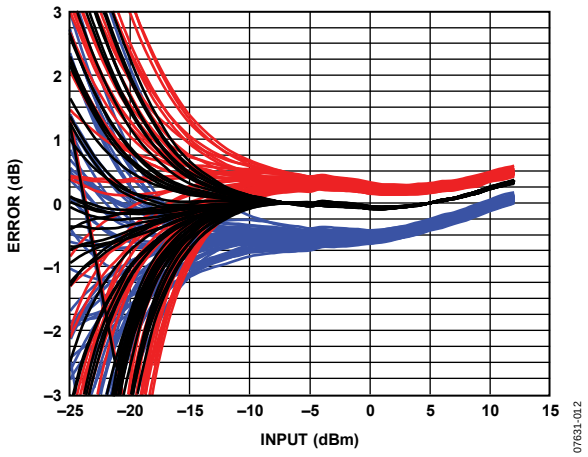

Figure 12. VRMS Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C, Frequency 3500 MHz

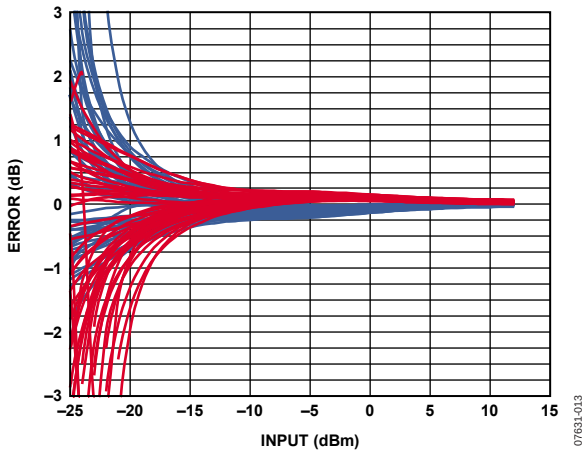

Figure 13. VRMS Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C, 900 MHz Frequency

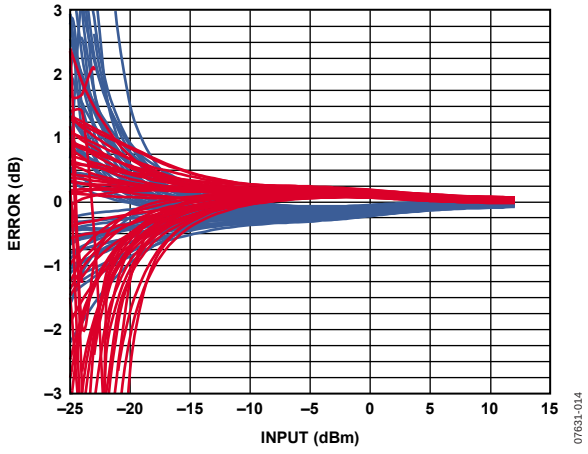

Figure 14. VRMS Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C, 1900 MHz Frequency

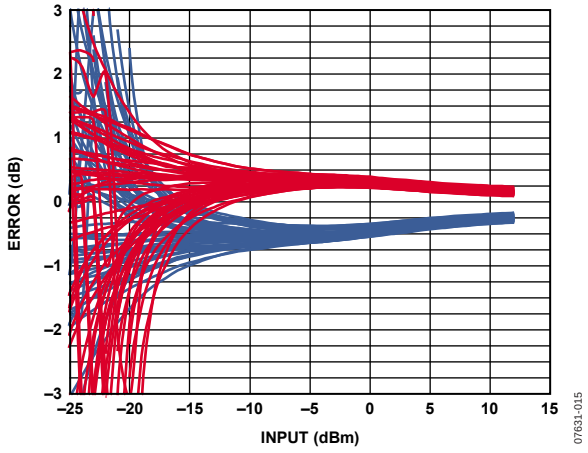

Figure 15. VRMS Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C, 3500 MHz Frequency

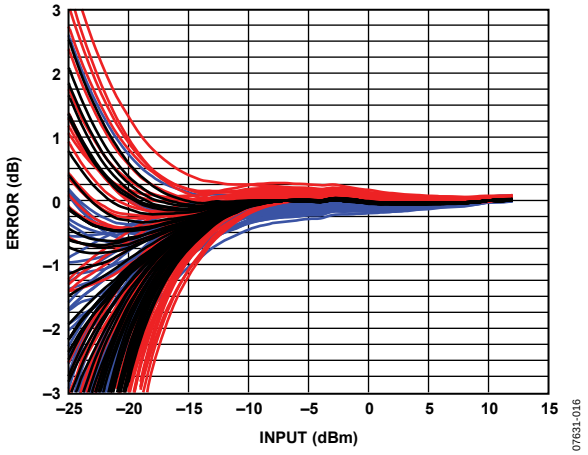

Figure 16. PEAK Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C, 900 MHz Frequency

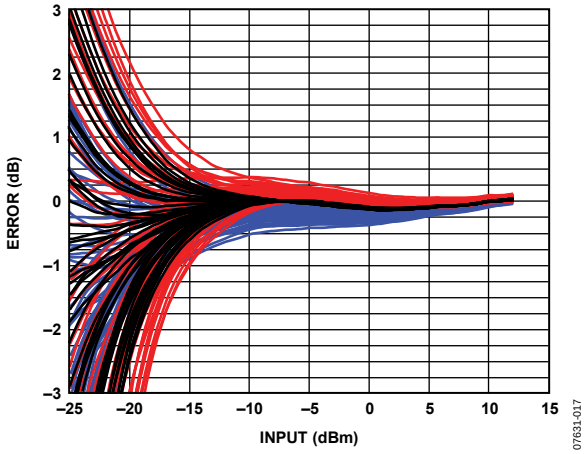

Figure 17. PEAK Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C, 1900 MHz Frequency

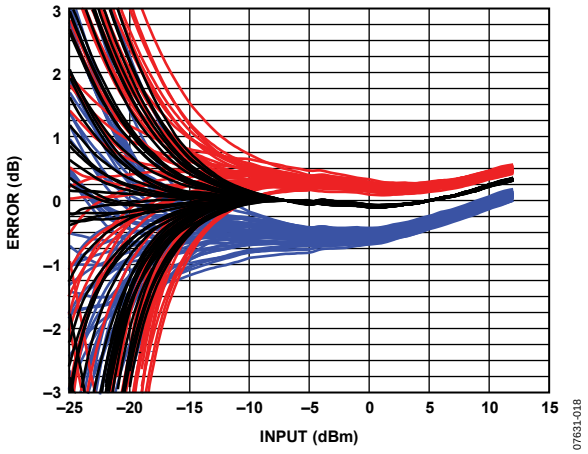

Figure 18. PEAK Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C, 3500 MHz Frequency

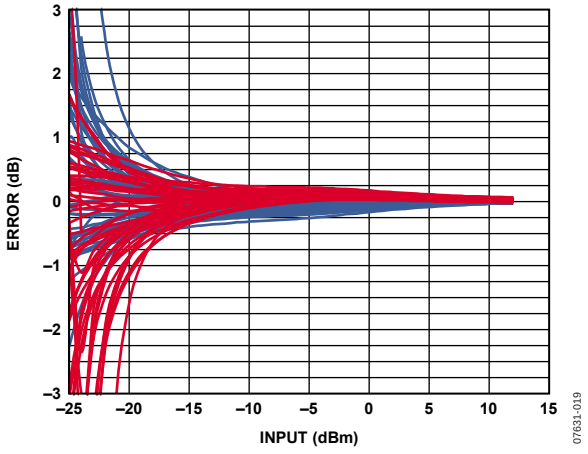

Figure 19. PEAK Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C, 900 MHz Frequency

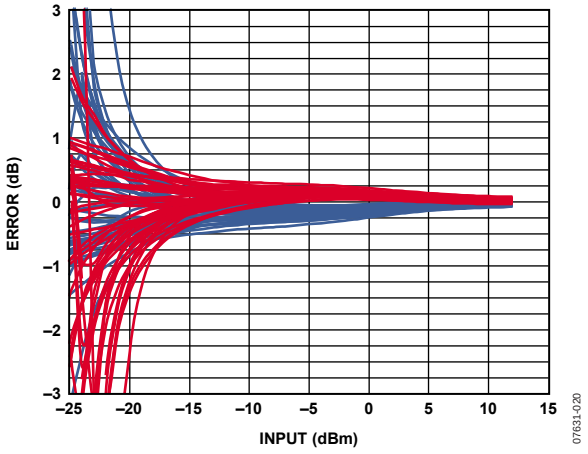

Figure 20. PEAK Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C, 1900 MHz Frequency

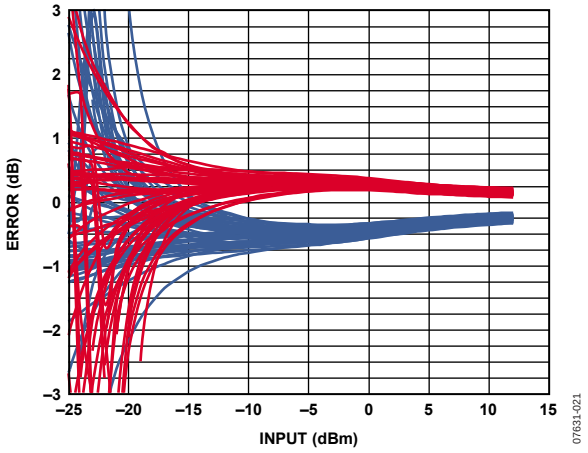

Figure 21. PEAK Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C, 3500 MHz Frequency

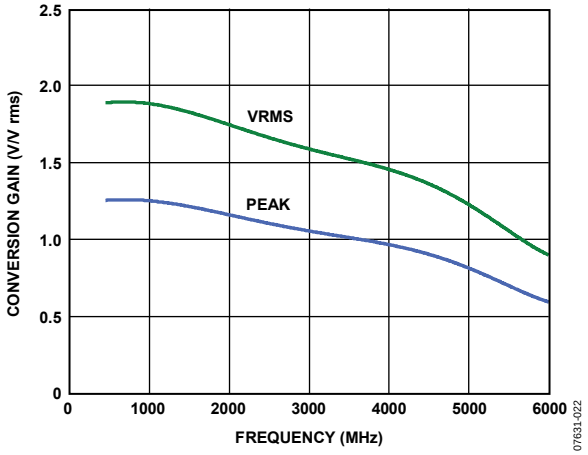

Figure 22. VRMS and PEAK Conversion Gain vs. Frequency, Supply 3 V

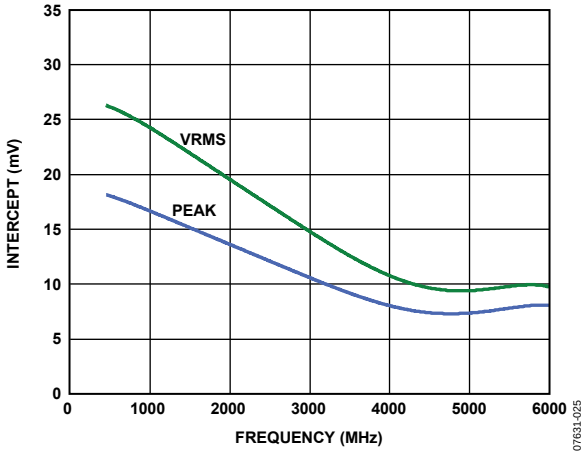

Figure 25. VRMS and PEAK Intercept vs. Frequency, Supply 3 V

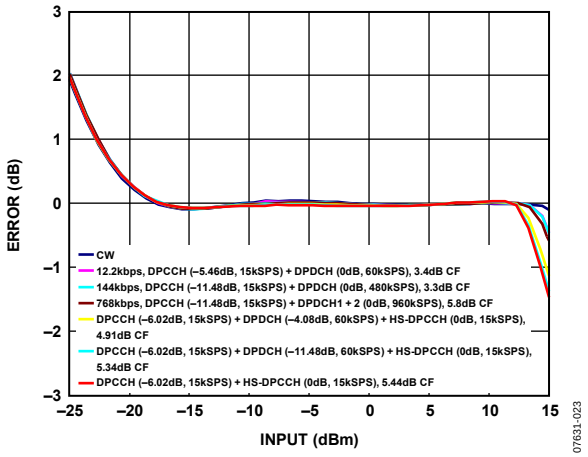

Figure 23. Error from CW Linear Reference vs. Input with Various W-CDMA Reverse Link Waveforms at 900 MHz, C_{FLTR} = 10 nF, C_{OUT} = Open

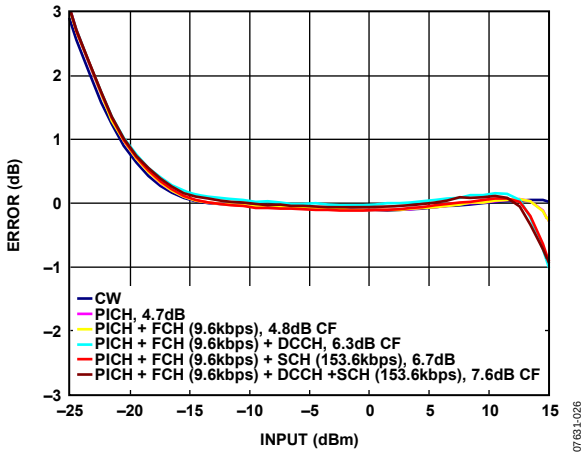

Figure 26. Error from CW Linear Reference vs. Input with Various CDMA2000 Reverse Link Waveforms at 1900 MHz, C_{FLTR} = 10 nF, C_{OUT} = Open

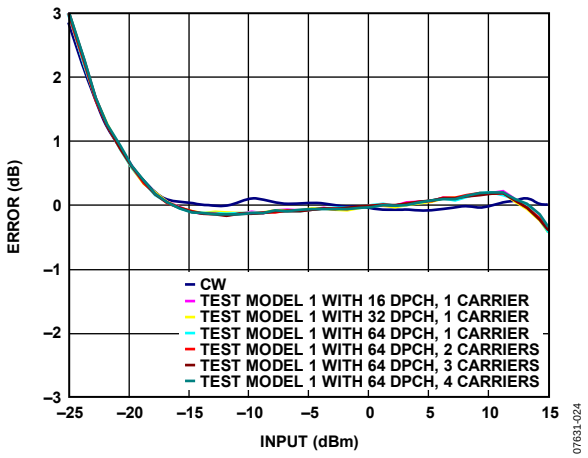

Figure 24. Error from CW Linear Reference vs. Input with Various W-CDMA Forward Link Waveforms at 2200 MHz, C_{FLTR} = 10 nF, C_{OUT} = Open

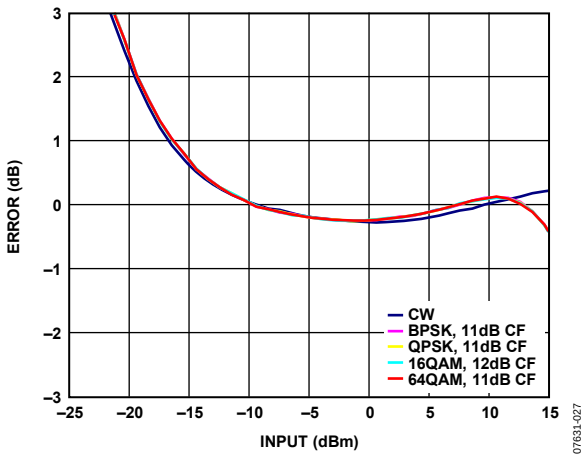

Figure 27. Error from CW Linear Reference vs. Input with Various 802.16 OFDM Waveforms at 3500 MHz, 10 MHz Signal BW, and 256 Subcarriers for All Modulated Signals, C_{FLTR} = 10 nF, C_{OUT} = Open

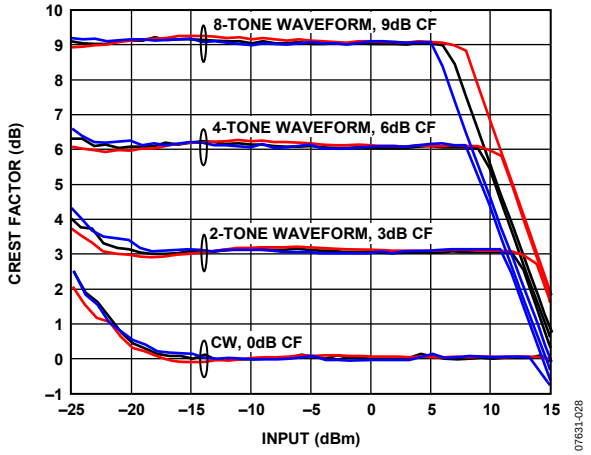

Figure 28. Crest Factor vs. Input of Various Complex Waveforms, 900 MHz, Temperatures −40°C, +25°C, and +85°C, Supply 3 V

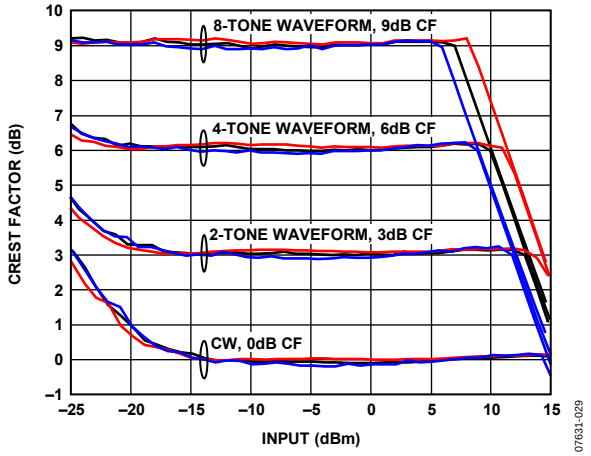

Figure 29. Crest Factor vs. Input of Various Complex Waveforms, 1900 MHz, Temperatures −40°C, +25°C, and +85°C, Supply 3 V

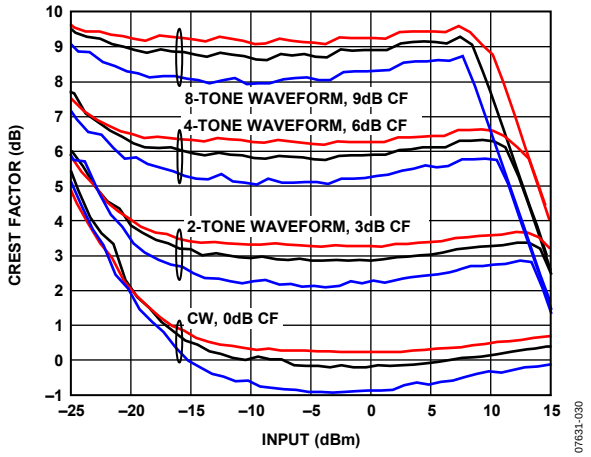

Figure 30. Crest Factor vs. Input of Various Complex Waveforms, 3500 MHz, Temperatures −40°C, +25°C, and +85°C, Supply 3 V

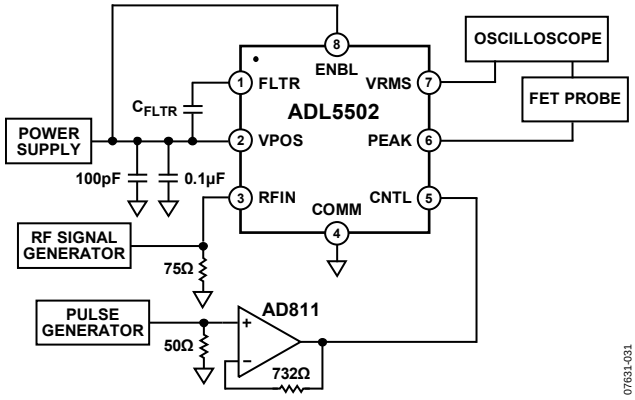

Figure 31. Hardware Configuration for Output Response During Reset Mode to Peak-Hold Transition

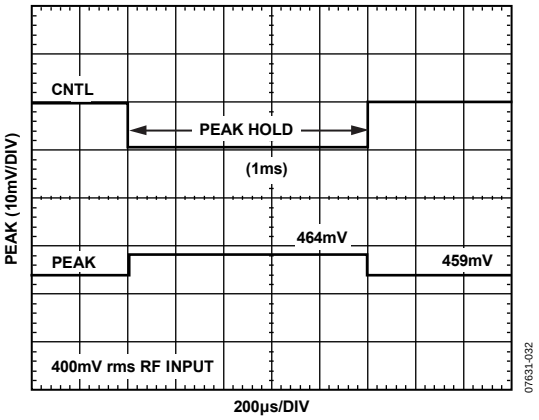

Figure 32. PEAK Response during Peak -Hold Transition, Supply 3 V, Frequency 900 MHz, CW Input, C_{FLTR} = 10 nF, C_{OUT} = Open

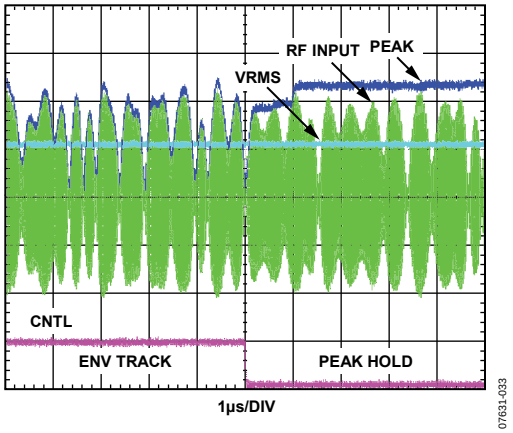

Figure 33. Reset Mode to Peak-Hold Transition, Supply 3 V, 900 MHz Frequency, W-CDMA RL (CF = 5.8 dB) Waveform, C_{FLTR} = 10 nF, C_{OUT} = Open

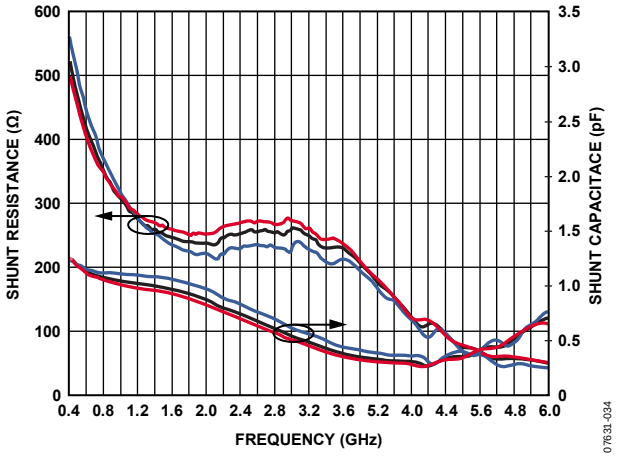

Figure 34. Input Impedance vs. Frequency, Supply 3 V, Temperatures −40°C, +25°C, and +85°C

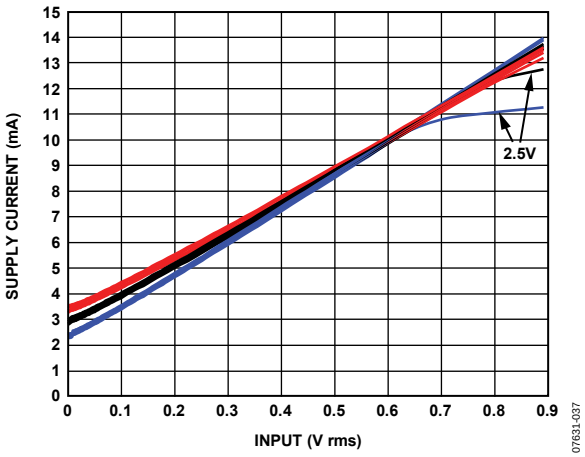

Figure 37. Supply Current vs. Input Level; 2.5 V, 3.0 V, and 3.3 V Supply; 900 MHz Frequency, Temperatures −40°C, +25°C, and +85°C

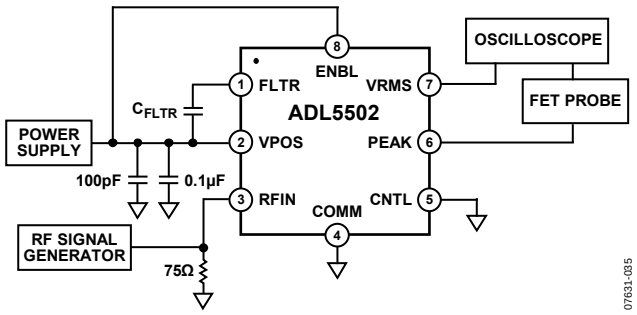

Figure 35. Hardware Configuration for Output Response to RF Input Pulse

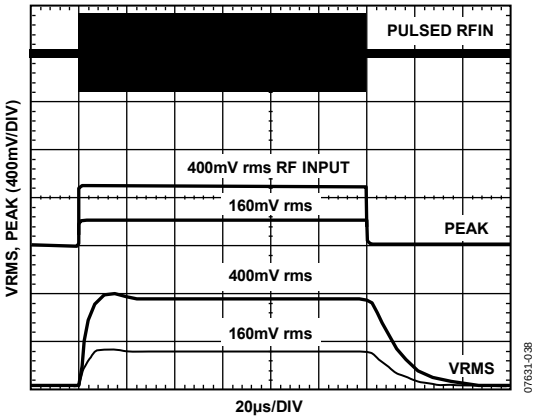

Figure 38. Output Response to Various RF Input Pulse Levels, Supply 3 V, 900 MHz Frequency, C_{FLTR} = 10 nF, C_{OUT} = Open

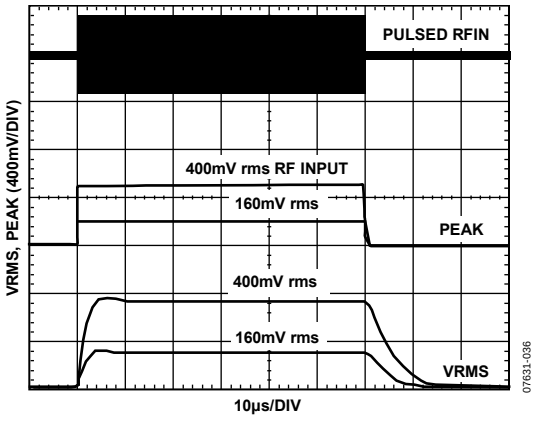

Figure 36. Output Response to Various RF Input Pulse Levels, Supply 3 V, 900 MHz Frequency, C_{FLTR} = Open, C_{OUT} = Open

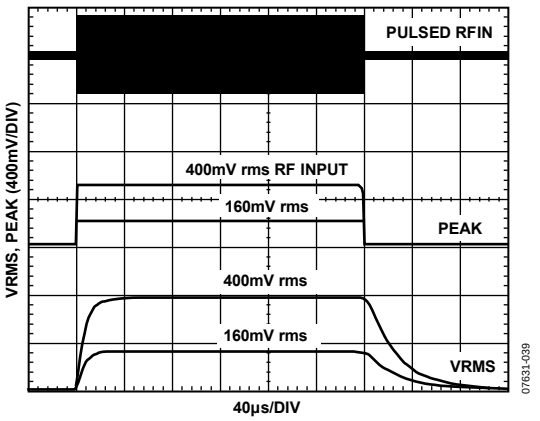

Figure 39. Output Response to Various RF Input Pulse Levels, Supply 3 V, 900 MHz Frequency, C_{FLTR} = 22 nF, C_{OUT} = Open

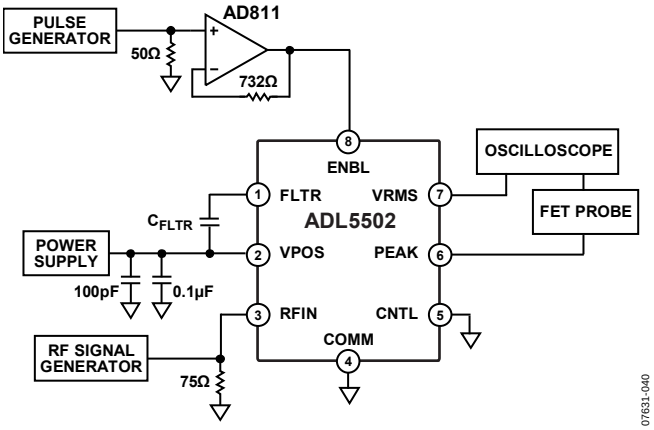

Figure 40. Hardware Configuration for Output Response to Enable Gating Measurements

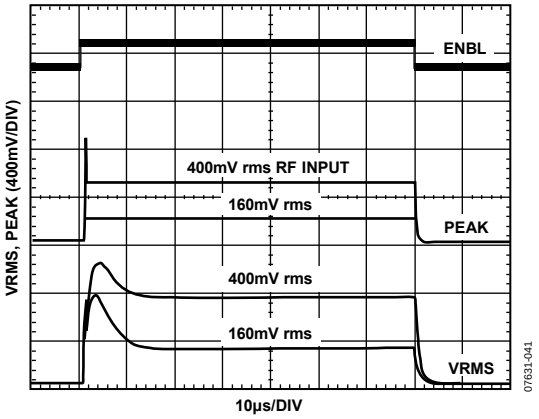

Figure 41. Output Response to Enable Gating at Various RF Input Levels, Supply 3 V, 900 MHz Frequency, C_{FLTR} = Open, C_{OUT} = Open

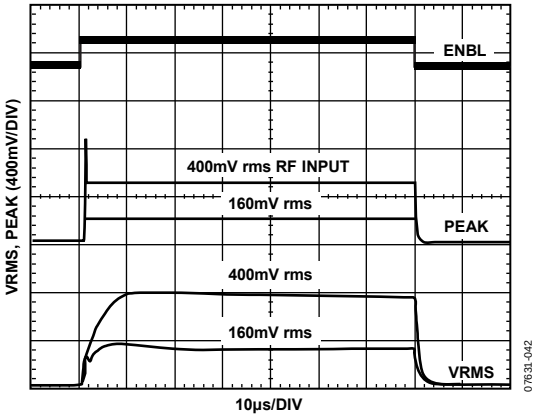

Figure 42. Output Response to Enable Gating at Various RF Input Levels, Supply 3 V, 900 MHz Frequency, C_{FLTR} = 10 nF, C_{OUT} = Open

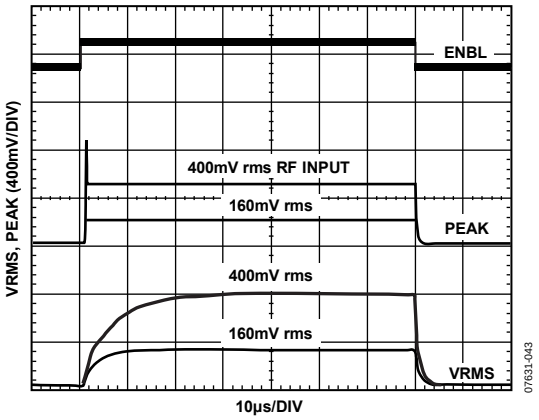

Figure 43. Output Response to Enable Gating at Various RF Input Levels, Supply 3 V, 900 MHz Frequency, C_{FLTR} = 22 nF, C_{OUT} = Open

CIRCUIT DESCRIPTION

The ADL5502 employs two-stage detection. The critical aspect of this technical approach is the concept of first stripping the carrier to reveal the envelope and then performing the required analog computation of rms and peak or any other aspect of the envelope. An on-chip, 2-pole, passive low-pass filter preserves the envelope frequencies up to 10 MHz and filters out the carrier. This carrier filtering ensures that the carrier does not introduce an error in the peak measurement.

The extracted envelope is further processed in two parallel channels, one computing the rms value of the envelope and the other transferring the envelope with appropriate scaling to the output buffer.

RMS CIRCUIT DESCRIPTION AND FILTERING

The rms processing is done using a proprietary translinear technique. This method is a mathematically accurate rms computing approach and allows achieving unprecedented rms accuracies for complex modulation signals irrespective of the crest factor of the input signal. An integrating filter capacitor does the square-domain averaging. The VRMS output can be expressed as

$$VRMS = A \times \sqrt{\frac{\int_{T1}^{T2} V_{IN}^2 \times dt}{T2 - T1}}$$

Note that A is a scaling parameter that is decided on by the on-chip resistor ratio, and there are no other scaling parameters involved in this computation, which means that the rms output is inherently free from any sources of error due to temperature, supply, and process variation.

FILTERING

The on-chip rms filtering is sufficient for most common handset applications, but an external filter capacitor can be connected if additional filtering is required; however, this increases the averaging time (see the Selecting the Square-Domain Filter and Output Low-Pass Filter section). The on-chip rms filter has a nominal corner frequency of 40 kHz. Any external capacitor acts on a 1 kΩ resistor to yield a new corner frequency for the rms filter (see Figure 1).

ENVELOPE PEAK-HOLD CIRCUIT

The envelope signal is processed through a peak-hold circuit, using the gate of an NMOS device with a charge holding capacitor connected to ground, driven by a one way charging path. This low leakage node allows peak-hold times of >1 ms without practically any drop in voltage. This circuit has the option of either transferring the envelope in real-time or in the peak-hold mode by toggling a control logic pin (CNTL). In the peak-hold mode, the output only is updated when a peak bigger than the previous biggest peak occurs. The PEAK output can be expressed as

$$PEAK\Big|_{T1}^{T2} = B \times \max\left[envelope\left(V_{IN}\right)\right]_{T1}^{T2}$$

where:
T1 is the time at which CNTL goes from high to low which is followed by a time where CNTL stays low.
T2 is the time at which the PEAK measurement is taken, while CNTL is still low. Here again the only scaling parameter involved is a Scalar B, which is also decided on by the on-chip resistor ratio.

OUTPUT BUFFERS

A dual buffer takes in internal rms and envelope/peak signals and gains these up accordingly before these are brought out on the VRMS and PEAK pins. The output stage of the rms buffer is a common source PMOS with a resistive load to provide a rail-to-rail output. However, output stage of the PEAK buffer is an emitter-follower NPN stage with a resistive load to provide high speed characteristics for this output. This however limits the maximum voltage on the PEAK output to about 1.2 V below supply, resulting in a lower scaling factor for the PEAK signal path. Such a stage allows fast tracking of a rising transition when a very narrow peak is to be followed in the 10 MHz signal bandwidth. It is highly recommended that capacitive loads greater than 2 pF are avoided on the PEAK output to realize the full bandwidth potential of the device.

Both the buffers have 100 Ω on-chip series resistances on the output. This allows for easy low-pass filtering of the two outputs.

MEASURING THE CREST FACTOR

After proper calibration of the rms and envelope channels, the ratio of the two outputs gives the crest factor of the signal, when envelope output is in peak-hold mode (see the Calculation of Crest Factor (CF) section for more details). The envelope extraction that precedes rms and peak/envelope measurement is common to both channels. In addition, the rms and envelope channels share bias lines and other critical devices that are matched between the two channels, wherever possible. This ensures that the relative measurement between the two channels or the crest factor measurement of the signal is more accurate than the individual measurements of the rms value and the peak value, although these measurements in themselves are very accurate over temperature, supply, and process variations as well.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 44 shows the basic connections for the ADL5502. The device is powered by a single supply between 2.5 V and 3.3 V, with a quiescent current of 3 mA. The VPOS pin is decoupled using 100 pF and 0.1 µF capacitors.

Placing a single 75 Ω resistor at the RF input provides a broadband match of 50 Ω. More precise resistive or reactive matches can be applied for narrow frequency band use (see the RF Input Interfacing section).

The rms averaging can be augmented by placing additional capacitance at C_{FLTR}. The ac residual can be reduced further by increasing the output capacitance, C_{OUT}. The combination of the internal 100 Ω output resistance and C_{OUT} produce a low-pass filter to reduce output ripple of the VRMS output (see the Selecting the Square-Domain Filter and Output Low-Pass Filter section for more details).

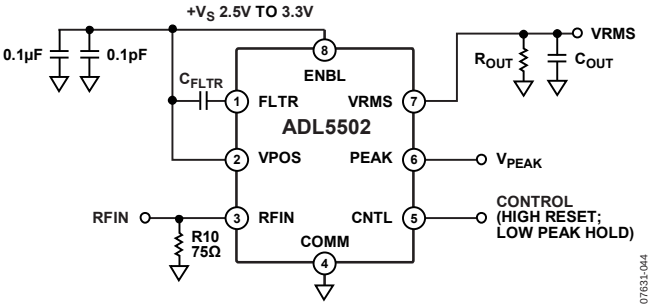

Figure 44. Basic Connections for ADL5502

To measure the peak of a waveform, the control line (CNTL) must be temporally set to high (reset mode for >1 µs) and then set back to low (peak-hold mode). This allows the ADL5502 to be initialized to a known state. When setting the device to measure peak, peak-hold mode should be toggled for a period in which the input rms power and CF is not likely to change.

If the ADL5502 is in peak-hold mode and the CF changes from high to low or the input power changes from high to low, a faulty peak measurement is reported. The ADL5502 simply keeps reporting the highest peak that occurred when the peak-hold mode was activated and the input power or the CF was high. Unless CNTL is reset, the PEAK output does not reflect the new peak in the signal.

RF INPUT INTERFACING

The input impedance of the ADL5502 decreases with increasing frequency in both its resistive and capacitive components (see Figure 34). The resistive component varies from 330 Ω at 900 MHz to about 240 Ω at 1900 MHz.

A number of options exist for input matching. For operation at multiple frequencies, a 75 Ω shunt to ground, as shown in Figure 45, provides the best overall match. For use at a single frequency, a resistive or a reactive match can be used. By plotting the input impedance on a Smith Chart, the best value for a resistive match can be calculated. (Both input impedance and input capacitance can vary by up to ±20% around their nominal values.) Where VSWR is critical, the match can be improved with a series inductor prior to the shunt component.

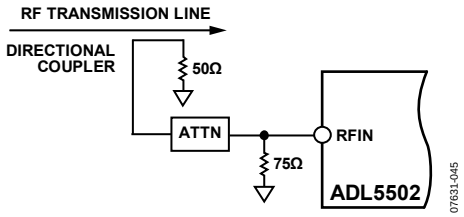

Figure 45. Input Interfacing to Directional Coupler

Resistive Tap RF Input

Figure 46 shows a technique for coupling the input signal into the ADL5502 that can be applicable where the input signal is much larger than the input range of the ADL5502. A series resistor combines with the input impedance of the ADL5502 to attenuate the input signal. Because this series resistor forms a divider with the frequency dependent input impedance, the apparent gain changes greatly with frequency. However, this method has the advantage of very little power being tapped off in RF power transmission applications. If the resistor is large compared to impedance of the transmission line, the VSWR of the system is relatively unaffected.

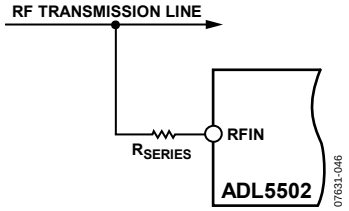

Figure 46. Attenuating the Input Signal

The resistive tap or series resistance, R_{SERIES}, can be expressed as

$$R_{SERIES} = R_{IN}\,(1 - 10^{ATTN/20})/(10^{ATTN/20}) \quad (1)$$

where:

R_{IN} is the input impedance of RFIN.

ATTN is the desired attenuation factor in dB.

For example, if a power amplifier with a maximum output power of 28 dBm is matched to the ADL5502 input at 5 dBm, then a −23 dB attenuation factor is required. At 900 MHz, the input resistance, R_{IN}, is 330 Ω.

$$R_{SERIES} = (330\ \Omega)(1 - 10^{-23/20})/(10^{-23/20}) = 4330\ \Omega \quad (2)$$

Thus, for an attenuation of −23 dB, a series resistance of approximately 4.33 kΩ is needed.

Multiple RF Inputs

Figure 47 shows a technique for combining multiple RF input signals to the ADL5502. Some applications can share a single detector for multiple bands. Three 16.5 Ω resistors in a T-network combine the three 50 Ω terminations (including the ADL5502 with the shunt 75 Ω matching component). The broadband resistive combiner ensures each port of the T-network sees a 50 Ω termination. Because there are only 6 dB of isolation from one port of the combiner to the other ports, only one band should be active at a time.

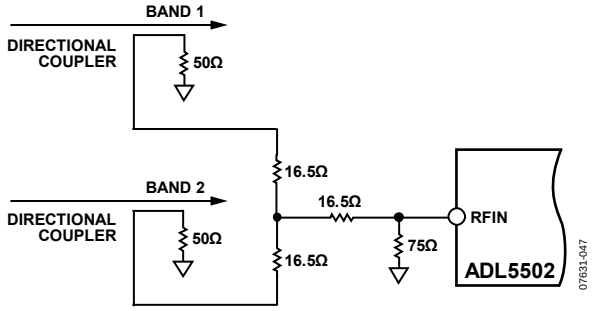

Figure 47. Combining Multiple RF Input Signals

LINEARITY

Because the ADL5502 is a linear responding device, plots of output voltage vs. input voltage result in a straight line (see Figure 4, Figure 5, and Figure 7) and the dynamic range in dB is not clearly visible. It is more useful to plot the error on a logarithmic scale, as shown in Figure 6 and Figure 8. The deviation of the plot for the ideal straight line characteristic is caused by input stage clipping at the high end and by signal offsets at the low end. However, offsets at the low end can be either positive or negative; therefore, the linearity error vs. input level plots could also trend upwards at the low end. Figure 10, Figure 11, Figure 12, Figure 16, Figure 17, and Figure 18 show error distributions for a large population of devices at specific frequencies over temperature.

It is also apparent in Figure 6 that the error at the lower portion of the dynamic range tends to shift up as frequency is increased This is due to the calibration points chosen, 0 dBm and 9 dBm (see the Device Calibration and Error Calculation section).

The absolute value cell has an input impedance that varies with frequency. The result is a decrease in the actual voltage across the squaring cell as the frequency increases, reducing the conversion gain. Similarly, conversion gain is less at frequencies near 450 MHz because of the small on-chip coupling capacitor. The dynamic range is near constant over frequency, but with a decrease in conversion gain as frequency is increased.

Output Swing

At 900 MHz, the VRMS output voltage is nominally 1.89 times the input rms voltage (a conversion gain of 1.89 V/V rms). Similarly, the PEAK output voltage is nominally 1.27 times the input rms voltage (a conversion gain of 1.27 V/V rms). The rms output voltage swings from near ground to 2.4 V on a 3.0 V supply.

Figure 9 shows the output swings of the ADL5502 to a CW input for various supply voltages. Only at the lowest supply voltage (2.5 V) is there a reduction in the dynamic range as the input headroom decreases.

VRMS Output Offset

The ADL5502 has a ±1 dB error detection range of about 30 dB, as shown in Figure 10 to Figure 12 and Figure 16 to Figure 18. The error is referred to the best-fit line defined in the linear region of the output response (see the Device Calibration and Error Calculation section for more details). Below an input power of −18 dBm, the response is no longer linear and begins to lose accuracy. In addition, depending on the supply voltage, saturation may limit the detection accuracy above 12 dBm. Calibration points should be chosen in the linear region, avoiding the nonlinear ranges at the high and low extremes.

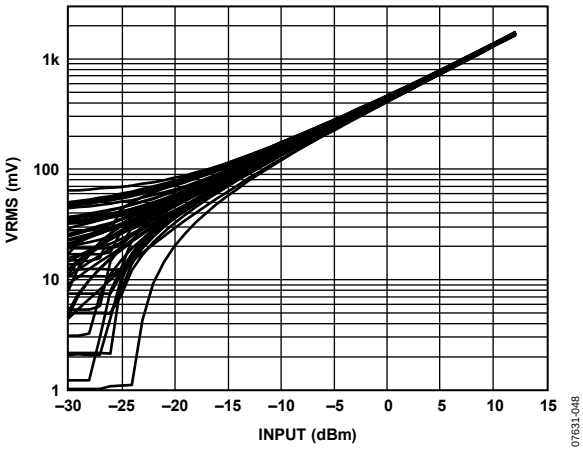

Figure 48. VRMS Output vs. Input Level Distribution of 50 Devices, 900 MHz Frequency, Supply 3.0 V

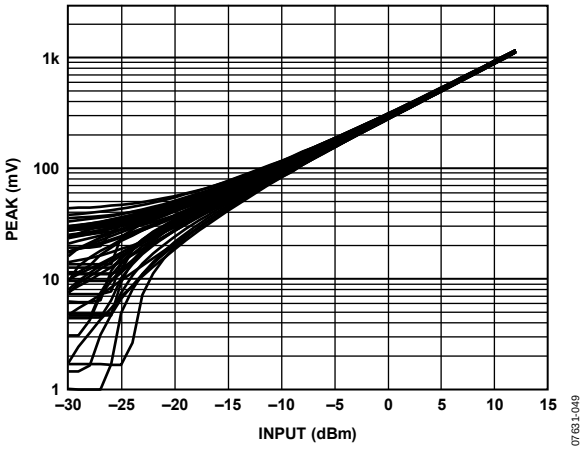

Figure 49. PEAK Output vs. Input Level Distribution of 50 Devices, 900 MHz Frequency, Supply 3.0 V

Figure 48 and Figure 49 show distributions of VRMS and PEAK output responses vs. the input power for multiple devices. The ADL5502 loses accuracy at low input powers as the output response begins to fanout. As the input power is reduced, the spread of the output response increases along with the error.

Although some devices follow the ideal linear response at very low input powers, not all devices continue the ideal linear regression to a near 0 V y-intercept. Some devices exhibit output responses that rapidly decrease and some flatten out.

With no RF signal applied, the ADL5502 has a typical output offset of 15 mV (with a maximum of 100 mV) on VRMS and an offset of 14 mV (with a maximum of 100 mV) on PEAK.

OUTPUT DRIVE CAPABILITY AND BUFFERING

The ADL5502 is capable of sourcing a VRMS output current of approximately 3 mA. The output current is sourced through the on-chip, 100 Ω series resistor; therefore, any load resistor forms a voltage divider with this on-chip resistance. It is recommended that the ADL5502 VRMS output drive high resistive loads to preserve output swing. If an application requires driving a low resistance load (as well as, in cases where increasing the nominal conversion gain is desired), a buffering circuit is necessary.

The PEAK output is designed to drive 2 pF loads. It is recommended that the ADL5502 PEAK output drive low capacitive loads to achieve a full output response time. The effects of larger capacitive loads are particularly visible when tracking envelopes during the falling transitions. When the envelope is in a fall transition, the load capacitor discharges through the on-chip load resistance of 1.9 kΩ. If the larger capacitive load is unavoidable, the additional capacitance can be counteracted by putting a shunt resistor to ground on the PEAK output to allow for fast discharge. Such a shunt resistor also makes the ADL5502 run higher current, and it should not be reduced beyond 500 Ω.

When viewing the PEAK output on an oscilloscope, a low capacitive FET probe should be used to interface with the PEAK output. This reduces the capacitance presented to the PEAK output and avoids the corresponding effects of larger capacitive loads.

SELECTING THE SQUARE-DOMAIN FILTER AND OUTPUT LOW-PASS FILTER

The internal filter capacitor of the ADL5502 provides averaging in the square domain but leaves some residual ac on the output. Signals with high peak-to-average ratios, such as W-CDMA or CDMA2000, can produce ac residual levels on the ADL5502 VRMS dc output. To reduce the effects of these low frequency components in the waveforms, some additional filtering is required.

The square-domain filter capacitance of the ADL5502 can be augmented by connecting a capacitor between Pin 1 (FLTR) and Pin 2 (VPOS). In addition, the VRMS output of the ADL5502 can be filtered directly by placing a capacitor between VRMS (Pin 7) and ground. The PEAK output can be filtered by placing a capacitor between Pin 6 (PEAK) and ground. The combination of the on-chip, 100 Ω output series resistance and the external shunt capacitor forms a low-pass filter to reduce the residual ac.

Figure 50 and Figure 51 show the effects on the residual ripple vs. the output and square-domain filter capacitor values at two communication standards with high peak-to-average ratios. Note that there is a tradeoff between ac residual and response time. Large filter capacitances increase the turn-on and pulse response times (see Figure 36, Figure 38, Figure 39, Figure 41, Figure 42, and Figure 43). Figure 52 shows the effect of the two filtering options, the output filter and the square-domain filter capacitor, on the pulse response time of the ADL5502. For more information on the effects of the filter capacitances on the response, see the Power Consumption, Enable, and Power-On/Power-Off Response Time section.

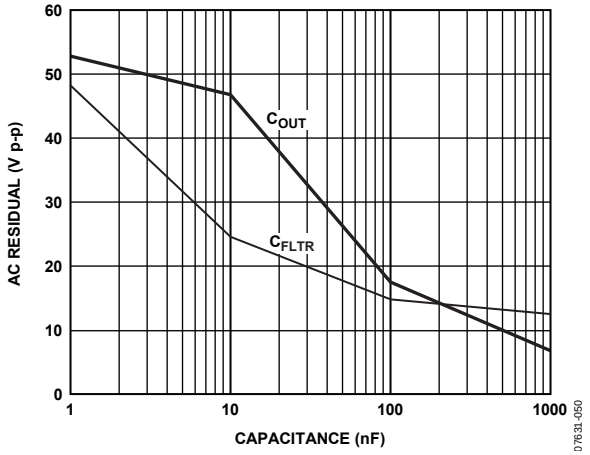

Figure 50. AC Residual vs. C_{FLTR} and C_{OUT}, W-CDMA Forward Link (4.6 dB CF) Waveform

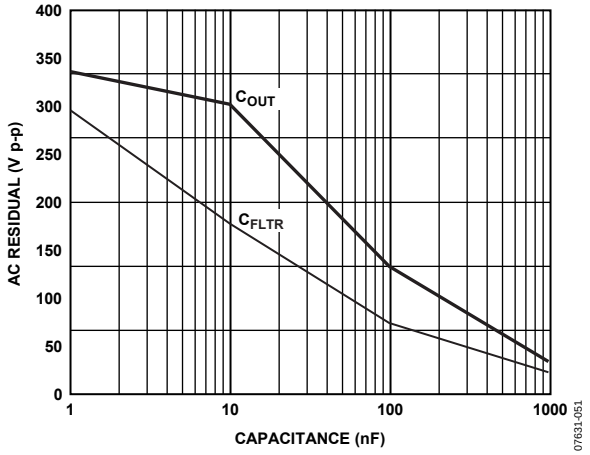

Figure 51. AC Residual vs. C_{FLTR} and C_{OUT}, W-CDMA Reverse Link (11.7 dB CF) Waveform

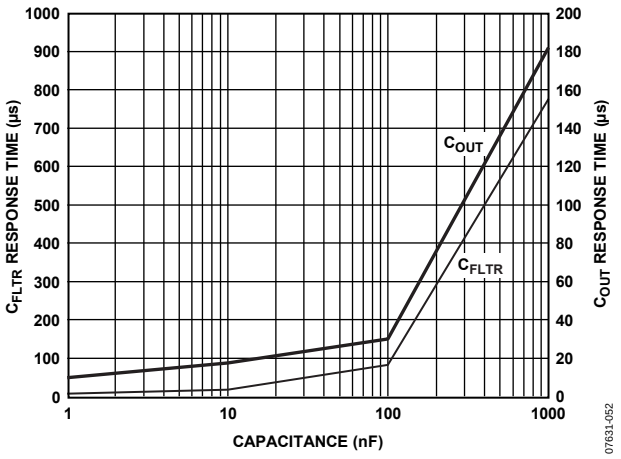

Figure 52. Response Time vs. C_{FLTR} and C_{OUT}

POWER CONSUMPTION, ENABLE, AND POWER-ON/POWER-OFF RESPONSE TIME

The quiescent current consumption of the ADL5502 varies linearly with the size of the input signal from approximately 3 mA for no signal up to 11 mA at an input level of 0.7 V rms (10 dBm, re: 50 Ω). There is little variation in quiescent current across power supply voltage or temperature, as shown in Figure 37.

The ADL5502 can be disabled either by pulling the ENBL (Pin 8) to COMM (Pin 4) or by removing the supply power to the device. Disabling the device via the ENBL function reduces the leakage current to less than 1 µA. When the device is disabled, the output impedance increases to approximately 5.5 kΩ on VRMS and 1.9 kΩ on PEAK.

The turn-on time and pulse response is strongly influenced by the size of the square-domain filter and output shunt capacitor. Figure 53 shows a plot of the output response to an RF pulse on the RFIN pin, with a 0.1 µF output filter capacitor and no square-domain filter capacitor. The falling edge is particularly dependent on the output shunt capacitance, as shown in Figure 53.

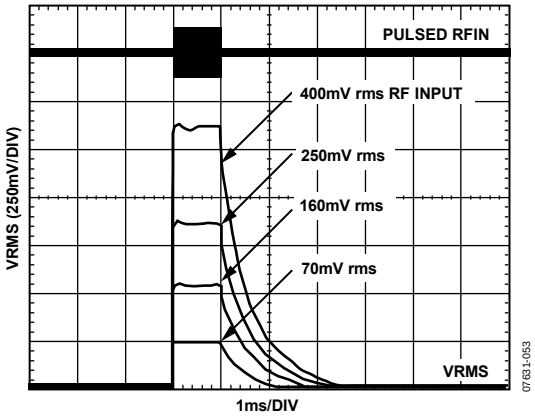

Figure 53. Output Response to Various RF Input Pulse Levels, Supply 3 V, 900 MHz Frequency, Square-Domain Filter Open, Output Filter 0.1 µF

To improve the falling edge of the enable and pulse responses, a resistor can be placed in parallel with the output shunt capacitor. The added resistance helps to discharge the output filter capacitor. Although this method reduces the power-off time, the added load resistor also attenuates the output (see the Output Drive Capability and Buffering section).

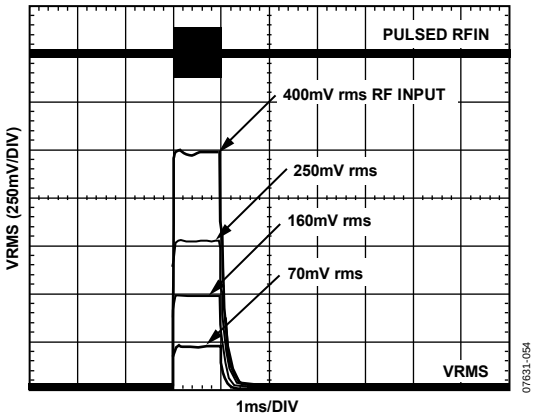

Figure 54. Output Response to Various RF Input Pulse Levels, Supply 3 V, 900 MHz Frequency, Square-Domain Filter Open, Output Filter 0.1 µF with Parallel 1 kΩ

The square-domain filter improves the rms accuracy for high crest factors (see the Selecting the Square-Domain Filter and Output Low-Pass Filter section), but it can hinder the response time. For optimum response time and low ac residual, both the square-domain filter and the output filter should be used. The square-domain filter at FLTR can be reduced to improve response time, and the remaining ac residual can be decreased by using the output filter, which has a smaller time constant.

DEVICE CALIBRATION AND ERROR CALCULATION

Because slope and intercept vary from device to device, board-level calibration must be performed to achieve high accuracy. In general, calibration is performed by applying two input power levels to the ADL5502 and measuring the corresponding output voltages. The calibration points are generally chosen to be within the linear operating range of the device. The best-fit line is characterized by calculating the conversion gain (or slope) and intercept using the following equations:

$$Gain = (V_{VRMS2} - V_{VRMS1})/(V_{IN2} - V_{IN1}) \quad (3)$$

$$Intercept = V_{VRMS1} - (Gain \times V_{IN1}) \quad (4)$$

where:
V_{IN} is the rms input voltage to RFIN.
V_{VRMS} is the voltage output at VRMS.

Once gain and intercept are calculated, an equation can be written that allows calculation of an (unknown) input power based on the measured output voltage.

$$V_{IN} = (V_{VRMS} - Intercept)/Gain \quad (5)$$

For an ideal (known) input power, the law conformance error of the measured data can be calculated as

$$ERROR\ (\text{dB}) = 20 \times \log\left[(V_{VRMS,\ MEASURED} - Intercept)/(Gain \times V_{IN,\ IDEAL})\right] \quad (6)$$

Figure 55 includes a plot of the error at 25°C, the temperature at which the ADL5502 is calibrated. Note that the error is not zero; this is because the ADL5502 does not perfectly follow the ideal linear equation, even within its operating region. The error at the calibration points is, however, equal to 0 by definition.

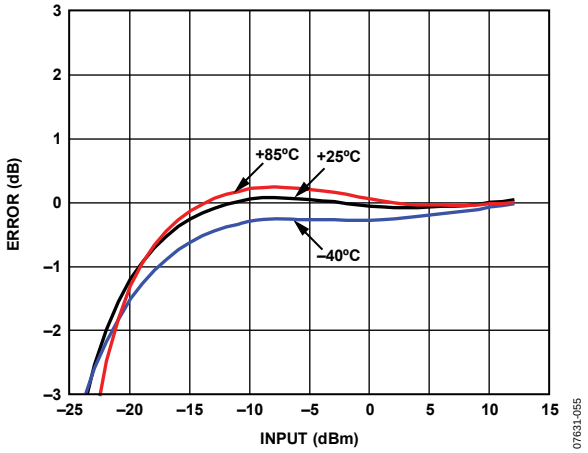

Figure 55. VRMS Error from Linear Reference vs. Input at −40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 1900 MHz, Supply 3.0 V

Figure 55 also includes error plots for the output voltage at −40°C and +85°C. These error plots are calculated using the gain and intercept at 25°C. This is consistent with calibration in a mass production environment where calibration at temperature is not practical.

The same procedure should be followed to calculate the linearity error for the PEAK output. In this case, replace V_{VRMS} with V_{PEAK} in the preceding equations.

CALIBRATION FOR IMPROVED ACCURACY

Another way of presenting the error function of the ADL5502 is shown in Figure 56. In this case, the dB error at hot and cold temperatures is calculated with respect to the transfer function at ambient temperature. This is a key difference in comparison to the previous plots. Up until now, the errors were calculated with respect to the ideal linear transfer function at ambient temperature. When this alternative technique is used, the error at ambient temperature becomes equal to zero by definition (see Figure 56).

This plot is a useful tool for estimating temperature drift at a particular power level with respect to the (nonideal) response at ambient. The linearity and dynamic range tend to be improved artificially with this type of plot because the ADL5502 does not perfectly follow the ideal linear equation (especially outside of its linear operating range). Achieving this level of accuracy in an end application requires calibration at multiple points in the operating range of the device.

In some applications, very high accuracy is required at just one power level or over a reduced input range. For example, in a wireless transmitter, the accuracy of the high power amplifier (HPA) is most critical at or close to full power. The ADL5502 offers a tight error distribution in the high input power range, as shown in Figure 56. The high accuracy range, beginning around 4 dBm at 1900 MHz, offers 8 dB of ±0.15 dB detection error over temperature. Multiple point calibration at ambient temperature in the reduced range offers precise power measurement with near 0 dB error from −40°C to +85°C.

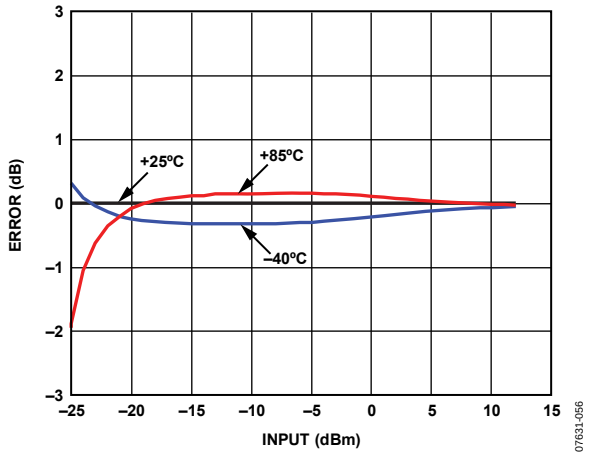

Figure 56. VRMS Error from +25°C Output Voltage at −40°C, +25°C, and +85°C After Ambient Normalization, Frequency 1900 MHz, Supply 3.0 V

Note that the high accuracy range center varies over frequency (see Figure 13, Figure 14, Figure 15, Figure 19, Figure 20, and Figure 21).

CALCULATION OF CREST FACTOR (CF)

The ADL5502 is a true rms power detector in combination with an envelope detector that accurately determines the crest factor of a modulated signal. The device has two outputs, VRMS and PEAK, which respectively provide the rms and envelope peak of the RF waveform present at RFIN. Therefore, these two outputs can be used to accurately calculate the crest factor of the waveform.

Before CF can be measured and calculated, both of the ADL5502 outputs must be calibrated (see the Device Calibration and Error Calculation section for the calibration procedure for VRMS and PEAK). It is suggested that the calibration step be completed by applying at least two input power levels with a CW signal. The CW signal (with a CF of 0 dB) serves as the reference for the CF calculation. When the characteristics (slope and intercept) of the VRMS and PEAK outputs are known, the calibration for the CF calculation is complete.

A three-stage process must be taken to measure and calculate the crest factor of any waveform. First, the unknown signal must be applied to the RF input and the corresponding VRMS level is measured. This level is indicated in Figure 57 as $V_{VRMS\text{-}UNKNOWN}$. The RF input, V_{IN}, is calculated using $V_{VRMS\text{-}UNKNOWN}$ and Equation 5.

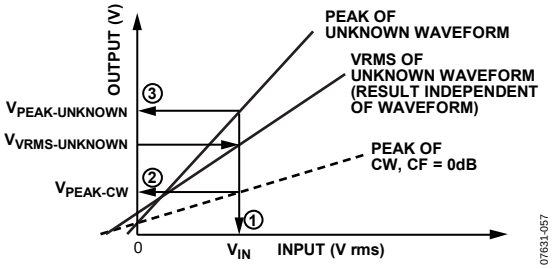

Figure 57. Procedure for Crest Factor Calculation

Next, the CW reference level of PEAK, $V_{PEAK\text{-}CW}$, is calculated using V_{IN} (that is, the output voltage that would be seen if the incoming waveform was a CW signal).

$$V_{PEAK\text{-}CW} = (V_{IN}\ Gain_{PEAK}) + Intercept_{PEAK} \quad (7)$$

Finally, the actual level of PEAK, $V_{PEAK\text{-}UNKNOWN}$, is measured and the CF can be calculated as

$$CF = 20 \cdot \log_{10}\ (V_{PEAK\text{-}UNKNOWN}/V_{PEAK\text{-}CW}) \quad (8)$$

where $V_{PEAK\text{-}CW}$, is used as a reference point to compare $V_{PEAK\text{-}UNKNOWN}$,. If both V_{PEAK} values are equal, then the CF is 0 dB, as shown in Figure 58 with the CW signal. Across the dynamic range, the calculated CF hovers about the 0 dB line. Likewise, for complex waveforms of 3 dB, 6 dB, and 9 dB CFs, the calculations accurately hover about the corresponding CF levels.

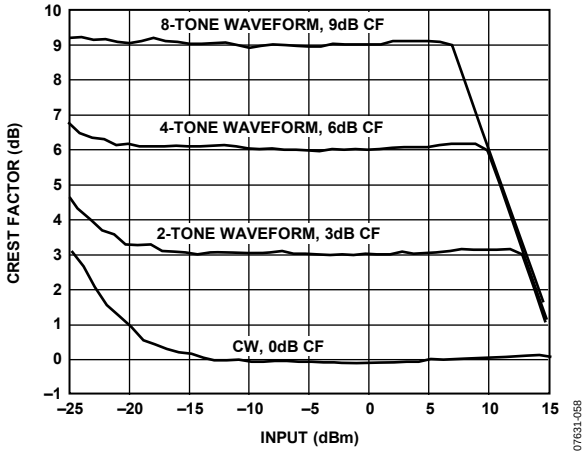

Figure 58. Reported Crest Factor of Various Waveforms

DRIFT OVER A REDUCED TEMPERATURE RANGE

Figure 59 and Figure 60 shows the error over temperature for a 1.9 GHz input signal. RMS error due to drift over temperature consistently remains within ±0.25 dB and only begins to exceed this limit when the ambient temperature rises above +65°C and drops below −30°C. For all frequencies using a reduced temperature range, higher measurement accuracy is achievable.

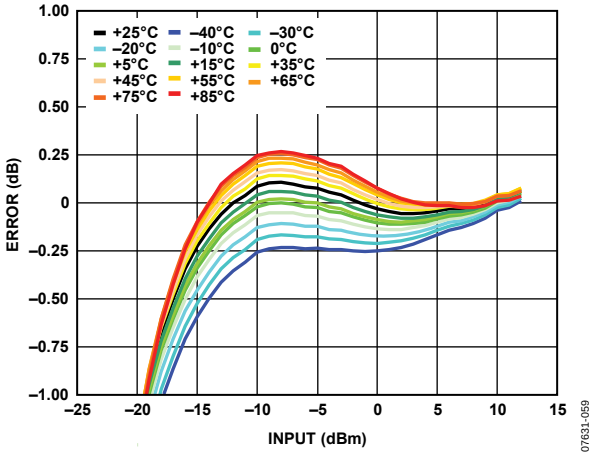

Figure 59. VRMS Typical Drift at 1.9 GHz for Various Temperatures

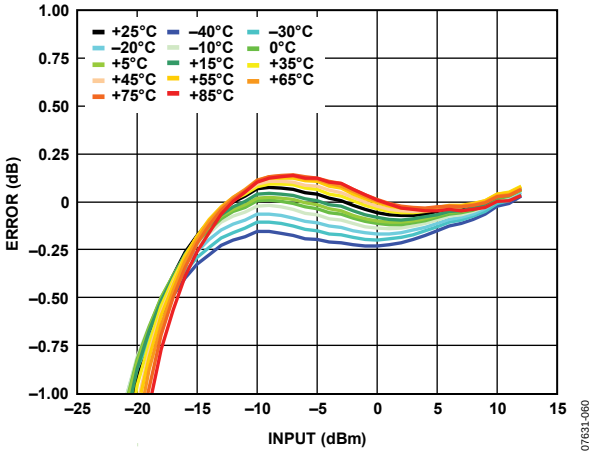

Figure 60. PEAK Typical Drift at 1.9 GHz for Various Temperatures

OPERATION AT HIGH FREQUENCIES

The ADL5502 works at high frequencies but exhibits slightly higher linearity error. Figure 61 and Figure 62 show the linearity error distributions for VRMS and PEAK of 50 devices at 6000 MHz over temperature. The typical slopes at 6000 MHz are 0.87 V/V rms and 0.58 V/V rms for VRMS and PEAK, respectively. The intercepts at 6000 MHz are 0.002 V and 0.005 V for each respective output.

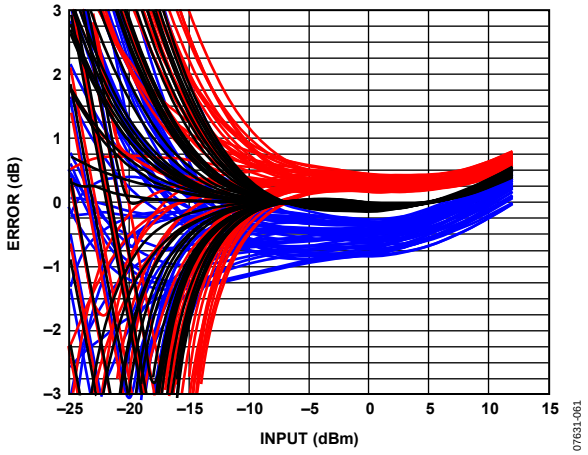

Figure 61. VRMS Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C, 6000 MHz, Supply 3.0 V

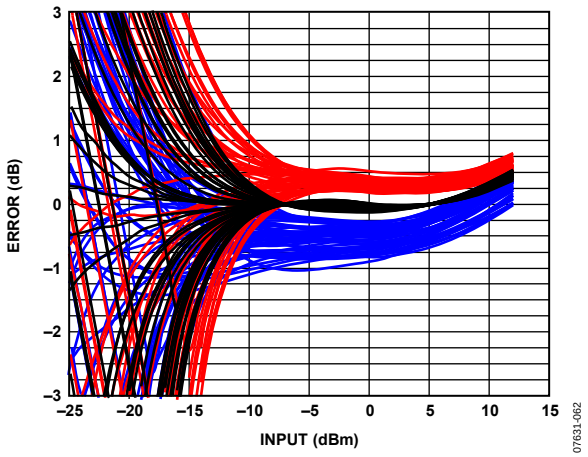

Figure 62. PEAK Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C, 6000 MHz, Supply 3.0 V

Due to the repeatability of the performance from part to part, compensation can be applied to reduce the effects of temperature drift and linearity error. To detect larger dynamic ranges at higher frequencies, the transfer function at ambient temperature can be calibrated, thus eliminating the linearity error. This technique is discussed in detail in the Calibration for Improved Accuracy section. Figure 63 and Figure 64 show the temperature drift distributions for both outputs of 50 devices at 6000 MHz.

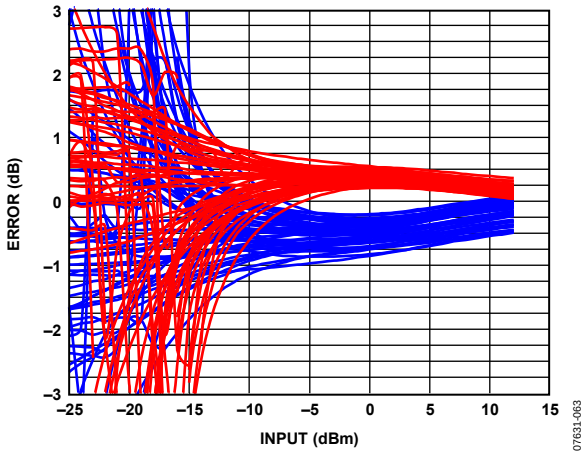

Figure 63. VRMS Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C, Frequency 6000 MHz, Supply 3.0 V

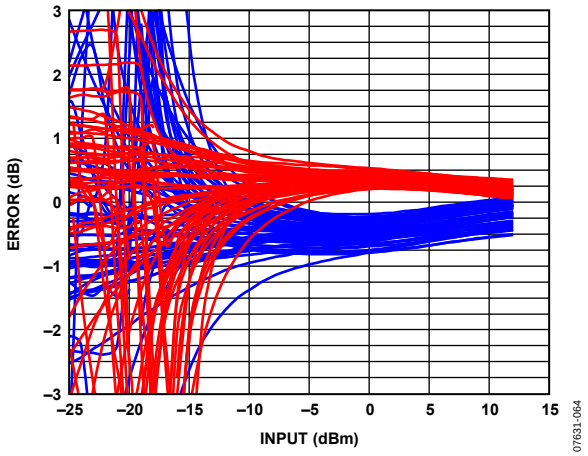

Figure 64. PEAK Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C, Frequency 6000 MHz, Supply 3.0 V

DEVICE HANDLING

The wafer-level chip scale package consists of solder bumps connected to the active side of the die. The part is lead-free with 95.5% tin, 4.0% silver, and 0.5% copper solder bump composition. The WLCSP can be mounted on printed circuit boards using standard surface-mount assembly techniques; however, caution should be taken to avoid damaging the die. See the AN-617 Application Note, *MicroCSP Wafer Level Chip Scale Package*, for additional information. WLCSP devices are bumped die; therefore, the exposed die can be sensitive to light, which can influence specified limits. Lighting in excess of 600 lux can degrade performance.

EVALUATION BOARD

Figure 65 shows the schematic of the ADL5502 evaluation board. The board is powered by a single supply in the 2.5 V to 3.3 V range. The power supply is decoupled by 100 pF and 0.1 µF capacitors.

Table 4 details the various configuration options of the evaluation board. Figure 66 and Figure 67 show the component and circuit layouts of the evaluation board.

The RF input has a broadband match of 50 Ω using a single 75 Ω resistor at R10. More precise matching at spot frequencies is possible using the pads for C15, C16, and R10 (see the RF Input Interfacing section).

The two outputs, accessible via the SMAs labeled VRMS and VENV, provide the rms response and the envelope/peak-hold measurement of the RF input power level. The device must be enabled by switching SW1 to high (setting the switch to the position opposite that of the SW1 label).

The device is placed in peak-hold mode by placing the switch SW2 in the position closes to the SW2 label. Envelope-tracking mode is possible by setting SW2 in the opposite switch position (away from the SW2 label). A signal generator can drive the control mode via the SMA labeled CNTL (see Table 4 for more details).

Operating in Peak-Hold Mode

To operate the device in peak-hold mode, the control line must be temporally set to high (reset mode for >1 µs) and then set back to low (peak-hold mode). This allows the ADL5502 initialize to a known state.

Land Pattern and Soldering Information

Pad diameters of 0.28 mm are recommended with a solder paste mask opening of 0.38 mm. For the RF input trace, a trace width of 0.30 mm is used, which corresponds to a 50 Ω characteristic impedance for the dielectric material being used (FR4). All traces going to the pads are tapered down to 0.15 mm. For the RFIN line, the length of the tapered section is 0.20 mm.

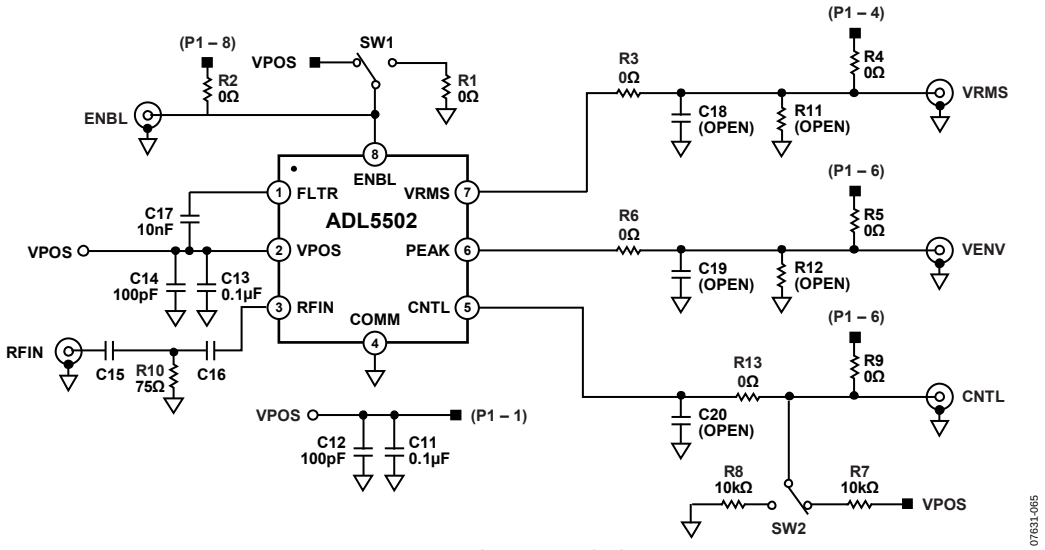

Figure 65. Evaluation Board Schematic

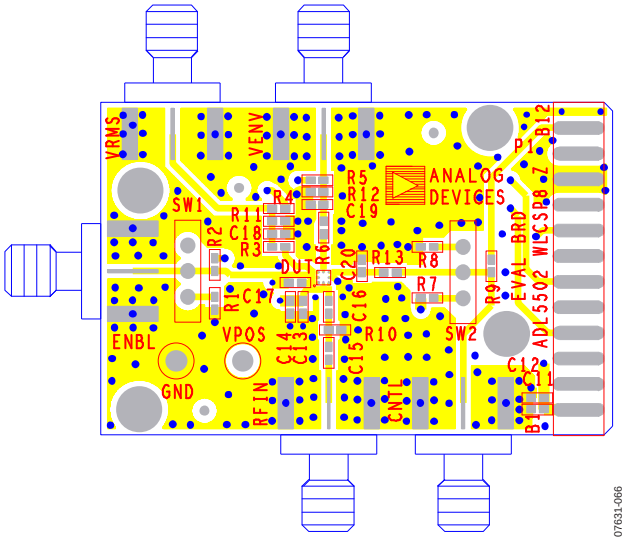

Figure 66. Layout of Evaluation Board, Component Side

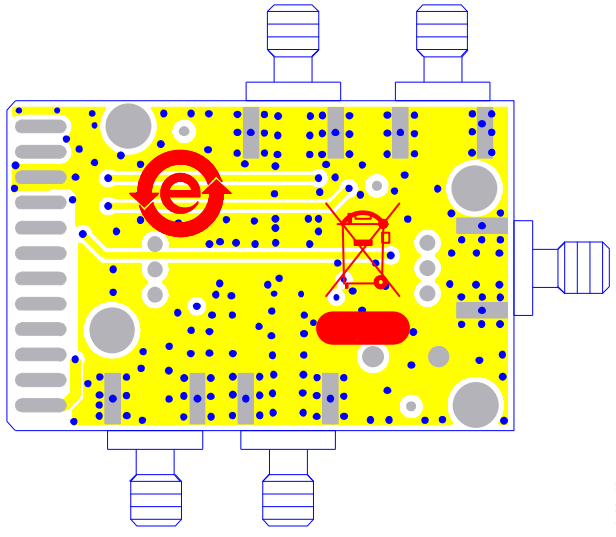

Figure 67. Layout of Evaluation Board, Circuit Side

Table 4. Evaluation Board Configuration Options

Component	Description	Default Condition
VPOS, GND	Ground and Supply Vector Pins.	Not applicable
C13, C14	Power Supply Decoupling. Nominal supply decoupling of 0.01 µF and 100 pF.	C13 = 0.1 µF (Size 0402) C14 = 100 pF (Size 0402)
C17	Filter Capacitor. The internal rms averaging capacitor can be augmented by placing additional capacitance in C17.	C17 = 10 nF (Size 0402)
R10, C15, C16	RF Input interface. The 75 Ω resistor at R10 combines with the ADL5502 internal input impedance to give a broadband input impedance of around 50 Ω. The pads for components C15, C16, and R10 can be used for more precise matching at a particular frequency.	R10 = 75 Ω (Size 0402) C15, C16 = 0 Ω (Size 0402)
R3, R6, R11, R12, C18, C19	Output Filtering. The combination of the internal 100 Ω output resistance and C18 produce a low-pass filter to reduce output ripple of the VRMS output. Similarly, C19 and the internal 100 Ω output resistance form a low-pass filter at the PEAK output. Either output can be scaled down using the resistor divider pads, R3, R11, R6, and R12.	R3, R6 = 0 Ω (Size 0402) R11, R12 = open (Size 0402) C18, C19 = open (Size 0402)
R1, SW1	Device Enable. When the switch is set toward the SW1 label, the ENBL pin is grounded (through the 0 Ω resistor) putting the device in power-down mode. In the opposite switch position, the ENBL pin is connected to VPOS and the ADL5502 is in enable mode. While the switch is in the disabled position, the ENBL pin can be driven by a signal generator via the SMA labeled ENBL. In this case, R1 must be removed or changed to provide a 50 Ω match.	R1 = 0 Ω (Size 0402) SW1 = away from SW1 label
R7, R8, R13, C20, SW2	Control Interface. When the switch is set toward the SW2 label, the CNTL pin is grounded (through a 10 kΩ resistor) putting the device in peak-hold mode. In the opposite switch position, the pin is connected to VPOS (through a 10 kΩ resistor) and the ADL5502 is in reset mode. While the switch is in the peak-hold position, the CNTL pin can be driven by a signal generator via the SMA labeled CNTL. In this case, R8 may be removed or changed to provide a 50 Ω match. R13 and C20 allow for a low-pass filter design for the control pin.	R7, R8 = 10 kΩ (Size 0402) R13 = 0 Ω (Size 0402) C20 = Open (Size 0402) SW2 = away from SW1 label
R2, R4, R5, R9, C11, C12	Alternate Interface. The end connector, P1, allows access to various ADL5502 signals. These signal paths are only used during factory test and characterization.	R2, R4, R5, R9 = 0 Ω (Size 0402) C11 = 0.1 µF (Size 0402) C12 = 100 pF (Size 0402)

OUTLINE DIMENSIONS

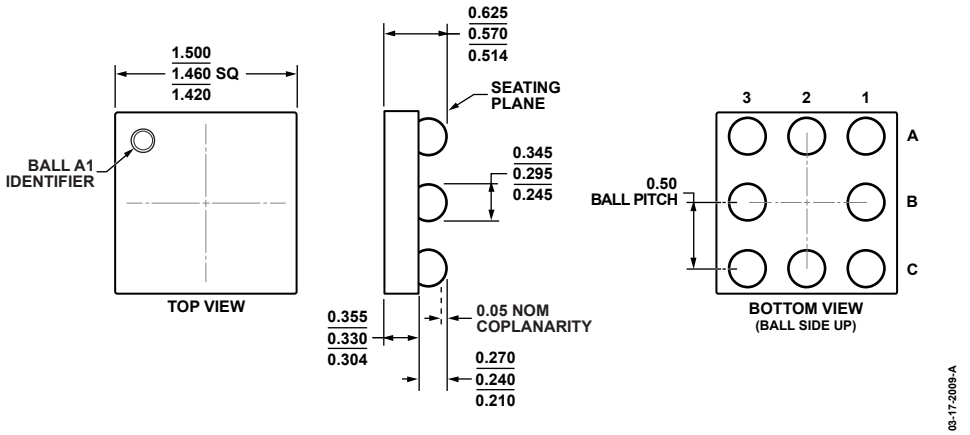

Figure 68. 8-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-8-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
ADL5502ACBZ-P7	–40°C to +85°C	8-Ball WLCSP, 7″ Pocket Tape and Reel	CB-8-3	Q1C	3,000
ADL5502ACBZ-P2	–40°C to +85°C	8-Ball WLCSP, 7″ Pocket Tape and Reel	CB-8-3	Q1C	250
ADL5502-EVALZ		Evaluation Board			

[1] Z = RoHS Compliant Part.

NOTES

NOTES

NOTES

D07631-0-1/11(A)