Serially Controlled, ±15 V/+12 V/±5 V, 8-Channel/ 4-Channel, *i*CMOS Multiplexers/Matrix Switches

ADG1438/ADG1439

FEATURES

Serial interface up to 50 MHz
SDO daisy-chaining option
9.5 Ω on resistance @ 25°C
1.6 Ω on-resistance flatness
Fully specified at ±15 V/+12 V/±5 V
3 V logic-compatible inputs
Rail-to-rail operation
20-lead TSSOP and 20-lead ,4 mm × 4 mm LFCSP packages

APPLICATIONS

Relay replacement
Audio and video routing
Automatic test equipment
Data acquisition systems
Temperature measurement systems
Avionics
Battery-powered systems
Communication systems
Medical equipment

FUNCTIONAL BLOCK DIAGRAM

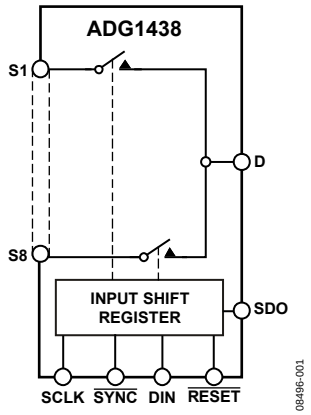


Figure 1.

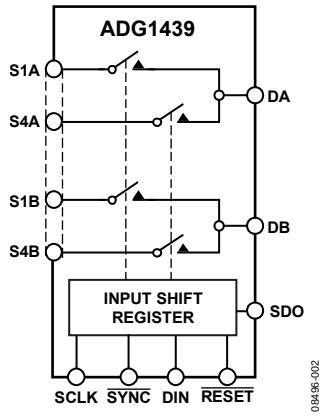


Figure 2.

GENERAL DESCRIPTION

The ADG1438 and ADG1439 are CMOS analog matrix switches with a serially controlled 3-wire interface. The ADG1438 is an 8-channel matrix switch, and the ADG1439 is a dual 4-channel matrix switch.

The ADG1438/ADG1439 use a versatile 3-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with standard SPI, QSPI™, MICROWIRE™, and DSP interface standards. The output of the shift register, SDO, enables a number of the ADG1438/ADG1439 parts to be daisy-chained. On power-up, the internal shift register contains all zeros, and all switches are in the off state.

Each switch conducts equally well in both directions when on, making these parts suitable for both multiplexing and demultiplexing applications. Because each switch is turned on or off by a separate bit, these parts can also be configured as a type of switch array, where any, all, or none of the eight switches can be closed at any time. The input signal range extends to the supply rails. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels.

The ultralow on resistance and on-resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications where low distortion is critical. *i*CMOS® construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

PRODUCT HIGHLIGHTS

1. 50 MHz serial interface.
2. 9.5 Ω on resistance.
3. 1.6 Ω on-resistance flatness.
4. 3 V logic-compatible digital input, V_{INH} = 2.0 V, V_{INL} = 0.8 V.

Table 1. Related Devices

Part No.	Description
ADG1408/ADG1409	Low on resistance, parallel interface, 4-/8-channel ±15 V multiplexers

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

10/09—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, V_L = 2.7 V to 5.5 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	9.5			Ω typ	V_{DD} = +13.5 V, V_{SS} = −13.5 V, V_S = ±10 V, I_S = −10 mA; see Figure 27.
	11.5	14	16	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	0.55			Ω typ	V_{DD} = +13.5 V, V_{SS} = −13.5 V, V_S = ±10 V, I_S = −10 mA.
	1	1.5	1.7	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	1.6			Ω typ	V_{DD} = +13.5 V, V_{SS} = −13.5 V, V_S = ±10 V, I_S = −10 mA.
	1.9	2.15	2.3	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V.
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 28.
	±0.15	±1	±2	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 28.
ADG1438	±0.25	±3	±12	nA max	
ADG1439	±0.25	±1.5	±6	nA max	
Channel On Leakage, I_D, I_S (On)	±0.01			nA typ	V_S = V_D = ±10 V; see Figure 29.
	±0.3	±3	±12	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current	±0.001			μA typ	V_{IN} = V_{GND} or V_L.
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
LOGIC OUTPUTS (SDO)					
Output Low Voltage, V_{OL} [1]			0.4	V max	I_{SINK} = 3 mA.
			0.6	V max	I_{SINK} = 6 mA.
High Impedance Leakage Current	0.001			μA typ	
			±1	μA max	
High Impedance Output Capacitance[1]	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Break-Before-Make Time Delay, t_{BBM}	55			ns typ	R_L = 100 Ω, C_L = 35 pF.
			30	ns min	V_{S1} = V_{S2} = 10 V; see Figure 31.
Transition Time, $t_{TRANSITION}$	80			ns typ	R_L = 100 Ω, C_L = 35 pF.
	100	120	130	ns max	V_S = 10 V; see Figure 30.
Charge Injection	4			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32.
Off Isolation	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 33.
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 34.
Total Harmonic Distortion (THD + N)	0.057			% typ	R_L = 110 Ω, 15 V p-p, f = 20 Hz to 20 kHz; see Figure 36.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF; see Figure 35.
ADG1438	82			MHz typ	
ADG1439	130			MHz typ	
Insertion Loss	0.7			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 35.
C_S (Off)	9			pF typ	f = 1 MHz.
C_D (Off)					
ADG1438	58			pF typ	f = 1 MHz.
ADG1439	28			pF typ	f = 1 MHz.
C_D, C_S (On)					
ADG1438	286			pF typ	f = 1 MHz.
ADG1439	139			pF typ	f = 1 MHz.
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V.
I_{DD}	0.001			µA typ	Digital inputs = 0 V or V_L.
			1	µA max	
I_L Inactive	0.3			µA typ	Digital inputs = 0 V or V_L.
			1	µA max	
I_L Active – 30 MHz	0.26			mA typ	Digital inputs toggle between 0 V and V_L.
		0.3	0.35	mA max	
I_L Active – 50 MHz	0.42			mA typ	Digital inputs toggle between 0 V and V_L.
		0.5	0.55	mA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V or V_L.
			1	µA max	
V_{DD}/V_{SS}			±4.5/±16.5	V min/Vmax	

[1] Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, V_L = 2.7 V to 5.5 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
On Resistance (R_{ON})	18			Ω typ	V_{DD} = 10.8 V, V_{SS} = 0 V; V_S = 0 V to 10 V, I_S = −10 mA; see Figure 27.
	21.5	26	28.5	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	0.55			Ω typ	V_{DD} = 10.8 V, V_{SS} = 0 V; V_S = 0 V to 10 V, I_S = −10 mA.
	1.2	1.6	1.8	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	5			Ω typ	V_{DD} = 10.8 V, V_{SS} = 0 V; V_S = 0 V to 10 V, I_S = −10 mA.
	6	6.9	7.3	Ω max	
LEAKAGE CURRENTS					V_{DD} = 10.8 V.
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 28.
	±0.15	±1	±2	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 28.
ADG1438	±0.25	±3	±12	nA max	
ADG1439	±0.25	±1.5	±6	nA max	
Channel On Leakage, I_D, I_S (On)	±0.05			nA typ	V_S = V_D = 1 V or 10 V; see Figure 29.
	±0.3	±3	±12	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current	±0.001			μA typ	V_{IN} = V_{GND} or V_L.
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
LOGIC OUTPUTS (SDO)					
Output Low Voltage, V_{OL}[1]			0.4	V max	I_{SINK} = 3 mA.
			0.6	V max	I_{SINK} = 6 mA.
High Impedance Leakage Current	0.001			μA typ	
			±1	μA max	
High Impedance Output Capacitance[1]	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Break-Before-Make Time Delay, t_{BBM}	115			ns typ	R_L = 100 Ω, C_L = 35 pF.
			60	ns min	V_{S1} = V_{S2} = 8 V; see Figure 31.
Transition Time, $t_{TRANSITION}$	155			ns typ	R_L = 100 Ω, C_L = 35 pF.
	195	235	260	ns max	V_S = 8 V; see Figure 30.
Charge Injection	7			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32.
Off Isolation	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 33.
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 34.
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF; see Figure 35.
ADG1438	58			MHz typ	
ADG1439	105			MHz typ	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Insertion Loss	1.3			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 35.
C_S (Off)	14			pF typ	f = 1 MHz.
C_D (Off)					
ADG1438	86			pF typ	f = 1 MHz.
ADG1439	42			pF typ	f = 1 MHz.
C_D, C_S (On)					
ADG1438	295			pF typ	f = 1 MHz.
ADG1439	145			pF typ	f = 1 MHz.
POWER REQUIREMENTS					V_{DD} = 13.2 V.
I_{DD}	0.001			µA typ	Digital inputs = 0 V or V_L.
			1	µA max	
I_L Inactive	0.3			µA typ	Digital inputs = 0 V or V_L.
			1	µA max	
I_L Active – 30 MHz	0.26			mA typ	Digital inputs toggle between 0 V and V_L.
		0.3	0.35	mA max	
I_L Active – 50 MHz	0.42			mA typ	Digital inputs toggle between 0 V and V_L.
		0.5	0.55	mA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V or V_L.
			1	µA max	
V_{DD}			5/16.5	V min/Vmax	

[1] Guaranteed by design, not subject to production test.

±5 V DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, V_L = 2.7 V to V_{DD}, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	21			Ω typ	V_{DD} = +4.5 V, V_{SS} = −4.5 V, V_S = ±4.5 V, I_S = −10 mA; see Figure 27.
	25	29	32	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	0.6			Ω typ	V_{DD} = +4.5 V, V_{SS} = −4.5 V, V_S = ±4.5V, I_S = −10 mA.
	1.3	1.7	1.9	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	5.2			Ω typ	V_{DD} = +4.5 V, V_{SS} = −4.5 V, V_S = ±4.5 V, I_S = −10 mA.
	6.4	7.3	7.6	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V.
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 28.
	±0.15	±1	±2	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 28.
ADG1438	±0.25	±3	±12	nA max	
ADG1439	±0.25	±1.5	±6	nA max	
Channel On Leakage, I_D, I_S (On)	±0.05			nA typ	V_S = V_D = ±4.5 V; see Figure 29.
	±0.3	±3	±12	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current	±0.001			μA typ	V_{IN} = V_{GND} or V_L.
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
LOGIC OUTPUTS (SDO)					
Output Low Voltage, V_{OL}[1]			0.4	V max	I_{SINK} = 3 mA.
			0.6	V max	I_{SINK} = 6 mA.
High Impedance Leakage Current	0.001			μA typ	
			±1	μA max	
High Impedance Output Capacitance[1]	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Break-Before-Make Time Delay, t_{BBM}	150			ns typ	R_L = 100 Ω, C_L = 35 pF.
			80	ns min	V_{S1} = V_{S2} = 3 V; see Figure 31.
Transition Time, $t_{TRANSITION}$	200			ns typ	R_L = 100 Ω, C_L = 35 pF.
	230	315	350	ns max	V_S = 3 V; see Figure 30.
Charge Injection	5			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32.
Off Isolation	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 33.
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 34.
Total Harmonic Distortion (THD + N)	0.14			% typ	R_L = 110 Ω, 5 V p-p, f = 20 Hz to 20 kHz; see Figure 36.
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF; see Figure 35.
ADG1438	62			MHz typ	
ADG1439	116			MHz typ	
Insertion Loss	1.2			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 35.
C_S (Off)	12			pF typ	f = 1 MHz.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
C_D (Off)					
ADG1438	76			pF typ	f = 1 MHz.
ADG1439	38			pF typ	f = 1 MHz.
C_D, C_S (On)					
ADG1438	311			pF typ	f = 1 MHz.
ADG1439	151			pF typ	f = 1 MHz.
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V.
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_L.
			1	μA max	
I_L Inactive	0.3			μA typ	Digital inputs = 0 V or V_L.
			1	μA max	
I_L Active – 30 MHz	0.26			mA typ	Digital inputs toggle between 0 V and V_L.
		0.3	0.35	mA max	
I_L Active – 50 MHz	0.42			mA typ	Digital inputs toggle between 0 V and V_L.
		0.5	0.55	mA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_L.
			1	μA max	
V_{DD}/V_{SS}			±4.5/±16.5	V min/Vmax	

[1] Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT PER CHANNEL

Table 5. ADG1438, One Channel On

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT PER CHANNEL[1]					
15 V Dual Supply					V_{DD} = +13.5 V, V_{SS} = −13.5 V
20-Lead TSSOP (θ_{JA} = 112.6°C/W)	169	97	48	mA max	
20-Lead LFCSP (θ_{JA} = 30.4°C/W)	295	139	55	mA max	
12 V Single Supply					V_{DD} = 10.8 V, V_{SS} = 0 V
20-Lead TSSOP (θ_{JA} = 112.6°C/W)	161	93	47	mA max	
20-Lead LFCSP (θ_{JA} = 30.4°C/W)	281	135	54	mA max	
5 V Dual Supply					V_{DD} = +4.5 V, V_{SS} = −4.5 V
20-Lead TSSOP (θ_{JA} = 112.6°C/W)	122	76	43	mA max	
20-Lead LFCSP (θ_{JA} = 30.4°C/W)	214	114	51	mA max	

[1] Guaranteed by design, not subject to production test.

Table 6. ADG1439, One Channel On Per Multiplexer

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT PER CHANNEL[1]					
15 V Dual Supply					V_{DD} = +13.5 V, V_{SS} = −13.5 V
20-Lead TSSOP (θ_{JA} = 112.6°C/W)	125	77	43	mA max	
20-Lead LFCSP (θ_{JA} = 30.4°C/W)	220	116	52	mA max	
12 V Single Supply					V_{DD} = 10.8 V, V_{SS} = 0 V
20-Lead TSSOP (θ_{JA} = 112.6°C/W)	119	74	42	mA max	
20-Lead LFCSP (θ_{JA} = 30.4°C/W)	210	112	51	mA max	
5 V Dual Supply					V_{DD} = +4.5 V, V_{SS} = −4.5 V
20-Lead TSSOP (θ_{JA} = 112.6°C/W)	159	93	47	mA max	
20-Lead LFCSP (θ_{JA} = 30.4°C/W)	90	59	37	mA max	

[1] Guaranteed by design, not subject to production test.

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$ (see Figure 3). V_{DD} = 4.5 V to 16.5 V; V_{SS} = −16.5 V to 0 V; V_L = 2.7 V to 5.5 V or V_{DD} (whichever is less); GND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 7.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
t_1[2]	20	ns min	SCLK cycle time
t_2	9	ns min	SCLK high time
t_3	9	ns min	SCLK low time
t_4	5	ns min	$\overline{SYNC}$ to SCLK active edge setup time
t_5	5	ns min	Data setup time
t_6	5	ns min	Data hold time
t_7	5	ns min	SCLK active edge to $\overline{SYNC}$ rising edge
t_8	15	ns min	Minimum $\overline{SYNC}$ high time
t_9	5	ns min	$\overline{SYNC}$ rising edge to next SCLK active edge ignored
t_{10}	5	ns min	SCLK active edge to $\overline{SYNC}$ falling edge ignored
t_{11}[3]	40	ns max	SCLK rising edge to SDO valid
t_{12}	15	ns min	Minimum $\overline{RESET}$ pulse width

[1] Guaranteed by design and characterization, not production tested.
[2] Maximum SCLK frequency is 50 MHz at V_{DD} = 4.5 V to 16.5 V; V_{SS} = −16.5 V to 0 V; V_L = 2.7 V to 5.5 V or V_{DD} (whichever is less); GND = 0 V.
[3] Measured with the 1 kΩ pull-up resistor to V_L and 20 pF load. t_{11} determines the maximum SCLK frequency in daisy-chain mode.

TIMING DIAGRAM

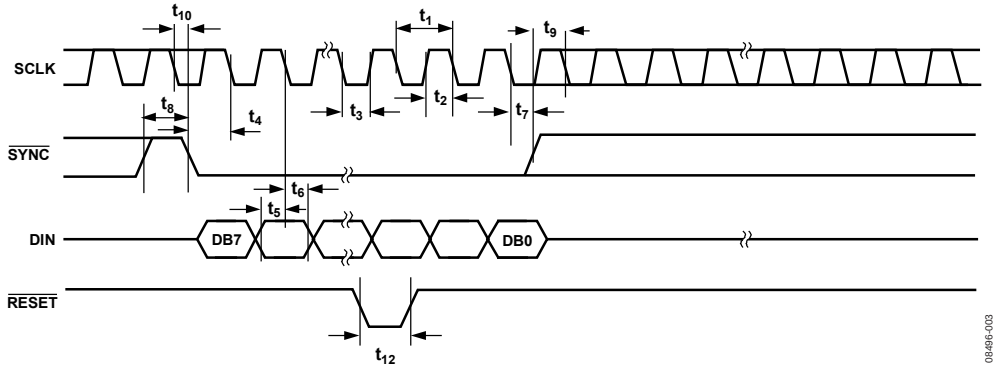


Figure 3. Serial Write Operation

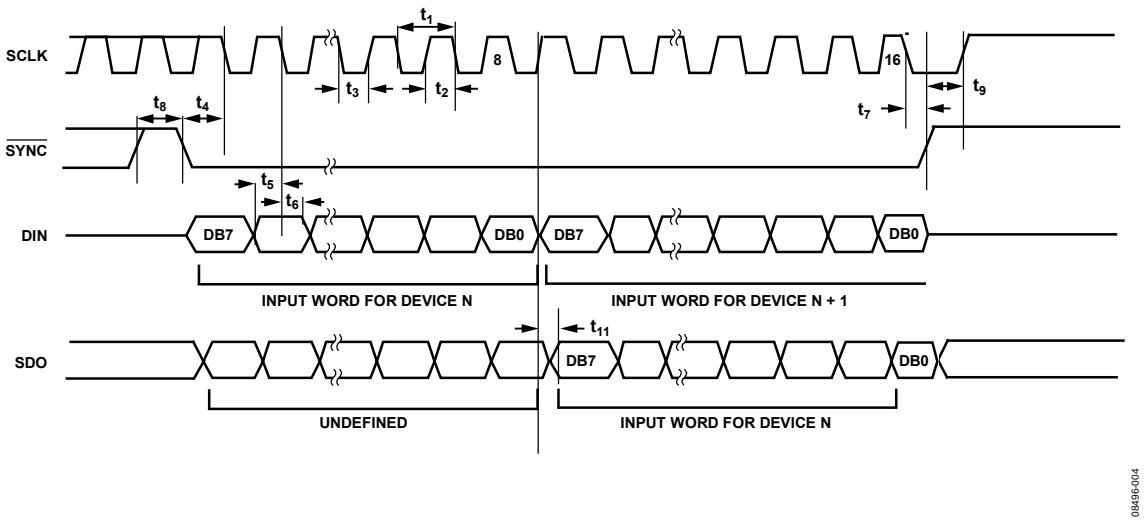


Figure 4. Daisy-Chain Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
V_L to GND	−0.3 V to +7 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	GND − 0.3 V to V_L + 0.3 V or 30 mA, whichever occurs first
Continuous Current, Sx or Dx Pins	Table 5 and Table 6 specifications + 15%
Peak Current, Sx or Dx Pins (Pulsed at 1 ms, 10% Duty Cycle Max)	
TSSOP	300 mA
LFCSP	400 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature (Pb-Free)	260(+0/−5)°C
Time at Peak Temperature	10 sec to 40 sec

[1] Overvoltages at the analog and digital inputs are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Table 9. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20 Lead TSSOP (4-Layer Board)	112.6	50	°C/W
20-Lead LFCSP (4-Layer Board and Exposed Paddle Soldered to V_{SS})	30.4	N/A	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

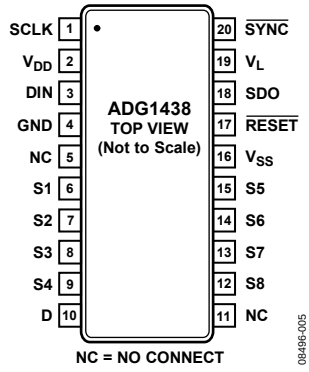
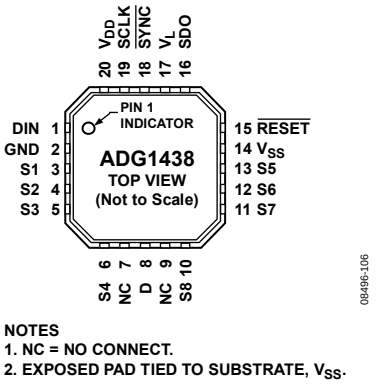


Figure 5. ADG1438 Pin Configuration (TSSOP)



NOTES
1. NC = NO CONNECT.
2. EXPOSED PAD TIED TO SUBSTRATE, V_{SS}.

Figure 6. ADG1438 Pin Configuration (LFCSP)

Table 10. ADG1438 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.
2	20	V_{DD}	Most Positive Power Supply Potential.
3	1	DIN	Serial Data Input. This device has an 8-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
4	2	GND	Ground (0 V) Reference.
5	7	NC	No Connect.
6	3	S1	Source Terminal 1. Can be an input or an output.
7	4	S2	Source Terminal 2. Can be an input or an output.
8	5	S3	Source Terminal 3. Can be an input or an output.
9	6	S4	Source Terminal 4. Can be an input or an output.
10	8	D	Drain Terminal. Can be an input or an output.
11	9	NC	No Connect.
12	10	S8	Source Terminal 8. Can be an input or an output.
13	11	S7	Source Terminal 7. Can be an input or an output.
14	12	S6	Source Terminal 6. Can be an input or an output.
15	13	S5	Source Terminal 5. Can be an input or an output.
16	14	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, it can be connected to ground.
17	15	$\overline{\text{RESET}}$	Active Low Logic Input. When this pin is low, all switches are open, and the appropriate registers are cleared to 0.
18	16	SDO	Serial Data Output. Can be used for daisy-chaining a number of these devices together or for reading back the data in the shift register for diagnostic purposes. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock. This is an open-drain output that should be pulled to the V_L supply with an external 1 kΩ resistor.
19	17	V_L	Logic Power Supply Input. Operates from 2.7 V to 5.5 V.
20	18	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the following clocks. Taking $\overline{\text{SYNC}}$ high updates the switch condition.
	EPAD		The exposed pad is tied to the substrate, V_{SS}.

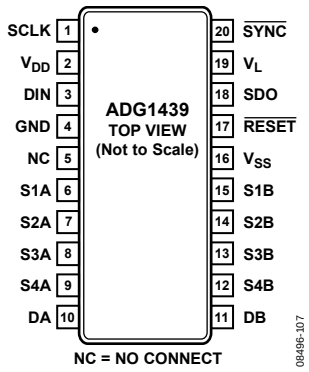


Figure 7. ADG1439 Pin Configuration (TSSOP)

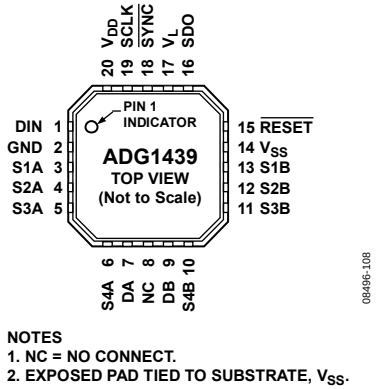


Figure 8. ADG1439 Pin Configuration (LFCSP)

Table 11. ADG1439 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.
2	20	V_{DD}	Most Positive Power Supply Potential.
3	1	DIN	Serial Data Input. This device has an 8-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
4	2	GND	Ground (0 V) Reference.
5	8	NC	No Connect.
6	3	S1A	Source Terminal 1A. Can be an input or an output.
7	4	S2A	Source Terminal 2A. Can be an input or an output.
8	5	S3A	Source Terminal 3A. Can be an input or an output.
9	6	S4A	Source Terminal 4A. Can be an input or an output.
10	7	DA	Drain Terminal A. Can be an input or an output.
11	9	DB	Drain Terminal B. Can be an input or an output.
12	10	S4B	Source Terminal 4B. Can be an input or an output.
13	11	S3B	Source Terminal 3B. Can be an input or an output.
14	12	S2B	Source Terminal 2B. Can be an input or an output.
15	13	S1B	Source Terminal 1B. Can be an input or an output.
16	14	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, it can be connected to ground.
17	15	$\overline{RESET}$	Active Low Logic Input. When this pin is low, all switches are open, and appropriate registers are cleared to 0.
18	16	SDO	Serial Data Output. Can be used for daisy-chaining a number of these devices together or for reading back the data in the shift register for diagnostic purposes. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock. This is an open-drain output that should be pulled to the V_L supply with an external 1 kΩ resistor.
19	17	V_L	Logic Power Supply Input. Operates from 2.7 V to 5.5 V.
20	18	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the following clocks. Taking $\overline{SYNC}$ high updates the switch condition.
	EPAD		The exposed pad is tied to the substrate, V_{SS}.

TYPICAL PERFORMANCE CHARACTERISTICS

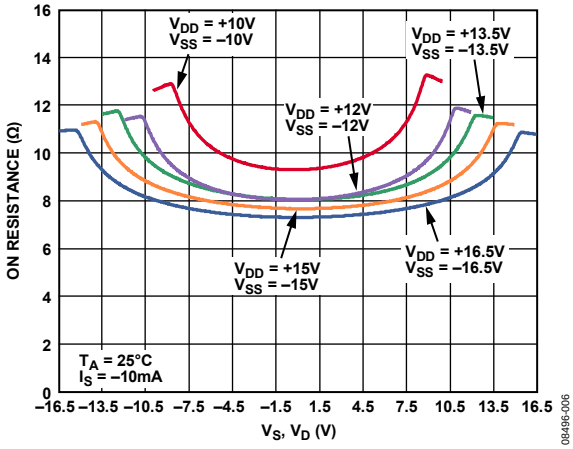


Figure 9. On Resistance as a Function of V_D (V_S), Dual Supply

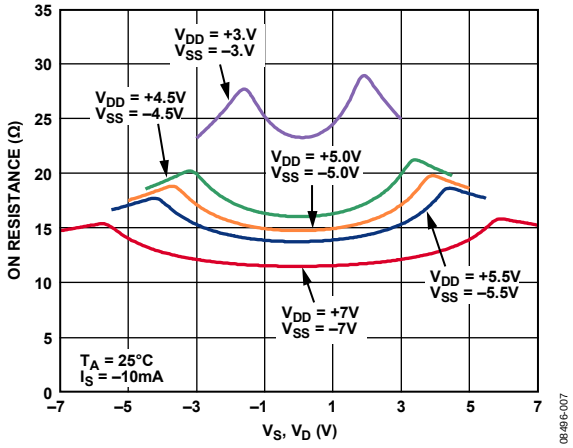


Figure 10. On Resistance as a Function of V_D (Vs), Dual Supply

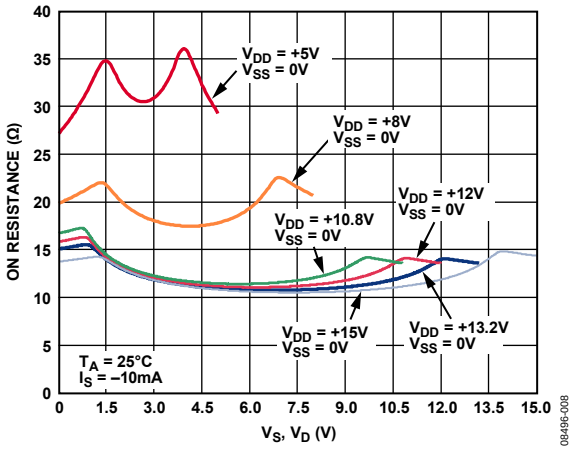


Figure 11. On Resistance as a Function of V_D (V_S), Single Supply

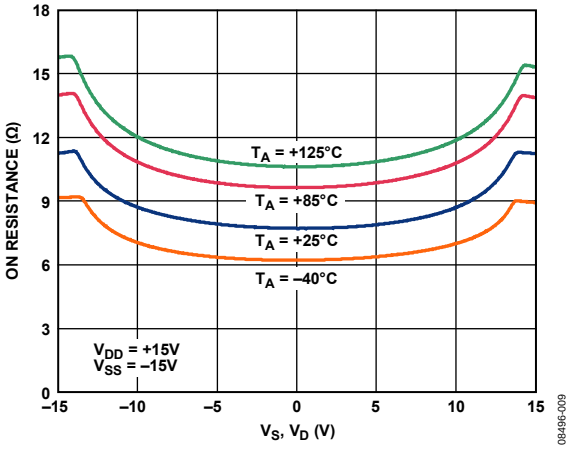


Figure 12. On Resistance as a Function of V_D (V_S) for Different Temperatures, 15 V Dual Supply

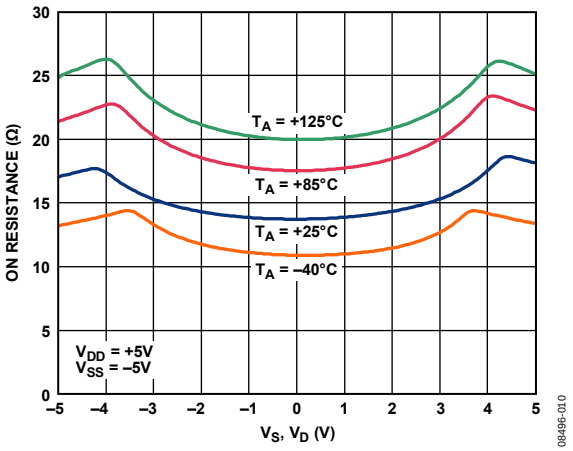


Figure 13. On Resistance as a Function of V_D (V_S) for Different Temperatures, 5 V Dual Supply

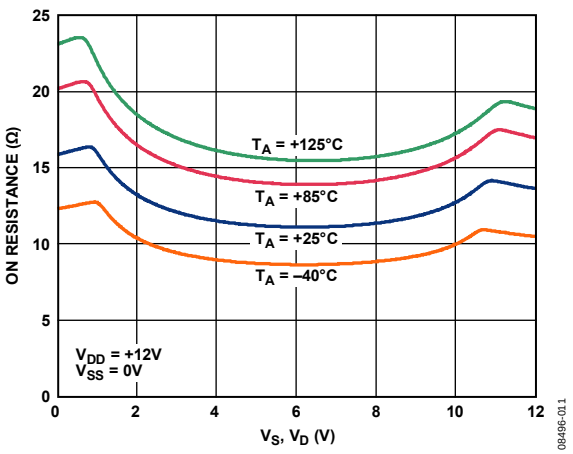


Figure 14. On Resistance as a Function of V_D (V_S) for Different Temperatures, 12 V Single Supply

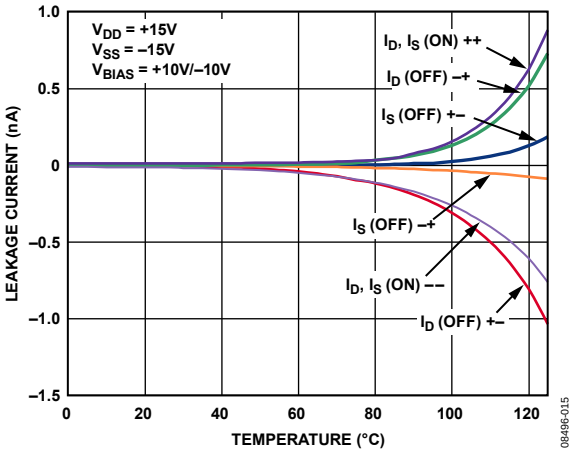


Figure 15. Leakage Current as a Function of Temperature, 15 V Dual Supply

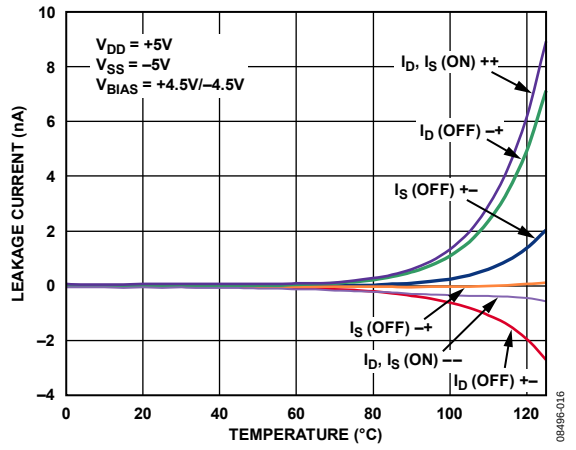


Figure 16. Leakage Current as a Function of Temperature, 5 V Dual Supply

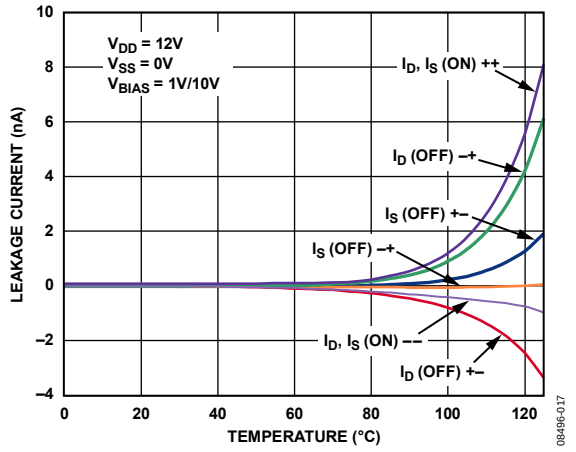


Figure 17. Leakage Current as a Function of Temperature, 12 V Single Supply

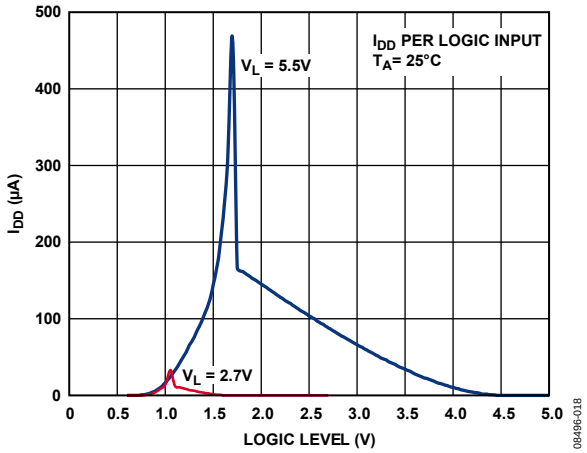


Figure 18. I_{DD} vs. Logic Level

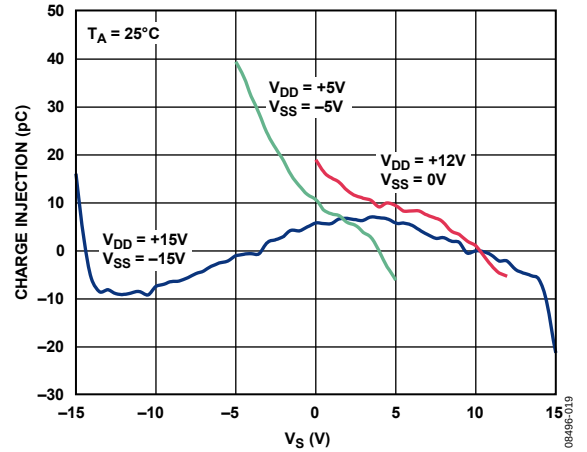


Figure 19. Charge Injection vs. Source Voltage

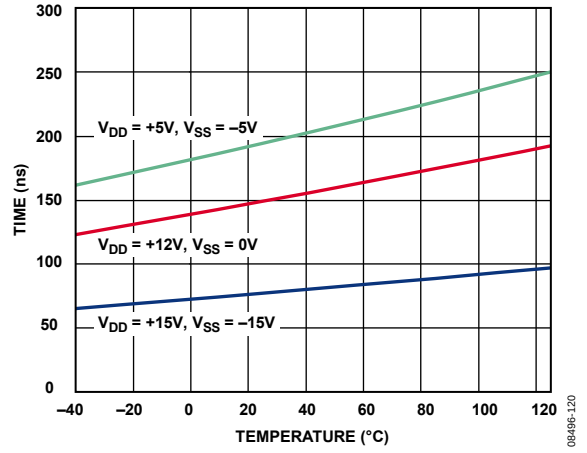


Figure 20. Transition Time vs. Temperature

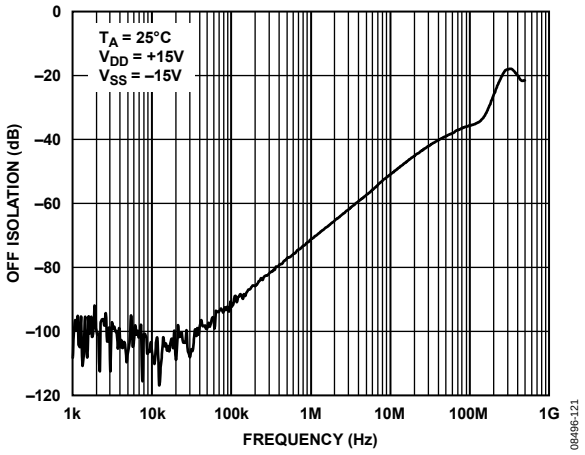


Figure 21. Off Isolation vs. Frequency

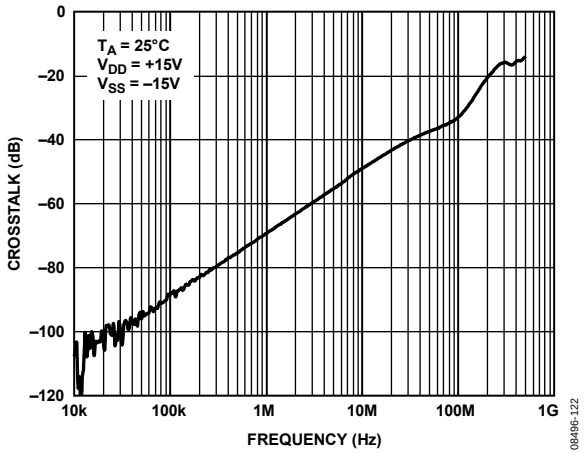


Figure 22. ADG1438 Crosstalk vs. Frequency

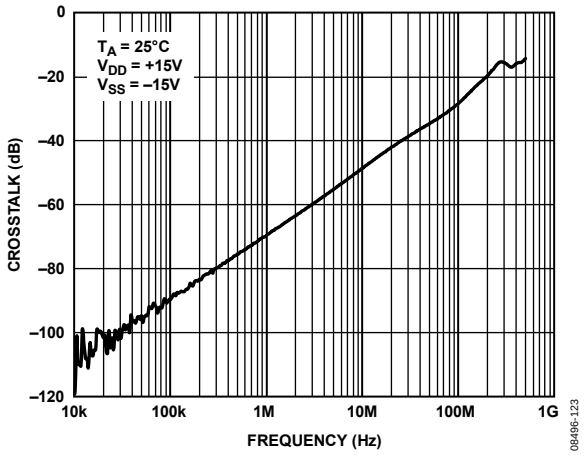


Figure 23. ADG1439 Crosstalk vs. Frequency

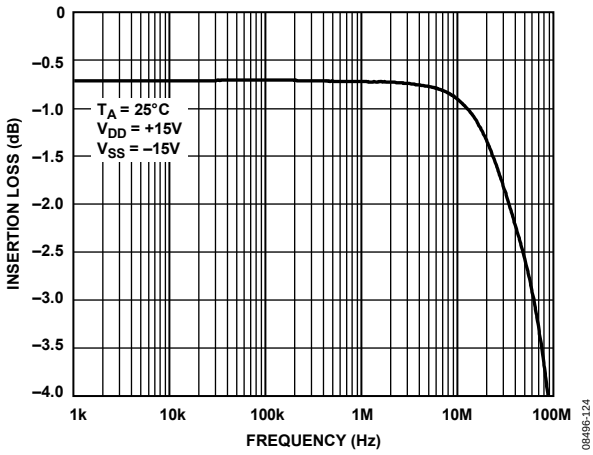


Figure 24. ADG1438 On Response vs. Frequency

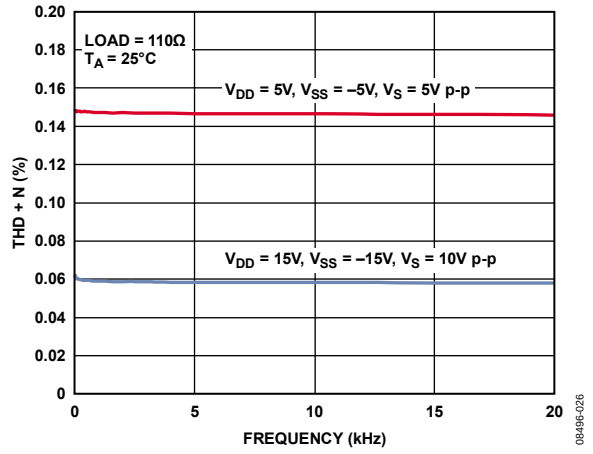


Figure 25. THD + N vs. Frequency

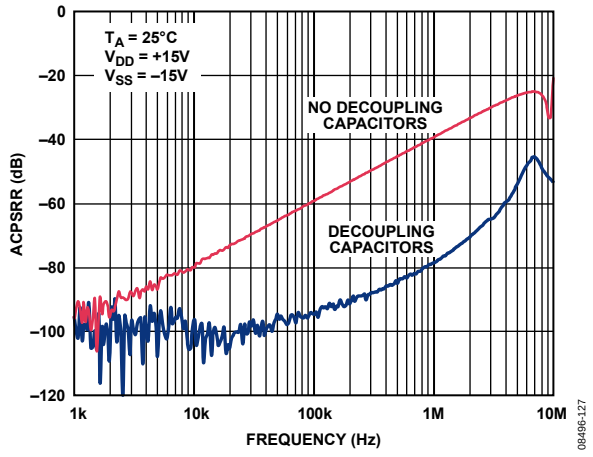


Figure 26. ACPSRR vs. Frequency

TEST CIRCUITS

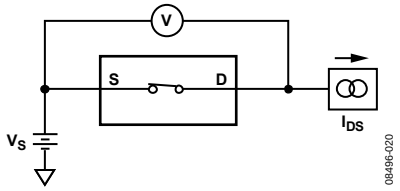


Figure 27. On Resistance

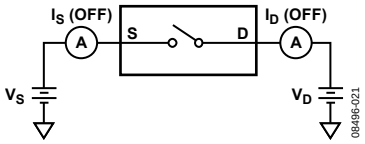


Figure 28. Off Leakage

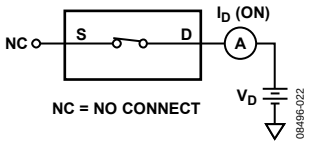


Figure 29. On Leakage

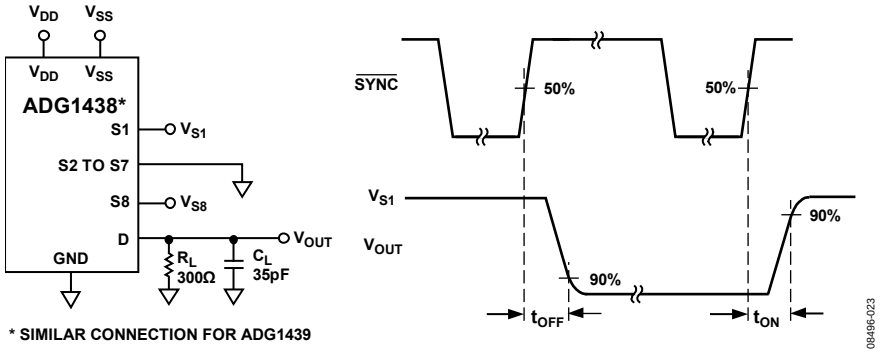


Figure 30. Switching Times, t_{ON}/t_{OFF}

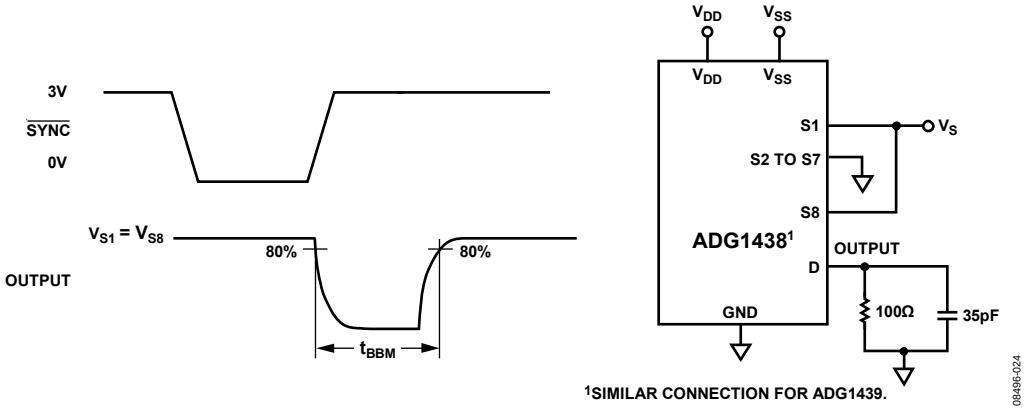


Figure 31. Break-Before-Make Delay, t_{BBM}

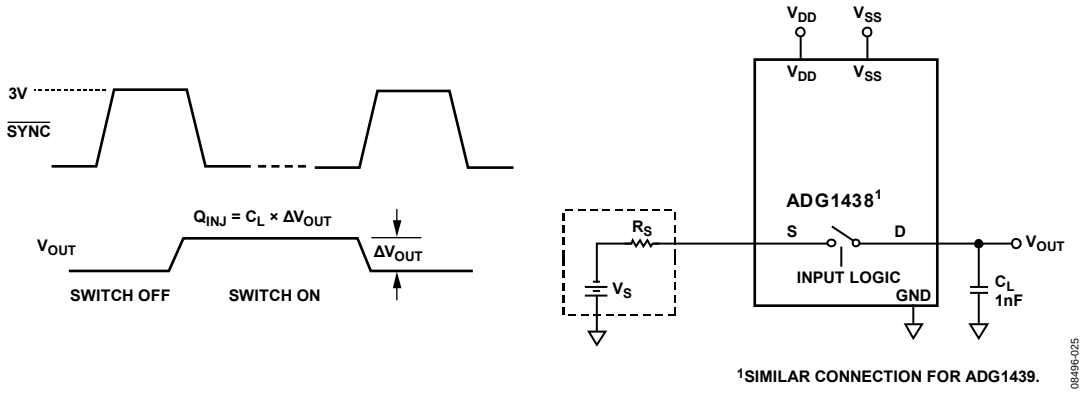


Figure 32. Charge Injection

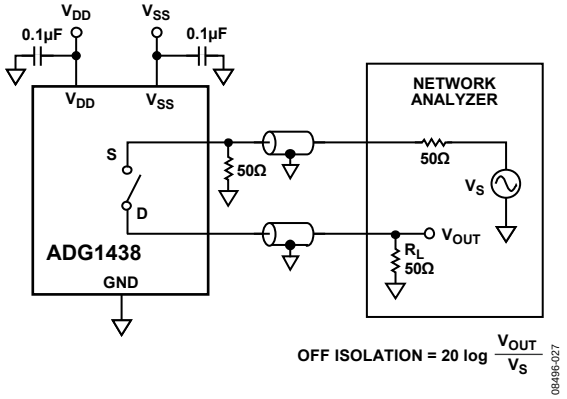


Figure 33. Off Isolation

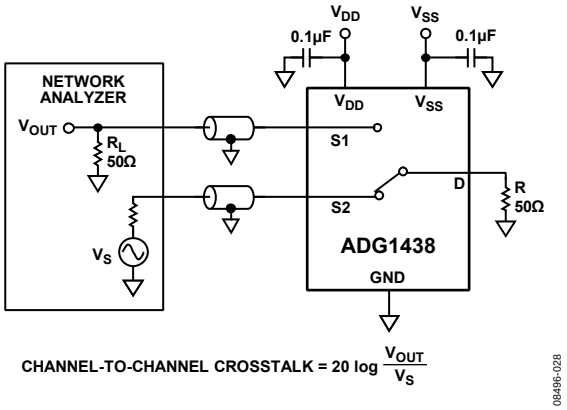


Figure 34. Channel-to-Channel Crosstalk

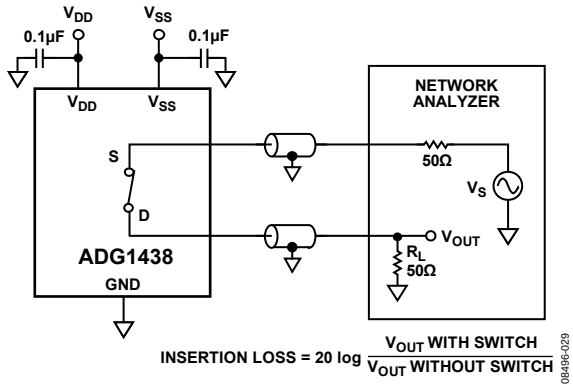


Figure 35. Insertion Loss

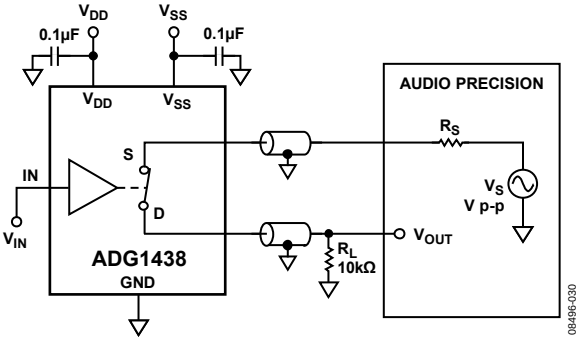


Figure 36. THD + Noise

TERMINOLOGY

R_{ON}
Ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}
Difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$
Flatness that is defined as the difference between the maximum and minimum values of on resistance as measured over the specified analog signal range..

I_S (Off)
Source leakage current when the switch is off.

I_D (Off)
Drain leakage current when the switch is off.

I_D, I_S (On)
Channel leakage current when the switch is on.

V_D (V_S)
Analog voltage on Terminal D (drain terminal) and Terminal S (source terminals, S1 to S8).

C_S (Off)
Channel input capacitance for off condition.

C_D (Off)
Channel output capacitance for off condition.

C_D, C_S (On)
On switch capacitance.

C_{IN}
Digital input capacitance.

t_{ON} (EN)

Delay time between the 50% and 90% points of the digital input and the switch on condition.

t_{OFF} (EN)
Delay time between the 50% and 90% points of the digital input and the switch off condition.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital input and the switch on condition when switching from one address state to another.

t_{BBM}
Off time measured between the 80% point of both switches when switching from one address state to another.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

Off Isolation
A measure of unwanted signal coupling through an off channel.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth
Frequency at which the output is attenuated by 3 dB.

On Response
Frequency response of the on switch.

Total Harmonic Distortion (THD + N)
Ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)
A measure of the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Insertion Loss
The loss due to the on resistance of the switch.

THEORY OF OPERATION

The ADG1438 and ADG1439 are serially controlled, 8-channel and dual 4-channel matrix switches, respectively. While providing the normal multiplexing and demultiplexing functions, these devices also provide the user with more flexibility as to where a signal can be routed. Each of the eight bits of the 8-bit write corresponds to one switch of the device. Logic 1 in a particular bit position turns the switch on, whereas Logic 0 turns the switch off. Because each switch is independently controlled by an individual bit, this provides the option of having any, all, or none of the switches on. This feature may be particularly useful in the demultiplexing application where the user may wish to direct one signal from the drain to a number of outputs (sources). Care must be taken, however, in the multiplexing situation where a number of inputs may be shorted together (separated only by the small on resistance of the switch).

SERIAL INTERFACE

The ADG1438/ADG1439 has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN pins) that is compatible with SPI, QSPI, and MICROWIRE interface standards, as well as most DSPs (see Figure 3 for a timing diagram of a typical write sequence).

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. This enables the input shift register. Data from the DIN line is clocked into the 8-bit input shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the ADG1438/ADG1439 compatible with high speed DSPs.

Data can be written to the shift register in more or fewer than eight bits. In each case, the shift register retains the last eight bits that are written. When all eight bits are written into the shift register, the $\overline{\text{SYNC}}$ line is brought high again. The switches are updated with the new configuration, and the input shift register is disabled. With $\overline{\text{SYNC}}$ held high, the input shift register is disabled so that further data or noise on the DIN line has no effect on the shift register.

Data appears on the SDO pin on the rising edge of SCLK, suitable for daisy-chaining or readback, delayed by eight bits.

INPUT SHIFT REGISTER

The input shift register is eight bits wide, as shown in Table 12 and Table 13. Each bit controls one switch. These data bits are transferred to the switch register on the rising edge of $\overline{\text{SYNC}}$.

Table 12. ADG1438 Input Shift Register Bit Map[1]

MSB							LSB
DB7	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
S8	S7	S6	S5	S4	S3	S2	S1

[1] Logic 0 = switch off, and Logic 1 = switch on.

Table 13. ADG1439 Input Shift Register Bit Map[1]

MSB							LSB
DB7	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
S4B	S3B	S2B	S1B	S4A	S3A	S2A	S1A

[1] Logic 0 = switch off, and Logic 1 = switch on.

POWER-ON RESET

The ADG1438/ADG1439 contain a power-on reset circuit. On power-up of the device, all switches are off, and the internal shift register is filled with zeros and remains so until a valid write takes place.

The part also has a $\overline{\text{RESET}}$ pin. When the $\overline{\text{RESET}}$ pin is low, all switches are off, and the appropriate registers are cleared to 0.

DAISY-CHAINING

For systems that contain several switches, the SDO pin can be used to daisy-chain several devices together. The SDO pin can also be used for diagnostic purposes and to provide serial readback where the user wants to read back the switch contents.

The SDO pin is an open-drain output that should be pulled to the V_L supply with an external resistor.

The SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than eight clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting this line to the DIN input on the next switch in the chain, a multiswitch interface is constructed. Each switch in the system requires eight clock pulses; therefore, the total number of clock cycles must equal 8N, where N is the total number of devices in the chain.

When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high. This prevents any further data from being clocked into the input shift register.

The serial clock can be a continuous or a gated clock. A continuous SCLK source can be used only if $\overline{\text{SYNC}}$ can be held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data. Gated clock mode reduces power consumption by reducing the active clock time.

OUTLINE DIMENSIONS

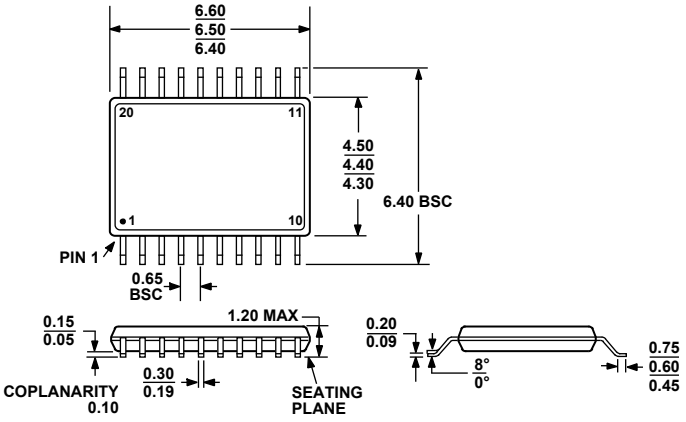


Figure 37. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

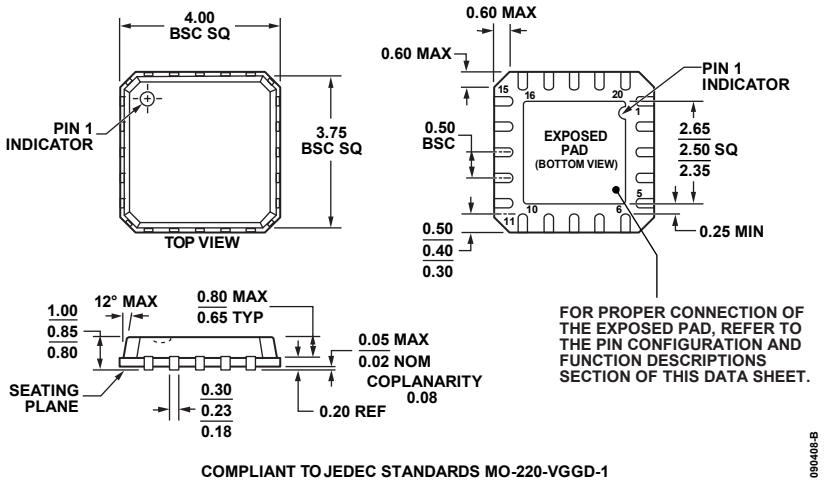


Figure 38. 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad (CP-20-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1438BRUZ[1]	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
ADG1438BRUZ-REEL7[1]	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
ADG1438BCPZ-REEL7[1]	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-20-4
ADG1439BRUZ[1]	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
ADG1439BRUZ-REEL7[1]	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
ADG1439BCPZ-REEL7[1]	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-20-4

[1] Z = RoHS Compliant Part.

D08496-0-10/09(0)