VNQ600AP-E

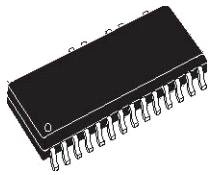
Quad channel high side driver

Features

Type	$R_{DS(on)}$ (1)	I_{lim}	V_{CC}
VNQ600AP-E	35 mΩ	25 A	36 V

1. Per each channel

- DC short circuit current: 25 A
- CMOS compatible inputs
- Proportional load current sense
- Undervoltage and overvoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Current limitation
- Very low standby power dissipation
- Protection against: loss of ground and loss of V_{CC}
- Reverse battery protection[a]
- In compliance with the 2002/95/EC european directive



SO-28 (DOUBLE ISLAND)

Description

The VNQ600AP-E is a quad HSD formed by assembling two VND600-E chips in the same SO-28 package. The VND600-E is a monolithic device designed in STMicroelectronics VIPower M0-3 Technology. The VNQ600AP-E is intended for driving any type of multiple loads with one side connected to ground. This device has four independent channels and four analog sense outputs which deliver currents proportional to the outputs currents. Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. Device automatically turns off in case of ground pin disconnection.

a. See *Application schematic on page 14*.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-28	VNQ600AP-E	VNQ600APTR-E

Contents

1 Block diagram and pin description 5

2 Electrical specifications 7

2.1 Absolute maximum ratings 7

2.2 Thermal data 8

2.3 Electrical characteristics 8

3 Application information 14

3.1 GND protection network against reverse battery 14

3.2 Load dump protection 15

3.3 Microcontroller I/O protection 15

3.4 Electrical characteristics curves 17

3.5 Maximum demagnetization energy (VCC = 13.5V) 19

4 Package and PCB thermal data 20

4.1 SO-28 thermal data 20

5 Package and packing information 23

5.1 ECOPACK® packages 23

5.2 SO-28 packing information 24

6 Revision history 25

List of tables

Table 1. Device summary . . . 1
Table 2. Suggested connections for unused and not connected pins . . . 6
Table 3. Absolute maximum rating . . . 7
Table 4. Thermal data (per island) . . . 8
Table 5. Power . . . 8
Table 6. Switching (V_{CC}=13 V) . . . 9
Table 7. V_{CC} - output diode . . . 9
Table 8. Logic input . . . 9
Table 9. Protections . . . 9
Table 10. Current sense (9 V< V_{CC}< 16 V) (see *Figure 7*) . . . 10
Table 11. Truth table . . . 10
Table 12. Electrical transient requirements (part 1/3) . . . 11
Table 13. Electrical transient requirements (part 2/3) . . . 11
Table 14. Electrical transient requirements (part 3/3) . . . 11
Table 15. Thermal calculation according to the PCB heatsink area . . . 20
Table 16. Thermal parameter . . . 22
Table 17. SO-28 mechanical data . . . 23
Table 18. Document revision history . . . 25

List of figures

Figure 1. Block diagram . . . 5
Figure 2. Configuration diagram (top view) . . . 6
Figure 3. Current and voltage conventions . . . 7
Figure 4. Switching characteristics (resistive load RL= 2.6 Ω). . . . 12
Figure 5. Waveforms (per each chip). . . . 13
Figure 6. Application schematic . . . 14
Figure 7. IOUT/ISENSE versus IOUT . . . 16
Figure 8. Off-state output current . . . 17
Figure 9. High level input current . . . 17
Figure 10. Input clamp voltage. . . . 17
Figure 11. Input high level . . . 17
Figure 12. Input low level . . . 17
Figure 13. Input hysteresis voltage . . . 17
Figure 14. Overvoltage shutdown . . . 18
Figure 15. ILIM vs Tcase . . . 18
Figure 16. Turn-on voltage slope . . . 18
Figure 17. Turn-off voltage slope . . . 18
Figure 18. On-state resistance vs Tcase . . . 18
Figure 19. On-state resistance vs VCC . . . 18
Figure 20. Maximum turn-off current versus load inductance . . . 19
Figure 21. Demagnetization . . . 19
Figure 22. SO-28 PC board . . . 20
Figure 23. Rthj-amb Vs PCB copper area in open box free air condition . . . 21
Figure 24. Thermal impedance junction ambient single pulse . . . 21
Figure 25. Thermal fitting model of a quad channel HSD in SO-28 . . . 22
Figure 26. SO-28 package dimensions . . . 23
Figure 27. SO-28 tube shipment (no suffix) . . . 24
Figure 28. SO-28 tape and reel shipment (suffix “TR”) . . . 24

1 Block diagram and pin description

Figure 1. Block diagram

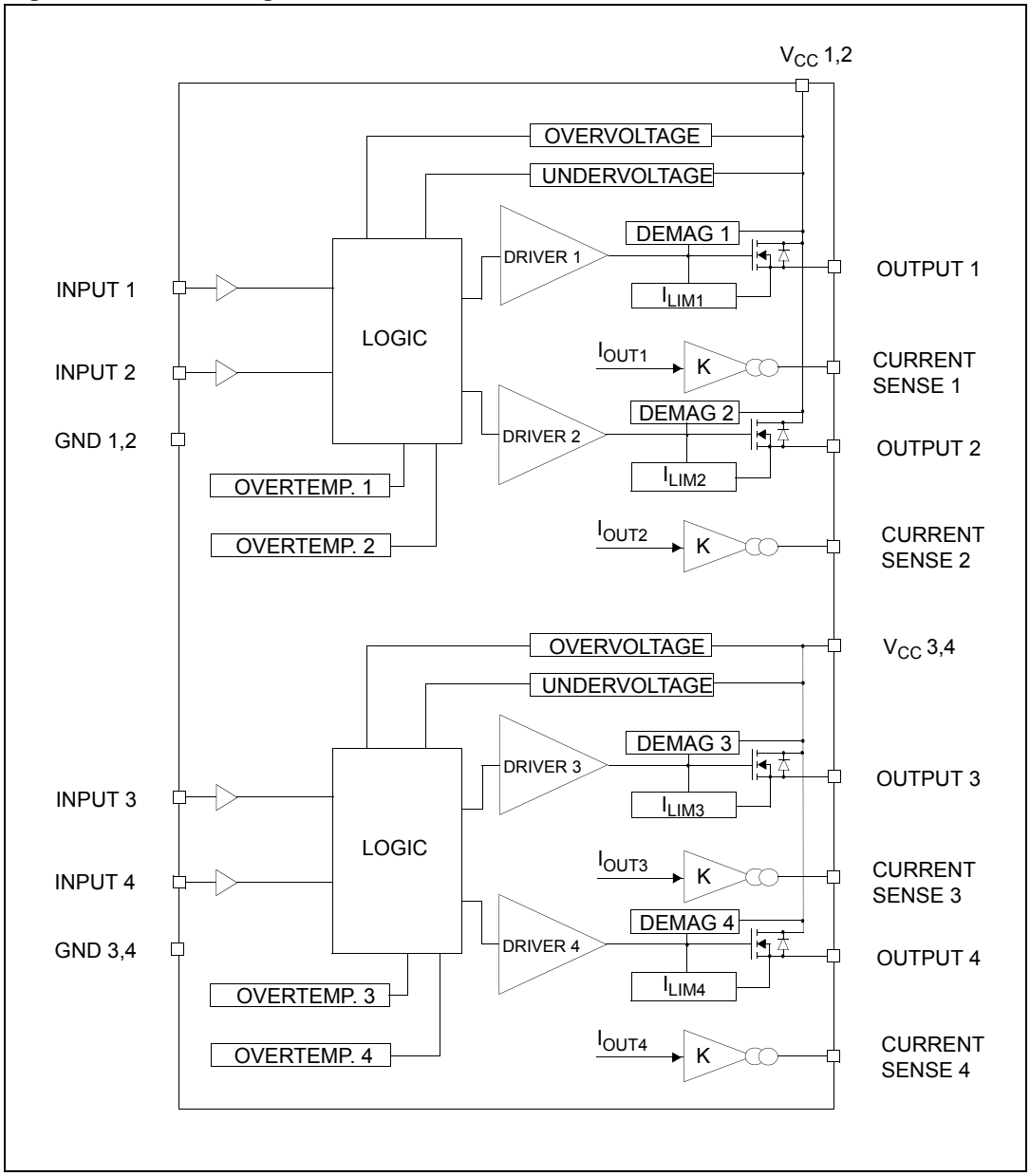


Figure 2. Configuration diagram (top view)

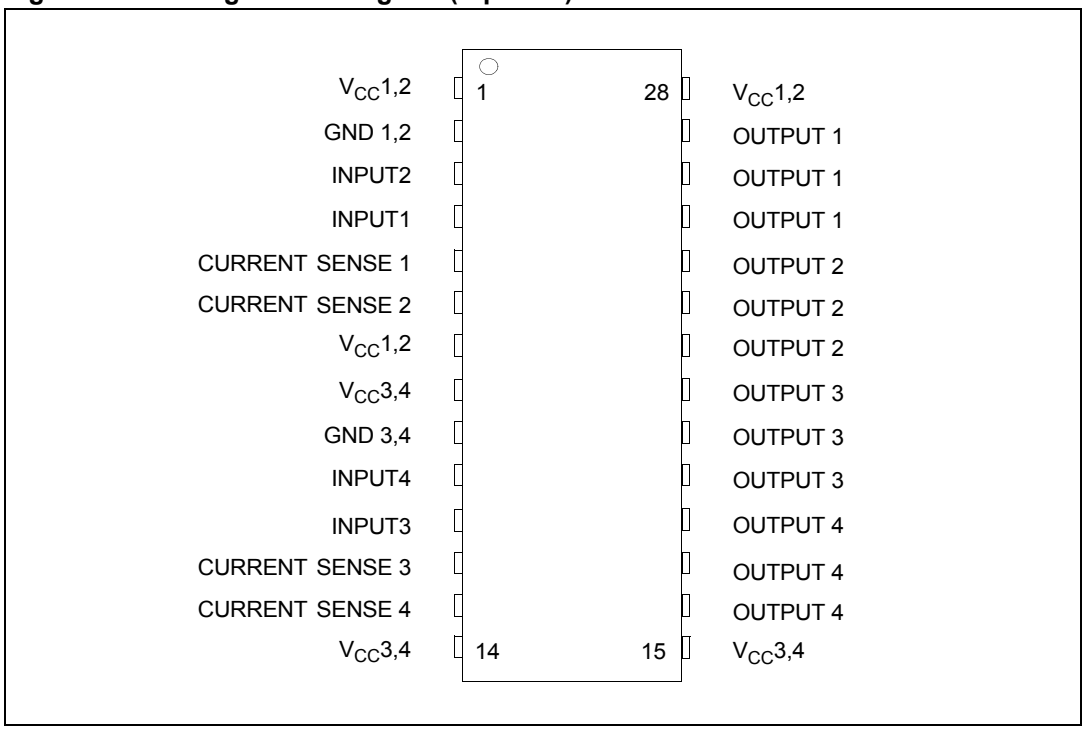
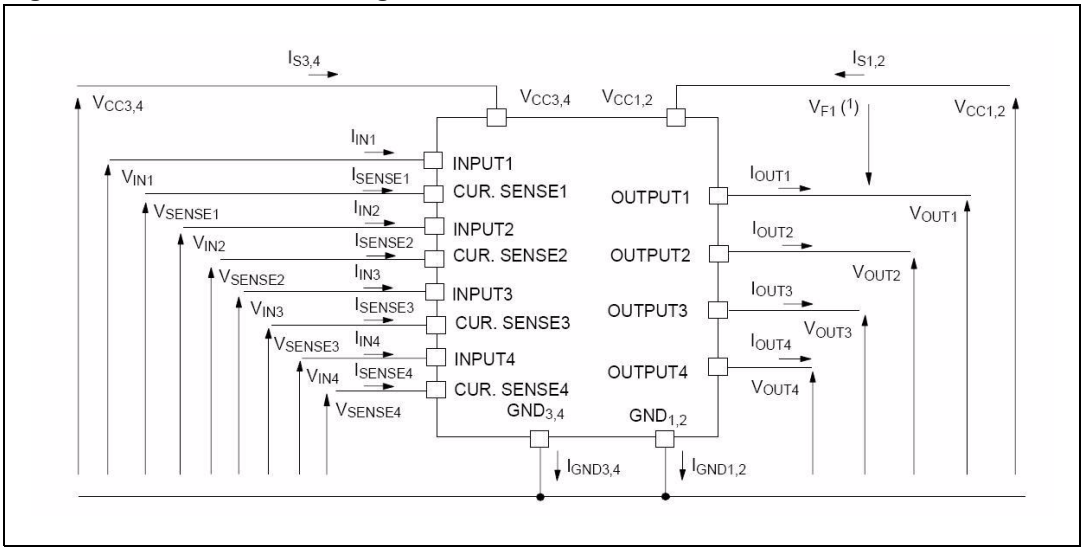


Table 2. Suggested connections for unused and not connected pins

Connection/pin	Current sense	N.C.	Output	Input
Floating	Not allowed	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 10 kΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



1. $V_{Fn} = V_{CCn} - V_{OUTn}$ during reverse battery condition

2.1 Absolute maximum ratings

Table 3. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (continuous)	41	V
$-V_{CC}$	Reverse supply voltage (continuous)	-0.3	V
I_{OUT}	Output current (continuous), for each channel	15	A
I_R	Reverse output current (continuous), for each channel	-15	A
I_{IN}	Input current	+/- 10	mA
V_{CSENSE}	Current sense maximum voltage	-3 +15	V V
I_{GND}	Ground current at $T_{pins} \leq 25$ °C (continuous)	-200	mA
V_{ESD}	Electrostatic discharge (Human Body Model: R=1.5 KΩ; C=100 pF) - Input - Current Sense - Output - V_{CC}	 4000 2000 5000 5000	 V V V V
E_{MAX}	Maximum switching energy (L=0.11 mH; R_L=0 Ω; V_{bat}=13.5 V; T_{jstart}=150 ºC; I_L=40 A)	126	mJ
P_{tot}	Power dissipation (per island) at T_{lead}=25 °C	6.25	W

Table 3. Absolute maximum rating (continued)

Symbol	Parameter	Value	Unit
T_j	Junction operating temperature	Internally limited	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data (per island)

Symbol	Parameter	Value		Unit
$R_{thj\text{-}lead}$	Thermal resistance Junction-lead (max)	15		°C/W
$R_{thj\text{-}amb}$	Thermal resistance Junction-ambient (one chip on max)	60(1)	44(2)	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient (two chips on max)	46(1)	31((2))	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5 cm^2 of Cu (at least 35 µm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.
2. When mounted on a standard single-sided FR-4 board with 6 cm^2 of Cu (at least 35 µm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

2.3 Electrical characteristics

Values specified in this section are for 8 V<V_{CC}<36 V; -40 °C< T_j <150 °C, unless otherwise specified.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}(1)	Operating supply voltage		5.5	13	36	V
V_{USD}(1)	Undervoltage shutdown		3	4	5.5	V
V_{OV}(1)	Overvoltage shutdown		36	-	-	V
R_{ON}	On-state resistance	I_{OUT}1,2,3,4=5 A; T_j=25 °C I_{OUT}1,2,3,4=5 A; T_j=150 °C I_{OUT}1,2,3,4=3 A; V_{CC}=6 V	-	-	35 70 120	mΩ mΩ mΩ
V_{clamp}	Clamp voltage	I_{CC}=20 mA(2)	41	48	55	V
I_S(1)	Supply current	Off-state; V_{CC}=13 V; V_{IN}=V_{OUT}=V_{SENSE}=0 V Off-state; V_{CC}=13 V; V_{IN}=V_{OUT}=V_{SENSE}=0V; T_j =25 °C On-state; V_{CC}=13 V; V_{IN}=5 V; I_{OUT}=0 A; R_{SENSE}=3.9 KΩ; V_{SENSE}=0 V	-	12 12	40 25 6	µA µA mA
$I_{L(off1)}$	Off-state output current	V_{IN}=V_{OUT}=V_{SENSE}=0V	0	-	50	µA

Table 5. Power (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{L(off3)}$	Off-state output current	$V_{IN}=V_{OUT}=V_{SENSE}=0$ V; $V_{CC}=13$ V; $T_j=125$ °C	-	-	5	µA
$I_{L(off4)}$	Off-state output current	$V_{IN}=V_{OUT}=V_{SENSE}=0$ V; $V_{CC}=13$ V; $T_j=25$ °C	-	-	3	µA

1. Per island
2. Vclamp and V_{OV} are correlated. Typical difference is 5 V.

Table 6. Switching (V_{CC}=13 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{D(on)}$	Turn-on delay time	R_L=2.6 Ω channels 1,2,3,4 (see *Figure 4*)	-	40	-	µs
$t_{D(off)}$	Turn-off delay time	R_L=2.6 Ω channels 1,2,3,4 (see *Figure 4*)	-	40	-	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L=2.6 Ω channels 1,2,3,4 (see *Figure 4*)	-	See relative diagram	-	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L=2.6 Ω channels 1,2,3,4 (see *Figure 4*)	-	See relative diagram	-	V/µs

Table 7. V_{CC} - output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	$-I_{OUT}$=2.3 A; T_j=150 °C	-	-	0.6	V

Table 8. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage		-	-	1.25	V
V_{IH}	High level input voltage		3.25	-	-	V
$V_{I(hyst)}$	Input hysteresis voltage		0.5	-	-	V
I_{IL}	Low level input current	V_{IN}=1.25 V	20	65	-	µA
I_{Ih}	High level input current	V_{IN}=3.25 V	-	75	110	µA
V_{ICL}	Input clamp voltage	I_{IN}=1 mA I_{IN}= -1 mA	6	6.8 -0.7	8	V V

Table 9. Protections(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{lim}	DC short circuit current	V_{CC}=13 V 5.5 V<V_{CC}<36 V	25	40	70 70	A A
T_{TSD}	Thermal shutdown temperature		150	175	200	°C
T_R	Thermal reset temperature		135	-	-	°C
T_{hyst}	Thermal hysteresis		7	15	-	°C
V_{demag}	Turn-off output voltage clamp	I_{OUT}=2 A; L=6 mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V
V_{ON}	Output voltage drop limitation	I_{OUT}=0.5 A; T_j= -40 °C...+150 °C	-	50	-	mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Current sense (9 V< V_{CC}< 16 V) (see *Figure 7*)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K1	I_{OUT}/I_{SENSE}	$I_{OUT1,2}$=0.35 A; V_{SENSE}=0.5 V; Tj= -40 °C...+150 °C	3100	4150	5560	
K2	I_{OUT}/I_{SENSE}	I_{OUT}=2 A; V_{SENSE}=2.5 V; Tj=-40 °C Tj= 25 °C...+150 °C	3750 4000	4600 4600	5700 5400	
K3	I_{OUT}/I_{SENSE}	I_{OUT}=4 A; V_{SENSE}=4 V; T_j=-40 °C Tj= 25 °C...+150 °C	4000 4100	4500 4500	5200 5150	
$V_{SENSE1,2}$	Max analog sense output voltage	V_{CC}=5.5 V; $I_{OUT1,2}$=2 A; R_{SENSE}=10 KΩ V_{CC}>8 V; $I_{OUT1,2}$=4 A; R_{SENSE}=10 KΩ	2 4	-	-	V V
V_{SENSEH}	Analog sense output voltage in over temperature condition	V_{CC}=13 V; R_{SENSE}=3.9 KΩ	-	5	-	V
$R_{VSENSEH}$	Analog sense output impedance in over temperature condition	V_{CC}=13 V; T_j>T_{TSD}; All channels open	-	400	-	Ω
t_{DSENSE}	Current sense delay response	to 90% I_{SENSE}(1)	-	-	500	µs

1. Current sense signal delay after positive input slope.

Table 11. Truth table

Conditions	Input	Output	Sense
Normal operation	L H	L H	0 Nominal
Over temperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overvoltage	L H	L L	0 0
Short circuit to GND	L H H	L L L	0 (T_j<T_{TSD}) 0 (T_j>T_{TSD}) V_{SENSEH}
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

Table 12. Electrical transient requirements (part 1/3)

ISO T/R 7637/1 test pulse	Test level				
	I	II	III	IV	Delays and impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms, 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms, 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs, 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs, 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

Table 13. Electrical transient requirements (part 2/3)

ISO T/R 7637/1 test pulse	Test levels result			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Table 14. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 4. Switching characteristics (resistive load R_L= 2.6 Ω)

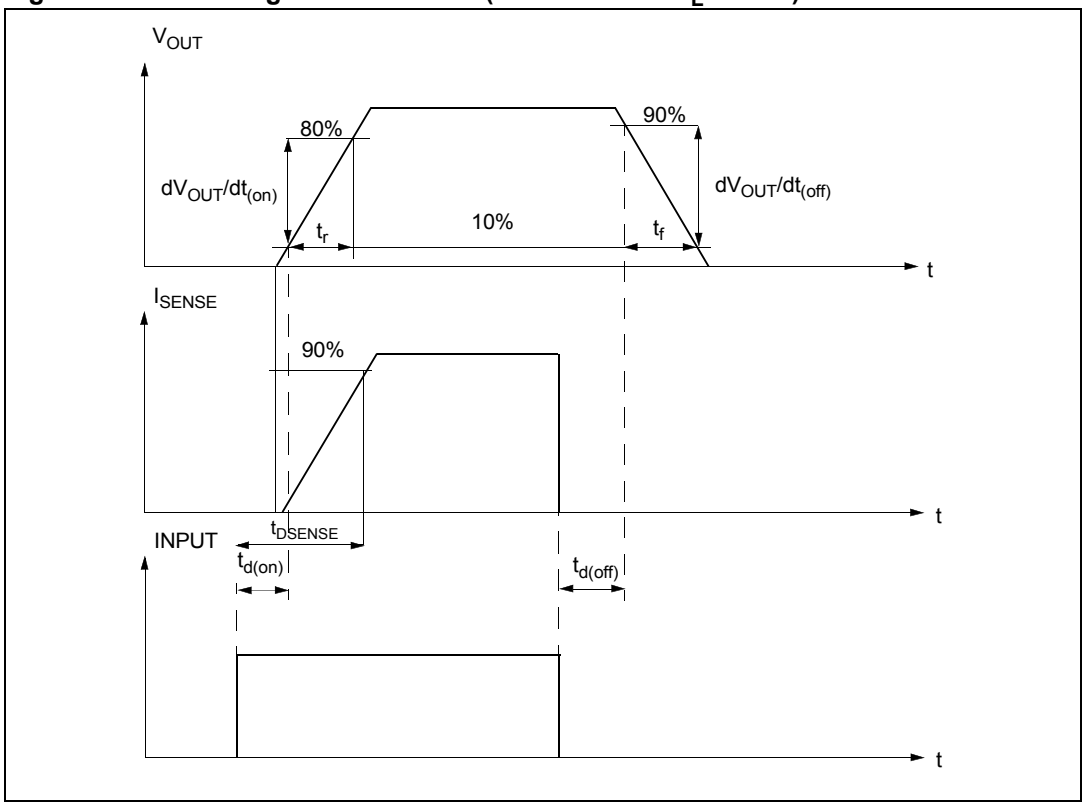
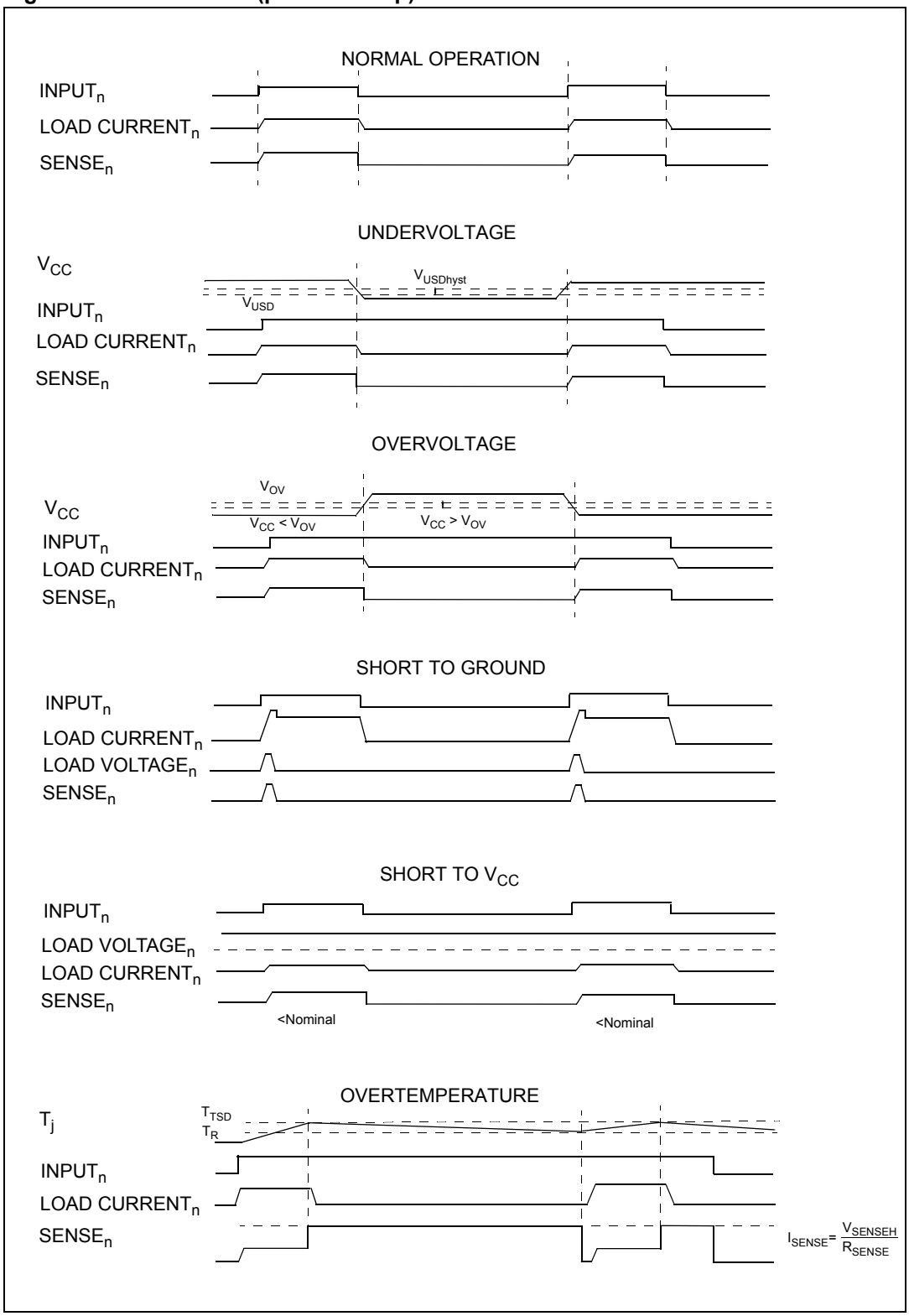
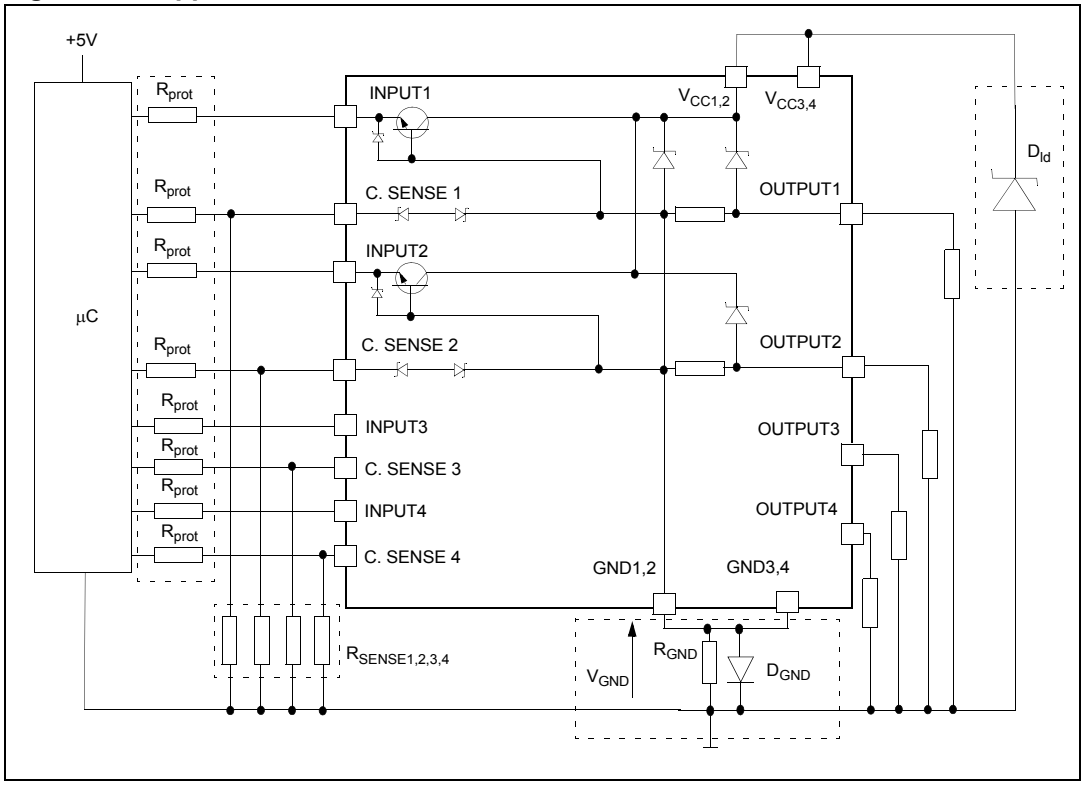


Figure 5. Waveforms (per each chip)



3 Application information

Figure 6. Application schematic



Note: Channels 3 and 4 have the same internal circuit as channel 1 and 2

3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load. The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600\ mV / 2(I_{S(on)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D = (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output

values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line. A resistor (R_{GND}=1 kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (≅ 600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in input line is also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

Safest configuration for unused input pin is to leave it unconnected, while unused sense pin has to be connected to ground pin.

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} maximum DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than those shown in the ISO T/R 7637/1 table.

3.3 Microcontroller I/O protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os:

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$$

Example

For the following conditions:

V_{CCpeak}= -100 V

$I_{latchup} \geq$ 20 mA

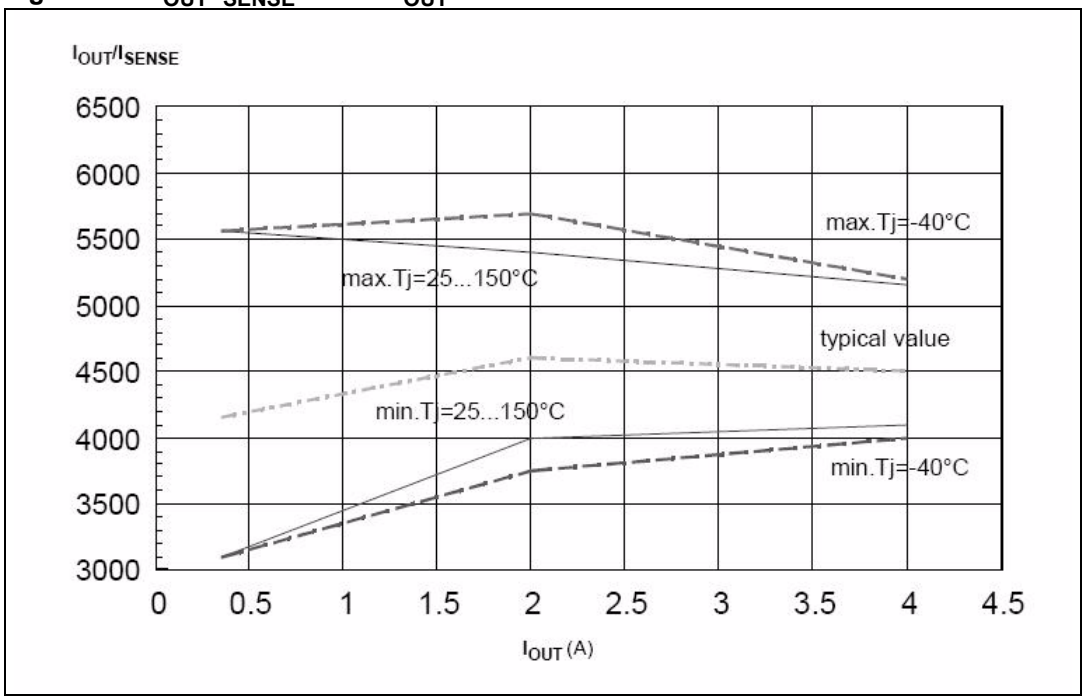
$V_{OH\mu C} \geq$ 4.5 V

5 kΩ ≤ R_{prot} ≤ 65 kΩ.

Recommended values are:

R_{prot} =5 kΩ

Figure 7. I_{OUT}/I_{SENSE} versus I_{OUT}



3.4 Electrical characteristics curves

Figure 8. Off-state output current

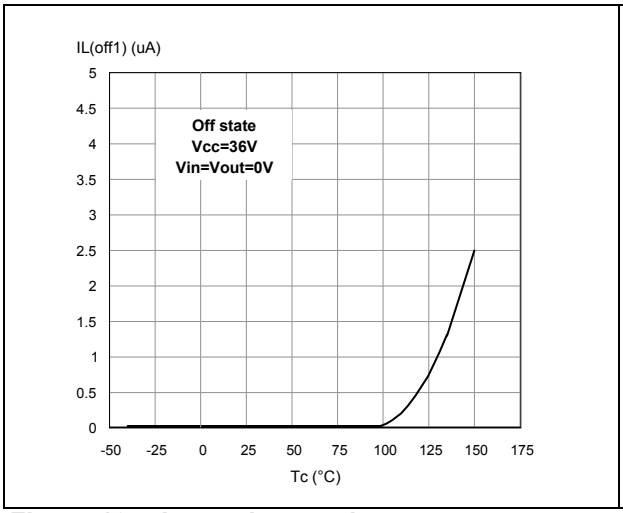


Figure 9. High level input current

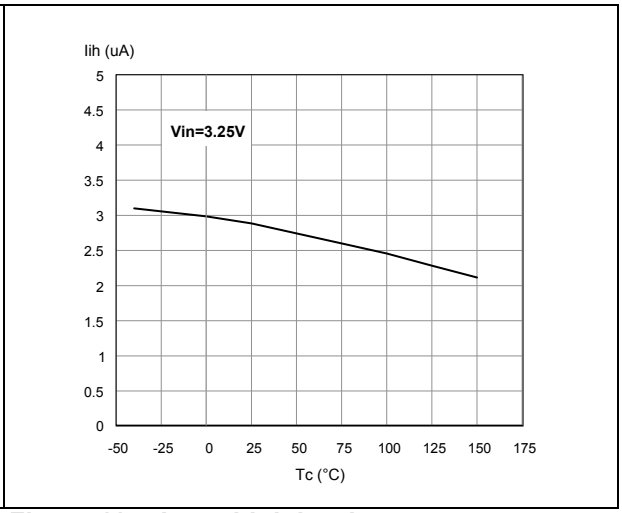


Figure 10. Input clamp voltage

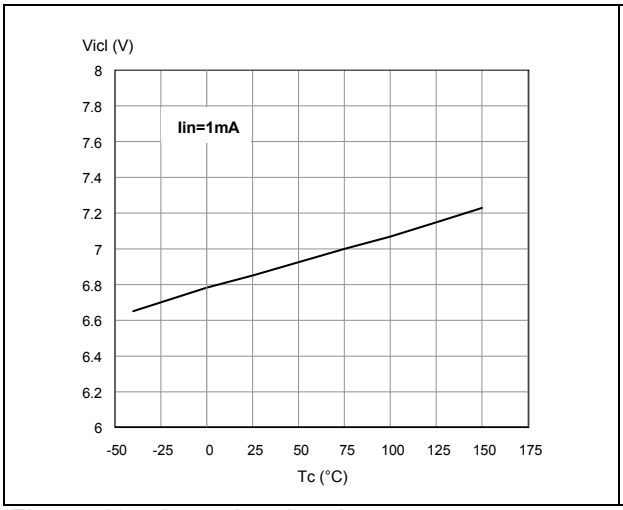


Figure 11. Input high level

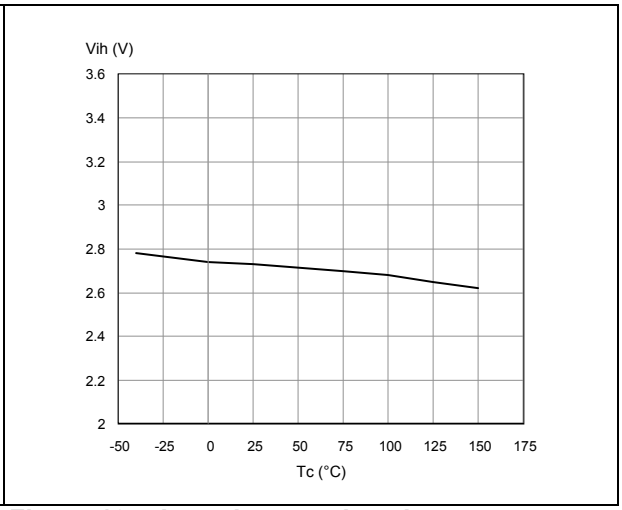


Figure 12. Input low level

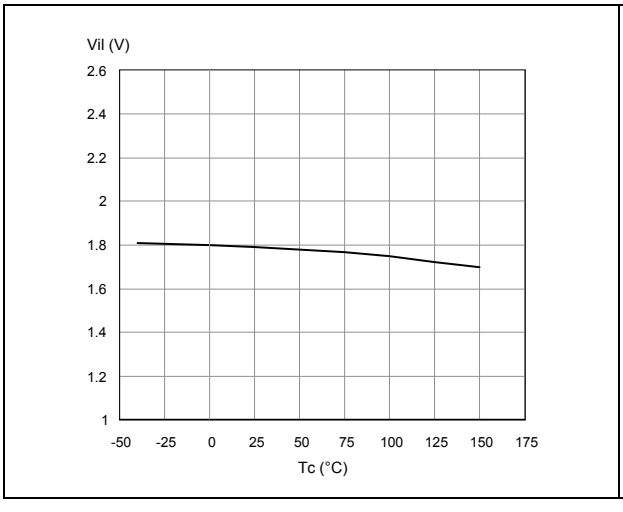


Figure 13. Input hysteresis voltage

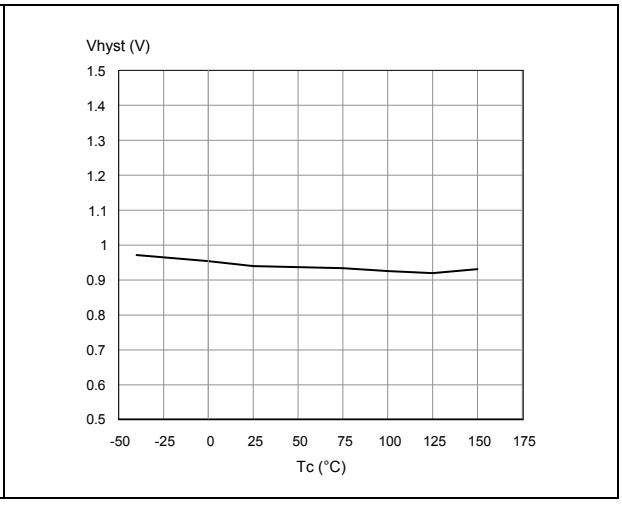


Figure 14. Overvoltage shutdown

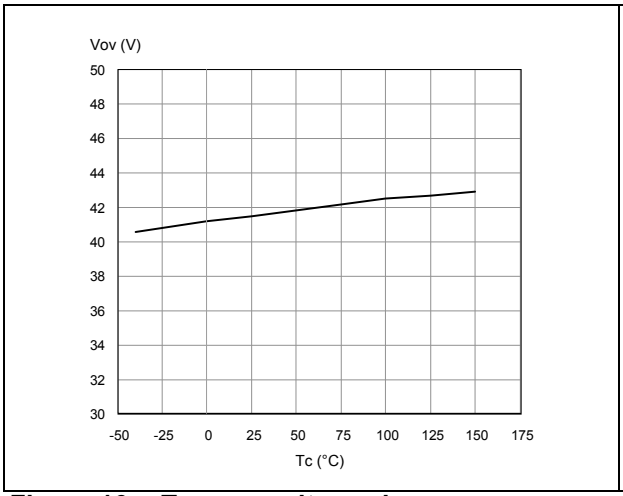


Figure 15. I_{LIM} vs T_{case}

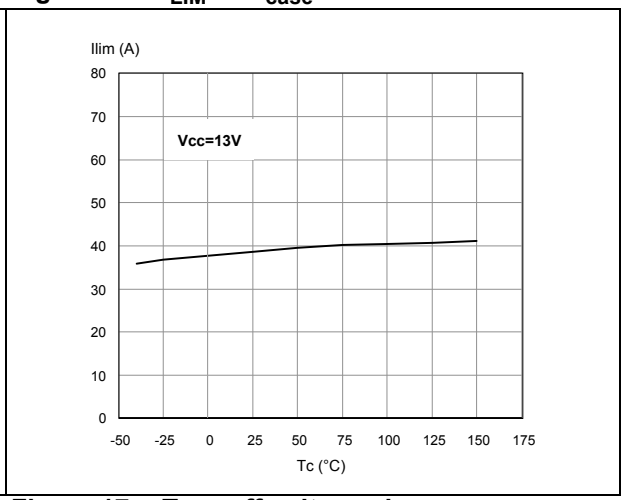


Figure 16. Turn-on voltage slope

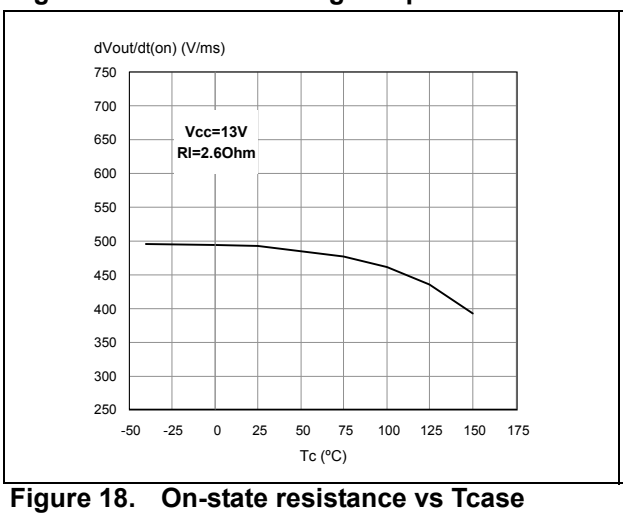


Figure 17. Turn-off voltage slope

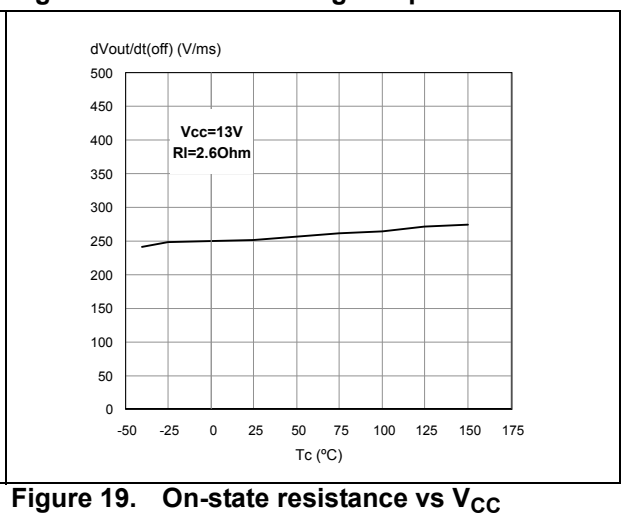


Figure 18. On-state resistance vs Tcase

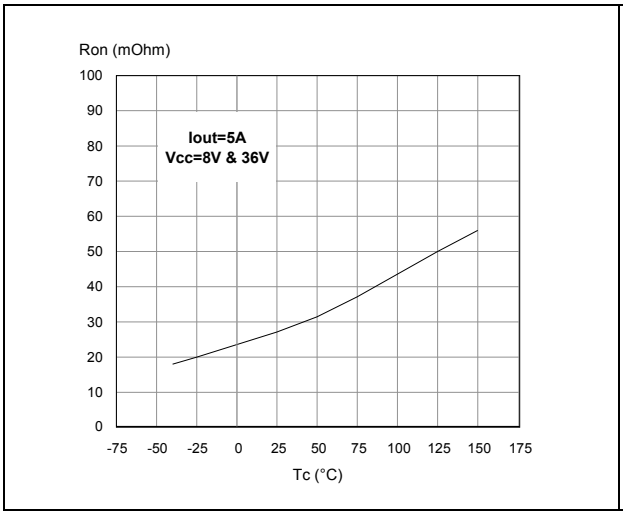
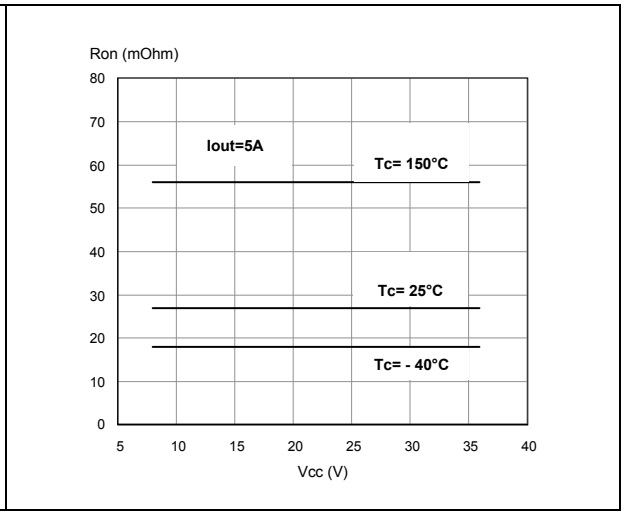
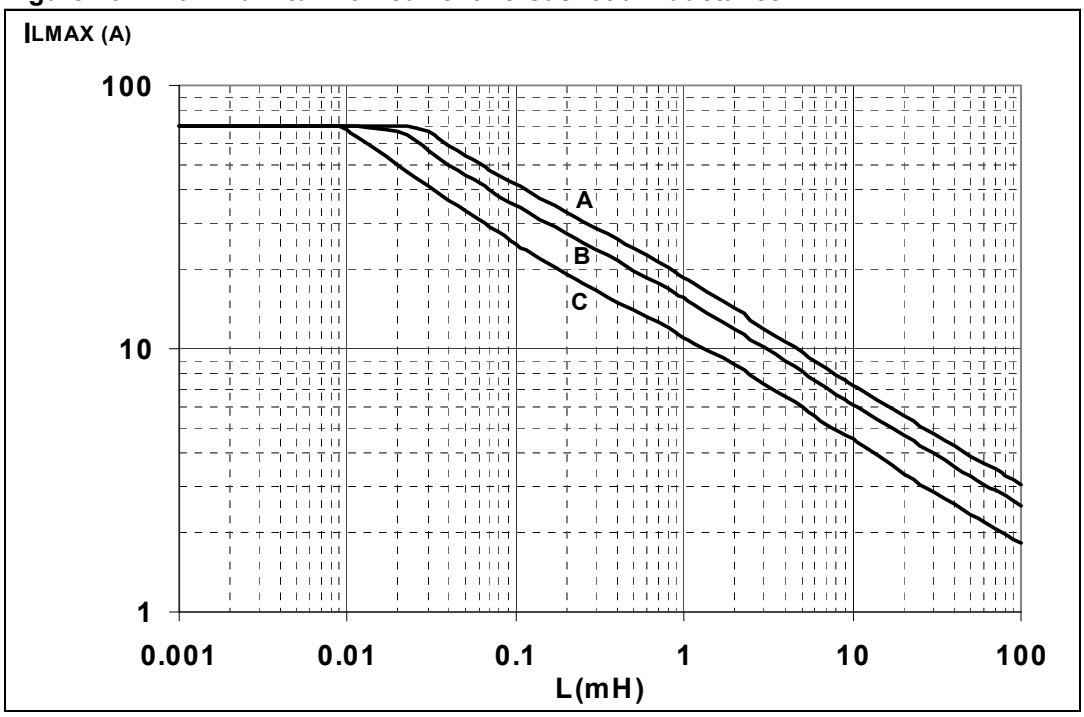


Figure 19. On-state resistance vs V_{CC}



3.5 Maximum demagnetization energy (VCC = 13.5V)

Figure 20. Maximum turn-off current versus load inductance



Legend:

A = Single Pulse at T_{Jstart}=150 ºC

B = Repetitive pulse at T_{Jstart}=100 ºC

C = Repetitive Pulse at T_{Jstart}=125 ºC

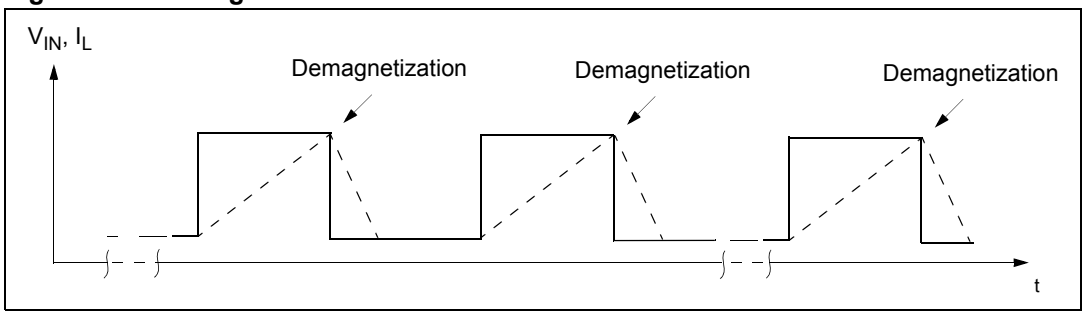
Conditions:

V_{CC}=13.5 V

Values are generated with RL=0 Ω

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

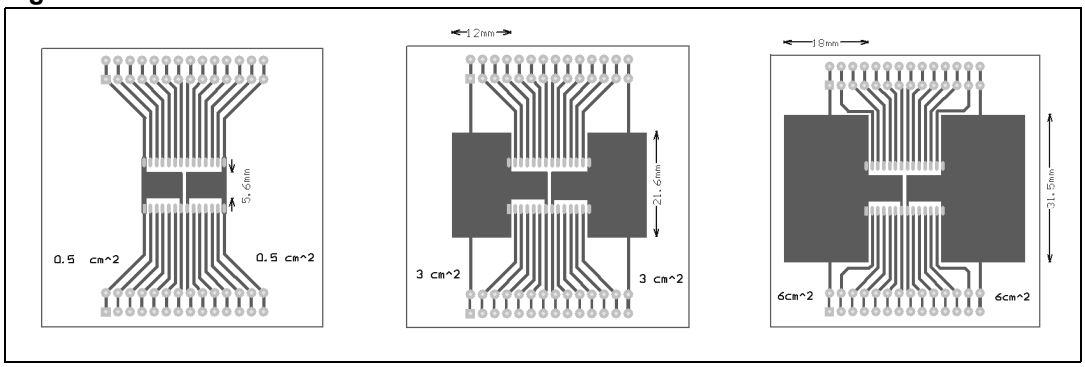
Figure 21. Demagnetization



4 Package and PCB thermal data

4.1 SO-28 thermal data

Figure 22. SO-28 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area=58 mm x 58 mm, PCB thickness=2 mm, Cu thickness=35 µm, Copper areas: 0.5 cm^2, 3 cm^2, 6 cm^2).

Table 15. Thermal calculation according to the PCB heatsink area

Chip 1	Chip 2	T_{jchip1}	T_{jchip2}	Note
On	Off	$R_{thA} \times P_{dchip1} + T_{amb}$	$R_{thC} \times P_{dchip1} + T_{amb}$	
Off	On	$R_{thC} \times P_{dchip2} + T_{amb}$	$R_{thA} \times P_{dchip2} + T_{amb}$	
On	On	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$P_{dchip1}=P_{dchip2}$
On	On	$(R_{thA} \times P_{dchip1}) + R_{thC} \times P_{dchip2} + T_{amb}$	$(R_{thA} \times P_{dchip2}) + R_{thC} \times P_{dchip1} + T_{amb}$	$P_{dchip1} \neq P_{dchip2}$

R_{thA} = Thermal resistance Junction to Ambient with one chip on

R_{thB} = Thermal resistance Junction to Ambient with both chips on and $P_{dchip1}=P_{dchip2}$

R_{thC} = Mutual thermal resistance

Figure 23. $R_{thj-amb}$ Vs PCB copper area in open box free air condition

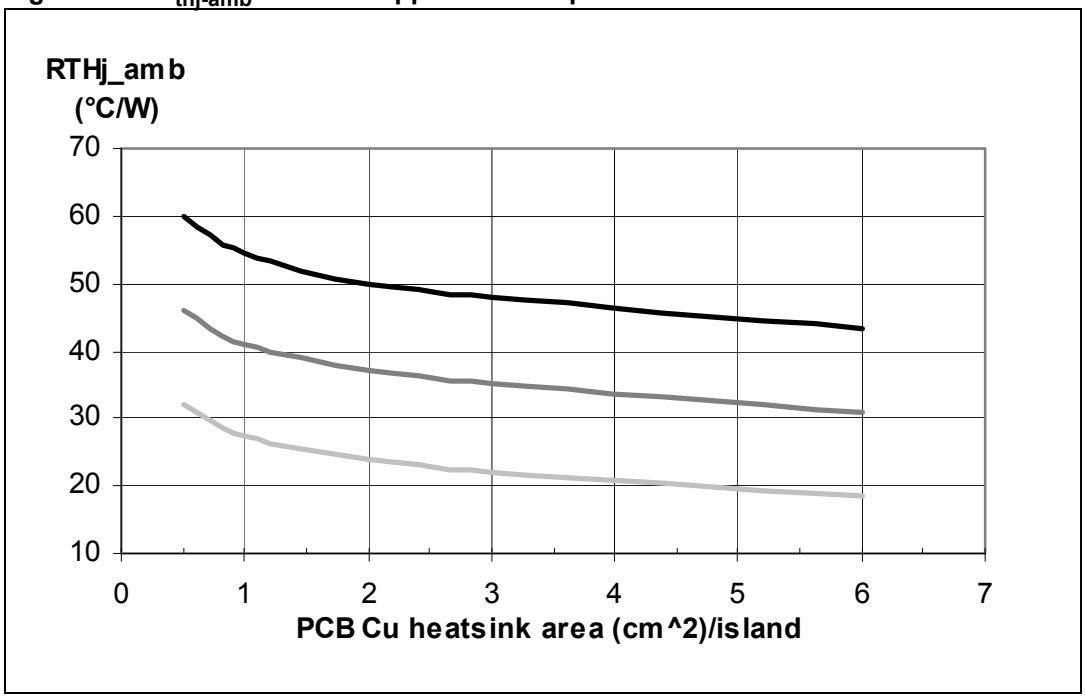
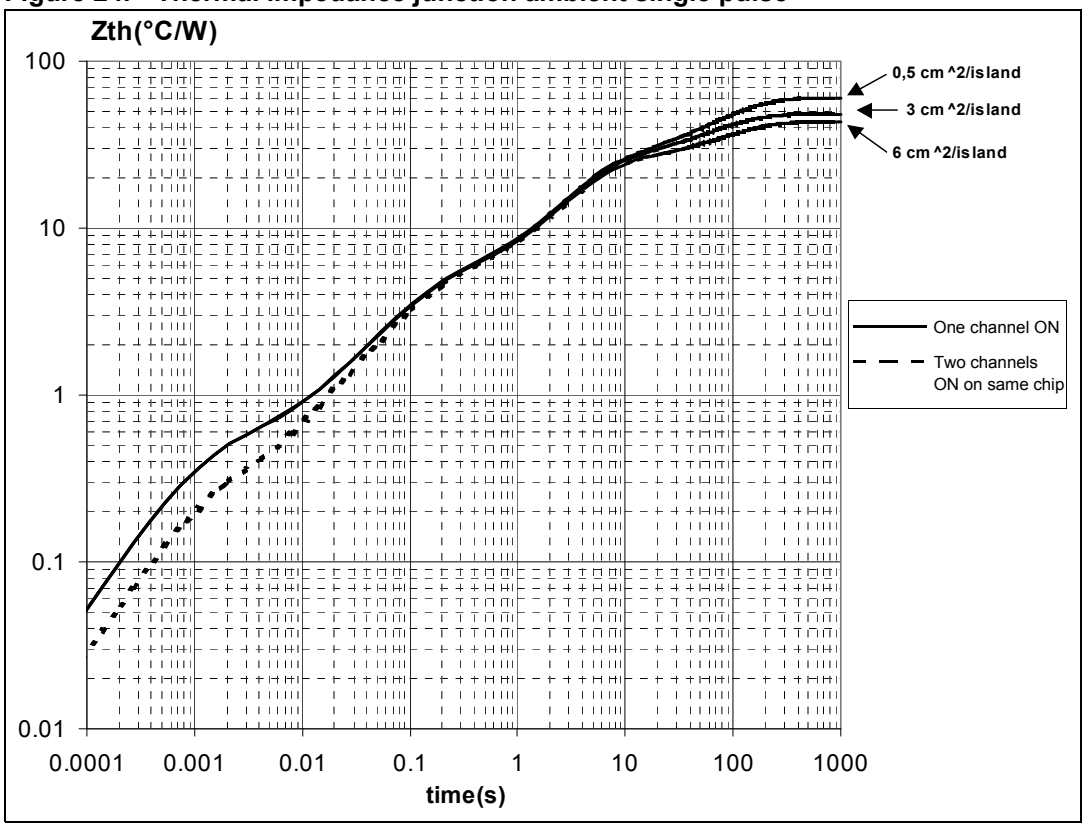


Figure 24. Thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_p / T$

Figure 25. Thermal fitting model of a quad channel HSD in SO-28

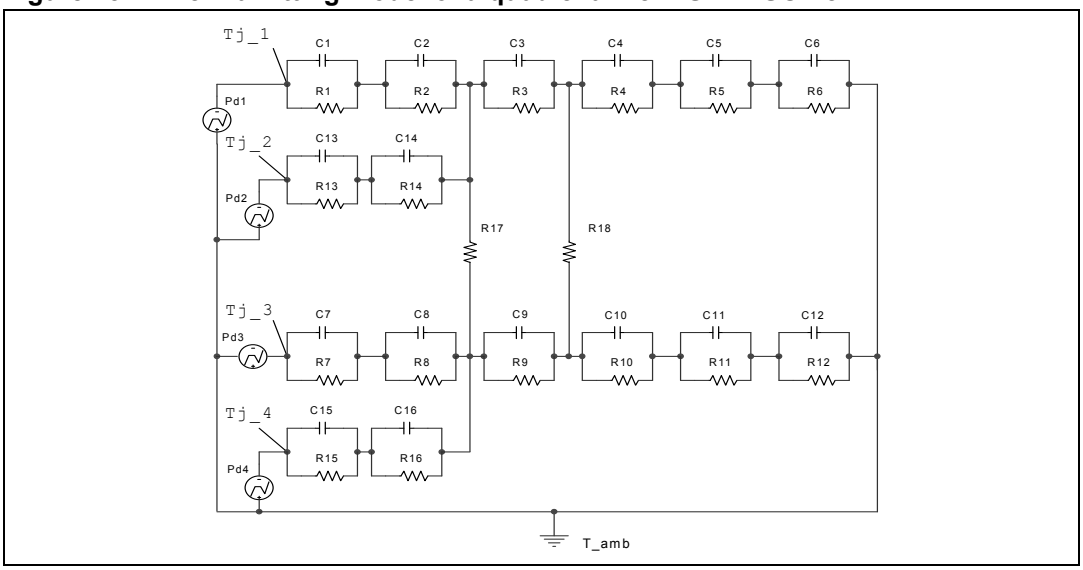


Table 16. Thermal parameter

Area/island (cm^2)	0.5	6
R1=R7=R13=R15 (°C/W)	0.05	-
R2=R8=R14=R16 (°C/W)	0.3	-
R3=R9 (°C/W)	3.4	-
R4=R10 (°C/W)	11	-
R5=R11 (°C/W)	15	-
R6=R12 (°C/W)	30	13
C1=C7=C13=C15 (W.s/°C)	0.001	-
C2=C8=C14=C16 (W.s/°C)	5.00E-03	-
C3=C9 (W.s/°C)	1.00E-02	-
C4=C10 (W.s/°C)	0.2	-
C5=C11 (W.s/°C)	1.5	-
C6=C12 (W.s/°C)	5	8
R17=R18 (°C/W)	150	-

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

Figure 26. SO-28 package dimensions

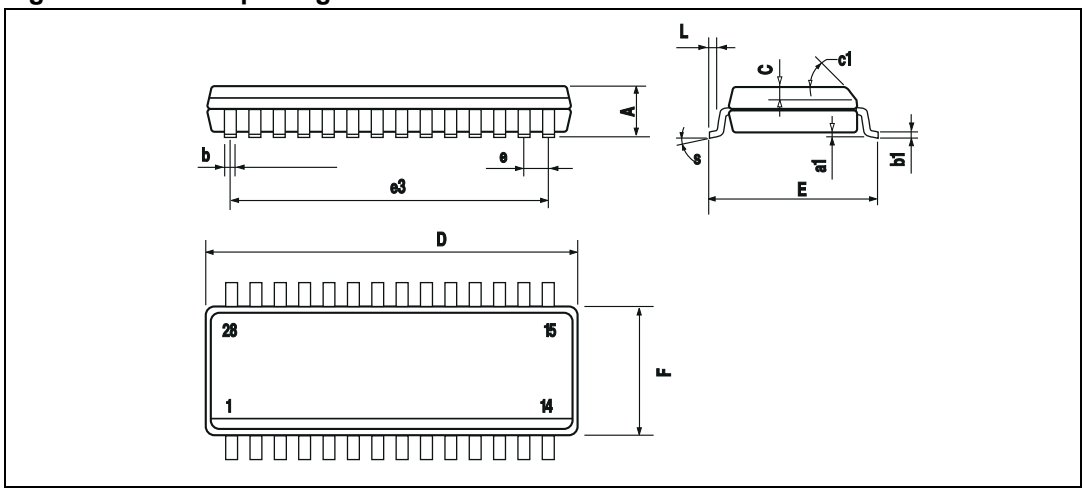
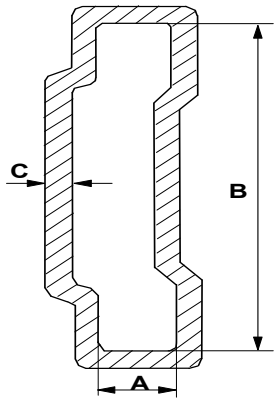


Table 17. SO-28 mechanical data

Dim.	mm.			inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	-	-	2.65	-	-	0.104
a1	0.10	-	0.30	0.004	-	0.012
b	0.35	-	0.49	0.013	-	0.019
b1	0.23	-	0.32	0.009	-	0.012
C	-	0.50	-	-	0.020	-
c1	45 (typ.)			-		
D	17.7	-	18.1	0.697	-	0.713
E	10.00	-	10.65	0.393	-	0.419
e	-	1.27	-	-	0.050	-
e3	-	16.51	-	-	0.650	-
F	7.40	-	7.60	0.291	-	0.299
L	0.40	-	1.27	0.016	-	0.050
S	8 (max.)			-		

5.2 SO-28 packing information

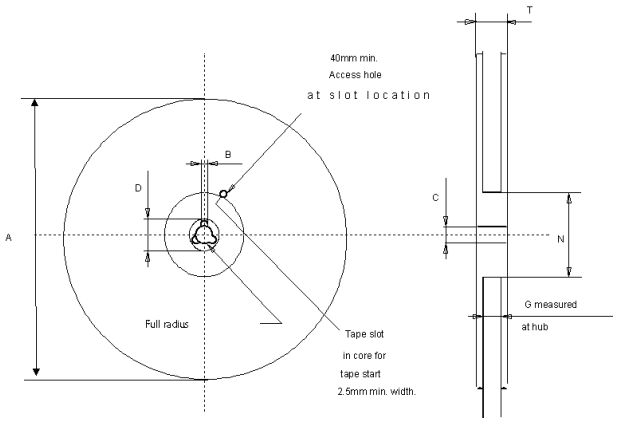
Figure 27. SO-28 tube shipment (no suffix)



Base Q.ty	28
Bulk Q.ty	700
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 28. SO-28 tape and reel shipment (suffix "TR")



Reel dimensions

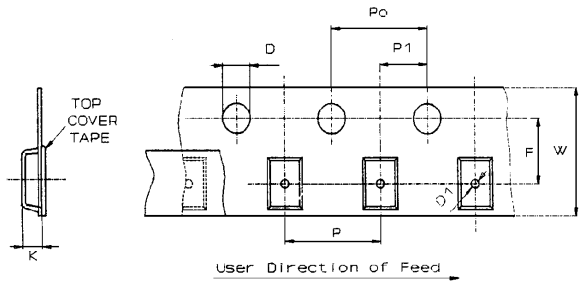
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

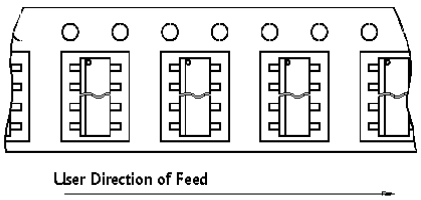
Tape dimensions

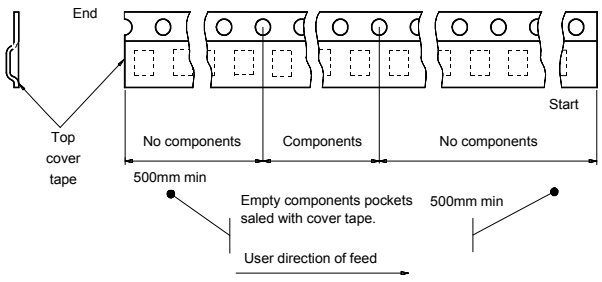
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	16
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	7.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







6 Revision history

Table 18. Document revision history

Date	Revision	Changes
01-Oct-2004	1	Initial release.
08-Jun-2009	2	Features: – Changed I_{lim} value from 22 A to 25 A – Changed DC short circuit current value from 22 A to 25 A *Table 9*: changed I_{lim} min value from 22 A to 25 A
15-Oct-2009	3	Updated *Figure 2: Configuration diagram (top view)*.
20-Sep-2013	4	Updated Disclaimer.

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