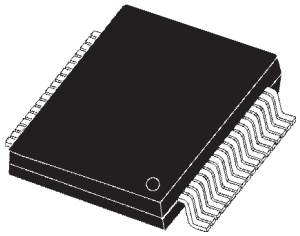
VNI8200XP

Octal high-side smart power solid state relay with serial/parallel selectable interface on chip

Datasheet - production data



PowerSSO-36

Features

Type	V_{demag} (1)	$R_{DS(on)}$ (1)	I_{out} (1)	V_{CC}
VNI8200XP	V_{CC}-45 V	0.11 Ω	0.7 A	45 V

1. Per channel

- Output current: 0.7 A per channel
- Serial/parallel selectable interface
- Short-circuit protection
- 8-bit and 16-bit SPI Interface for IC command and control diagnostic
- Channel overtemperature detection and protection
- Thermal independence of separate channels
- Drives all type of loads (resistive, capacitive, inductive load)
- Loss of GND protection
- Power Good diagnostic
- Undervoltage shutdown with hysteresis
- Overvoltage protection (V_{CC} clamping)
- Very low supply current
- Common fault open drain output
- IC warning temperature detection
- Channel output enable
- 100 mA high efficiency step-down switching regulator with integrated boot diode
- Adjustable regulator output
- Switching regulator disable
- 5 V and 3.3 V compatible I/Os
- Channel outputs status LED driving 4 x 2 multiplexed array
- Fast demagnetization of inductive loads
- ESD protection
- Designed to meet IEC 61131-2, IEC61000-4-4, and IEC61000-4-5

Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines

Table 1. Device summary

Part number	Package	Packing
VNI8200XP	PowerSSO-36	Tube
VNI8200XPTR		Tape and reel

Contents

1 Description

The VNI8200XP is a monolithic 8-channel driver featuring a very low supply current, with integrated SPI interface and high efficiency 100 mA micropower step-down switching regulator peak current control loop mode. The IC, realized in STMicroelectronics™ VIPower™ technology, is intended for driving any kind of load with one side connected to ground.

Active channel current limitation combined with thermal shutdown, independent for each channel, and automatic restart, protect the device against overload.

Additional embedded functions are: loss of GND protection that automatically turns off the device outputs in case of ground disconnection, undervoltage shutdown with hysteresis, Power Good diagnostic for valid supply voltage range recognition, output enable function for immediate power outputs ON/OFF, and programmable watchdog function for microcontroller safe operation; case overtemperature protection to control the IC case temperature.

The device embeds a four-wire SPI serial peripheral with selectable 8 or 16-bit operations; through a select pin the device can also operate with a parallel interface.

Both the 8-bit and 16-bit SPI operations are compatible with daisy chain connection.

The SPI interface allows command of the output driver by enabling or disabling each channel featuring, in 16-bit format, a parity check control for communication robustness. It also allows the monitoring of the status of the IC signaling Power Good, overtemperature condition for each channel, IC pre-warning temperature detection.

Built-in thermal shutdown protects the chip from overtemperature and short-circuit. In overload condition, the channel turns OFF and ON again automatically after the IC temperature decreases below a threshold fixed by a temperature hysteresis so that junction temperature is controlled. If this condition makes case temperature reaching case temperature limit, T_{CSD}, overloaded channels are turned OFF and restart, non-simultaneously, when case and junction temperature decrease below their own reset threshold. If the case of thermal reset, the channels loaded are not switched on until the junction temperature reset event. Non-overloaded channels continue to operate normally. Case temperature above T_{CSD} is reported through the $\overline{\text{TWARN}}$ open drain pin.

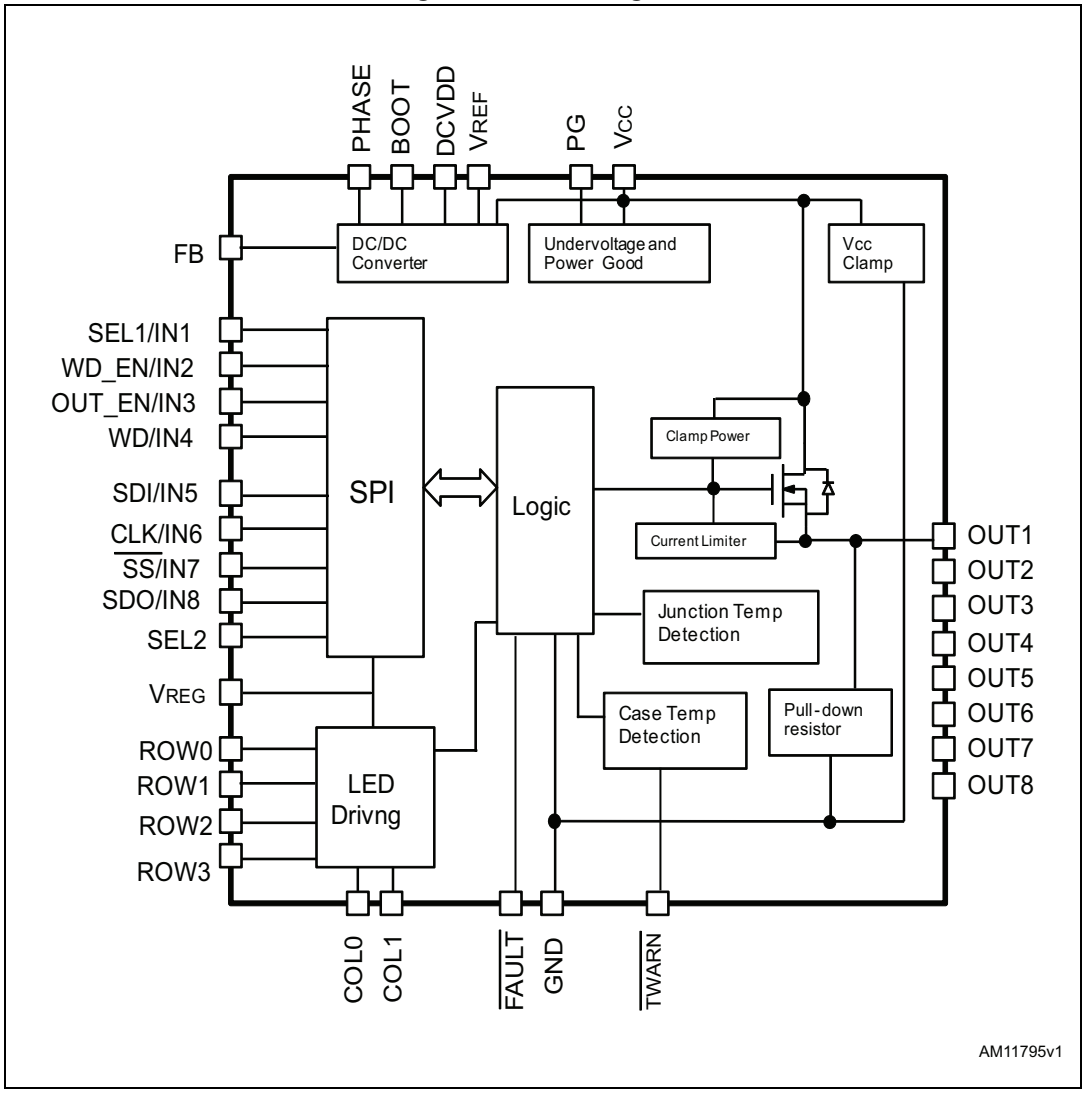
An internal circuit provides a not latched common $\overline{\text{FAULT}}$ indicator reporting if one of the following events occurs: channel OVT (overtemperature), parity check fail. The Power Good diagnostic warns the controller that the supply voltage is below a fixed threshold.

The watchdog function is used to detect the occurrence of a software fault of the host controller. The watchdog circuitry generates an internal reset on expiry of the internal watchdog timer. The watchdog timer reset can be achieved by applying a negative pulse on the WD pin. The watchdog function can be disabled by the WD_EN dedicated pin. This pin also allows the programming of a wide range of watchdog timings.

An internal LED matrix driver circuitry (4 rows, 2 columns) allows the detection of the status of the single outputs. An integrated step-down voltage regulator provides supply voltage to the internal LED matrix driver and logic output buffers and can be used to supply the external optocouplers if the application requires isolation. The regulator is protected against short-circuit or overload conditions by means of pulse-by-pulse current limit with a peak current control loop.

2 Block diagram

Figure 1. Block diagram



3 Pin connection

Figure 2. Pin connection (top view)

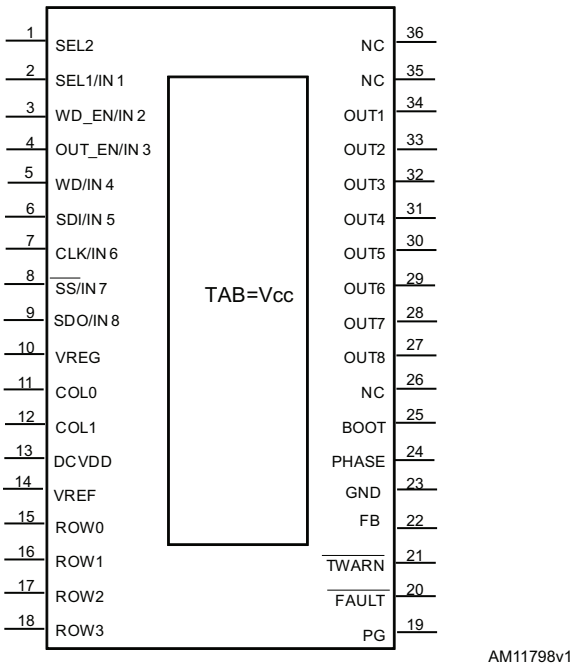


Table 2. Pin description

Pin	Name	Type	Description
1	SEL2	Logic input	SPI/parallel selection mode
2	SEL1/IN1	Logic input	8/16-bit SPI selection mode/channel 1 input
3	WD_EN/ IN2	Logic/analog input	Watchdog enable_setting/channel 2 input
4	OUT_EN /IN3	Logic input	Output enable/channel 3 input
5	WD/IN4	Logic input	Watchdog input. The internal watchdog counter is cleared on the falling edges/channel 4 input.
6	SDI/IN5	Logic input	Serial data input/channel 5 input
7	CLK/IN6	Logic input	Serial clock/channel 6 input
8	$\overline{SS}$/IN7	Logic input	Slave select/channel 7 input
9	SDO/IN8	Logic input/output	Serial data output/channel 8 input
10	VREG	Power supply	SPI/inputs/LED supply voltage
11	COL0	Open source output	LED source output
12	COL1	Open source output	LED source output
13	DCVDD	Analog output	Internally generated DC-DC low voltage supply. (To be connected to external 10 nF capacitor).

Table 2. Pin description (continued)

Pin	Name	Type	Description
14	VREF	Analog output	Internally generated DC-DC voltage reference (To be connected to external 10 nF capacitor).
15	ROW0	Open drain output	Status channel 1-2
16	ROW1	Open drain output	Status channel 3-4
17	ROW2	Open drain output	Status channel 5-6
18	ROW3	Open drain output	Status channel 7-8
19	PG	Open drain output	Power Good diagnostic - active low
20	$\overline{\text{FAULT}}$	Open drain output	Fault indication - active low
21	$\overline{\text{TWARN}}$	Open drain output	IC case warning temperature detection - active low
22	FB	Analog input	Step-down feedback input. Connecting the output voltage directly to this pin results in an output voltage of 3.3 V. An external resistor divider is required for higher output voltages.
23	GND		Ground
24	PHASE	Power output	Step-down output
25	BOOT	Power output	Step-down bootstrap voltage. Used to provide a drive voltage, higher than the supply voltage, to power the switch of the step-down regulator.
26	NC		Not connected
27	OUT8	Power output	Channel 8 power output
28	OUT7	Power output	Channel 7 power output
29	OUT6	Power output	Channel 6 power output
30	OUT5	Power output	Channel 5 power output
31	OUT4	Power output	Channel 4 power output
32	OUT3	Power output	Channel 3 power output
33	OUT2	Power output	Channel 2 power output
34	OUT1	Power output	Channel 1 power output
35	NC		Not connected
36	NC		Not connected
TAB	TAB	Power supply	Exposed tab internally connected to V_{CC}

4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Power supply voltage	45	V
$-V_{CC}$	Reverse supply voltage	-0.3	V
V_{REG}	Logic supply voltage	-0.3 to +6	V
V_{FAULT} V_{TWARN} V_{PG}	Voltage range at pins $\overline{TWARN}$, $\overline{FAULT}$, PG	-0.3 to +6	V
V_{BOOT}	Bootstrap peak voltage $V_{PHASE} = V_{cc}$	V_{CC}+6	V
V_{ROW}	Voltage range at ROW pins	-0.3 to +6	V
V_{COL}	Voltage range at COL pins	-0.3 to +6	V
V_{dig}	Voltage level range at logic input pins	-0.3 to +6	V
I_{OUT}	Output current (continuous)	Internally limited (1)	A
I_R	Reverse output current (per channel)	-5	A
I_{GND}	DC ground reverse current	-250	mA
I_{REG}	V_{REG} input current	-1/10	mA
I_{FAULT} $I_{TWARN,}$ I_{PG}	Current range at pins $\overline{TWARN}$, $\overline{FAULT}$, PG	-1 to +10	mA
I_{IN}	Input current range	-1 to +10	mA
I_{ROW}	Current range at ROW pins (ROW in ON state)	+20	mA
	Current range at ROW pins (ROW in OFF state)	-1 to +10	mA
I_{COL}	Current range at COL pins (COL in ON state)	-10	mA
	Current range at COL pins (COL in OFF state)	-1 to +10	mA
V_{ESD}	Electrostatic discharge (R = 1.5 kΩ; C = 100 pF)	2000	V
E_{AS}	Single pulse avalanche energy per channel not simultaneously	300	mJ
P_{TOT}	Power dissipation at T_c = 25 °C	Internally limited(1)	W
T_J	Junction operating temperature	Internally limited	°C
T_{STG}	Storage temperature	-55 to 150	°C

1. Protection functions are intended to avoid IC damage in fault conditions and are not intended for continuous operation. Continuous and repetitive operation of protection functions may reduce the IC lifetime.

4.1 Thermal data

Table 4. Thermal data

Symbol	Parameter		Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case (1)	Max.	2	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient (2)	Max.	15	°C/W

1. Per channel.
2. PSSO36 mounted on the evaluation board STEVALIFP022V1 developed on four layer FR4, with about 8 cm^2 for each layer.

5 Electrical characteristics

5.1 Power section

10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{cc}	Supply voltage		10.5		36	V
V_{cc}Clamp	Clamp on V_{cc}	Current 20 mA	45	50	52	V
$R_{DS(on)}$	On state resistance	I_{OUT} = 0.5 A at T_J = 25 °C I_{OUT} = 0.5 A		0.11 	 0.2	Ω
I_S	V_{cc} supply current	All channels in OFF state, DC-DC in OFF state, V_{REG}=5 V, SPI OFF(1)		1		mA
		All channels in ON state, DC-DC in ON state V_{REG}=5 V, SPI ON (2)		5.6		mA
I_{DS}	V_{REG} supply current	DC-DC OFF V_{REG}= 5 V SPI OFF WD_EN=0		200		µA
		DC/DC OFF V_{REG}=5 V SPI ON WD_EN=V_{REG}		250		µA
I_{LGND}	Output current at GND disconnection	All pins at 0 V except V_{OUT} = 24 V			0.5	mA
$V_{OUT(OFF)}$	OFF state output voltage	V_{IN} = 0 V, IOUT = 0 A			1	V
$I_{OUT(OFF)}$	OFF state output current	V_{IN} = V_{OUT} = 0 V	0		2	µA
F_{CP}	Charge pump frequency	Channel in ON state (3)		1.45		MHz

1. $\overline{SS}$ signal high, NO communication.
2. $\overline{SS}$ signal low, communication ON.
3. To cover EN55022 class A and class B normatives.

5.2 SPI characteristics

10.5 V < V_{CC} < 36 V; 2.7 V < V_{REG} < 5 V; -40 <T_j <125; unless otherwise specified.

Table 6. SPI characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_{CLK}	SPI clock frequency			-	5	MHz
t_r(CLK), t_f(CLK)	SPI clock rise/fall time			-	20	ns
$t_{su}(\overline{SS})$	$\overline{SS}$ setup time		120	-		ns
$t_h(\overline{SS})$	$\overline{SS}$ hold time		120	-		ns
t_w(CLK)	CLK high time		80	-		ns
t_{su}(SDI)	Data input setup time		100	-		ns
t_h(SDI)	Data input hold time		100	-		ns
t_a(SDO)	Data output access time			-	100	ns
t_{dis}(SDO)	Data output disable time			-	200	ns
t_v(SDO)	Data output valid time			-	100	ns
t_h(SDO)	Data output hold time		0	-		ns
V_{SDO}	Voltage on serial data output	I_{SDO} = 15 mA	V_{REG}-0.8	-		V
		I_{SDO} = -4 mA		-	0.8	V

5.3 Switching

V_{CC} = 24 V; -40 °C < T_J < 125 °C.

Table 7. Switching

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(ON)}$	Turn-ON delay time	I_{OUT} = 0.5 A, resistive load, input rise time < 0.1 µs	-	5	-	µs
t_r	Rise time	I_{OUT} = 0.5 A, resistive load, input rise time < 0.1 µs	-	5	-	µs
$t_{d(OFF)}$	Turn-OFF delay time	I_{OUT} = 0.5 A, resistive load, input rise time < 0.1 µs	-	10	-	µs
t_f	Fall time	I_{OUT} = 0.5 A, resistive load, input rise time < 0.1 µs	-	5	-	µs
$dV/dt_{(ON)}$	Turn-ON voltage slope	I_{OUT} = 0.5 A, resistive load, input rise time < 0.1 µs	-	3	-	V/µs
dV/dt(off)	Turn-OFF voltage slope	I_{OUT} = 0.5 A, resistive load, input rise time < 0.1 µs	-	4	-	V/µs

5.4 Logic inputs

10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified.

Table 8. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.8	V
V_{IH}	Input high level voltage		2.20			V
$V_{I(HYST)}$	Input hysteresis voltage			0.15		V
I_{IN}	Input current	V_{IN} = 5 V	8			µA

5.5 Protection and diagnostic

10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified.

Table 9. Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{PGH1}	Power Good diagnostic ON threshold		16.6	17.5	18.4	V
V_{PGH2}	Power Good diagnostic OFF threshold		15.6	16.5	17.4	
V_{PGHYS}	Power Good diagnostic hysteresis			1		
V_{USD}	Undervoltage ON protection			9.5	10.5	V
	Undervoltage OFF protection			9		V
V_{USDHYS}	Undervoltage hysteresis		0.4	0.5		V
V_{demag}	Output voltage at turn-OFF	I_{OUT} = 0.5 A; L_{LOAD} ≥ 1 mH	V_{CC}-52	V_{CC}-50	V_{CC}-45	V
V_{TWARN}	$\overline{TWARN}$ pin low-state output voltage	I_{TWARN} = 3 mA (active condition)			0.6	V
V_{FAULT}	$\overline{FAULT}$ pin low-state output voltage	I_{FAULT} = 3 mA (fault condition)			0.6	V
V_{PG}	PG pin low-state output voltage	I_{PG} = 3 mA (active condition) V_{REG}=3.3 V V_{CC}=0			0.7	V
I_{PEAK}	Maximum DC output current before limitation			1.4		A
I_{LIM}	Short-circuit current limitation per channel	R_{LOAD} = 0	0.7	1.1	1.7	A

Table 9. Protection and diagnostic (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Hyst	I_{LIM} tracking limits	R_{LOAD} = 0		0.3		A
I_{LFAULT}	$\overline{FAULT}$ leakage current	V_{pin} = 5 V			2	µA
I_{TWARN}	$\overline{TWARN}$ leakage current					
I_{PG}	PG leakage current					
T_{TSD}	Junction shutdown temperature		160	180		°C
T_R	Junction reset temperature			160		°C
T_{HIST}	Junction thermal hysteresis			20		°C
T_{CSD}	Case shutdown temperature		115	130	155	°C
T_{CR}	Case reset temperature			110		°C
T_{CHYST}	Case thermal hysteresis			20		°C
t_{WD}	Watchdog hold time	See *Figure 6*	50			ns
t_{WM}	Watchdog time	See *Table 14* and *Figure 6*				
t_{OUT_EN}	OUT_EN pin propagation delay(1)	V_{cc}= 24 V I_{out} 72 mA		10		us
t_{res}	OUT_EN hold time		50			ns
t_{WO}	Watchdog timeout(2)				t_{WM} + $t_{d(off)}$	ms

1. Time from reset active low and power out disable.
2. The time from t_{WM} elapsed to power out disable.

5.6 Step-down switching regulator

10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified.

Table 10. Step-down switching regulator

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DC_out}	Regulated output voltage	Ireg from 0 to 100 mA V_{REG} 3.3 V, *Figure 8.*	3.1	3.3	3.5	V
		Ireg from 0 to 100 mA V_{REG} 5 V, *Figure 9*.		5		
V_{FB}	Voltage feedback		3.1	3.3	3.5	V
$R_{DS(on)}$	MOSFET on-resistance			1.5		Ω

Table 10. Step-down switching regulator (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{lim}	Limitation current		0.55		0.9	A
I_{qop}	Total operating quiescent current			0.6		mA
$I_{qst\text{-}by}$	Total standby quiescent current	Regulator standby		15.8		µA
f_s	Switching frequency			400		kHz
D_{max}	Maximum duty cycle			80%		%
Ton_{min}	Minimum on-time			150		ns
f_{sc}	Frequency in short-circuit condition			50		kHz

5.7 LED driving array

10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified.

Table 11. LED driving array

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{COL}	Output source voltage at COL pins	Output current 0 to 7 mA	V_{REG}-0.3	V_{REG}-0.2		V
V_{ROW}	Open drain voltage at ROW pins	Output current 0 to 15 mA		0.2	0.3	V
Fsw	Row refresh frequency with duty=25%			780		Hz

6 Reverse polarity protection

The reverse polarity protection (which is not available in this device), could be implemented on the board by a diode or by a resistance in series to the GND. The resistance value has to be calculated considering the maximum operating supply voltage V_{cc}, the maximum V_{cc} reverse voltage evaluated as drop on the device ($-V_{cc}$) and the maximum reverse current I_{GND}.

7 Truth table

Table 12. Truth table

Condition	Input	Output	SPI Status bit	Fault	Twarn	Power Good
Normal operation	High	On	Reset	High	High	High
	Low	Off	Reset	High	High	High
Junction overtemperature	High	Off	Set	Low	X	X
	Low	Off	Set(1)	High	X	X
Case overtemperature	High	Off	Set(1)	X	Low	X
	Low	Off	Set(1)	X	Low(1)	X
Undervoltage	High	Off	Reset	X	X	X
	Low	Off	Reset	X	X	X
Power Good	High	On	Set(2)	High	High	Low
	Low	Off	Set(2)	High	High	Low

1. This signal becomes high after the temperature falls below the reset threshold.
2. If fault expires, the reset condition occurs after SPI communication, otherwise it is set again.

8 Functional pin description

8.1 SPI/parallel selection mode (SEL2)

This pin allows the selection of the IC interfacing mode. The SPI interface is selected if SEL2 = H, while the parallel interface is selected if SEL2 = L, according to *Table 13*:

Table 13. Pin description

Pin	Function			
	SEL2[1] = H SPI operation		SEL2 = L Parallel operation	
SDO/IN8	SDO	Serial data output	IN8	Input to channel 8
$\overline{SS}$/IN7	$\overline{SS}$	Slave select	IN7	Input to channel 7
CLK/IN6	CLK	Serial clock	IN6	Input to channel 6
SDI/IN5	SDI	Serial data input	IN5	Input to channel 5
WD/IN4	WD	Watchdog input	IN4	Input to channel 4
OUT_EN/IN3	OUT_EN	IC OUTPUT enable / disable	IN3	Input to channel 3
WD_EN/IN2	WD_EN	Watchdog enable / disable and timing preset	IN2	Input to channel 2
SEL1/IN1	SEL1	8/16-bit SPI selection mode	IN1	Input to channel 1

1. SEL2 has an internal weak pull-down.

8.2 Serial data in (SDI)

If SEL2 = H, this pin is the input of the serial control frame. SDI is read on CLK rising edges and, therefore, the microcontroller must change SDI state during the CLK falling edges. After the $\overline{SS}$ falling edge, the SDI is equal to the most significant bit of the control frame (*Figure 3*).

8.3 Serial data out (SDO)

If SEL2 = H, this pin is the output of the serial fault frame. SDO is updated on CLK falling edges and, therefore, the microcontroller must read SDO state during the CLK rising edges.

The SDO pin is tri-stated when $\overline{SS}$ signal is high and it is equal to the most significant bit of the fault frame after the $\overline{SS}$ falling edge (*Figure 3*).

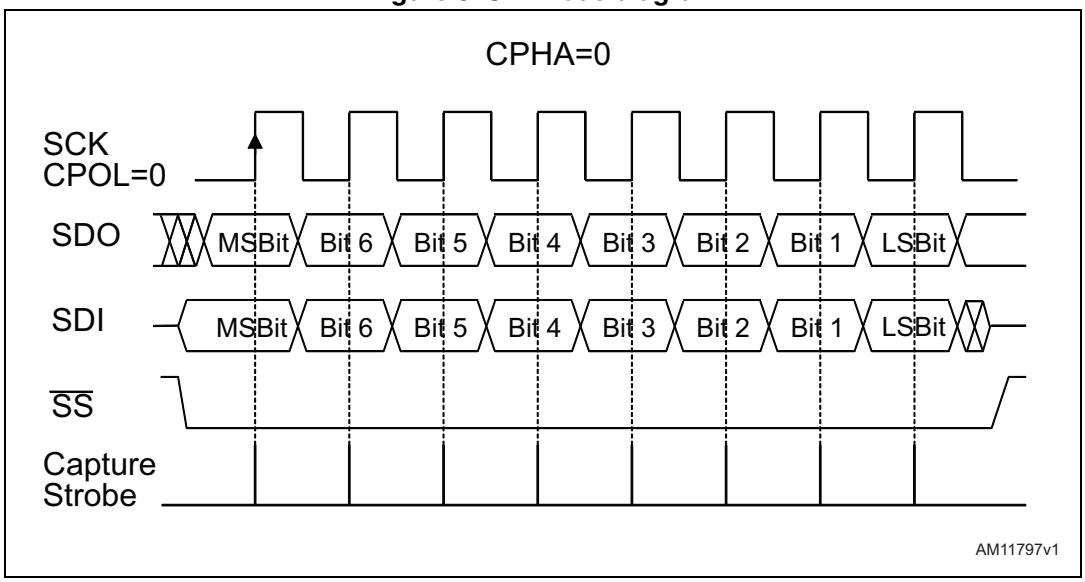
8.4 Serial data clock (CLK)

If SEL2 = H, the CLK line is the input clock for serial data sampling. On CLK rising edge the SDI input is sampled by the IC and the SDO output is sampled by the host microcontroller. On CLK falling edge, both SDI and SDO lines are updated to the next bit of the frame, from the most to the less significant one (see *Figure 3*). When the $\overline{SS}$ signal is high, slave not selected, the microcontroller should drive the CLK low (the settings for the MCU SPI port are CPHA = 0 and CPOL = 0).

8.5 Slave select ($\overline{SS}$)

If SEL2 = H, the slave select ($\overline{SS}$) signal is used to enable the VNI8200XP serial communication shift register; data is flushed-in through the SDI pin and flushed-out from the SDO pin only when the $\overline{SS}$ pin is low. On the $\overline{SS}$ pin falling edge the shift register (containing the fault conditions) is frozen, so any change on the power switches status is latched until the next $\overline{SS}$ falling edge event and the SDO output is enabled. On the $\overline{SS}$ pin rising edge event the 8/16 bits present on the SPI shift register are evaluated and the outputs are driven according to this frame. If more than 8/16 bits (depending on the SPI settings) are flushed inside only the last 8/16 are evaluated; the others are flushed out from the SDO pin after fault condition bits; in this way a proper communication is possible also in a daisy chain configuration.

Figure 3. SPI mode diagram



8.6 8/16-bit selection (SEL1)

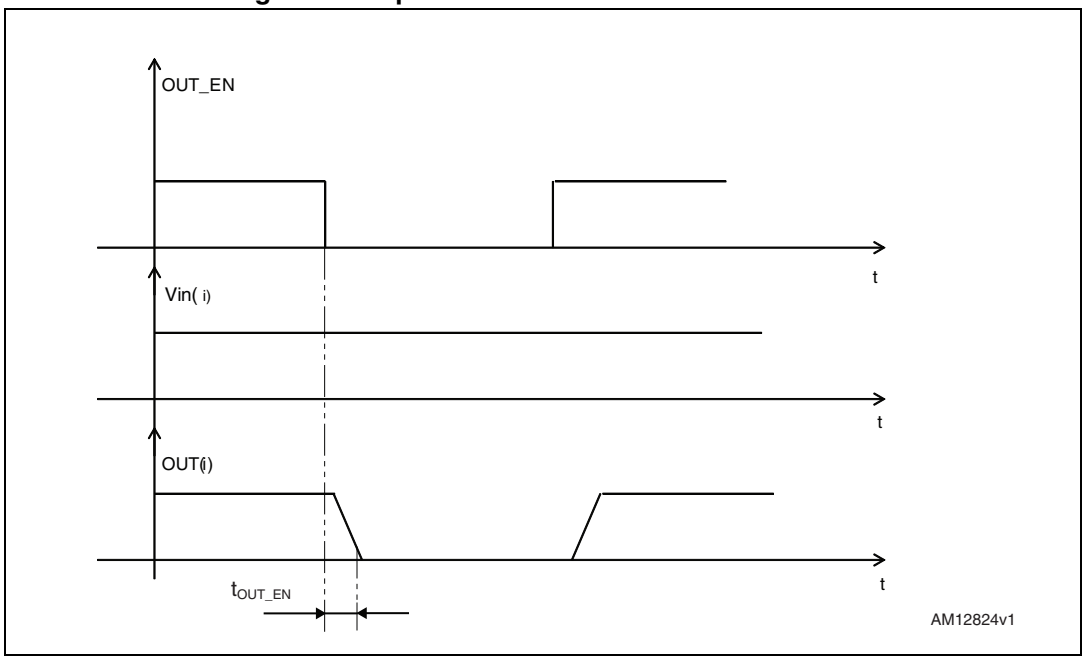
If SEL2 = H, SEL1 is used to select between two possible SPI configurations: the 8-bit SPI mode (SEL1 = L) and the 16-bit SPI mode (SEL1 = H). 8/16-bit SPI operation is described below.

8.7 Output enable (OUT_EN)

If SEL2 = H, the OUT_EN pin provides a fast way to disable all the outputs simultaneously. When the OUT_EN pin is driven low for at least T_{RES}, the outputs are disabled while fault conditions in the SPI register are latched. To enable the outputs it is then necessary to raise the OUT_EN pin and re-program the IC through the SPI interface. As fault conditions are latched inside the IC and SPI interface is working also while the OUT_EN pin is driven low, it's possible to use SPI to detect if a fault condition occurred before than the reset event.

The device is ready to operate normally after a T_{SU} period. The OUT_EN pin is the fastest way to disable all the outputs when a fault occurs.

Figure 4. Output channel enable/disable behavior



8.8 IC warning case temperature detection ($\overline{\text{TWARN}}$)

The $\overline{\text{TWARN}}$ pin is an active low open drain output. This pin is activated if the IC case temperature exceeds T_{CSD}. According to the PCB thermal design and R_{thJC} value, this function allows a warning about a PCB overheating condition to be given.

The $\overline{\text{TWARN}}$ bit is also available through SPI. This bit is not latched: the $\overline{\text{TWARN}}$ pin is low only while the case overtemperature condition is active ($T_C > T_{CSD}$) and is released when this condition is removed ($T_C < T_{CR}$).

8.9 Fault indication ($\overline{\text{FAULT}}$)

The $\overline{\text{FAULT}}$ pin is an open drain active low fault indication pin. This pin is activated by one or more of the following conditions:

- Channel overtemperature (OVT)

  This pin is activated when at least one of the channels is in junction overtemperature.

  Unlike the SPI fault detection bits, this signal is not latched: the FAULT pin is low only when the fault condition is active and is released if the input driving signal is off or after the OVT protection condition has been removed. This last event occurs if the channel temperature decreases below the threshold level and the case temperature has not exceeded TCSD or is below TCR. This means that the FAULT pin is low only while the junction overtemperature is active (T_J >TTSD) and is released after this condition has been removed (T_J < TR and TC < TCR).

- Parity check fail

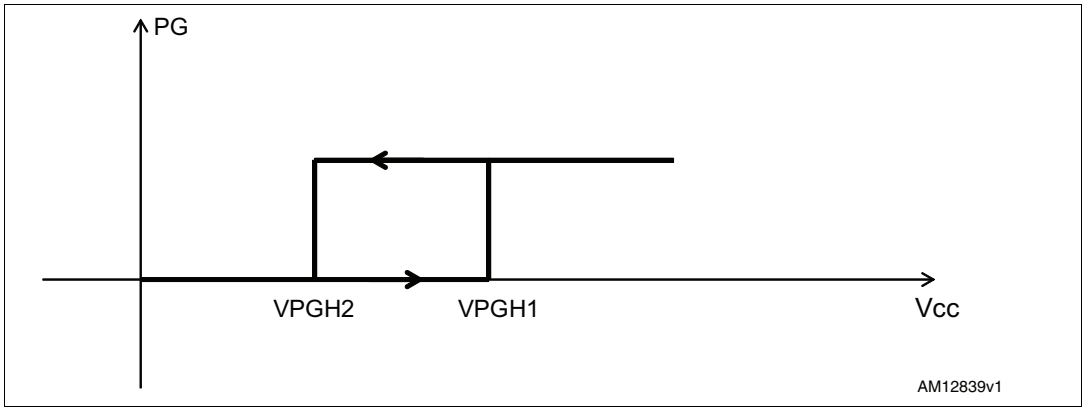
  When SPI mode is used (SEL2 = H), if a parity check fault of the incoming SPI frame is detected or counted, CLK rising edges are different by a multiple of 8, the $\overline{\text{FAULT}}$ pin is kept low. When counted CLK rising edges are a multiple of 8 and parity check is valid, the $\overline{\text{FAULT}}$ pin is kept high.

8.10 Power Good (PG)

The PG terminal is an open drain, that indicates the status of the supply voltage. When V_{CC} supply voltage reaches the Vsth1 threshold, PG goes into a high impedance state. It goes into a low impedance state when V_{CC} falls below the Vsth2 threshold.

In 16-bit SPI mode, a PG bit is also available. This bit is set high when the Power Good diagnostic is active, it is otherwise cleared.

Figure 5. Power Good diagnostic



8.11 Programmable watchdog counter reset (WD)

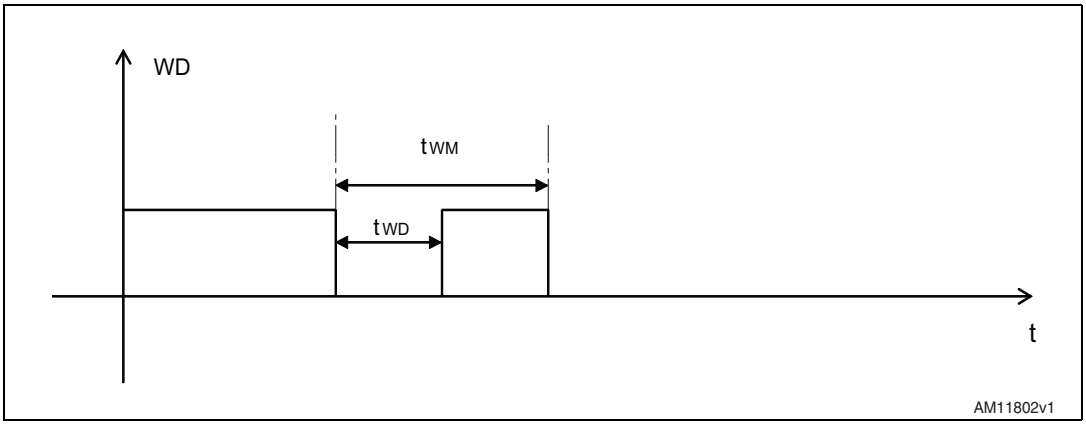
If SEL2 = H, the VNI8200XP embeds a watchdog counter that must be erased, with a negative pulse on the WD pin, before it expires. If the WD counter elapses, the VNI8200XP goes into an internal RESET state where all the outputs are disabled; to restart normal operation a negative pulse must be applied to the WD pin.

The watchdog enable/disable pin should be connected through an external divider to V_{REG}. The watchdog time is fixed in the following *Table 14*:

Table 14. Programmable watchdog time

V_{WD_EN}	t_{WM}
0.25 V_{REG} > V_{WD_EN}	Disable
0.25 V_{REG} ≤V_{WD_EN} < 0.5 V_{REG}	40 ± 12% ms
0.5 V_{REG} ≤V_{WD_EN} < 0.75 V_{REG}	80 ± 12% ms
0.75 V_{REG} ≤V_{WD_EN} = V_{REG}	160 ± 12% ms

Figure 6. Watchdog reset



9 SPI operation (SEL2 = H)

9.1 8-bit SPI mode (SEL1 = L)

If SEL2 = H, the 8-bit SPI mode is based on an 8-bit command frame sent from the microcontroller to the IC; each bit directly drives the corresponding output where LSB drives output 0 and MSB drives output 7. Each bit, set to '1', activates (closes) the corresponding output.

At the same time, the IC transfers the channel fault conditions (OVT) to the microcontroller. These fault conditions are latched at the occurrence and cleared after each communication (each time the $\overline{SS}$ signal has a positive transition). Each bit, set to '1', indicates an OVT condition for the corresponding channel.

Table 15. Command 8-bit frame (master to slave)

MSB							LSB
IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

Table 16. Fault 8-bit frame (slave to master)

MSB							LSB
F7	F6	F5	F4	F3	F2	F1	F0

9.2 16-bit SPI mode (SEL1 = H)

The 16-bit SPI mode is based on a 16-bit command frame sent from the microcontroller to the IC; the first 8 bits directly drive the output channels (each bit, set to '1', activates the corresponding output), the other 8 bits contain a 4-bit parity check code where the last bit (the inversion of the previous one) is used to detect a communication error condition (providing at least a transition in each frame):

P0 = IN0 ⊕ IN1 ⊕ IN2 ⊕ IN3 ⊕ IN4 ⊕ IN5 ⊕ IN6 ⊕ IN7

P1 = IN1 ⊕ IN3 ⊕ IN5 ⊕ IN7

P2 = IN0 ⊕ IN2 ⊕ IN4 ⊕ IN6

nP0 = NOT P0

Table 17. Command 16-bit frame (master to slave)

MSB															LSB
IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0	-	-	-	-	P2	P1	P0	nP0

At the same time, the IC transfers to the microcontroller a 16-bit fault frame where the first 8 bits indicate a channel fault (OVT) condition (each bit, set to '1', indicates an OVT event), the following 4 bits provide general fault condition information. FB_OK: this bit is related to the DC-DC regulation: at the DC-DC turn-on, this bit is low and becomes high after FB rises above 90% of the nominal V_{FB} voltage and a correct SPI communication occurred. If the FB

voltage falls below 80% of the nominal V_{FB} voltage, this bit is zero; TWARN (IC warning case temperature, see *Section 8.8*), PC (parity check fail, the bit, set to '1', indicates a PC fail or the length is not a multiple of 8) and $\overline{PG}$ (Power Good, see *Section 8.10*). The last 4 bits are used as parity check bits and communication error condition (see command 16 bit frame):

P0 = F0 ⊕ F1 ⊕ F2 ⊕ F3 ⊕ F4 ⊕ F5 ⊕ F6 ⊕ F7

P1 = PC ⊕ FB_OK ⊕ F1 ⊕ F3 ⊕ F5 ⊕ F7

P2 = $\overline{PG}$ ⊕ TWARN ⊕ F0 ⊕ F2 ⊕ F4 ⊕ F6

nP0 = NOT P0

Table 18. Fault 16-bit frame slave to master

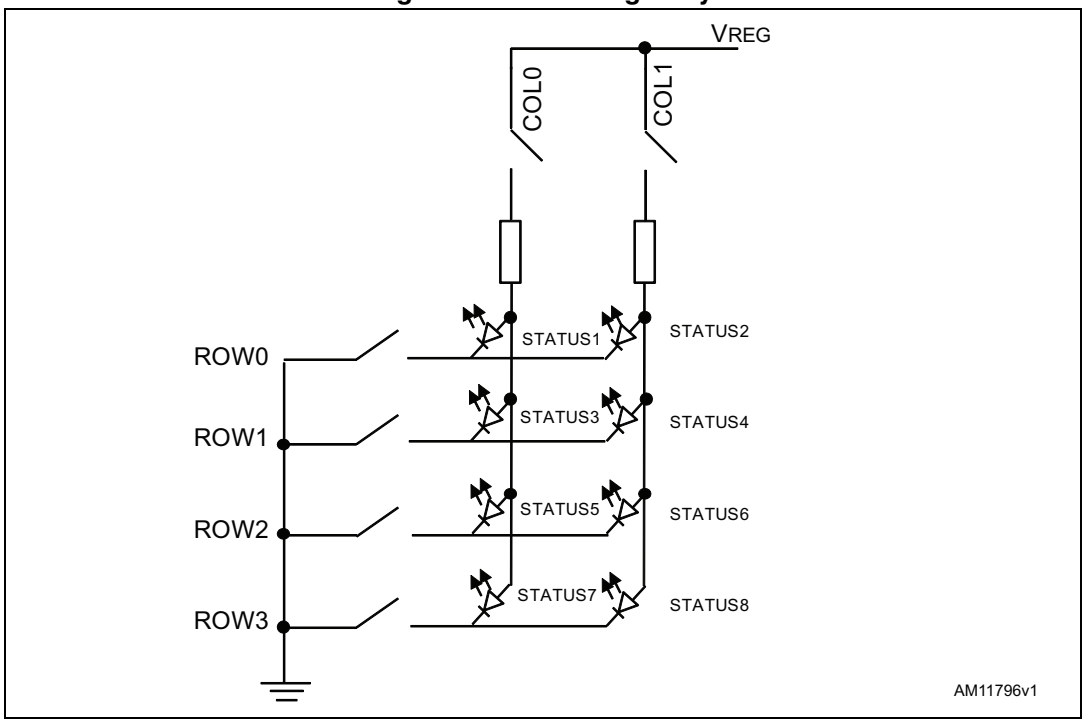
MSB															LSB
F7	F6	F5	F4	F3	F2	F1	F0	FB_OK	TWARN	PC	$\overline{PG}$	P2	P1	P0	nP0

Channel indications are latched and cleared after a communication only.

10 LED driving array

The LED driving array carries out the status of the output channels (ON or OFF)

Figure 7. LED driving array



The following is an indication of how to choose the R_{ext} resistor value.

Equation 1

$$R_{ext} = \frac{(V_{COLmin}) - (V_{ROWmax}) - V_{F(LED)}}{I_{F(LED)}}$$

Note: *$I_{F(LED)} \leq 7$ mA.*

Where (V_{COL} min.) and (V_{ROW} max.) can be found in *Table 11* and $V_{F(LED)}$ and $I_{F(LED)}$ depend on the electrical characteristics of the LEDs.

11 Step-down switching regulator

The IC embeds a high efficiency 100 mA micropower step-down switching regulator. The regulator is protected against short-circuit or overload conditions. Pulse-by-pulse current limit regulation is obtained in normal operation through a current loop control.

A low ESR output capacitor connected to the $V_{REG\ pin}$ helps to limit the regulated voltage ripple; a low ESR (less than 10 mΩ) capacitor is preferable. The control loop pin FB allows 3.3 V to be regulated, connecting it directly to V_{REG}, or 5 V connecting it through a voltage divider Rl/Rfbl. The DC-DC converter can be turned off by connecting the feedback pin to the DCVDD pin. In some applications it is possible to supply a 5 V or 3.3 V voltage externally or, in the case of two or more VNI8200XPs inside the same board, it's possible to configure the DC-DC converter on only one device and supply also the other ICs.

Note: if the DC-DC converter is adjusted to provide 3.3 V regulation and the V_{dc_out} is used to power an external load and not the device, a 33 kΩ resistor has to be connected on Vdc_out pin.

12 Typical circuits and conventions

Figure 8. Typical circuit for switching regulation $V_{DC\text{-}out}$ = 3.3 V

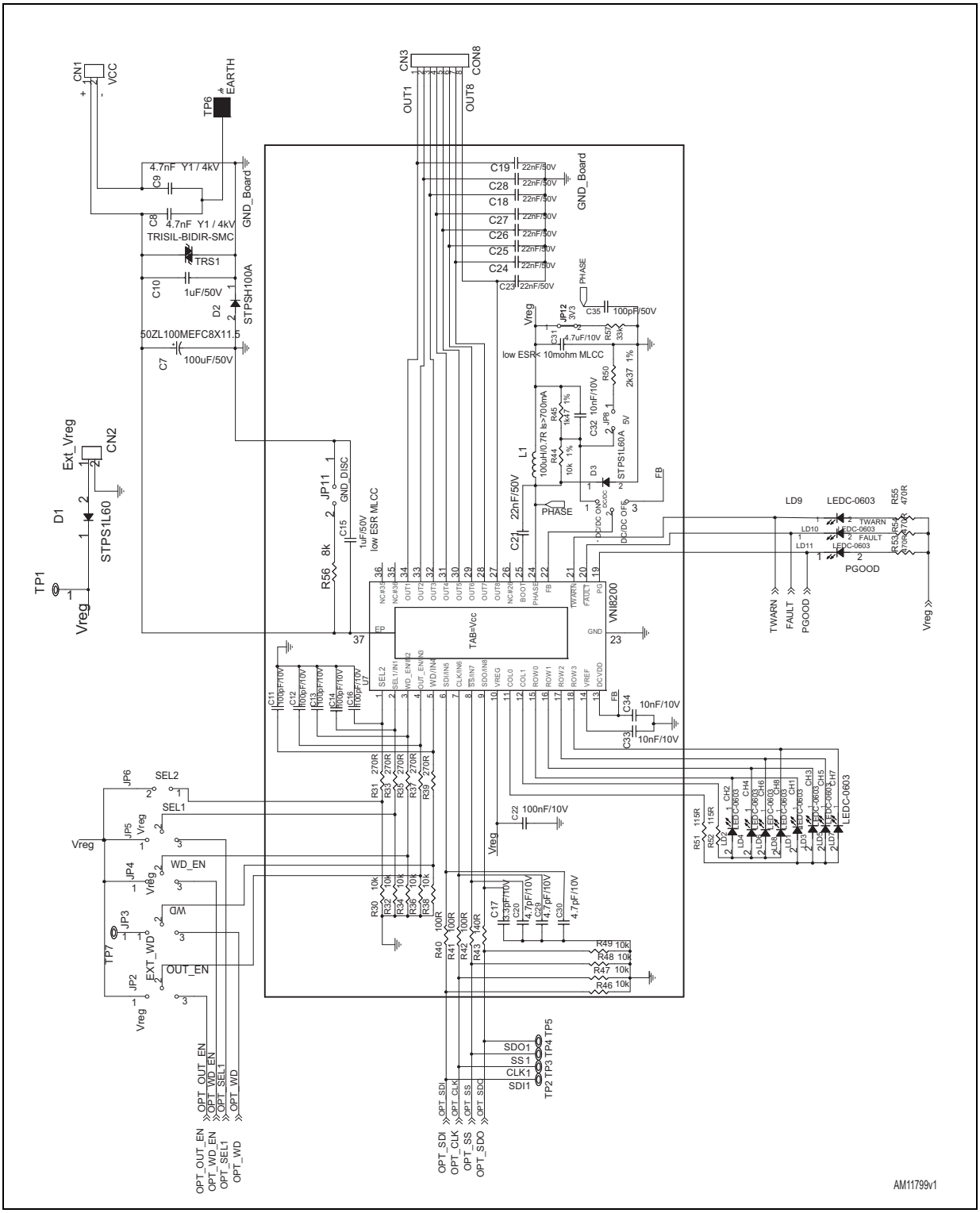


Figure 9. Typical circuit for switching regulation $V_{DC\text{-}out}$ = 5 V

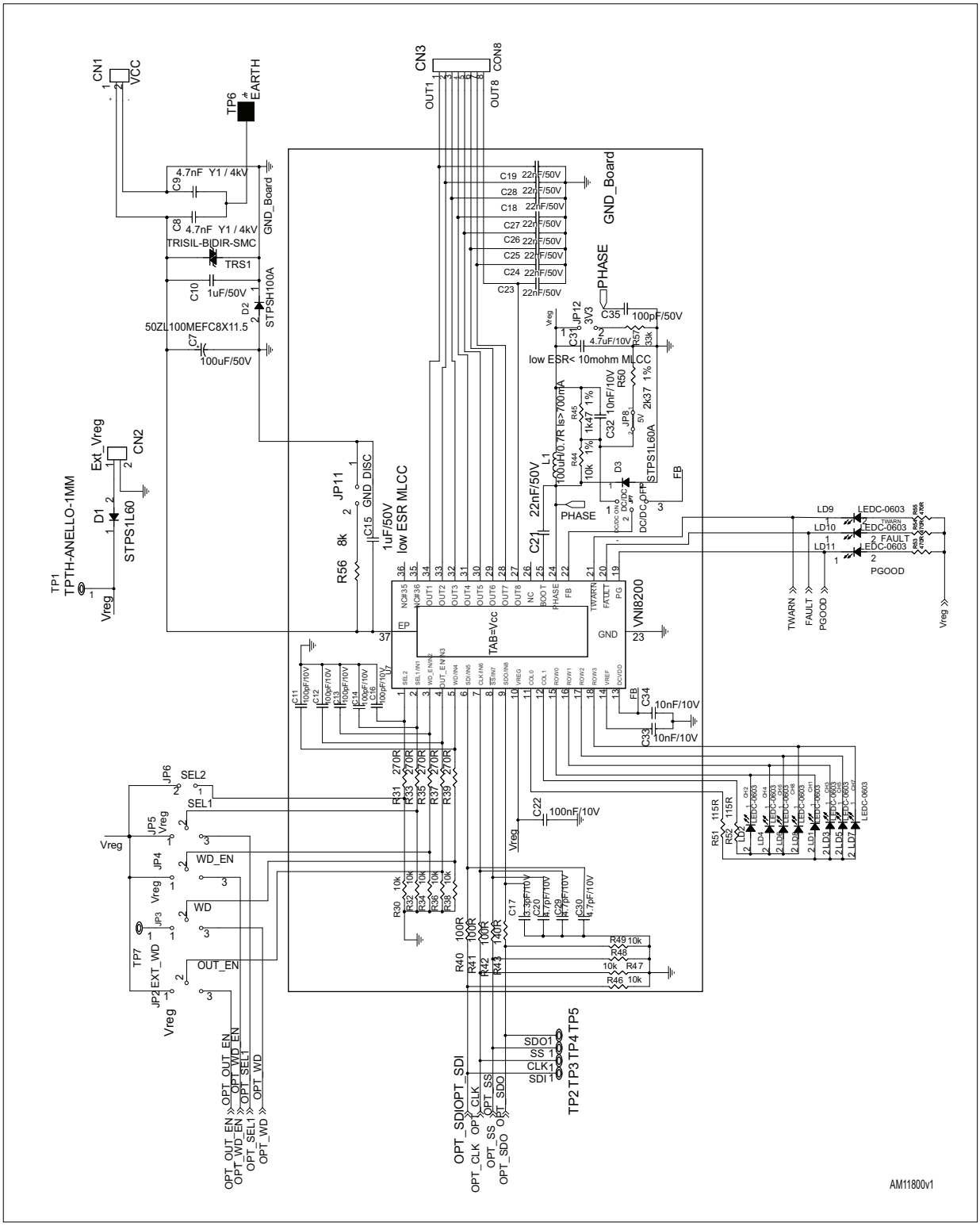
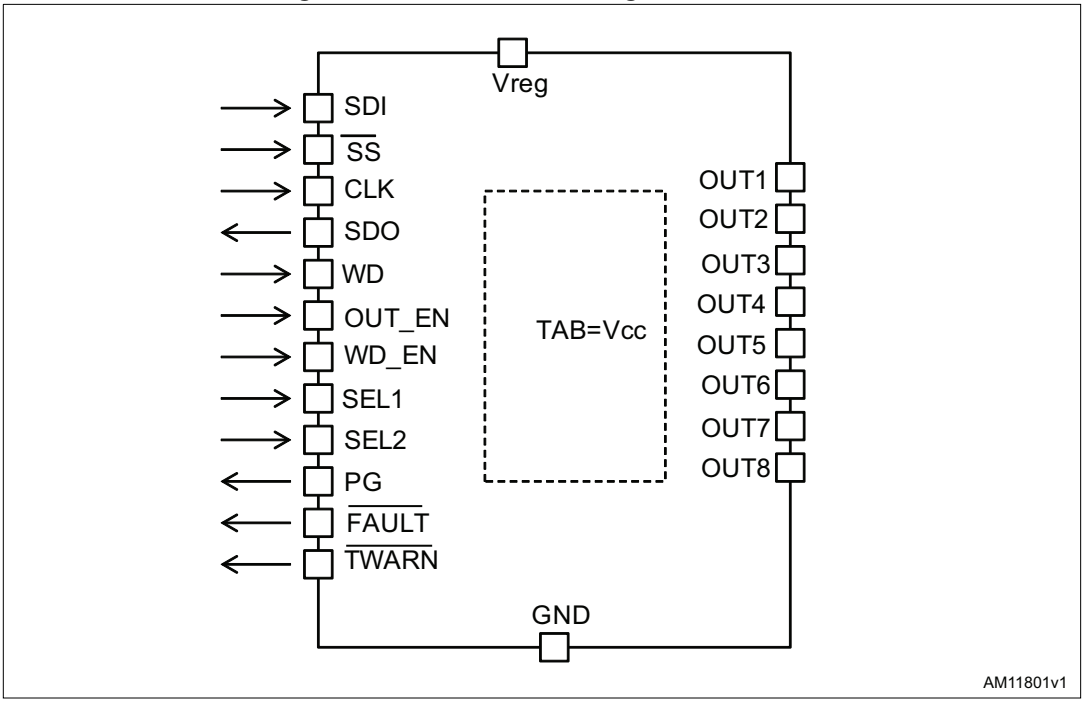


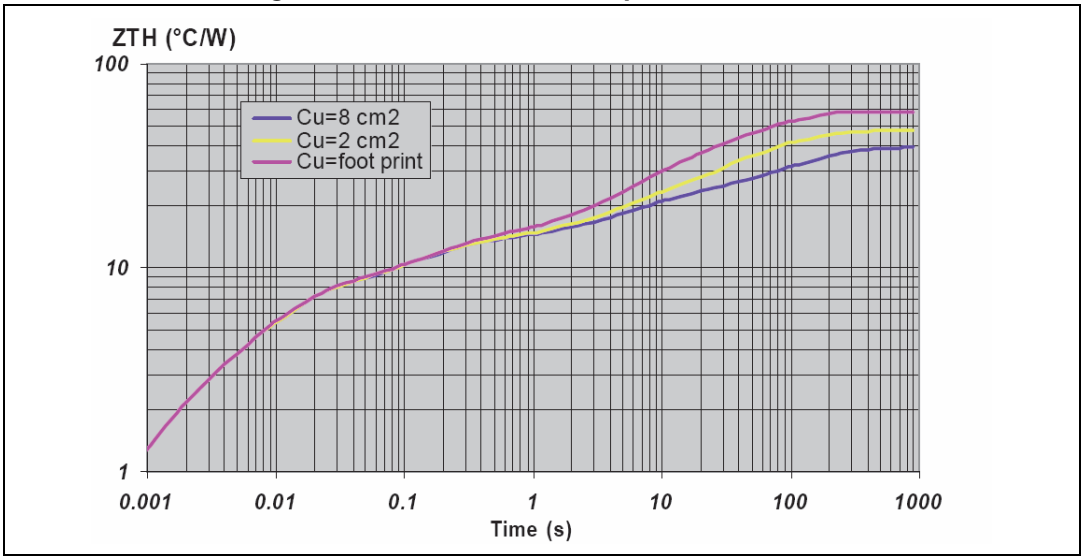
Figure 10. SPI directional logic convention



13 Thermal management

The power dissipation in the IC is the main factor that sets the safe operating condition of the device in the application. Therefore, it must be taken into account very carefully. Heatsinking can be achieved using copper on the PCB with proper area and thickness. The following image (*Figure 11*) shows the junction-to-ambient thermal impedance values for the PSSO36 package.

Figure 11. PSSO36 thermal impedance vs. time

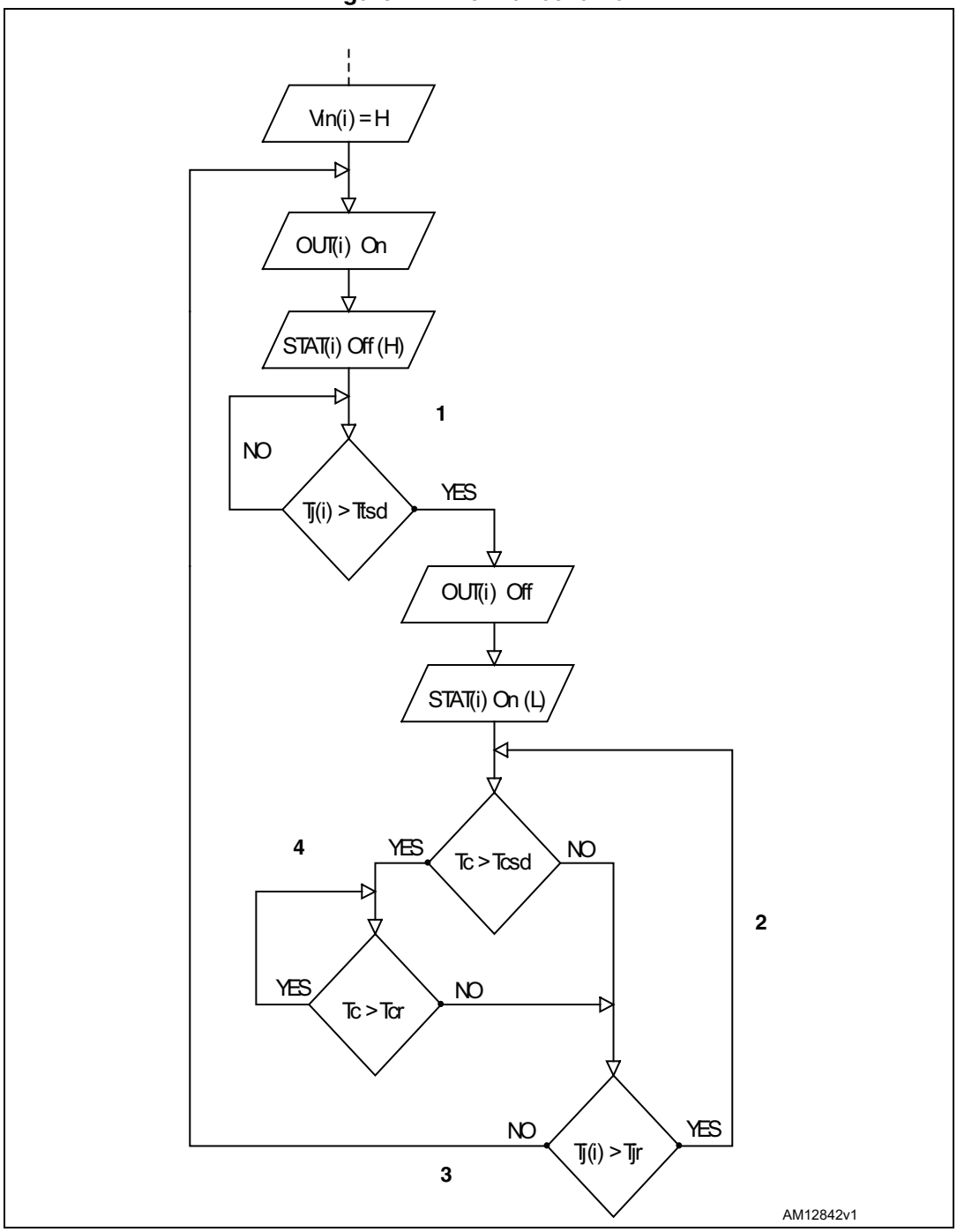


For instance, three cases have been considered using a PSSO36 packaged with copper slug soldered on a 1.6 mm thickness FR4 board with dissipating footprint (copper thickness of 70 µm):

- single layer PCB with just IC footprint dissipating area
- double layer PCB with footprint dissipating area on the top side and a 2 cm^2 dissipating layer on the bottom side through 15 via holes
- double layer PCB with footprint dissipating area on the top side and an 8 cm^2 dissipating layer on the bottom side through 15 via holes.

13.1 Thermal behavior

Figure 12. Thermal behavior



Note: 1 Thermal shutdown.

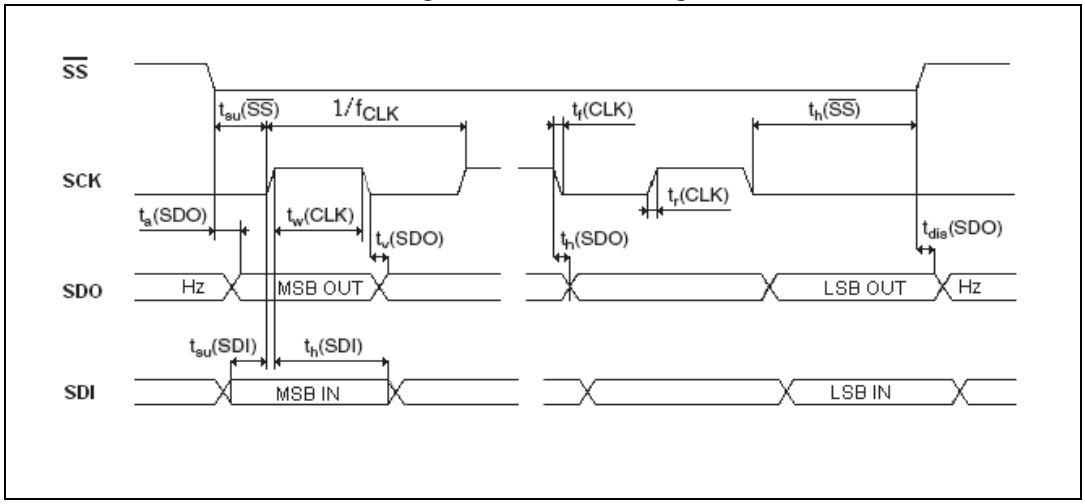
2 Junction hysteresis.

3 Restore to idle condition.

4 Case hysteresis.

14 Interface timing diagram

Figure 13. Serial timing



15 Switching parameter test conditions

Figure 14. dV/dt(ON) and dV/dt(OFF) time diagram test conditions

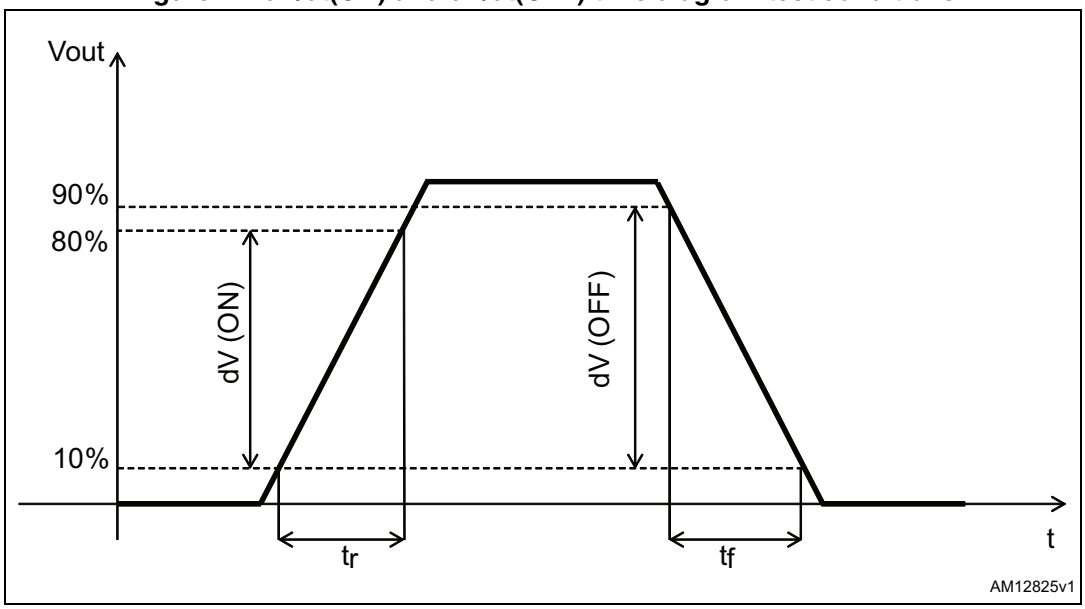
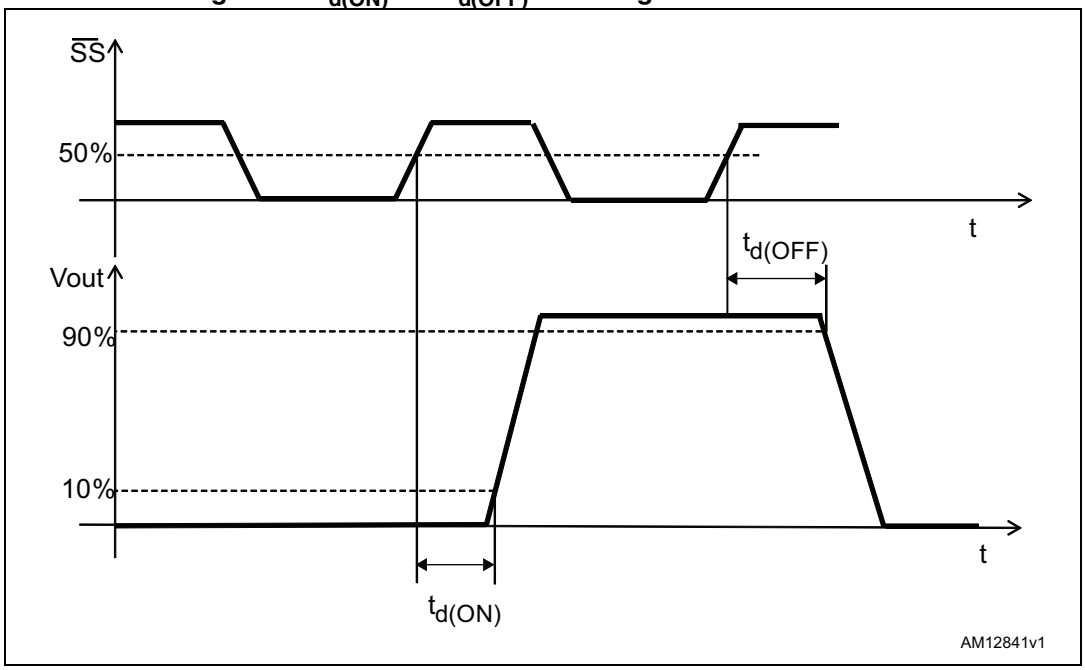


Figure 15. $t_{d(ON)}$ and $t_{d(OFF)}$ time diagram test conditions



16 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 19. PowerSSO-36 mechanical data

Symbol	mm		
	Min.	Typ.	Max.
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.18		0.36
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.5	
e3		8.5	
F		2.3	
G			0.075
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
M		4.3	
N			10deg
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1.0	
X	4.1		4.7
Y	4.9		5.5

Figure 16. PowerSSO-36 package dimensions

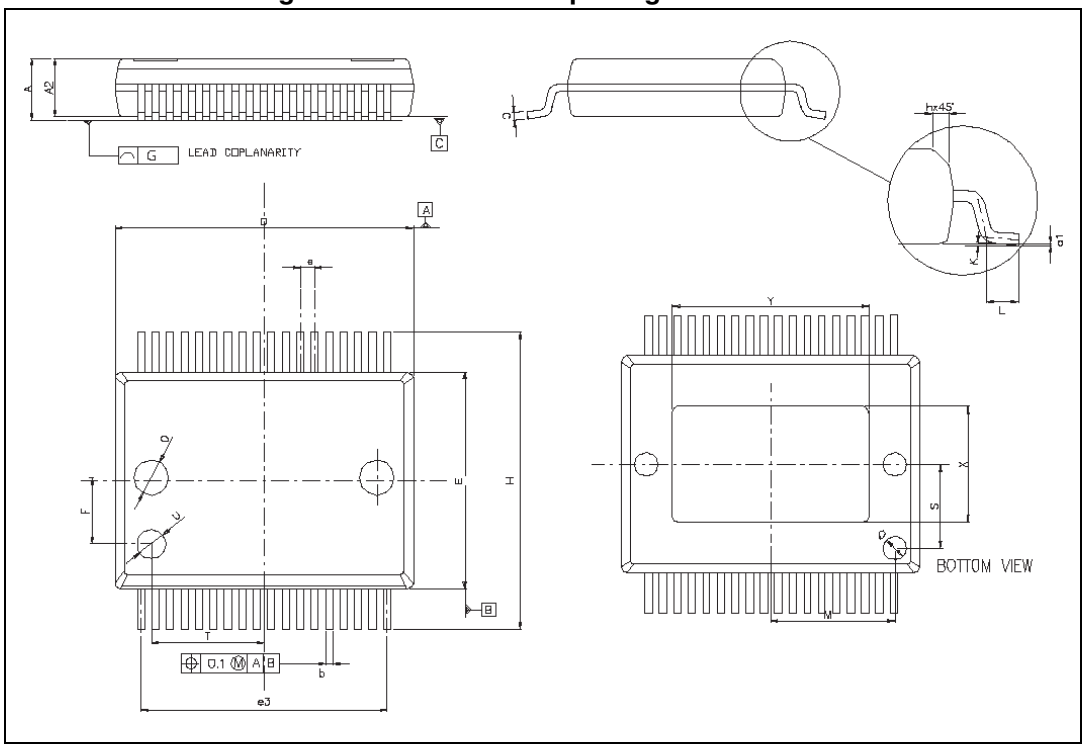


Figure 17. PowerSSO-36 tube shipment (no suffix)

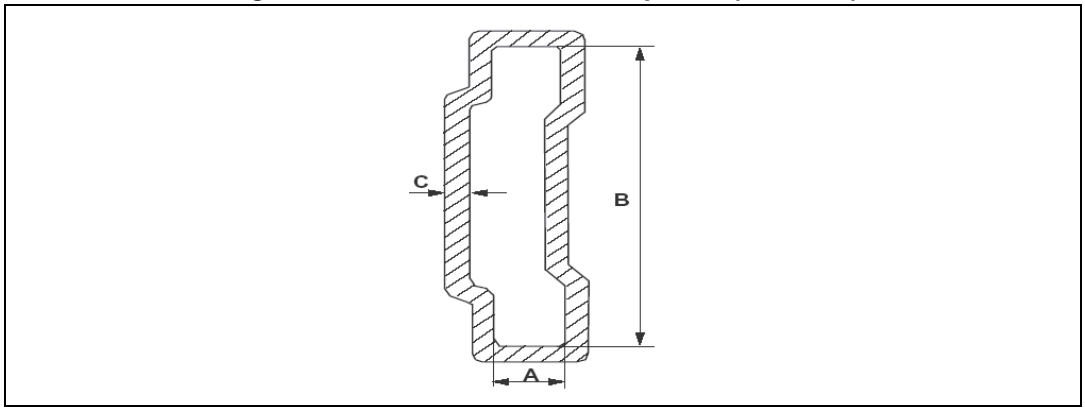


Table 20. PowerSSO-36 tube shipment

Base Q.ty	49
Bulk Q.ty	1225
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

Note: All dimensions are in mm.

Figure 18. PowerSSO-36 reel shipment (suffix “TR”)

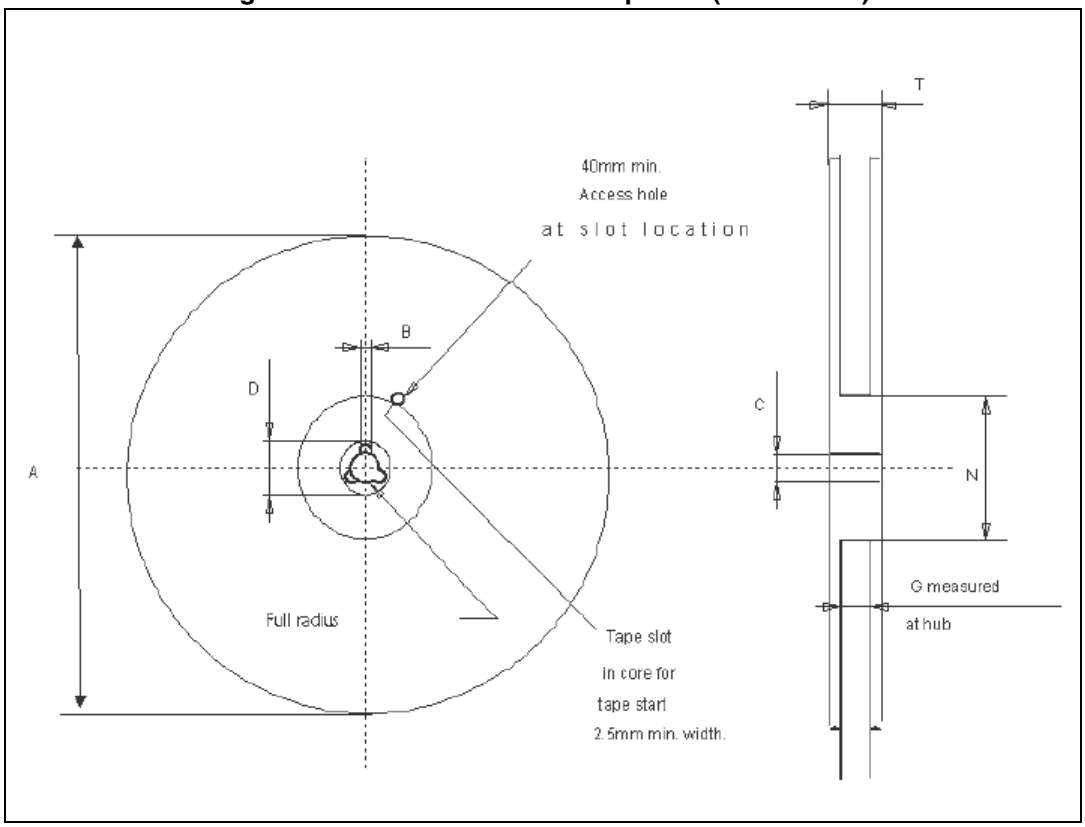


Table 21. PowerSSO-36 reel dimensions

Base Q.ty	1000
Bulk Q.ty	1000
A (max.)	330
B (min.)	1.5
C (± 0.2)	13
F	20.2
G (2 ± 0)	24.4
N (min.)	100
T (max.)	30.4

Figure 19. PowerSSO-36 tape dimensions

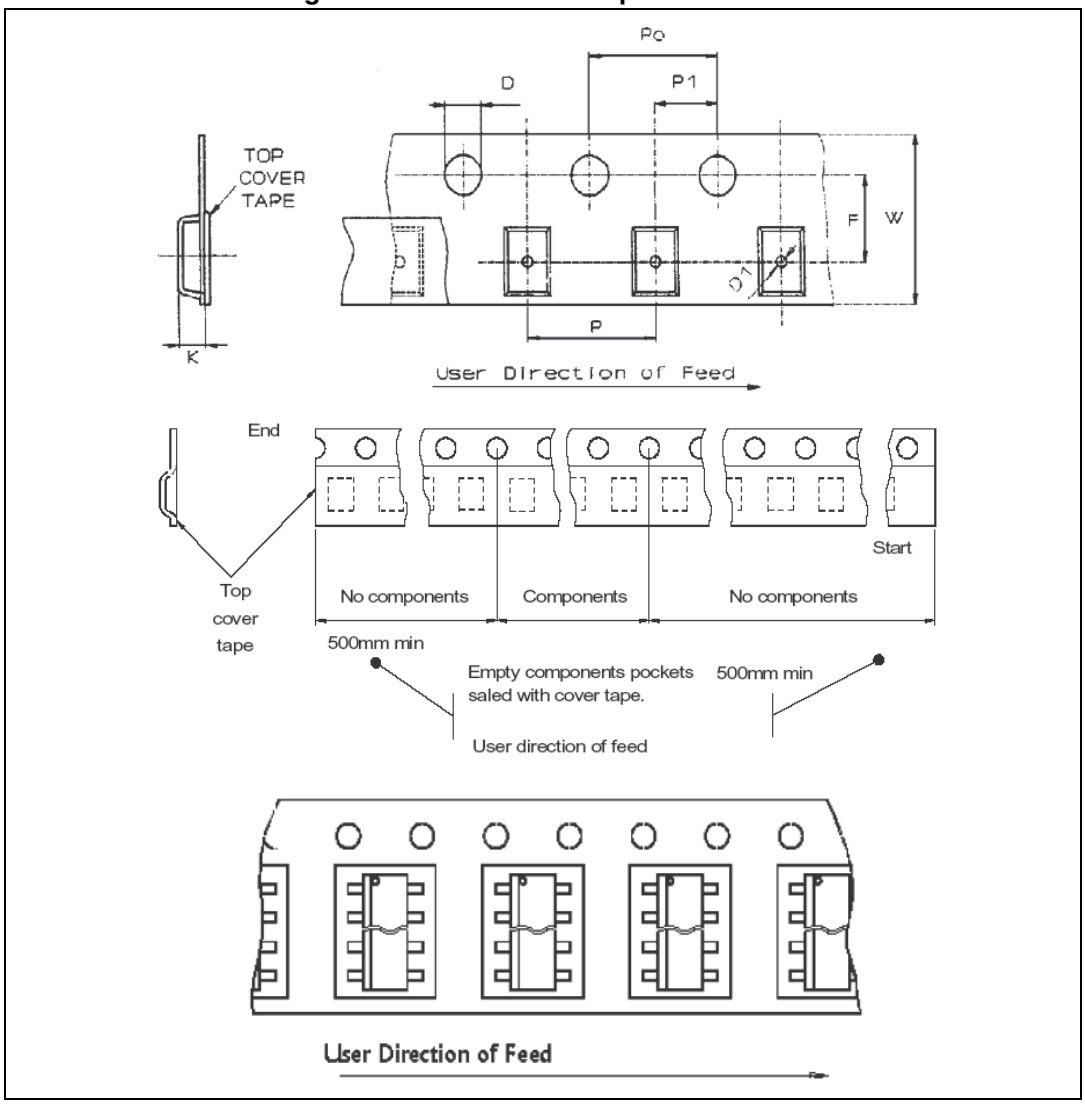


Table 22. PowerSSO-36 tape dimensions

Tape width	W	24
Tape hole spacing	P0 (± 0.1)	4
Component spacing	P	12
Hole diameter	D (± 0.05)	1.55
Hole diameter	D1 (min.)	1.5
Hole position	F (± 0.1)	11.5
Compartment depth	K (max.)	2.85
Hole spacing	P1 (± 0.1)	2

Note: According to the Electronic Industries Association (EIA) standard 481 rev. A, Feb 1986.

17 Revision history

Table 23. Document revision history

Date	Revision	Changes
04-Dec-2008	1	Initial release
29-Apr-2009	2	Updated *Table 5 on page 9*
19-Jun-2012	3	Updated: *Features*,*Section 8.4*,*Section 8.7*,*Section 8.9*,*Section 8.10*, *Section 11*,*Table 2*,*Table 3*,*Table 5*,*Table 7*,*Table 8*,*Table 9*, *Table 10*,*Table 11*,*Table 14*,*Figure 1*,*Figure 2*. Changed: *Figure 4*,*Figure 5*,*Figure 6*,*Figure 15*,*Figure 15*. Content reworked to improve the readability.
27-Jun-2012	4	Changed: Symbols in 16-bit frame *Section 9.2*.
08-Mar-2013	5	Updated *Table 5*, *Table 9*, *Table 10*, *Table 14*. Updated footnote *2.* in *Table 4*. Updated *Section 11*. Added *Section 6*. Changed *Figure 8* and *Figure 9*. Added *Table 12*. Changed product status to production data.

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