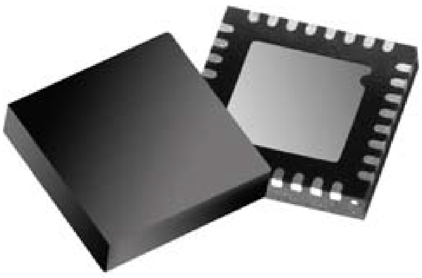
VNF1048F

Datasheet

High-side switch Controller with intelligent fuse protection for 12 V, 24 V and 48 V automotive applications



QFN32L 5x5

Product status link
VNF1048F

Product summary	
Order code	VNF1048FTR
Package	QFN32L
Packing	Tape and reel

Features

Max transient supply voltage	VS	70 V
Operating voltage range	VS	6 V to 60 V
Operating voltage range (extended)	VS	6 V to 70 V
Standby current (max)	IS_Q	70 µA
SPI I/O supply voltage	VSPI	3 V to 5.5 V
SPI standby current (max)	I_STBY	5 µA

- AEC-Q100 automotive qualified
- General
  - High side switch Control IC with e-fuse protection for Automotive 12 V, 24 V and 48 V applications
  - SPI slave interface for host control
  - 32-bit ST-SPI interface compatible with 3.3 V and 5 V CMOS level
  - 2 stage charge pump
  - Gate drive for an external MOSFET in high side configuration
  - High precision uni-directional digital current sense via SPI through an external high side shunt resistor
  - Input for a NTC resistor to monitor the external MOSFET temperature
  - Very low standby current
  - Robust fail-safe functionality through internal and external controls
  - SPI register lock-out by a dedicate digital input pin
  - Integrated ADC for TJ, VNTC, VOUT and VDS conversion
- Protections
  - Battery under-voltage shut-down
  - External MOSFET desaturation shutdown configurable via SPI
  - Hard short circuit latch-off configurable via SPI
  - Current vs time latch-off configurable via SPI (fuse-emulation)
  - Device overtemperature shutdown
  - External MOSFET overtemperature shutdown
- Intelligent high current fuse replacement for automotive applications
- Especially intended for automotive power distribution applications

Description

The device is an advanced controller for a power MOSFET in high side configuration, designed for the implementation of an Intelligent High Side Switch for 12 V, 24 V and 48 V automotive applications. The Control IC is interfaced to a host microcontroller through a 3.3 V and 5 V CMOS-compatible SPI interface and provides protection and diagnostics to the system.

1 Block diagram and pin description

Figure 1. **Block diagram**

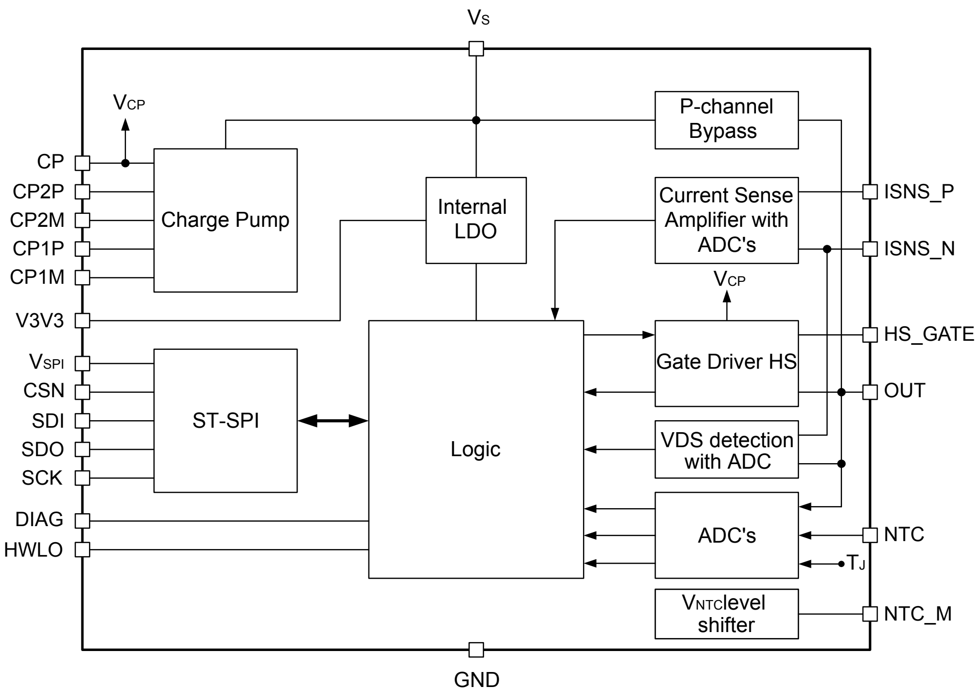
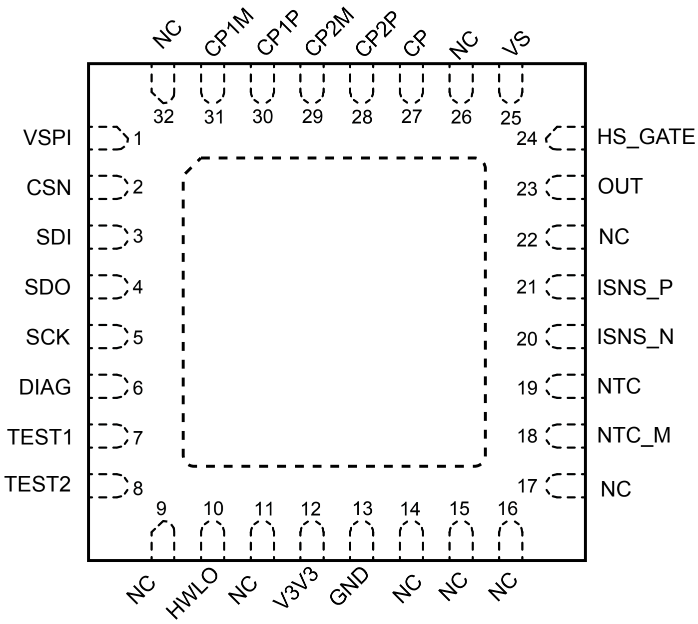


Figure 2. **Configuration diagram (top view)**



Note: TAB connection must be to ground. TAB is not intended as device reference ground (dedicated pin shall be used).

Table 1. **Pin functions**

Name	Function
VS	Input supply pin. Connect to the 12 V, 24 V, 48 V battery voltage.
CP	Charge pump output.
CP2P	Charge pump–Positive terminal of the flying capacitor C_{P2}.
CP2M	Charge pump–Negative terminal of the flying capacitor C_{P2}.
CP1P	Charge pump–Positive terminal of the flying capacitor C_{P1}.
CP1M	Charge pump–Negative terminal of the flying capacitor C_{P1}.
GND	Ground connection.
VSPI	DC supply input for the SPI interface. 3.3 V and 5 V compatible.
V3V3	Output of the 3.3 V internal LDO voltage regulator (logic and I/O supply). Connect a low ESR capacitor (1 µF) close to this pin.
CSN	Chip select not (active low) for SPI communication. It is the selection pin of the device. CMOS compatible input.
SDI	Serial data input for SPI communication. Data is transferred serially into the device on SCK rising edge.
SDO	Serial data output for SPI communication. Data is transferred serially out of the device on SCK falling edge.
SCK	Serial clock for SPI communication. It is a CMOS compatible input.
DIAG	Open drain logic output. Diagnostic feedback. DIAG = '0' if (SR1.WAKEUPM = '1') or (GSB.DIAGS = '1') or (GSB.DE = '1') else '1'
HWLO	Active high input pin compatible with 3.3 V and 5 V CMOS; it causes transitions to states where the registers are locked from writing.
ISNS_P	Current sense amplifier positive input.
ISNS_N	Current sense amplifier negative input.
HS_GATE	Output of the gate driver for the external FET.
OUT	External FET source connection.
NTC	Positive input pin for external NTC resistor.
NTC_M	Negative input pin for external NTC resistor.
TEST1	Test mode pin 1- must be connected to ground.
TEST2	Test mode pin 2- must be connected to ground.

2 Electrical specification

2.1 Absolute maximum ratings

Stressing the device above the rating listed in Table 2 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the table below for extended periods may affect device reliability.

Table 2. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0.3 to 70	V
$-I_{GND}$	DC reverse ground pin current	200	mA
V_{SPI}	DC input voltage	-0.3 to 5.5	V
V_{3V3}	DC Output voltage	-0.3 to 4.6	V
V_{CSN}, V_{SDI}, V_{SCK}	SPI pins DC input voltage	-0.3 to 5.5	V
V_{SDO}	SPI pins DC output voltage	-0.3 to V_{SPI} +0.3	V
V_{HWLO}	DC input voltage	-0.3 to 5.5	V
V_{DIAG}	DC Output voltage	-0.3 to V_SPI + 0.3	V
I_{DIAG}	DC Input current	Internally limited if V_S< 3.3 V	mA
V_{ISNS_P}	DC input voltage	-0.3 to V_S +0.3 if V_S< 3.3 V	V
V_{ISNS_N}		V_S-3.3 to V_S +0.3 if V_{OUT}<V_{CP}-20 V	V
V_{HS_GATE}	DC Output voltage	V_{out}-0.3 V to V_{out} + 20 V if V_{out} < V_{CP}-20 V	V
		V_{out}-0.3 V to V_{CP} + 0.3 V	
V_{OUT}	DC Output voltage	-2 to V_S +3	V
V_{OUT} transient	Transient Output voltage	-10 to V_S +3 For 10 µs max	V
V_{NTC}	DC input voltage	-0.3 to V_S +0.3 if V_S<3.3 V	V
		V_S -3.3 to V_S +0.3	V
V_{NTC_M}	DC input voltage	-0.3 to V_S +0.3 if V_S<3.3 V	V
		V_S -3.3 to V_S +0.3	V
V_{CP}	DC input voltage	V_S -0.3 to V_S+20	V
V_{CP1P}	DC input voltage	V_S -0.3 to V_S+20	V
V_{CP2P}	DC input voltage	V_S -0.6 to V_S+20	V
V_{CP1M}, V_{CP2M}	DC input voltage	-0.3 to V_S +0.3	V
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F)	2000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	±500(1)	V
		±750(2)	
T_j	Junction operating temperature	-40 to 150	°C

Symbol	Parameter	Value	Unit
T_{stg}	Storage temperature	-55 to 150	°C

1. *All pins except corners.*
2. *Corner pins.*

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5) (1)	56	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7)	26	

1. *Device mounted on two-layer 2s0p PCB with 2 cm² heatsink copper trace*

2.3 Main electrical characteristics

6 V < V_S < 60 V; -40 °C < T_J < 150 °C, unless otherwise specified.

All typical values refer to V_S = 48 V; T_J = 25 °C, unless otherwise specified.

Table 4. Supply specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
1.1	V_S	Operating supply voltage		6	48	60	V
1.2	V_{S_EXT}	Extended operating supply voltage	100 ms max duration	6		70	V
1.3	V_{S_USD}	Under voltage shutdown		4.5			V
1.4	$V_{S\_USD\_RES}$	Under voltage shutdown reset				6	V
1.5	$V_{S\_USD\_HYS}$	Under voltage shutdown hysteresis			0.1		V
1.6	t_{VS_USD}	Under voltage shutdown filtering time.			33		µs
1.7	V_{SPI}	SPI I/Os supply voltage		3.0		5.5	V
1.8	I_{SPI}	SPI supply current during frame communication				3	mA
1.9	I_{SPI_STBY}	SPI supply current in standby state				5	µA
1.10	$I_{S(ON)}$	Supply current (includes logic)	f_{PWM} = 1 Hz, Q_G = 250 nC, V_S= 48 V, OUT = V_S (1)		8	11	mA
			f_{PWM} = 1 Hz, Q_G = 250 nC, V_S= 48 V, OUT = V_S		12		mA
1.11	I_{OUT}	Output current	V_S = 48 V, Stand-by mode, OUT = GND, Bypass switch OFF			250	µA
			V_S = 13 V, Stand-by mode OUT = GND, Bypass switch OFF			75	µA
			V_S = 48 V, Unlocked mode OUT=GND, Bypass switch OFF			1.3	mA
			V_S = 13 V, Unlocked mode OUT=GND, Bypass switch OFF			1.15	mA
1.12	I_{S_Q}	Vs quiescent current (includes logic) – independently from bypass switch condition	V_S = 48 V, T_J = 25 °C, OUT = V_S			80	µA
			V_S = 48 V, T_J = 25 °C, OUT = GND			310	µA
			V_S = 13 V, T_J = 25 °C, OUT = V_S			70	µA
			V_S = 13 V, T_J = 25 °C, OUT = GND			130	µA
1.13	$V_{S\_POR\_ON}$	Power-on reset threshold. Device leaves the Reset mode			2.5		V
1.14	$V_{S\_POR\_OFF}$	Power-on shutdown threshold. Device enters Reset mode			2.3		V
1.15	$V_{S\_POR\_HYST}$	Power-on reset hysteresis			0.2		V
1.16	t_{PWON}	Time from Power-on to stand-by	V_S>$V_{S\_POR\_ON}$ V3V3 external capacitor 1 µF			500	µs

1. *Measured in test mode with the charge pump off.*

Table 5. SPI logic inputs (CSN, SCK and SDI) specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
2.1	I_{IL}	Low level Input current (SCK and SDI)	V_{IL} = 0.3 * V_{SPI}	0.5		5	µA
		Low level Input current (CSN)		-0.5			µA
2.2	I_{IH}	High level Input current (SCK and SDI)	V_{IL} = 0.7 * V_{SPI}	0.5		5	µA
		High level Input current (CSN)		-0.5			µA
2.3	V_{IL}	Low level Input voltage				0.3 * V_{SPI}	V
2.4	V_{IH}	High level input voltage		0.7 * V_{SPI}			V
2.5	V_{I_HYST}	Input hysteresis voltage			0.4		V
2.6	V_{ICL}	SCK and SDI clamping voltage			V_{SPI} + 0.6		V

Table 6. SPI logic outputs (SDO) Specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
2.7	V_{OL}	Low level output voltage				0.2 * V_{SPI}	V
2.8	V_{OH}	High level output voltage		0.8 * V_{SPI}			V
2.9	I_{LO}	Output leakage current		-10		10	µA

Table 7. HWLO logic input pin specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
2.10	I_{IL}	Low level Input current		0.5		1	µA
2.11	I_{IH}	High level Input current		10			µA
2.12	V_{IL}	Low level Input voltage				0.9	V
2.13	V_{IH}	High level input voltage		2.1			V
2.14	V_{I_HYST}	Input hysteresis voltage			0.4		V
2.15	t_{HWLO}	HWLO filtering time			33		µs

Table 8. DIAG logic output pin specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
2.16	V_{DIAG_PD}	DIAG pin open-drain pull down voltage				0.2	V
2.17	I_{DIAG_PD}	DIAG pin open-drain input current	V_{DIAG} = V_{DIAG_PD}			1	mA
2.18	I_{DIAG_LKG}	DIAG pin open-drain leakage current	V_{DIAG} = V_{SPI} = 5.5 V	0		1	µA

Table 9. Device Thermal shutdown

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
2.19	T_{TSD}	Junction temperature thermal shutdown threshold		160	175	190	°C
2.20	T_{TSD_HYS}	Junction temperature thermal shutdown hysteresis			15		°C

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
2.21	$T_{J\_ADC\_CONV}$	Junction Temperature ADC full scale range resolution	$T_{J\_ADC}[9:0] = (T_J + 72) * 3$	0		1023	
2.22	$T_{J\_ADC\_RATE}$	Junction Temperature ADC sample rate			10		kSamples/s

Table 10. ST-SPI Specification: Timings

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
3.1	f_C	SPI Clock frequency				8	MHz
3.2	t_{WHCH}	CSN low timeout	V_{SPI} = 3.3 V, ext R_{PROT} < 1 kΩ	30		70	ms
3.3	t_{WDTB}	Watchdog toggle bit timeout. WD_TIME Configuration:		- 10 %		+ 10 %	ms
		00			50		
		01			100		
		10			150		
		11			200		
3.4	t_{STBY_OUT}	Minimum time during which CSN must be toggled low to go out of STDBY mode		20		100	µs

Table 11. Charge Pump Specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
4.1	V_{CP_6V}	Charge Pump output voltage	V_S = 6V	V_S + 7	V_S + 11		V
4.2	V_{CP_10V}	Charge Pump output voltage	V_S > 10 V	V_S + 13.5	V_S + 14.5	V_S + 15.5	V
4.5	$V_{CP\_LOW\_H}$	Charge Pump output under voltage high threshold	Ramp up on V_{CP}	V_S + 5.5	V_S + 6	V_S + 6.5	V
	$V_{CP\_LOW\_L}$	Charge Pump output under voltage low threshold	Ramp down on V_{CP}	V_S + 5.1	V_S + 5.6	V_S + 6.2	V
	$V_{CP\_LOW\_hyst}$	Charge Pump output under voltage hysteresis			0.4		V
4.6	f_{CP}	Charge Pump frequency		- 5 %	400	+ 5 %	kHz
4.7	t_{CP_RISE}	Charge Pump low (CP_LOW diagnostic) rising edge filtering time		- 5 %	60	+ 5 %	µs
4.8	t_{CP_FALL}	Charge Pump low (CP_LOW diagnostic) falling edge filtering time		- 10 %	2.3	+ 10 %	µs

Table 12. External FET Gate Driver Specification

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
5.1	V_{GSON_6V}	Gate-On Voltage	V_S = 6 V, IG = 50 µA	6			V
5.2	V_{GSON_10V}	Gate-On Voltage	V_S > 10 V, IG = 50 µA	12		15	V
5.4	V_{GSOFF}	Gate-Off Voltage				0.5	V
5.5	V_{GSMAX}	Maximum Gate Voltage (internally limited)				20	V
5.6	t_{ON}	Gate turn on	V_{GS} = 0.5 V to V_{GS} = 10 V			4	µs

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
			C_{GATE} = 80 nF				
5.7	t_{OFF}	Gate turn off	Full V_{GS} to V_{GS} < 0.5 C_{GATE} = 80 nF			2.6	µs
5.8	$V_{GS\_UVLO\_6V}$	Gate under voltage lockout	V_S = 6 V	5			V
5.9	$V_{GS\_UVLO\_10V}$	Gate under voltage lockout	V_S >10 V	8.5			V
5.10	$V_{G\_UVLO\_BLK}$	Gate under voltage lockout blanking	Enable at Charge Pump startup if Ext FET turn-on is required, and applied after CP_LOW expiration (falling edge)	- 6 %	100	+ 6 %	µs
5.11	$V_{G\_UVLO\_DEGLITCH}$	Gate under voltage lockout de-glitch filtering time		- 15 %	8	+ 15 %	µs
5.12	Q_{GMAX}	Maximum gate charge	V_{GS} = 10 V			800	nC

Table 13. **Current sense amplifier with integrated ADC**

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
6.1	V_{SENSE_CM}	Common-mode input voltage range		0		70	V
6.2	V_{SENSE_FSR}	Differential input voltage full scale range		0		160	mV
6.3	$I_{\_SENSE\_P}$	CSA positive input current			400		µA
6.4	$I_{\_SENSE\_N}$	CSA negative input current			560		µA
6.5	$V_{SENSE\_ADC\_CONV}$	Current Sense ADC Full scale range resolution	V_{SENSE_ADC}[12:0] = MIN((V_{SENSE}/160 * 8192), 8191)	0		8191	
6.6	$V_{SENSE\_REFRESH}$	Current Sense ADC sample rate			2.4		kSample/s
6.7	$V_{SENSE\_ACC\_6mV}$	Digital Current Sense Accuracy	6 mV < V_{SENSE_DIFF} < 10 mV	-10		+10	%
6.8	$V_{SENSE\_ACC\_10mV}$		V_{SENSE_DIFF} = 10 mV	-5		+5	%
6.9	$V_{SENSE\_ACC\_20mV}$		V_{SENSE_DIFF} > 20 mV	-3		+3	%
6.10	$V_{SENSE\_ACC\_1.8mV}$		1.8 mV < V_{SENSE_DIFF} < 6 mV	-17		+17	%

Table 14. **External FET VDS Protection**

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
7.1	$V_{DS\_THRS\_RANGE}$	V_{DS} monitor threshold range 31 steps adjustable through SPI		300		1800	mV
7.2	$V_{DS\_THRS\_STEP}$	V_{DS} monitor threshold step			50		mV
7.3	$V_{DS\_THRS\_0}$	V_{DS} monitor thresholds			300		mV
	$V_{DS\_THRS\_1}$				350		
	$V_{DS\_THRS\_2}$				400		
	$V_{DS\_THRS\_3}$				450		
	$V_{DS\_THRS\_4}$				500		
	$V_{DS\_THRS\_5}$				550		

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
7.3	$V_{DS\_THRS\_6}$	V_{DS} monitor thresholds			600		mV
	$V_{DS\_THRS\_7}$				650		
	$V_{DS\_THRS\_8}$				700		
	$V_{DS\_THRS\_9}$				750		
	$V_{DS\_THRS\_10}$				800		
	$V_{DS\_THRS\_11}$				850		
	$V_{DS\_THRS\_12}$				900		
	$V_{DS\_THRS\_13}$				950		
	$V_{DS\_THRS\_14}$				1000		
	$V_{DS\_THRS\_15}$				1050		
	$V_{DS\_THRS\_16}$				1100		
	$V_{DS\_THRS\_17}$				1150		
	$V_{DS\_THRS\_18}$				1200		
	$V_{DS\_THRS\_19}$				1250		
	$V_{DS\_THRS\_20}$				1300		
	$V_{DS\_THRS\_21}$				1350		
	$V_{DS\_THRS\_22}$				1400		
	$V_{DS\_THRS\_23}$				1450		
	$V_{DS\_THRS\_24}$				1500		
	$V_{DS\_THRS\_25}$				1550		
	$V_{DS\_THRS\_26}$				1600		
	$V_{DS\_THRS\_27}$				1650		
	$V_{DS\_THRS\_28}$				1700		
	$V_{DS\_THRS\_29}$				1750		
	$V_{DS\_THRS\_30}$				1800		
7.4	$V_{DS\_THRS\_ACC}$	V_{DS} monitor threshold accuracy		-5		5	%
7.5	$V_{DS\_DEGLITCH}$	V_{DS} monitor shut-off deglitch time		-25%	5	+25%	µs
7.6	V_{DS_DELAY}	V_{DS} monitor shut-off delay time				5	µs
7.7	V_{DS_BLK}	V_{DS} monitor shut-off blanking time	At High Side External FET startup	-10%	960	+10%	µs
7.8	$V_{DS\_ADC\_CONV}$	VDS monitor ADC full scale range resolution	V_{DS_ADC}[9:0] = MIN((V_{SENSE_N} - V_{OUT})/2 * 1024, 957)	0		957	
7.9	$V_{DS\_ADC\_RATE}$	VDS monitor ADC sample rate			0.9		MSample/s

Table 15. Hard Short Circuit protection

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
8.1	$V_{HSC\_THRS\_RANGE}$	Hard Short Circuit protection threshold range 16 steps adjustable thru SPI		20		160	mV

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
8.2	$V_{HSC\_THRS\_0}$	Hard Short Circuit protection thresholds			20		mV
	$V_{HSC\_THRS\_1}$				23		
	$V_{HSC\_THRS\_2}$				26.4		
	$V_{HSC\_THRS\_3}$				30.3		
	$V_{HSC\_THRS\_4}$				34.8		
	$V_{HSC\_THRS\_5}$				40		
	$V_{HSC\_THRS\_6}$				45.9		
	$V_{HSC\_THRS\_7}$				52.8		
	$V_{HSC\_THRS\_8}$				60.6		
	$V_{HSC\_THRS\_9}$				69.6		
	$V_{HSC\_THRS\_10}$				80		
	$V_{HSC\_THRS\_11}$				91.9		
	$V_{HSC\_THRS\_12}$				105.6		
	$V_{HSC\_THRS\_13}$				121.3		
	$V_{HSC\_THRS\_14}$				139.3		
	$V_{HSC\_THRS\_15}$				160.00		
8.3	$V_{HSC\_THRS\_ACC}$	Hard Short Circuit protection threshold accuracy		-5		5	%
8.4	V_{HSC_DELAY}	Hard Short Circuit protection delay time				5	µs
8.5	$V_{HSC\_ADC\_CONV}$	Hard Short Circuit protection ADC full range resolution	V_{HSC_ADC}[9:0] = MIN((V_{SENSE}/ 160*1024), 1023)	0		1023	
8.6	$V_{HSC\_ADC\_RATE}$	Hard Short Circuit ADC sample rate			0.9		MSample/s

Table 16. Overcurrent protection

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
9.1	$V_{OC\_THRS\_RANGE}$	Overcurrent protection threshold range 32 steps adjustable thru SPI		6		90	mV
9.2	$V_{OC\_THRS\_0}$	Overcurrent protection thresholds		-12%	6	+12%	mV
	$V_{OC\_THRS\_1}$				7.2		
	$V_{OC\_THRS\_2}$				8.7		
	$V_{OC\_THRS\_3}$			-7%	10.4	+7%	
	$V_{OC\_THRS\_4}$				11.8		
	$V_{OC\_THRS\_5}$				13		
	$V_{OC\_THRS\_6}$				13.8		
	$V_{OC\_THRS\_7}$				14.8		
	$V_{OC\_THRS\_8}$				15.8		
	$V_{OC\_THRS\_9}$				16.8		
	$V_{OC\_THRS\_10}$				17.9		

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
9.2	$V_{OC\_THRS\_11}$	Overcurrent protection thresholds		-7%	19.1	+7%	mV
	$V_{OC\_THRS\_12}$				20.4		
	$V_{OC\_THRS\_13}$			-5%	21.8	+5%	
	$V_{OC\_THRS\_14}$				23.3		
	$V_{OC\_THRS\_15}$				24.8		
	$V_{OC\_THRS\_16}$				26.5		
	$V_{OC\_THRS\_17}$				28.2		
	$V_{OC\_THRS\_18}$				30.1		
	$V_{OC\_THRS\_19}$				32.2		
	$V_{OC\_THRS\_20}$				34.3		
	$V_{OC\_THRS\_21}$				36.6		
	$V_{OC\_THRS\_22}$				39.1		
	$V_{OC\_THRS\_23}$				41.7		
	$V_{OC\_THRS\_24}$				44.5		
	$V_{OC\_THRS\_25}$				47.5		
	$V_{OC\_THRS\_26}$				50.6		
	$V_{OC\_THRS\_27}$				54		
	$V_{OC\_THRS\_28}$				61.3		
	$V_{OC\_THRS\_29}$				69.5		
	$V_{OC\_THRS\_30}$				78.8		
	$V_{OC\_THRS\_31}$				89.3		
9.3	i-time_tol_t	I-t tolerance on time step (y axis)		(t-10%) - 32		(t+10%) +32	µs
9.4	$t_{I\_SAMPLING}$	Shunt current sampling time		-10%	61	+10%	µs

Note: Overcurrent protection is based on the same 10-bit ADC used for Hard Short protection.

Table 17. External FET Thermal Shutdown via NTC input

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
10.1	V_{NTC_FSR}	NTC input voltage full scale range		VSENSE_N – 1.2		VSENSE_N	V
10.2	V_{NTC_M}	NTC_M output voltage			VSENSE_N – 1.2		V
10.3	V_{NTC_ACC}	NTC input voltage threshold accuracy		-3		3	mV
10.4	$V_{NTC\_THRS\_0}$	External FET thermal shutdown NTC input voltage thresholds			110.92		mV
	$V_{NTC\_THRS\_1}$				98.76		
	$V_{NTC\_THRS\_2}$				88.07		
	$V_{NTC\_THRS\_3}$				78.66		
	$V_{NTC\_THRS\_4}$				70.38		
	$V_{NTC\_THRS\_5}$				63.08		

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
10.4	$V_{NTC\_THRS\_6}$	External FET thermal shutdown NTC input voltage thresholds			56.64		mV
	$V_{NTC\_THRS\_7}$				50.95		
	$V_{NTC\_THRS\_8}$				45.92		
	$V_{NTC\_THRS\_9}$				41.46		
	$V_{NTC\_THRS\_10}$				37.50		
	$V_{NTC\_THRS\_11}$				37.50		
	$V_{NTC\_THRS\_12}$				37.50		
	$V_{NTC\_THRS\_13}$				37.50		
	$V_{NTC\_THRS\_14}$				37.50		
	$V_{NTC\_THRS\_15}$				37.50		
10.5	$V_{NTC\_DEGLITCH}$	External FET thermal shutdown deglitch time		10		500	µs
10.6	$V_{NTC\_ADC\_CONV}$	External FET thermal shutdown ADC full range resolution	$V_{NTC\_ADC}[9:0]$ = MIN(((V_{SENSE_N} - V_{NTC})/1.2 * 1024), 1023)	0		1023	
10.7	$V_{NTC\_ADC\_RATE}$	External FET thermal shutdown ADC sample rate			4.9		kSample/s

Note:
- *VNTC = VBG * RNTC / (RT_REF + RNTC)*
- *RNTC = B57232V5103F360 (10 kΩ @ 25 °C)*
- *RT-REF = 10 kΩ +/- 1 %*

Figure 3. NTC bridge

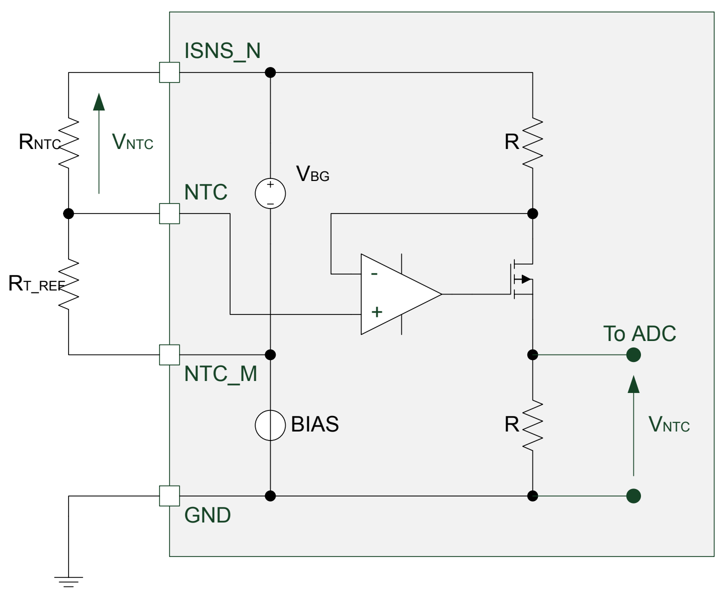


Table 18. **Bypass switch**

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
11.1	$V_{DS\_BYPASS\_SAT}$	Bypass switch VDS saturation protection threshold		1		2	V
11.2	I_{BYPASS_SAT}	Bypass switch saturation current	V_S - V_{OUT} = $V_{DS\_BYPASS\_SAT}$	100			mA
11.3	$R_{DS(ON)\_BYPASS}$	Bypass switch on state resistance		4	7	10	Ω
11.4	t_{ON_BYPOFF}	Output turn-on time on bypass-sutthing off				100	µs
11.5	$t_{BYPASS\_STA\_DEGLITCH}$	Bypass switch saturation diagnostic de-glitch filtering time		4		5	µs

Table 19. **V_{OUT} A-to-D Conversion**

ID	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
12.1	$V_{OUT\_ADC\_CONV}$	V_{OUT} ADC full range resolution	V_{OUT_ADC}[9:0] = MIN(V_{OUT}/(51*1.2)*1024, 1023)	0		1023	
12.2	$V_{OUT\_ADC\_RATE}$	V_{OUT} ADC sample rate			4.9		kSample/s

3 eFuse function

Protection of wire harness and PCB can be performed by defining an ideal time to fuse curve as a result of a maximum power dissipation over the time in the wire or copper PCB traces themselves. This function can guarantee that the insulation of wires and PCB are subject to a limited temperature and time budget that is below the reliability specified values. Not respecting such specified limits can lead to the formation of a conducting path by carbonization across the organic insulation materials and therefore local hot spot can conduct to sparking and fire ignition.

The VNF1048F embeds the ST proprietary eFuse functionality for the implementation of a robust and flexible overcurrent protection mechanism. The eFuse functionality features an intelligent circuit breaking aimed at protecting PCB traces, connectors and wire harness from overheating, with no impact on load transients like inrush currents and capacitance charging.

This function is set by two parameters called I_{NOM} and t_{NOM}. The value of I_{NOM} corresponds to the maximum continuous current while t_{NOM} will determine a current versus time-to-fuse curve when load current is higher than I_{NOM}. The expression of current versus time-to-fuse is approximated by an optimized stepwise function, which can be adjusted in a range between the wire I^2-t limit on one side and load transient characteristics on the other side. The value of t_{NOM} corresponds to the first step up of the curve. The current time curve is always active in combination with very fast overcurrent protection that will be triggered when the current reaches a defined threshold for hard short circuit condition.

When the current in the load is pulse wide modulated the eFuse function calculates the mean square root of the current. Mean square root of the current is also calculated when switching on/off the power switch during normal operation or after a switch off due to short circuit/overload condition. So if for example the circuit is broken due to an overload and after a while the circuit is activated again, the eFuse keeps in memory the previous condition and still avoids that maximum I_{RMS} is higher than I_{NOM}.

VIP-Fuse is programmed via SPI as follows:

- VOC_THRS sets I_{NOM} = VOC_THRS/Rsense
- VHSC_THRS sets hard short circuit current = VHSC_THRS/Rsense
- T_NOM sets t_{NOM} from 1 to 511 s

No intervention occurs for VSENSE < VOC_THRS, whilst an immediate shut-off occurs for VSENSE > VHSC_THRS.

The eFuse functionality operating range is defined between VOC_THRS and VHSC_THRS. In that range, the circuit breaking profile is defined by the stepwise function reported in Figure 4. The number of steps is consequential to the selection of VOC_THRS and VHSC_THRS, the maximum being 15, when VOC_THRS = 6 mV and VHSC_THRS = 160 mV. This corresponds to a 1:26.67 ratio between the maximum allowed continuous current and hard short circuit.

The Figure 5 shows the I^2-t curve when VOC_THRS = 26.5 mV and VHSC_THRS = 105.60 mV. The number of steps is reduced to 9 accordingly.

Figure 4. eFuse I^2-t typical curve (VOC_thrs minimum - VHSC_thrs maximum)

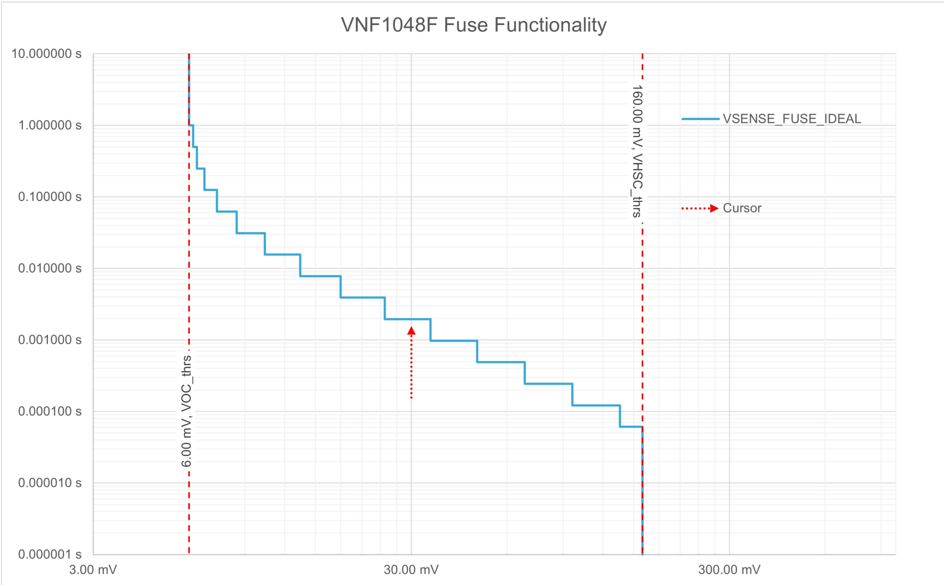
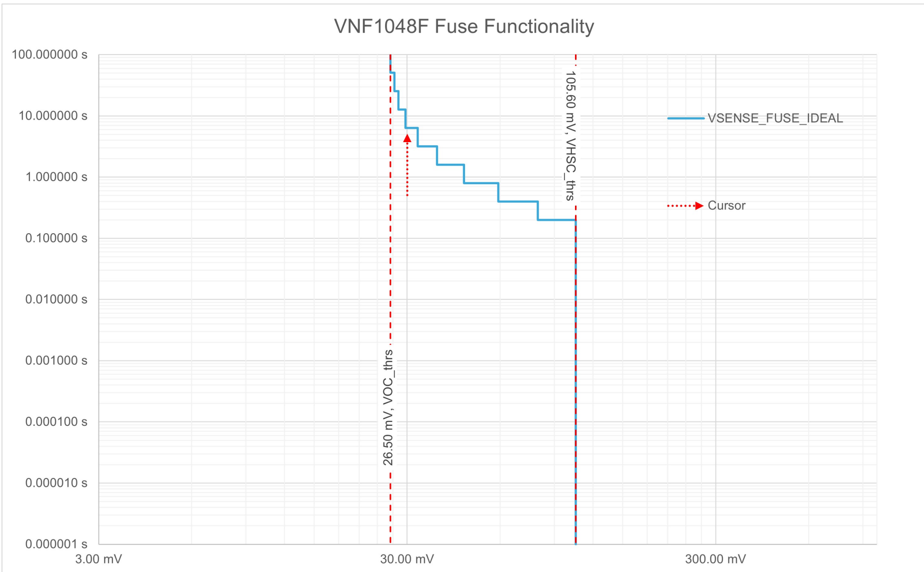


Figure 5. eFuse I^2-t typical curve (generic thresholds)



4 Self Test

The following sections describe how the device supports the execution of the in-application tests, needed to verify the proper behavior of the hardware diagnostic verification during product lifetime. Configuration, control and check for each of the tests are performed in close relationship with micro-controller, through SPI interface communication.

Activities related to self-test are possible in a specific device state (Self Test) in order to distinguish it from operating modes (Stand-by, WakeUp, Unlocked and Locked modes), allowing to manage differently diagnostic faults according to the hardware feature under test.

Self test control interface

The initialization of the Self Test sequence (selection of the Self Test, start and stop command) is done through the Control Register 1 (CR#1). Results are accessible through the Status Register 5 (SR#5), Status Register 6 (SR#6) and Status Register 7 (SR#7).

4.1 Current Sense Self Test

The goal of the Current Sense Self Test is to verify the proper behavior of the full current-sense chain, from the analog input to the digital output.

Starting from the Unlocked State, the Current sense Self Test is activated through a dedicated SPI frame. The duration of this test is around 10 μs; the first 5 μs are intended to convert the value of the voltage across the Rsense.

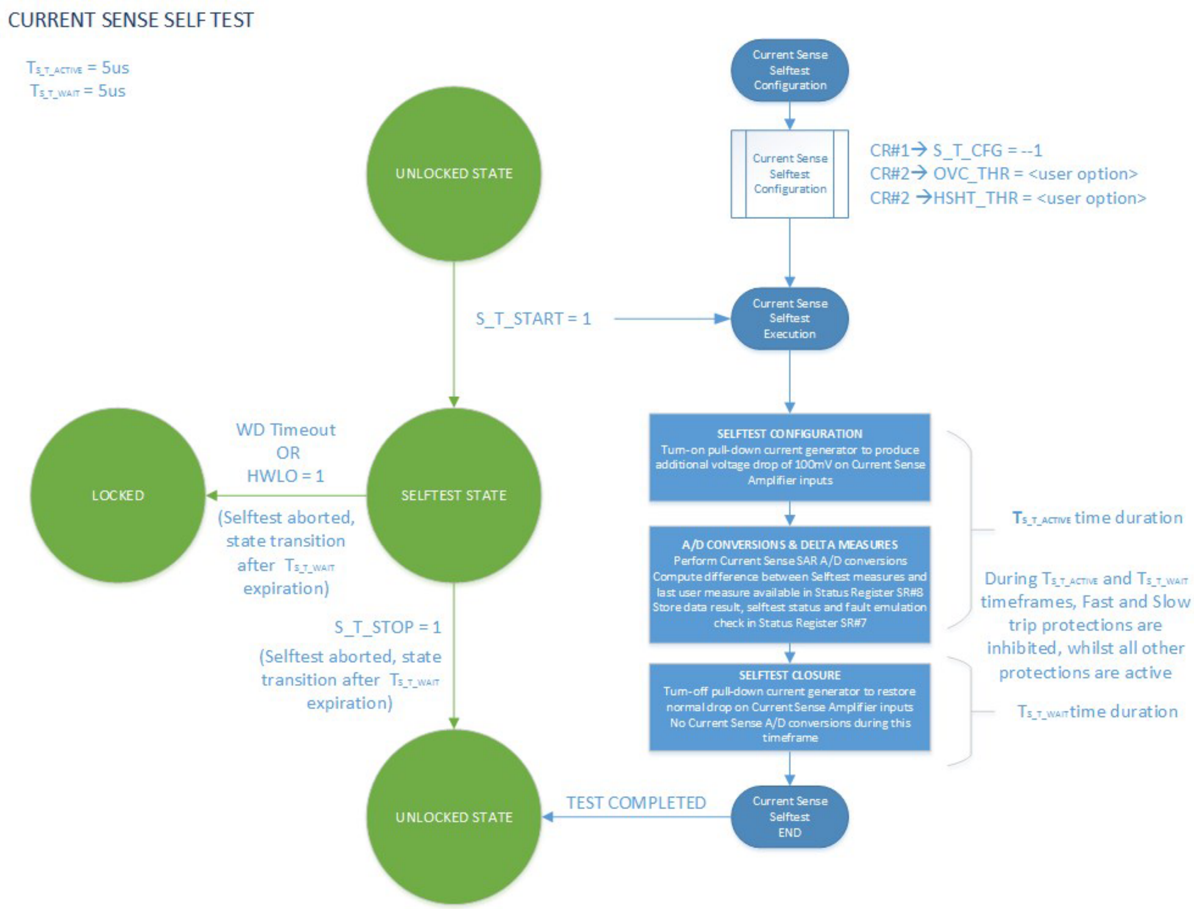
Once the Self Test is started, an internal current generator provides a current sink able to produce an additional voltage drop of 100 mV at the input pin of the internal comparator.

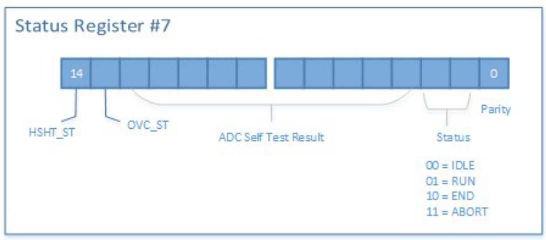
The result of the Self Test is the difference between this converted value and the value already stored in SR#8 (HSHT), corresponding to the normal measurement performed during operation; such result is stored in SR#7 together with the Self Test status.

The transition from Self Test state to Unlocked state is automatically guaranteed after the test is completed (around 10 μs) or if the test is stopped through S_T_STOP = 1 (Self Test aborted).

The transition from the Self Test state to the Locked state can occur in case of watchdog timeout or HWLO = 1 (Self Test aborted).

Figure 6. Current sense self test flow sequence





4.2 External FET V_{DS} Detection Self Test

The goal of the external FET V_{DS} Detection Self Test is to verify the proper behavior of the complete V_{DS} monitor chain (sense/process/detection), from the analog input to the digital output.

Starting from the Unlocked State, the V_{DS} Detection Self Test is activated through a dedicated SPI frame. The duration of this test is around 10 μs; the first 5 μs are intended to convert the value of the voltage across Drain and Source terminals of external FET, remaining 5 μs are required to bring back analog circuitry to normal configuration.

Once the Self Test is started, an internal current generator provides a current sink able to produce an additional voltage offset of 100 mV on V_{DS} monitor circuit inputs, to distinguish Self Test execution from normal operation. In order to guarantee proper data conversions, special care must be taken to avoid V_{DS} ADC saturation by keeping the overall V_{DS} sensed by monitor circuit below maximum scale range (1.87 V).

V_{DS} Detection Self Test result is the difference between converted value obtained during Self Test execution and the value already stored in SR#4 (V_{DS} field), corresponding to the normal measurement performed during operation; such delta measure result is stored in SR#5 (S_T_VDS field) together with the Self Test status.

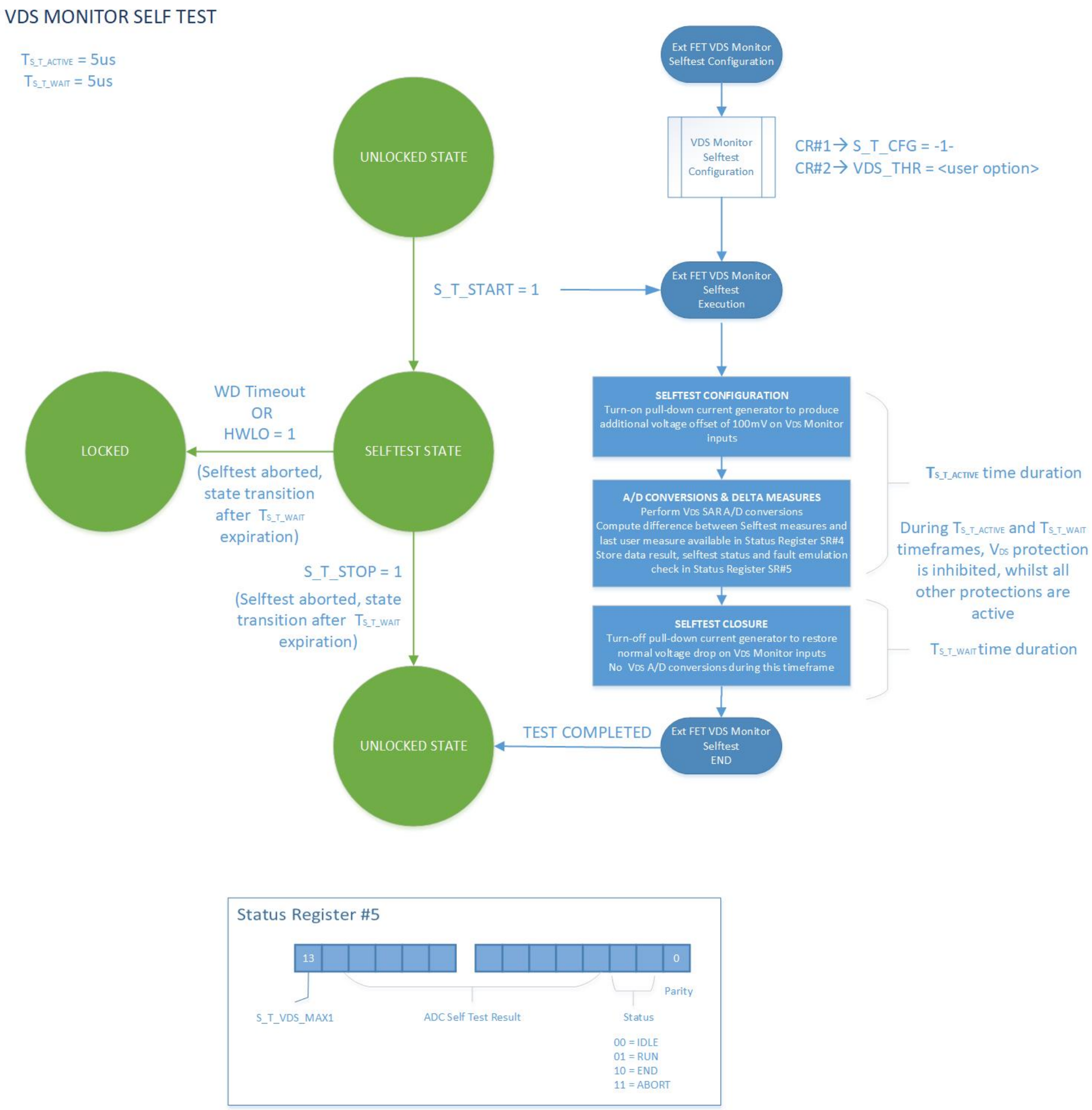
During Self Test execution it is also possible to emulate external FET V_{DS} fault condition by playing with programmable thresholds available through register CR#2 (VDS_THR field); fault emulation result is stored in SR#5 (S_T_VDS_MAX1 bit field).

To be noted that diagnostic fault for normal operation (VDS_MAX, SR#1) is inhibited during execution, while all the others are kept enabled.

The transition from Self Test state to Unlocked state is automatically guaranteed after the test is completed (around 10 μs) or if the test is stopped through S_T_STOP = 1 (Self Test aborted).

The transition from the Self Test state to the Locked state can occur in case of watchdog timeout or HWLO = 1 (Self Test aborted).

Figure 7. VDS monitor self test flow sequence



4.3 External FET Stuck-on Self Test

The goal of this Self Test is to verify proper turn-off of the external power switch, by monitoring its V_{DS} behavior in time.

Starting from the Unlocked State, the external FET Stuck-on Self Test is activated through a dedicated SPI frame (CR#1, S_T_START & S_T_CFG fields).

At execution start the external FET is automatically turned-off, regardless of its status during previous operations, then continuous AtoD conversions of V_{DS} voltage, sensed across external power switch terminals, are performed in order to allow the user to monitor V_{DS} evolution in time.

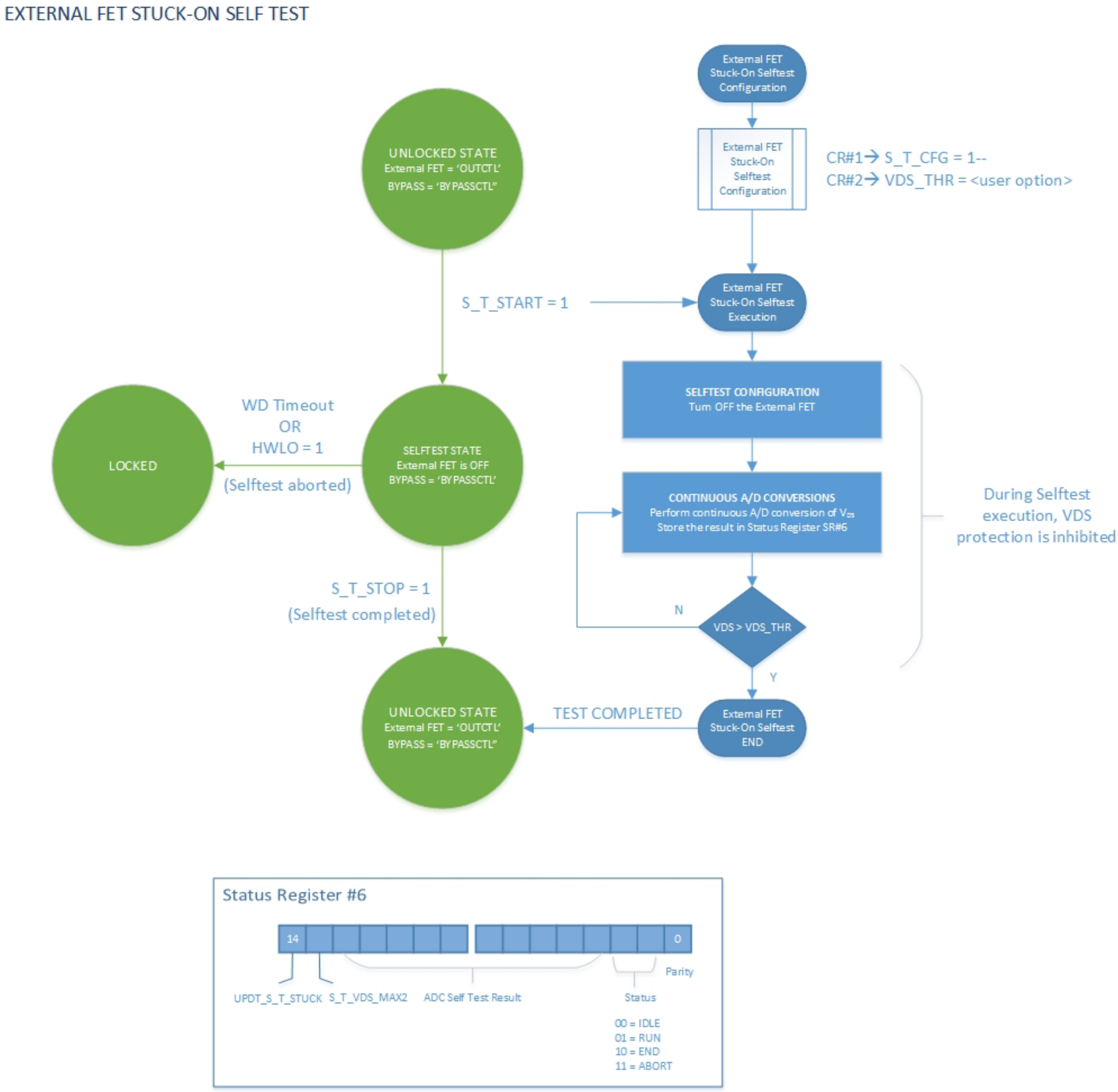
Data conversion values are made available through dedicated register SR#6 (S_T_STUCK field); in addition, a specific bit informs the user if the data have been updated with a new measure or are still relative to the previous one (UPDT_S_T_STUCK bit). Status of Self Test execution is available in the same register.

Self Test completion can be controlled directly by sending S_T_STOP command (CR#1, bit 8) or by setting programmable V_{DS} threshold (CR#2, VDS_THR field): in this case, Self Test is stopped automatically as soon as the external FET V_{DS} overcomes the aforementioned threshold and a specific bit is set to flag this situation (SR#6, S_T_VDS_MAX2 bit). In both cases device FSM performs transition from Self Test to Unlocked state.

To be noted that diagnostic fault for normal operation (VDS_MAX, SR#1) is inhibited during execution, while all the others are kept enabled; bypass switch control is left to the user.

The transition from the Self Test state to the Locked state can occur in case of watchdog timeout or HWLO = 1 (Self Test aborted).

Figure 8. **External FET Stuck-on self test - flow sequence for entry**



5 Protections

5.1 Battery undervoltage shutdown

The device is able to operate down to Vs = 6 V, with the charge pump still active. If the battery supply voltage Vs falls below the undervoltage shutdown threshold, the device enters in Battery undervoltage mode. The current sense diagnostic is not available. The charge pump, the output stage and the bypass switch are off regardless of the SPI status.

If V_S rises above the threshold (V_{S_USD} + $V_{S\_USD\_hys}$) the device returns to the last mode.

An undervoltage flag is set in the SPI register when $V_S < V_{S\_USD}$, and automatically reset when $V_S > V_{S\_USD} + V_{S\_USD\_hys}$.

5.2 Device overtemperature shutdown

The device temperature is internally monitored. An overtemperature shut-down of the device occurs when T_J exceeds T_{TSD}. The charge pump, the output stage and the bypass switch are off. A fault indication is given via SPI.

The device restarts when T_J decreased below T_{TSD} - T_{TSD_HYS}.

V_{TJ} is converted by a dedicated ADC converter. The converted result is stored in the Status register and can be read via SPI.

5.3 External MOSFET overtemperature shutdown

The external MOSFET temperature is monitored through a 10 kΩ NTC thermistor with one terminal connected to the Drain of the MOSFET, in order to allow optimal component placement.

R_{NTC} is part of a V_{BG} (1.2 V) voltage divider through NTC and NTC_M pins:

$$V_{NTC} = \frac{V_{BG} \times R_{NTC}}{R_{T\_REF} + R_{NTC}} \quad (1)$$

V_{NTC} is converted by a dedicated ADC converter. The converted result is stored in the Status register and can be read via SPI.

An overtemperature shut-down of the MOSFET occurs when V_{NTC} voltage decreases under a preset threshold. The threshold can be set via SPI in the range from 100 °C to 150 °C in steps of 5 °C. In this case both output stages and bypass switch are turned off.

The MOSFET and the bypass switch are re-armed via SPI by clearing latched fault NTC_OVT bit.

This protection is not active in case of external MOSFET in OFF state.

5.4 External MOSFET desaturation shut-down

The external MOSFET drain-source voltage is monitored by the Control IC. A desaturation shut-down of the MOSFET occurs when the VDS exceeds the preset threshold. In this case both output stage and bypass switch are turned off. The threshold can be set via SPI in the range 0.3 V to 1.80 V in steps of 50 mV (default = 300 mV).

The MOSFET and bypass switch are re-armed via SPI by clearing latched fault VDS_MAX bit.

V_{DS} is converted by a dedicated ADC converter. The converted result is stored in the Status register and can be read via SPI.

This protection is not active in case of external MOSFET in OFF state.

5.5 Hard short circuit latch-off

The external MOSFET drain-source current is monitored by the Control IC through the current sense amplifier, which reads the voltage drop across a high side shunt resistor. A hard short circuit shut-down of the MOSFET occurs when the current sense voltage exceeds the preset threshold. In this case both output stage and bypass switch are turned off. The threshold can be set via SPI in the range from 20 mV to 160 mV.

The MOSFET is re-armed via SPI by clearing HSHT latched fault bit.

V_{HSHT} is converted by a dedicated ADC converter. The converted result is stored in the Status register and can be read via SPI.

This protection is not active in case the external MOSFET is in OFF state.

5.6 Current vs time latch-off

The external MOSFET drain-source current is monitored by the Control IC through the current sense amplifier, which reads the voltage drop across a high side shunt resistor. The overload detection circuitry emulates the response of a traditional fuse. An overcurrent shut-down of the MOSFET occurs when the current sense voltage exceeds the preset threshold for longer than the preset time. In this case both output stages and bypass switch are turned off. The threshold can be set via SPI in the range 6 mV to 90 mV, while the nominal trip time can be programmed in the range from 1 s to 511 s.

The MOSFET is re-armed via SPI by clearing FUSE_LATCH latched fault bit. This protection is not active in case the external MOSFET is in OFF state.

In case of hard short protection event occurrence, reported by HSHT flag bit, FUSE_LATCH bit is set as well.

5.7 Low Current Bypass desaturation shut-down

Internal bypass switch VDS voltage (VS - VOUT) is monitored by the IC, to protect the switch from load current sink changes.

A desaturation shut-down of the bypass occurs when its VDS exceeds a fixed threshold (~1.3V); in this situation, the bypass switch is turned off while the external FET is turned on through HS_GATE output, directly by hardware, regardless of their software controlled bit status, in order to protect the bypass and provide the requested current capability to connected load.

This represents the so-called AUTO-ON event and it is flagged by bit #4 (AUTOON) of the Global Status Byte, that corresponds to BYPASS_SAT flag of Status Register #1.

Bypass switch can be re-armed through SPI control by clearing BYPASS_SAT fault latched bit.

This protection is not active in case bypass switch is in OFF state.

A particular case is represented by Stand-By wakeup event occurrence, with FSM state transition to Wake-Up state, due to bypass switch desaturation: only in this situation, in addition to the aforementioned actions on bypass switch and external FET, the device will signal, by driving DIAG pin low, that it has been woken up by hardware event (load current increase), in order to allow host control to take proper actions.

It is important to notice that bypass switch cannot be used to charge any type of load, even those requesting small currents capability: on the contrary, it shall be used to keep powered application loads, previously charged by external FET, when they switch to low-power consumption modes (i.e. Stand-By).

6 SPI functional description

6.1 SPI Communication

The SPI communication is based on the “ST-SPI Specification”.

The device operates in Slave mode on a bus configuration through CSN, SDI, SDO and SCK signal lines, with 32 bits SPI frames.

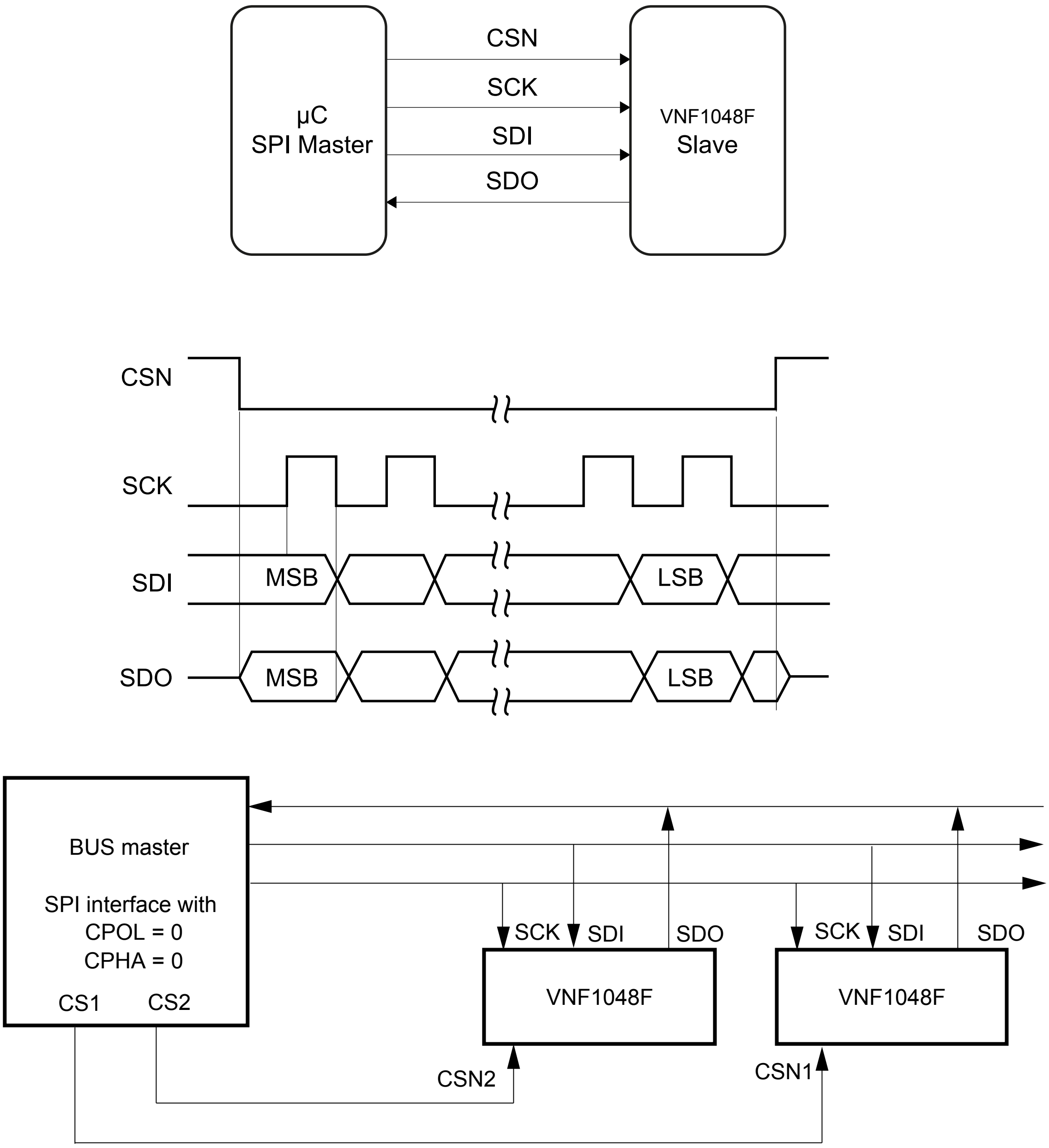
A SPI Master device (Host Microcontroller) initiates the communication.

The SPI Master device must be configured in the following mode:

CPOL = 0, CPHA = 0

Input data are shifted into SDI, MSB first while output data are shifted out on SDO, MSB first.

Figure 9. SPI functional diagram



6.2 Signal description

Serial clock SCK

This input signal provides the timing of the serial interface. Data present at Serial Data Input (SDI) are latched on the rising edge of Serial Clock (SCK). Data on Serial Data Output (SDO) change after the falling edge of Serial Clock (SCK).

Serial data input SDI

This input signal is used to transfer data serially into the device. It receives data to be written. Values are sampled on the rising edge of Serial Clock (SCK).

Serial data output SDO

This output signal is used to transfer data serially out of the device. Data are shifted out on the falling edge of Serial Clock (SCK).

Chip select CSN

The communication interface is deselected, when this input signal is logically high. A falling edge on CSN enables and starts the communication while a rising edge finishes the communication and the sent command is executed when a valid frame was sent. During communication start and stop the Serial Clock (SCK) has to be logically low.

6.3 SPI protocol

SDI format during each communication frame starts with a command byte. It begins with two bits of operating code (OC1, OC0) which specify the type of operation (read, write, read and clear status, read device information) and it is followed by a 6-bit address (A5 : A0). The command byte is followed by three input data bytes: (D23 : D16), (D15 : D8) and (D7 : D0).

Table 20. Command byte

MSB							LSB
OC1	OC0	A5	A4	A3	A2	A1	A0

Table 21. Input data byte 1

MSB							LSB
D23	D22	D21	D20	D19	D18	D17	D16

Table 22. Input data byte 2

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8

Table 23. Input data byte 3

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

Table 24. Global status byte

SDO format during each communication frame starts with a specific byte called Global Status Byte (see GSB byte for more details on bit0 - bit7). This byte is followed by three output data bytes (D23 : D16), (D15 : D8) and (D7 : D0).

MSB							LSB
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

Table 25. Output data byte 1

MSB							LSB
D23	D22	D21	D20	D19	D18	D17	D16

Table 26. **Output data byte 2**

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8

Table 27. **Output data byte 3**

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

6.4 Operating code definition

The SPI interface features four different addressing modes which are listed in Table 28.

Table 28. **Operating codes**

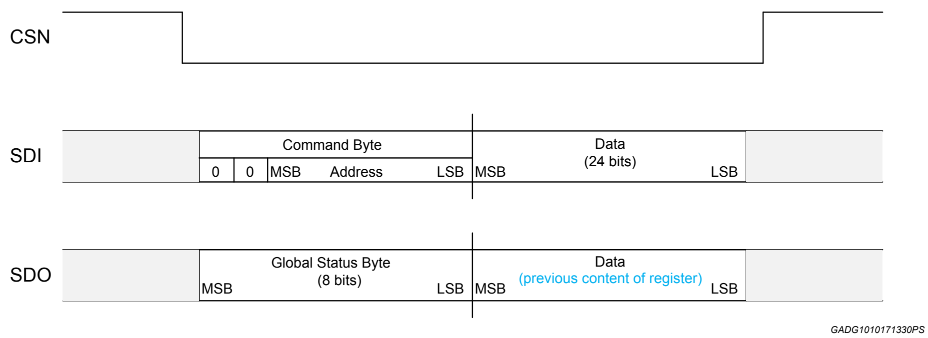
OC1	OC0	Meaning
0	0	Write operation
0	1	Read operation
1	0	Read and clear status operation
1	1	Read device information

6.5 Write mode

The write mode of the device allows to write the content of the input data byte into the addressed register (see list of registers in Table 33. RAM memory map (ID 12.1)). Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first.

During the same sequence outgoing data are shifted out MSB first on the falling edge of the CSN pin and subsequent bits on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status Byte, second, third and forth bytes to the previous content of the addressed register. Unused bits will be always read as 0.

Figure 10. **SPI write operation**



6.6 Read mode

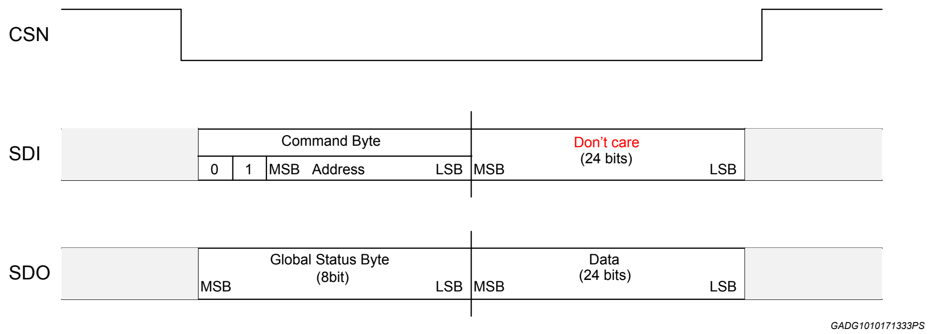
The read mode of the device allows to read and to check the state of any registers.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status Byte, second, third and forth byte to the content of the addressed register.Unused bits will be always read as 0.

In order to avoid inconsistency between the Global Status byte and the Status register, the Status register contents are frozen during SPI communication.

Figure 11. SPI read operation



6.7 Read and clear status command

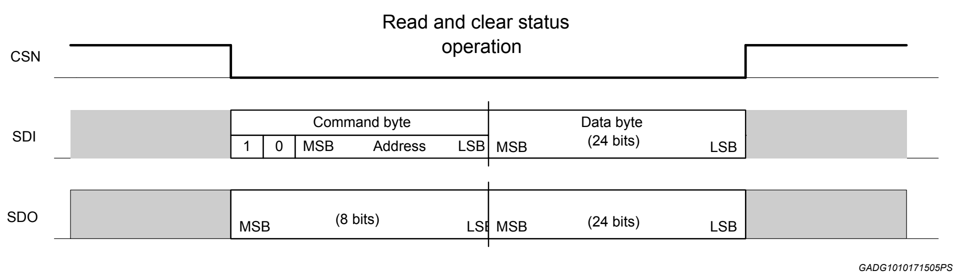
The read and clear status operation is used to clear the content of the addressed status register (see Table 33. RAM memory map (ID 12.1)). A read and clear status operation with address 0x3Fh clears all Status registers simultaneously.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which register content is read and the payload bits set to 1 into the data byte determine the bits into the register which have to be cleared.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status byte, second, third and forth byte to the content of the addressed register. Unused bits will be always read as 0.

In order to avoid inconsistency between the Global Status byte and the Status register, the Status register contents are frozen during SPI communication.

Figure 12. SPI read and clear operation



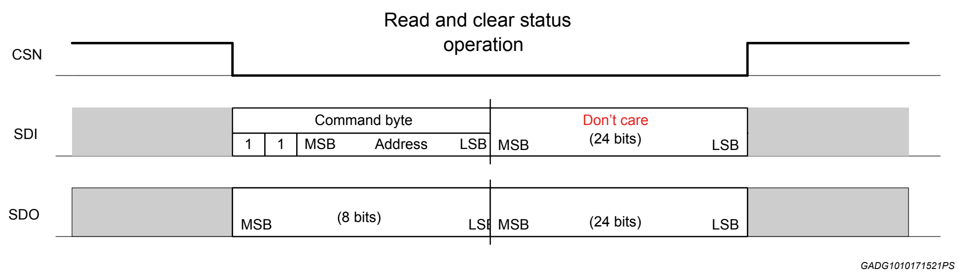
6.8 SPI device information

Specific information can be read but not modified during this mode.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which information is read, whilst the other three data bytes are "don’t care".

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status byte, second byte to the content of the addressed register, third and forth bytes are 0x00.

Figure 13. SPI read device information



6.9 Special commands

0xFF — SWReset: set all control registers to default and clears all status register

An Opcode ‘11’ (read device information) addressed at ‘111111’ forces a Software Reset of the device, second, third and forth bytes are "don't care" provided that at least one bit is zero.

Note: an OpCode '11' at address '111111' with data field equal to '1111111111111111' the SPI frame is recognized as a frame error and SPIE bit of GSB is set.

Table 29. 0xFF: (SW_Reset)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command							
OC1	OC0	Address					
1	1	1	1	1	1	1	1
DATA1	X(1)	X	X	X	X	X	X
	0	0	0	0	0	0	0
DATA2	X	X	X	X	X	X	X
	0	0	0	0	0	0	0
DATA3	X	X	X	X	X	X	X
	0	0	0	0	0	0	0

1. *X: do not care*

0xBF — clear all status registers (RAM access)

When an OpCode ‘10’ (read and clear operation) at address b’111111 is performed.

Table 30. Clear all status registers (RAM access)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command							
OC1	OC0	Address					
1	0	1	1	1	1	1	1
DATA1	X[(1)]	X	X	X	X	X	X
	0	0	0	0	0	0	0
DATA2	X	X	X	X	X	X	X
	0	0	0	0	0	0	0
DATA3	X	X	X	X	X	X	X
	0	0	0	0	0	0	0

1. *X: do not care*

6.10 Global status byte

As per **ST SPI 4.1** specification, the device features an In-Frame response mechanism.

A global status byte is transmitted to the SPI Master on the SDO line while the command byte is received on the SDI line.

The global status byte reports the global status of the device:

Table 31. Global status byte

Global status byte								
Bit	MSB	30	29	28	27	26	25	LSB
Name	GSBN	RSTB	SPIE	AUTOON	DIAGS	DE	OVC	FS

Table 32. Global status byte - bit description

Bit #	Name	Description
31	GSBN	**Global status bit NOT** This bit is a NOR combination of the remaining bits of this register: GSBN = NOT (RSTB or SPIE or AUTOON or DIAGS or DE or OVC or FS) This bit can also be used as Global Status Flag without starting a complete communication frame as it is present directly after pulling CSN low.
30	RSTB	**Reset bit** The RSTB indicates a device hardware reset. This bit is set in PowerON mode. All internal Control Registers are set to default and kept in that state until the bit is automatically cleared by the first valid SPI communication.
29	SPIE	**SPI error** The SPIE is a logical OR combination of errors related to a wrong SPI communication: SDI stuck-at fault, SPI frame length ≠ 32bit (wrong number of clock pulses while CSN is low), parity check error
28	AUTOON	**AUTOON** The AUTOON indicates the automatic turn-on of the external FET due to Low Current Bypass de-saturation (BYPASS_SAT = 1) when its VDS exceeds fixed threshold (~1.3 V). This bit will be also set by a transition from WakeUp to Unlocked mode. AUTOON = BYPASS_SAT
27	DIAGS	**Diagnostic signal bit**

Bit #	Name	Description
		The DIAGS is a logical OR combination of all faults which cause the External FET to be switched off DIAGS = VS_UV or HSHT or VDS_MAX or FUSE_LATCH or DEV_OVT or NTC_OVT or VGS_LOW or DIS_OUT_FAULT
26	DE	**Device error bit** The DE is a logical OR combination of errors related to device specific blocks: charge pump output under voltage DE = CP_LOW
25	OVC	**Overcurrent bit** The OVC is a ‘realtime’ bit indicating an over-current event (VIP-fuse counter running)
24	FS	**Fail safe** If FS bit is set, device was forced into a safe state. This bit is set in WakeUp mode (WAKEUPM = 1) or in Locked mode (LOCKEDM = 1) FS = WAKEUPM or LOCKEDM

6.11 Address map

Table 33. **RAM memory map (ID 12.1)**

Address	Name	Access type	Content
01h	Control Register 1	R/W	**CR#1**: 1st Control Register (CONTROLS)
02h	Control Register 2	R/W	**CR#2**: 2nd Control Register (CONFIG 1)
03h	Control Register 3	R/W	**CR#3**: 3rd Control Register (CONFIG 2)
…	…	…	…
11h	Status Register 1	R/C	**SR#1**: 1st Status Register (DIAGNOSTICS + PROTECTIONS)
12h	Status Register 2	R	**SR#2**: 2nd Status Register (CURRENT SENSE)
13h	Status Register 3	R	**SR#3**: 3rd Status Register (NTC + TJ)
14h	Status Register 4	R	**SR#4**: 4th Status Register (VOUT + VDS)
15h	Status Register 5	R/C	**SR#5**: 5th Status Register (SELFTEST VDS)
16h	Status Register 6	R/C	**SR#6**: 6th Status Register (SELFTEST STUCK ON)
17h	Status Register 7	R/C	**SR#7**: 7th Status Register (SELFTEST CURRENT SENSE)
18h	Status Register 8	R	**SR#8**: 8th Status Register (HSHT)
…	…	…	…

Address	Name	Access type	Content
21h	Reserved		
22h	Reserved		
…	…	…	
31h	Reserved		
32h	Reserved		
33h	Reserved		
34h	Reserved		
…	…	…	
3Fh	Advanced Operation Code	C	A R&C operation to this address causes all clearable status registers to be cleared

6.12 ROM memory map

Table 34. **ROM Memory Map (ID 12.2)**

Address	Name	Access	Content	Comments
00h	Company Code	Read Only	00h	00h =STMicroelectronics
01h	Device family	Read Only	01h	BCD product family
02h	Product Code 1	Read Only	55h	ST internal Product Code = ‘UR5J’
03h	Product Code 2	Read Only	52h	
04h	Product Code 3	Read Only	05h	
05h	Product Code 4	Read Only	4Ah	
0Ah	Silicon version	Read Only	02h	AD silicon version
10h	SPI Mode	Read Only	31h	Bit7 = 0, burst read is disabled, SPI data length = 32bit Bit6, DL2 = 0 Bit5, DL1 = 1 Bit4, DL0 = 1 Bit3, SPI8 =0: 8-bit frame option not available Bit2 =0: Parity check is used Bit1, S1=0 Bit0, S0=1
11h	WD Type 1	Read Only	4Ah	A WD is implemented Bit7, WD1 =0 Bit6, WD0 =1 WD period 5ms = 10*ms -> WT[5:0] = 0xA Bit5, WT5 = 0 Bit4, WT4 = 0 Bit3, WT3 = 1 Bit2, WT2 = 0 Bit1, WT1 = 1 Bit0, WT0 = 0

Address	Name	Access	Content	Comments
13h	WD bit pos. 1	Read Only	43h	Bit7,WB1 = 0 Bit6,WB2 = 1 WBA[5-0], Bit[5-0] = address of the config. register, where the WD bit is located = 03h = 000011b
14h	WD bit pos. 2	Read Only	C1h	Bit7,WB1 = 1 Bit6,WB0 = 1 Bit position of the WD bit within the corresponding configuration register = 01d = 000001b
3Fh	Advanced Operation Code	Read Only	00h	Access to this address provokes a SW reset (all control registers are set to their default values; in addition, all clearable status registers are cleared too). *Note: data field should not be “all ones”, otherwise an “SDI stuck at” error occurs.*

6.13 Control registers

Table 35. CR#1: Control Register 1 (read/write); Address 01h (ID 13.1)

Bit	Default	Name	Description
23 ÷ 12		Unused	
11	0	**GOSTBY**	GOSTBY can be set to 1 only if UNLOCK = 1; trying to set this bit to 1 when UNLOCK = 0 will have no effects and it will maintain its previous value. GOSTBY can be reset to 0 also when UNLOCK = 0. To send a GOToStandby sequence it is necessary to send two consecutive SPI frames, as follows: 1st SPI write operation to set UNLOCK bit to 1 2nd SPI write operation to set GOSTBY bit to 1 and EN bit to 0. A transition to Standby state causes GOSTBY to be reset to 0.
10	0	**EN**	EN can be set to 1 only if UNLOCK = 1; trying to set this bit to 1 when UNLOCK = 0 will have no effects and it will maintain its previous value. EN can be reset to 0 also when UNLOCK = 0. To send a GOToUnlocked sequence it is necessary to send two consecutive SPI frames as follows: 1st SPI write operation to set UNLOCK bit to 1 2nd SPI write operation to set GOSTBY bit to 0 and EN bit to 1. A transition to Unlocked state causes EN to be set to 1. A transition to Locked state causes EN to be reset to 0.
9	0	**S_T_START**	When it is set to 1, starts selected self-test. If current state is Unlocked and S_T_CFG is not 000, then setting this bit causes a transition to Self-Test state. This bit is automatically reset.
8	0	**S_T_STOP**	When it is set to 1, stops execution of selected self-test. This bit is automatically reset.
7 ÷ 5	000	**S_T_CFG**	Self Test selection: 000: No selection 001: Current sense

Bit	Default	Name	Description
			010: VDS detection 100: Power switch stuck-on 011: Current sense + VDS detection 101: Current sense + Power switch stuck-on 110: VDS detection + Power switch stuck-on 111: Current sense + VDS detection + Power switch stuck-on
4	0	**OUTCTL**	Enables High Side through SPI 1: HS Gate driver commanded on 0: HS Gate driver commanded off
3	0	**BYPASSCTL**	Enables Low Current Bypass through SPI 1: LCB commanded on 0: LCB commanded off
2		Unused	
1	0	**WD_TRIG**	Mirror of WD_TRIG bit
0	0	**Parity Bit**	Odd Parity Bit Check

Table 36. **CR#2: Control Register 2 (read/write); Address 02h (ID 13.20)**

Bit	Default	Name	Description
23 ÷ 16	00000000	**T_NOM**	Configures the value of Nominal Time, required for the fuse emulation: t_{NOM} (s) = b{T_NOM(7:0), 1} T_NOM_{min} = 00000000 → t_{NOM} (s) = b000000001 = 1s T_NOM_{max} = 11111111 → t_{NOM} (s) = b111111111 = 511s Nominal Time corresponds to the trip time obtained when current is equal to the Nominal Overcurrent Threshold (OVC_THR).
15 ÷ 11	00000	**OVC _THR**	Configures the value of Nominal Overcurrent Threshold. The threshold can be set in the range 6 mV to 90 mV See Table 16
10 ÷ 7	0000	**HSHT_THR**	Configures a threshold for Hard Short Circuit Latch-off. The threshold can be set in the range from 20 mV to 160 mV. See Table 15
6 ÷ 2	00000	**VDS_THR**	Configures a threshold for External MOSFET desaturation shut-down. The threshold can be set in the range from 0.3 V to 1.80 V in steps of 50 mV (default = 300 mV). Configuration 0x1F is reserved.
1	0	**WD_TRIG**	Mirror of WD_TRIG bit
0		**Parity Bit**	Odd Parity Bit Check

Table 37. **CR#3: Control Register 3 (read/write); Address 03h (ID 13.3)**

Bit	Default	Name	Description
23 ÷ 10		unused	
9	0	**UNLOCK**	0: bits GOSTBY, EN cannot be set to 1 but can be reset; 1: bits GOSTBY, EN can be set to 1, but only with the next valid SPI frame. When UNLOCK = 1, it will be automatically reset with the next valid SPI frame.

Bit	Default	Name	Description
8 ÷ 5	0000	**NTC_THR**	Configures a threshold for External MOSFET over-temperature shutdown via NTC. The threshold can be set in the range 37.50 to 110.92. See Table 17
4 ÷ 3	00	**WD_TIME**	Watchdog time selection: 00: t_{WD} = 50ms 01: t_{WD} = 100ms 10: t_{WD} = 150ms 11: t_{WD} = 200ms
2	0	**DIS_OUT_MODE**	Outputs status in Locked state: 0: leave output and bypass as they are (default) 1: shut off output and bypass
1	0	**WD_TRIG**	In order to keep device in Unlocked Mode, this bit must be cyclically toggled within a period equal to t_{WD} to refresh the watchdog.
0		**Parity Bit**	Odd Parity Bit Check

6.14 Status registers

Table 38. **SR#1: Status Register 1; Address 11h (ID 14.1)**

Bit	Default	Name	Description	Access
23 ÷ 19		unused		
18	0	**DIS_OUT_FAULT**	Disable Output Fault: a transition to Locked Mode state causes this bit to be set to 1, but only when DIS_OUT_MODE = 1. When DIS_OUT_FAULT = 1, both High Side and Bypass are switched off.	R/C
17	0	**SELFTEST**	Self-Test state flag bit	R
16	0	**OUTST**	High Side Gate Driver Status Bit 1: HS Gate Driver turned on 0: HS Gate Driver turned off	R
15	0	**BYPASSST**	Low Current Bypass Status Bit 1: LCB turned on 0: LCB turned off	R
14	0	**WAKEUPM**	Wake Up mode flag bit	R
13	0	**LOCKEDM**	Locked Mode flag bit	R
12	0	**HWLO_ST**	HWLO mirror bit: provides the logical level of HWLO pin after having applied a symmetrical filter on both its rising and falling edges (filtering time is tHWLO)	R
11	0	**VS_UV**	V_S undervoltage “real-time” bit 0: $V_S > V_{USD} + V_{S\_USD\_HYS}$ 1: $V_S \leq V_{S\_USD}$ If the battery supply voltage VS falls below the under-voltage shutdown threshold, then the External MOSFET, the charge pump and the bypass switch are switched off.	R
10	0	**HSHT**	Hard short circuit latch-off: a hard short circuit shut-down of the MOSFET (HSHT = 1) and the bypass switch occurs when the current sense voltage exceeds the preset threshold. The MOSFET and the bypass switch are re-armed via SPI.	R/C

Bit	Default	Name	Description	Access
9	0	**VDS_MAX**	External MOSFET desaturation shut-down: a desaturation shut-down of the MOSFET (VDS_MAX = 1) and the bypass switch occurs if the VDS exceeds the preset threshold when HS is in on-state after $V_{DS\_DEGLITCH}$ time. The MOSFET and the bypass switch are re-armed via SPI.	R/C
8	0	**BYPASS_SAT**	Low Current Bypass desaturation shut-down: a desaturation shut-down of the Low Current Bypass (BYPASS_SAT = 1) occurs if the VDS exceeds the fixed threshold when HS is in off-state and bypass is in on-state. When BYPASS_SAT = 1, External MOSFET is automatically commanded on, independently on OUTCTL bit value. The Low Current Bypass is re-armed via SPI. A transition to WakeUp mode causes this bit to be set to 1.	R/C
7	0	**FUSE_LATCH**	Current vs Time latch-off: an overcurrent shut-down of the MOSFET (FUSE_LATCH = 1) and the bypass switch occurs when the current sense voltage exceeds the preset threshold for longer than the preset time (I2-t curve emulating a traditional fuse). The MOSFET and bypass switch are re-armed via SPI.	R/C
6	0	**OVC**	Overcurrent warning: an overcurrent warning (OVC = 1) occurs even when average current sense value evaluated in a time interval equal to $t_{I\_SAMPLING}$ (time basis used by fuse emulation algorithm) exceeds current threshold programmed through OVC_THR. This is a “real-time” bit OVC bit keeps memory of the previous events: once this bit is set, it will be reset automatically after a time depending on current level previously reached and on the related timings. Moreover, after a FUSE_LATCH bit setting, OVC will be automatically reset in a time interval proportional to the TNOM value previously programmed (provided that in the meantime FUSE_LATCH is not cleared, high side restarts and current is again above OVC_THR). Resetting FUSE_LATCH bit when OVC bit is still set to 1 is possible, but in this case user can expect that trip time will be lower than expected.	R
5	0	**DEV_OVT**	Over-temperature shut-down (“real-time” bit). When DEV_OVT = 1, the MOSFET, the charge pump and the bypass switch are turned off.	R
4	0	**NTC_OVT**	External MOS Over-Temperature: this bit is latched when NTC is lower than NTC_THR. When NTC_OVT = 1 both External MOS and bypass switch are turned off. The MOSFET and the bypass switch are re-armed via SPI.	R/C
3	0	**VGS_LOW**	This bit will be set in on-state when VGS falls below UV threshold ($V_{GS\_UVLO\_10V}$) for more than $V_{G\_UVLO\_DEGLITCH}$. When this bit is set, external FET is switched off.	R/C
2	0	**CP_LOW**	This bit will be set when V_{CP} falls below V_{CP_LOW} threshold for more than t_{CP_RISE}. When this bit is set, external FET driver is disabled. This is a “real-time” bit.	R
1	0	**WD_FAIL**	Watchdog failure bit: 0: Watchdog OK; 1: Watchdog failure in Unlocked / Selftest states When this bit is set, device goes to Locked state. To go back to the unlocked mode through the GoToUnlocked sequence this bit must be cleared.	R/C
0	0	**Parity Bit**	Odd Parity Bit Check	

Table 39. **SR#2: Status Register 2; Address 12h (ID 14.2)**

Bit	Default	Name	Description	Access
23 ÷ 15		unused		
14 ÷ 2	0000000000000	**CURR_SENSE**	13 bit ADC conversion related to Current Sense Amplifier, ranging from 0 V to 160 mV; unidirectional current through an external sense resistor.	R
1	0	**UPDT_CURR**	Updated status bit. This bit is set when value is updated and cleared when register is read.	R
0		**Parity Bit**	ODD Parity Bit Check	

Table 40. **SR#3: Status Register 3; Address 13h (ID 14.3)**

Bit	Default	Name	Description	Access
23		unused		
22 ÷ 13	0000000000	**TJ**	10 bit ADC conversion related to TJ (Device temperature)	R
12	0	**UPDT_TJ**	Updated status bit. This bit is set when value is updated and cleared when register is read.	R
11 ÷ 2	0000000000	**NTC**	10 bit ADC conversion related to NTC (External MOSFET temperature sensing through an external NTC resistor)	R
1	0	**UPDT_NTC**	Updated status bit. This bit is set when value is updated and cleared when register is read.	R
0		**Parity Bit**	ODD Parity Bit Check	

Table 41. **SR#4: Status Register 4; Address 14h (ID 14.4)**

Bit	Default	Name	Description	Access
23 ÷ 12		unused		
22 ÷ 13	0000000000	**VDS**	10 bit ADC conversion of the voltage across HS switch (VS-OUT). This register is not refreshed during VDS Self-Test execution.	R
12	0	**UPDT_VDS**	Updated status bit. This bit is set when value is updated and cleared when register is read.	R
11 ÷ 2	0000000000	**VOUT**	10 bit ADC conversion of the OUT pin	R
1	0	**UPDT_VOUT**	Updated status bit. This bit is set when value is updated and cleared when register is read.	R
0		**Parity Bit**	ODD Parity Bit Check	

Table 42. **SR#5: Status Register 5; Address 15h (ID 14.5)**

Bit	Default	Name	Description	Access
23 ÷ 14		unused		
13		**S_T_VDS_MAX1**	This bit is set if VDS_THR is reached during VDS self-test.	R/C
12 ÷ 3	0000000000	**S_T_VDS**	Difference between 10 bit ADC conversion of the VDS, performed during VDS self-test and content of VDS register latched during self-test execution.	R/C
2 ÷ 1	00	**S_T_VDS_STATUS**	Status of VDS self-test 00: IDLE: Self-test not started 01: RUN: Self-test execution in progress	R/C

Bit	Default	Name	Description	Access
			10: END: Self-test completed successfully (consistent data available on dedicated registers) 11: ABORT: Self-test aborted (watchdog timeout, HWLO, S_T_STOP when not required)	
0		**Parity Bit**	ODD Parity Bit Check	

Table 43. **SR#6: Status Register 6; Address 16h (ID 14.6)**

Bit	Default	Name	Description	Access
23 ÷ 15		unused		
14	0	**UPDT_S_T_STUCK**	Updated status bit. This bit is set when value is updated and cleared when register is read.	R/C
13	0	**S_T_VDS _MAX2**	This bit is set if VDS_THR is reached during STUCK ON self-test.	R/C
12 ÷ 3	0000000000	**S_T_STUCK**	10 bit ADC conversion of the VDS, performed during STUCK ON self-test	R/C
2 ÷ 1	00	**S_T_STUCK_STATUS**	Status of STUCK _ON self-test 00: IDLE: Self-test not started 01: RUN: Self-test execution in progress 10: END: Self-test completed successfully (consistent data available on dedicated registers) 11: ABORT: Self-test aborted (watchdog timeout, HWLO, S_T_STOP when not required)	R/C
0		**Parity Bit**	ODD Parity Bit Check	

Table 44. **SR#7: Status Register 7; Address 17h (ID 14.7)**

Bit	Default	Name	Description	Access
23 ÷ 15		unused		
14	0	**S_T_HSHT**	This bit is set if HSHT_THR is reached during CURRENT SENSE self-test.	R/C
13	0	**S_T_OVC**	This bit is set if OVC_THR is reached during CURRENT SENSE self-test.	R/C
12 ÷ 3	0000000000	**S_T_CURR**	Difference between 10 bit ADC conversion of the CURRENT SENSE, performed during CURRENT SENSE self-test and content of HSHT_SAR register latched during self-test execution.	R/C
2 ÷ 1	00	**S_T_CURR_STATUS**	Status of CURRENT SENSE self-test 00: IDLE: Self-test not started 01: RUN: Self-test execution in progress 10: END: Self-test completed successfully (consistent data available on dedicated registers) 11: ABORT: Self-test aborted (watchdog timeout, HWLO, S_T_STOP when not required)	R/C
0		**Parity Bit**	ODD Parity Bit Check	

Table 45. **SR#8: Status Register 8; Address 18h (ID 14.8)**

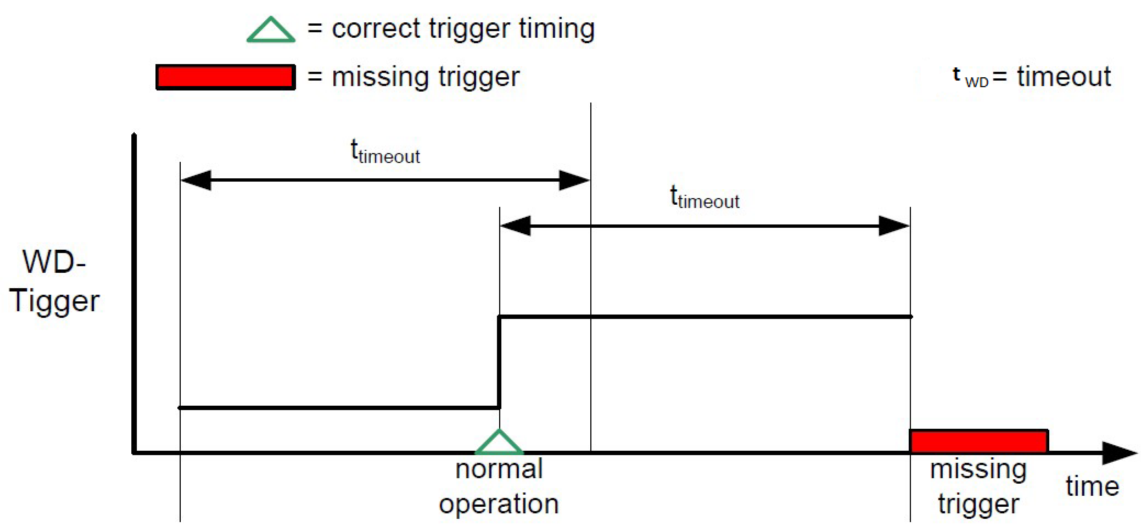
Bit	Default	Name	Description	Access
23 ÷ 12		unused		

Bit	Default	Name	Description	Access
11 ÷ 2	0000000000	**HSHT_SAR**	10 bit ADC SAR fast conversion related to Current Sense Amplifier, ranging from 0 V to 160 mV; unidirectional current through an external sense resistor. This register is not refreshed during Current Sense Self-Test execution.	R
1	00	**UPDT_HSHT**	Updated status bit. This bit is set when value is updated and cleared when register is read.	R
0		**Parity Bit**	ODD Parity Bit Check	

6.15 Timeout watchdog

In order to serve the timeout watchdog, the relevant WD_TRIG bit (Watchdog Trigger bit) must be toggled within a given timeout window.

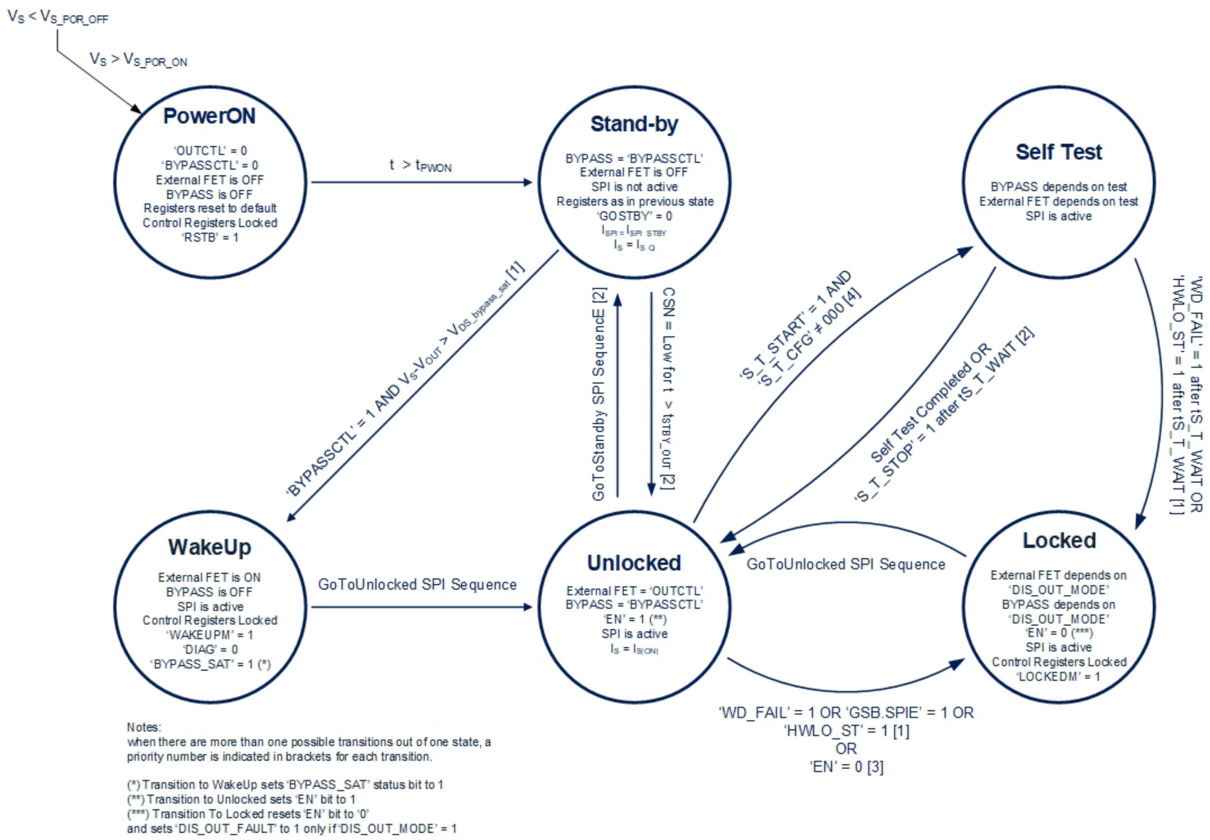
Figure 14. Timeout watchdog



7 Operating modes

7.1 State Diagram

Figure 15. State diagram



7.2 PowerON mode

The PowerON mode is the device reset state at V_S power on, due to device Start-up or Power-on Reset conditions. At PowerON, the registers are loaded with the default values and the RSTB is set to 1.

External FET, BYPASS switch and Charge Pump are in OFF state.

7.3 Stand-by mode

In Stand-by mode, the device is in quiescent power consumption and operates under the following conditions:

- High current path through External FETs is off
- Protections for the external FETs are disabled
- All diagnostics are disabled, but BYPASS switch saturation is monitored, if BYPASS switch is in ON state during Stand-by mode, in order to detect potential de-saturation
- Low-Current Bypass can be ON or OFF according to 'BYPASSCTL' bit
- Device is self-protected
- Charge Pump is OFF

The Standby mode characteristics are:

- VSPI and VS low consumption
- SPI inactive
- Registers are frozen (powered but with clock stopped) allowing to keep either previous configuration, in case of transition from Unlocked state, or default reset configuration, in case of transition from power-on state.

The Standby mode is reached in case of power-on state transition from Unlocked mode through the following SPI frame sequence:

1. Frame #1 to set UNLOCK bit in CR#3
2. Frame #2 to reset EN and set GOSTBY in CR#1

Exit from Standby mode occurs in any of the following cases:

CSN Low for a time $t > t_{STBY\_OUT}$ or BYPASS switch in ON state and de-saturation event occurrence.

7.4 WakeUp mode

The device enters in WakeUp mode from Stand-by when the $V_S – V_{OUT} > V_{DS\_BYPASS\_SAT}$

In WakeUp mode, the device fuse functionality is armed and the device operates under the following conditions:

- High current path through external FETs is ON
- Protections for the external FETs are enabled
- Low-Current Bypass is OFF
- All diagnostics are enabled
- Control registers are locked to write operations
- Device is self-protected
- SPI is active
- Charge Pump is ON

7.5 Unlocked mode

In Unlocked mode, the device fuse functionality is armed and SPI communication is allowed. The device operates under the following conditions:

- High current path through external FETs can be ON or OFF, depending on the SPI setting
- Protections for the external FETs are enabled
- All diagnostics are enabled
- Low-Current Bypass can be ON or OFF, depending on the SPI setting
- Device is self-protected
- SPI is active
- Charge Pump is ON

7.6 Locked mode

In locked mode, the device fuse functionality is armed. The device operates under the following conditions:

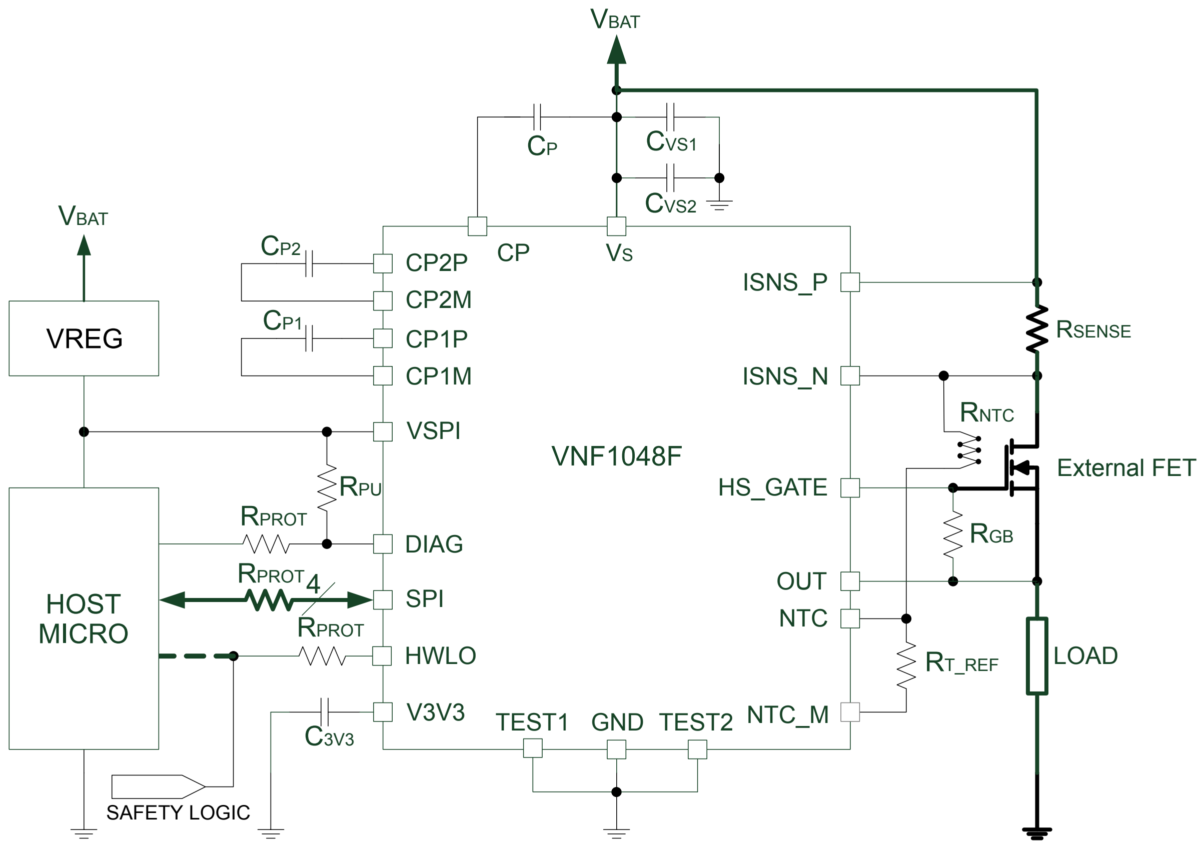
- External FETs status is defined by 'OUTCTL' and 'DIS_OUT_MODE' control bits
- Protections for the external FETs are enabled
- All diagnostics are enabled
- Low-Current Bypass is defined by 'BYPASSCTL' and 'DIS_OUT_MODE' control bits
- Device is self-protected
- SPI is active, all registers can be read, Control registers are locked to write operations
- Charge Pump is ON

7.7 Self-test mode

See Section 4 Self Test in this document.

8 Application information

Figure 16. Application diagram



Note: *Suggested components*

- C_{VS1} = 20 µF
- C_{VS2} = 100 nF
- C_{P1} = 470 nF
- C_{P2} = 470 nF
- C_P = 470 nF
- R_{PU} = 4.7 kΩ
- C_{3V3} = 1 µF
- R_{GB} = 47 kΩ
- R_{T_REF} = 10 kΩ
- R_{SENSE} = 1 mΩ

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 QFN32L 5x5 package information

Figure 17. QFN32L 5x5 Package outline

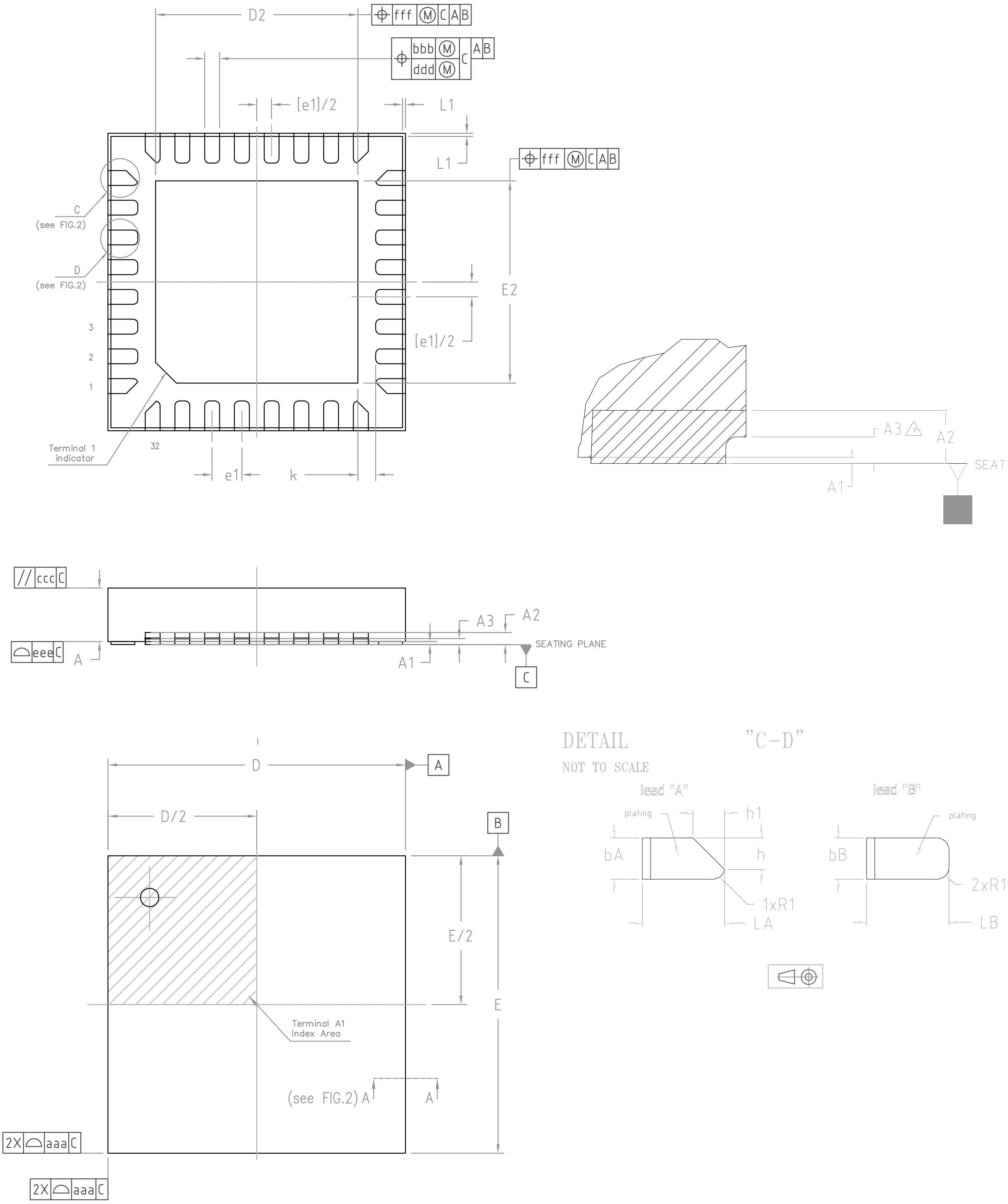


Table 46. QFN32L 5x5 mechanical data

Ref.	Dimension		
	Millimeters		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	-	0.05
A2		0.2 REF	
A3	0.1		
D	5.00 BSC		
D2	3.40	3.50	3.60
E	5.00 BSC		
E2	3.40	3.50	3.60
e1	0.5 BSC		
k	0.20	-	-
L1		.	0.05
La	0.40	0.50	0.50
bA	0.20	0.25	0.30
h		0.19 REF	
h1		0.19 REF	
LB	0.45	0.5	0.55
bB	0.20	0.25	0.30
N	32		
R1	-		0.1

Table 47. Tolerance of form and position

Symbol	Tolerance
aaa	0.15
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08
fff	0.10

Revision history

Table 48. **Document revision history**

Date	Version	Changes
16-Oct-2019	1	Initial release.
05-Aug-2020	2	Updated: -Section 9.1 QFN32L 5x5 package information -Table 4. Supply specification (also added ID 1.11) - Table 5. SPI logic inputs (CSN, SCK and SDI) specification - Table 7. HWLO logic input pin specification - Table 9. Device Thermal shutdown (added ID 2.21 and 2.22) - Table 10. ST-SPI Specification: Timings - Table 11. Charge Pump Specification - Table 12. External FET Gate Driver Specification - Table 13. Current sense amplifier with integrated ADC - Table 14. External FET VDS Protection (also removed VDS_THRS_31, added ID 7.8 and 7.9) - Table 15. Hard Short Circuit protection (added ID 8.5 and 8.6) - Table 16. Overcurrent protection (added note) - Table 17. External FET Thermal Shutdown via NTC input (added ID 10.6 and 10.7) - Table 18. Bypass switch (removed tS_T_WAIT parameter) - Figure 1. Block diagram - Figure 16. Application diagram (also added note) Added: - Section 5.7 Low Current Bypass desaturation shut-down - Section 6.15 Timeout Watchdog - Table 19. VOUT A-to-D Conversion - Figure 5. eFuse I2-t curve (generic thresholds) Minor text changes in: - Section 5.6 Current vs time latch-off - Section 6.10 Global Status Byte - Section 7.3 Stand-by mode - Table 1. Pin functions - Table 2. Absolute maximum rating - Table 36. CR#2: Control Register 2 (read/write); Address 02h (ID 13.20)
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