UCD90320 32-Rail PMBus™ Power Sequencer and System Manager

1 Features

- Sequence, Monitor, and Margin 24 Voltage Rails Plus 8 Digital Rails With a Small (12 mm × 12 mm × 0.8 mm Pitch) Footprint
- Monitor and Respond to OV, UV, OC, UC, Temperature, Time-Out, and GPI-Triggered Faults
- Flexible Sequence-On and Off Dependencies, Delay Time, Boolean Logic, and GPIO Configuration to Support Complex Sequencing Applications
- 4 Rail Profiles for Adaptive Voltage Identification (AVID) Voltage Regulator
- High-Accuracy Closed-Loop Margining
- Active Trim Function Improves Rail Output Voltage Accuracy
- Advanced Nonvolatile Event Logging To Assist System Debugging
  - Single-Event Fault Log (100 entries)
  - Peak Value Log
  - Black Box Fault Log to Save Status of All Rails and I/O Pins at the First Fault
- Easily Cascade Up to 4 Power Sequencers and Take Coordinated Fault Responses
- Programmable Watchdog Timer and System Reset
- Pin-Selected Rail State
- Flexible Pin MUX for ENx, LGPOx, GPIOx, and PWMx Pins
- PMBus™ 1.2 Compliant

2 Applications

- Industrial and ATE
- Telecom and Networking Equipment
- Servers and Storage Systems
- Systems Requiring Sequencing and Monitoring of Multiple Power Rails

3 Description

The UCD90320 device is a 32-rail PMBus™ addressable power sequencer and system manager in a compact (12 mm × 12 mm × 0.8 mm pitch) BGA package.

The device provides 24 analog monitor (AMONx) pins to monitor power-supply voltage, current, or temperature with two 12-bit ADC engines, 8 digital monitor (DMONx) pins to monitor external digital event, 32 enable (ENx) pins to control power rail ON and OFF, 24 MARx pins for closed-loop margining, 16 logic GPO (LGPOx) pins to support flexible Boolean logic and state machine functions, and 32 GPIOx pins which can be configured as GPI, GPO, system reset, cascading fault pins, or watchdog I/O.

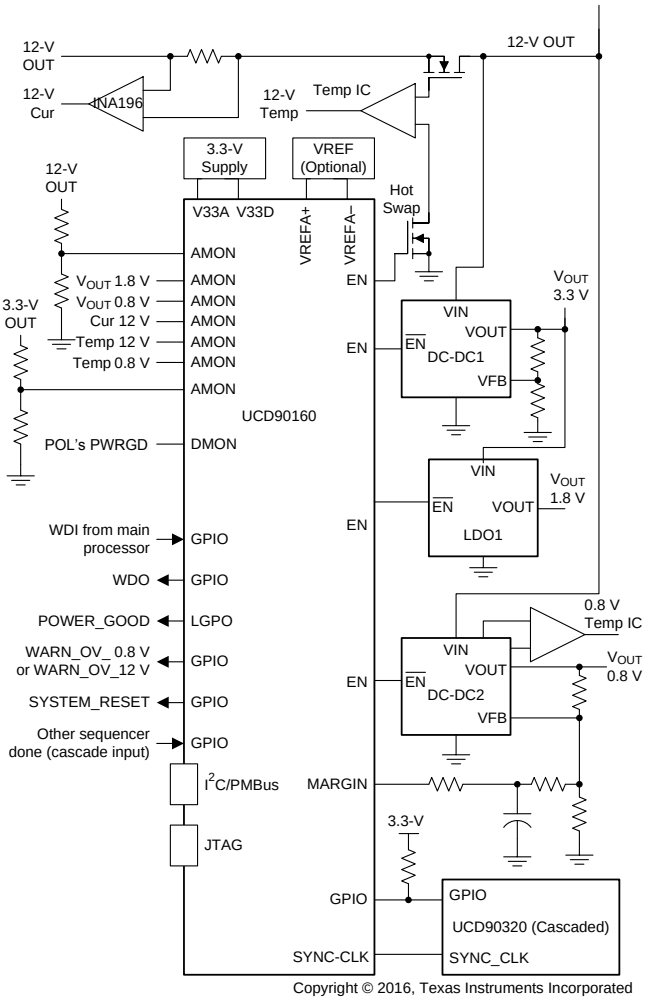
The 32 ENx pins and the 12 LGPOx pins can be configured to be active driven or open drain outputs.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCD90320	BGA (169)	12.0 mm × 12.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



PRODUCT PREVIEW

4 Description Continued

Nonvolatile event logging preserves fault events after power dropout. Black box fault log feature preserves the status for all rails and I/O pins when the first fault occurs.

The cascading feature offers convenient ways to manage up to 96 voltage rails through one SYNC_CLK pin connection. Fault Pin feature coordinates among cascaded devices to take synchronized fault responses.

The pin-selected rail states feature employs up to 3 GPIs to control up to eight user-defined power states. These states can implement system low-power modes as outlined in the (*Advanced Configuration and Power Interface ACPI*) specification.

Four profiles per rail support AVID-compatible voltage regulators.

The TI Fusion Digital Power™ designer software is an intuitive PC-based graphic user interface (GUI) that can configure, store, and monitor all system operating parameters.

5 Pin Configuration and Functions

ZWS Package
169-Pin BGA
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	DVSS	Unused-NC	AMON6	AMON8	AMON10	AMON12	AMON22	AMON24	LGPO3	JTAG_TMS	JTAG_TDO	GPIO4	MAR15	A
B	AMON15	AMON16	AMON5	AMON7	AMON9	AMON11	AMON21	AMON23	LGPO2	JTAG_TDI	GPIO1	GPIO2	MAR16	B
C	AMON13	AMON14	AVSS	LGPO8	LGPO6	LGPO7	DVSS	LGPO4	LGPO1	JTAG_TCK	GPIO3	MAR14	MAR18	C
D	VREFA-	VREFA+	V33A	MAR5	LGPO5	BPCap	V33D	MRGN3	DVSS	DMON4	MAR13	MAR17	PMBUS_DATA	D
E	AMON2	AMON1	AVSS	MAR6	DVSS	V33D	DVSS	V33D	V33D	PMBUS_CLK	PMBUS_CNTRL	MAR19	MAR20	E
F	AMON4	AMON3	DMON2	DMON1	MAR7	DVSS	DVSS	DVSS	DVSS	V33D	PMB ALERT#	EN26	EN25	F
G	AMON18	AMON17	DMON3	EN24	DVSS	DVSS	DVSS	DVSS	DVSS	$\overline{\text{RESET}}$	EN27	Unused-DVSS	Unused-NC	G
H	AMON19	AMON20	EN23	EN22	DVSS	DVSS	DVSS	DVSS	DVSS	EN28	EN31	EN30	EN29	H
J	BPCap	EN20	EN21	EN19	DVSS	BPCap	V33D	DVSS	V33D	V33D	DVSS	MAR24	MAR1	J
K	PMBUS_ADDR2	SYNC_CLK	EN17	EN18	MAR10	MAR4	EN13	EN10	EN6	EN4	Unused-DVSS	Unused-V33D	BPCap	K
L	PMBUS_ADDR1	PMBUS_ADDR0	LGPO9	LGPO13	MAR2	MAR12	EN14	EN9	EN5	EN3	DMON5	MAR22	EN32	L
M	LGPO10	LGPO11	LGPO12	LGPO15	MAR23	MAR11	EN12	EN8	EN1	Unused-DVSS	DMON8	Unused-NC	MAR21	M
N	LGPO14	LGPO16	EN16	EN15	MAR8	MAR9	EN11	EN7	EN2	Unused-NC	DMON7	DMON6	Unused-DVSS	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

PRODUCT PREVIEW

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ANALOG MONITOR PINS(1)			
AMON1	E2	I	Analog input monitor pin
AMON2	E1	I	Analog input monitor pin
AMON3	F2	I	Analog input monitor pin
AMON4	F1	I	Analog input monitor pin
AMON5	B3	I	Analog input monitor pin
AMON6	A3	I	Analog input monitor pin
AMON7	B4	I	Analog input monitor pin
AMON8	A4	I	Analog input monitor pin
AMON9	B5	I	Analog input monitor pin
AMON10	A5	I	Analog input monitor pin
AMON11	B6	I	Analog input monitor pin
AMON12	A6	I	Analog input monitor pin
AMON13	C1	I	Analog input monitor pin
AMON14	C2	I	Analog input monitor pin
AMON15	B1	I	Analog input monitor pin
AMON16	B2	I	Analog input monitor pin
AMON17	G2	I	Analog input monitor pin
AMON18	G1	I	Analog input monitor pin
AMON19	H1	I	Analog input monitor pin
AMON20	H2	I	Analog input monitor pin
AMON21	B7	I	Analog input monitor pin
AMON22	A7	I	Analog input monitor pin
AMON23	B8	I	Analog input monitor pin
AMON24	A8	I	Analog input monitor pin
ENABLE PINS			
EN1(GPIO)	M9	I/O	Digital output, rail enable signal or GPIO(2)
EN2(GPIO)	N9	I/O	Digital output, rail enable signal or GPIO
EN3(GPIO)	L10	I/O	Digital output, rail enable signal or GPIO
EN4(GPIO)	K10	I/O	Digital output, rail enable signal or GPIO
EN5(GPIO)	L9	I/O	Digital output, rail enable signal or GPIO
EN6(GPIO)	K9	I/O	Digital output, rail enable signal or GPIO
EN7(GPIO)	N8	I/O	Digital output, rail enable signal or GPIO
EN8(GPIO)	M8	I/O	Digital output, rail enable signal or GPIO
EN9(GPIO)	L8	I/O	Digital output, rail enable signal or GPIO
EN10(GPIO)	K8	I/O	Digital output, rail enable signal or GPIO
EN11(GPIO)	N7	I/O	Digital output, rail enable signal or GPIO
EN12(GPIO)	M7	I/O	Digital output, rail enable signal or GPIO
EN13(GPIO)	K7	I/O	Digital output, rail enable signal or GPIO
EN14(GPIO)	L7	I/O	Digital output, rail enable signal or GPIO
EN15(GPIO)	N4	I/O	Digital output, rail enable signal or GPIO
EN16(GPIO)	N3	I/O	Digital output, rail enable signal or GPIO
EN17(GPIO)	K3	I/O	Digital output, rail enable signal or GPIO
EN18(GPIO)	K4	I/O	Digital output, rail enable signal or GPIO
EN19(GPIO)	J4	I/O	Digital output, rail enable signal or GPIO

(1) TI recommends placing a 200-Ω resistor between analog input and monitor pins.
(2) GPIO: GPI, Command GPO, WDI, WDO, system reset ($\overline{\text{RESET}}$), FAULT pin for multiple chip cascading

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
EN20(GPIO)	J2	I/O	Digital output, rail enable signal or GPIO
EN21(GPIO)	J3	I/O	Digital output, rail enable signal or GPIO
EN22(GPIO)	H4	I/O	Digital output, rail enable signal or GPIO
EN23(GPIO)	H3	I/O	Digital output, rail enable signal or GPIO
EN24(GPIO)	G4	I/O	Digital output, rail enable signal or GPIO
EN25(GPIO)	F13	I/O	Digital output, rail enable signal or GPIO
EN26(GPIO)	F12	I/O	Digital output, rail enable signal or GPIO
EN27(GPIO)	G11	I/O	Digital output, rail enable signal or GPIO
EN28(GPIO)	H10	I/O	Digital output, rail enable signal or GPIO
EN29(GPIO)	H13	I/O	Digital output, rail enable signal or GPIO
EN30(GPIO)	H12	I/O	Digital output, rail enable signal or GPIO
EN31(GPIO)	H11	I/O	Digital output, rail enable signal or GPIO
EN32(GPIO)	L13	I/O	Digital output, rail enable signal or GPIO
CLOSED-LOOP MARGIN PINS			
MAR1(GPIO)	J13	I/O	Closed-loop margin PWM output or General GPIO
MAR2(GPIO)	L5	I/O	Closed-loop margin PWM output or General GPIO
MAR3(GPIO)	D8	I/O	Closed-loop margin PWM output or General GPIO
MAR4(GPIO)	K6	I/O	Closed-loop margin PWM output or General GPIO
MAR5(GPIO)	D4	I/O	Closed-loop margin PWM output or General GPIO
MAR6(GPIO)	E4	I/O	Closed-loop margin PWM output or General GPIO
MAR7(GPIO)	F5	I/O	Closed-loop margin PWM output or General GPIO
MAR8(GPIO)	N5	I/O	Closed-loop margin PWM output or General GPIO
MAR9(GPIO)	N6	I/O	Closed-loop margin PWM output or General GPIO
MAR10(GPIO)	K5	I/O	Closed-loop margin PWM output or General GPIO
MAR11(GPIO)	M6	I/O	Closed-loop margin PWM output or General GPIO
MAR12(GPIO)	L6	I/O	Closed-loop margin PWM output or General GPIO
MAR13(GPIO)	D11	I/O	Closed-loop margin PWM output or General GPIO
MAR14(GPIO)	C12	I/O	Closed-loop margin PWM output or General GPIO
MAR15(GPIO)	A13	I/O	Closed-loop margin PWM output or General GPIO
MAR16(GPIO)	B13	I/O	Closed-loop margin PWM output or General GPIO
MAR17(GPIO)	D12	I/O	Closed-loop margin PWM output or General GPIO
MAR18(GPIO)	C13	I/O	Closed-loop margin PWM output or General GPIO
MAR19(GPIO)	E12	I/O	Closed-loop margin PWM output or General GPIO
MAR20(GPIO)	E13	I/O	Closed-loop margin PWM output or General GPIO
MAR21(GPIO)	M13	I/O	Closed-loop margin PWM output or General GPIO
MAR22(GPIO)	L12	I/O	Closed-loop margin PWM output or General GPIO
MAR23(GPIO)	M5	I/O	Closed-loop margin PWM output or General GPIO
MAR24(GPIO)	J12	I/O	Closed-loop margin PWM output or General GPIO
GPIO AND CASCADING PINS			
DMON1(GPIO)	F4	I/O	Digital input monitor pin or GPIO
DMON2(GPIO)	F3	I/O	Digital input monitor pin or GPIO
DMON3(GPIO)	G3	I/O	Digital input monitor pin or GPIO
DMON4(GPIO)	D10	I/O	Digital input monitor pin or GPIO
DMON5(GPIO)	L11	I/O	Digital input monitor pin or GPIO
DMON6(GPIO)	N12	I/O	Digital input monitor pin or GPIO
DMON7(GPIO)	N11	I/O	Digital input monitor pin or GPIO

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DMON8(GPIO)	M11	I/O	Digital input monitor pin or GPIO
GPIO			
GPIO1	B11	I/O	GPIO
GPIO2	B12	I/O	GPIO
GPIO3	C11	I/O	GPIO
GPIO4	A12	I/O	GPIO
SYNC_CLK	K2	I/O	Synchronization clock I/O for multiple chip cascading
LOGIC GPO PINS			
LGPO1(GPIO)	C9	I/O	Logic GPO or GPIO
LGPO2(GPIO)	B9	I/O	Logic GPO or GPIO
LGPO3(GPIO)	A9	I/O	Logic GPO or GPIO
LGPO4(GPIO)	C8	I/O	Logic GPO or GPIO
LGPO5(GPIO)	D5	I/O	Logic GPO or GPIO
LGPO6(GPIO)	C5	I/O	Logic GPO or GPIO
LGPO7(GPIO)	C6	I/O	Logic GPO or GPIO
LGPO8(GPIO)	C4	I/O	Logic GPO or GPIO
LGPO9(GPIO)	L3	I/O	Logic GPO or GPIO
LGPO10(GPIO)	M1	I/O	Logic GPO or GPIO
LGPO11(GPIO)	M2	I/O	Logic GPO or GPIO
LGPO12(GPIO)	M3	I/O	Logic GPO or GPIO
LGPO13(GPIO)	L4	I/O	Logic GPO or GPIO
LGPO14(GPIO)	N1	I/O	Logic GPO or GPIO
LGPO15(GPIO)	M4	I/O	Logic GPO or GPIO
LGPO16(GPIO)	N2	I/O	Logic GPO or GPIO
PMBus COMM INTERFACE			
PMBUS_CLK	E10	I	PMBus clock (must pull up to V33D)
PMBUS_DATA	D13	I/O	PMBus data (must pull up to V33D)
$\overline{\text{PMBALERT}}$	F11	O	PMBus alert, active-low, open-drain output (must pull up to V33D)
PMBUS_CNTRL	E11	I	PMBus control pin
PMBUS_ADDR0	L2	I	PMBus digital address input. Bit 0
PMBUS_ADDR1	L1	I	PMBus digital address input. Bit 1
PMBUS_ADDR2	K1	I	PMBus digital address input. Bit 2
JTAG			
JTAG_TMS	A10	I	Test mode select with internal pull-up
JTAG_TCK	C10	I	Test clock with internal pull-up
JTAG_TDO	A11	O	Test data out with internal pull-up
JTAG_TDI	B10	I	Test data in with internal pull-up
INPUT POWER, GROUND, AND EXTERNAL REFERENCE PINS			
$\overline{\text{RESET}}$	G10	I	Active-low device reset input. Pull up to V33D.
V33A	D3	I	Analog 3.3-V supply. Decouple from V33D to minimize the electrical noise contained on V33D from affecting the analog functions.
V33D	D7, E6, E8, E9, F10, J7, J9, J10	I	Digital 3.3-V supply for I/O and some logic.
BPCap	D6, J1, J6, K13	I	Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The BPCap pins should only be connected to each other and an external capacitor as specified in *On-Chip Low Drop-Out (LDO) Regulator* section of the table.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
AVSS	C3, E3	I	Analog ground. These are separated from DVSS to minimize the electrical noise contained on V33D from affecting the analog functions.
DVSS	A1, C7, D9, E5, F9, H5, H9, J5, J8, J11, H6, H7, H8, G5, G6, G7, G8, G9, F6, F7, F8, E7	I	Ground reference for logic and I/O pins.
VREFA+	D2	I	(Optional) positive node of external reference voltage
VREFA-	D1	I	(Optional) negative node of external reference voltage
UNUSED PINS			
UNUSED-NC	A2, G13, M12, N10	–	Do not connect. Leave floating or isolated.
UNUSED-DVSS	G12, K11, M10, N13	–	Tie to DVSS.
UNUSED-V33D	K12	–	Tie to V33D.

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6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Trademarks

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All other trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCD90320ZWSR	PREVIEW	NFBGA	ZWS	169	1000	TBD	Call TI	Call TI	-40 to 85		
UCD90320ZWST	PREVIEW	NFBGA	ZWS	169	250	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

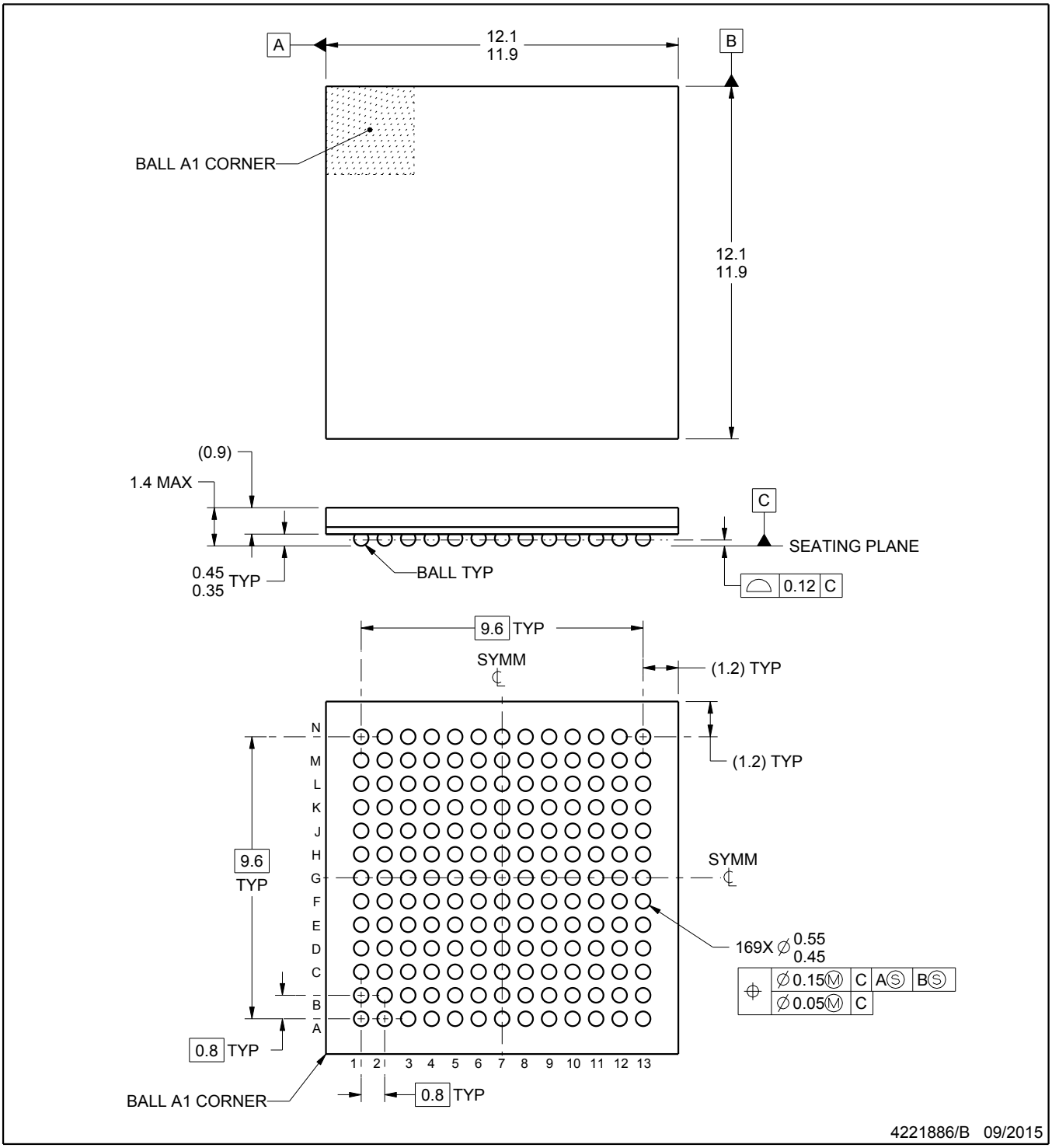
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

ZWS0169A

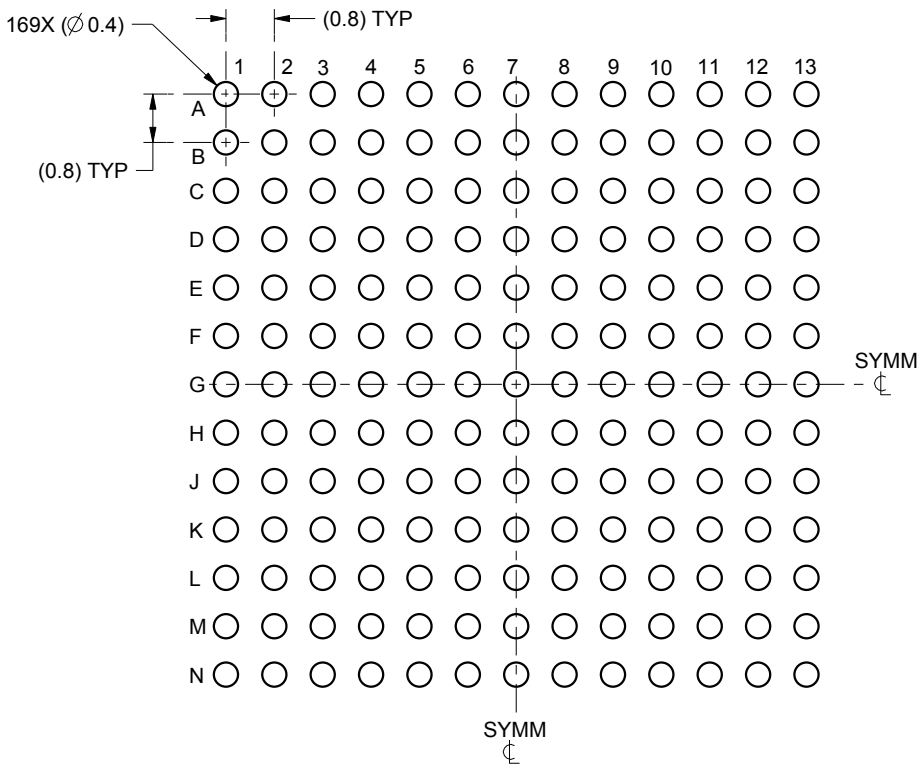
PBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY

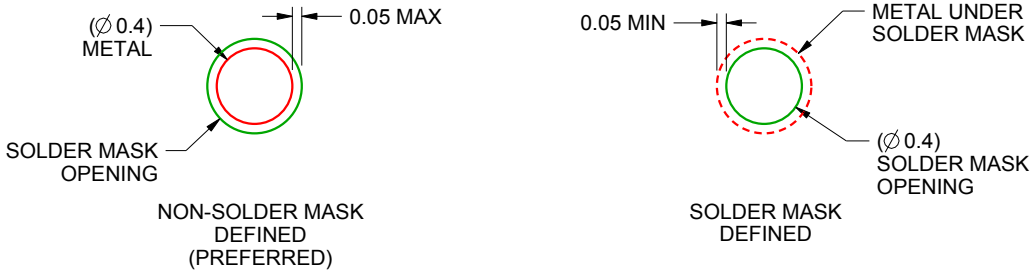


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:8X

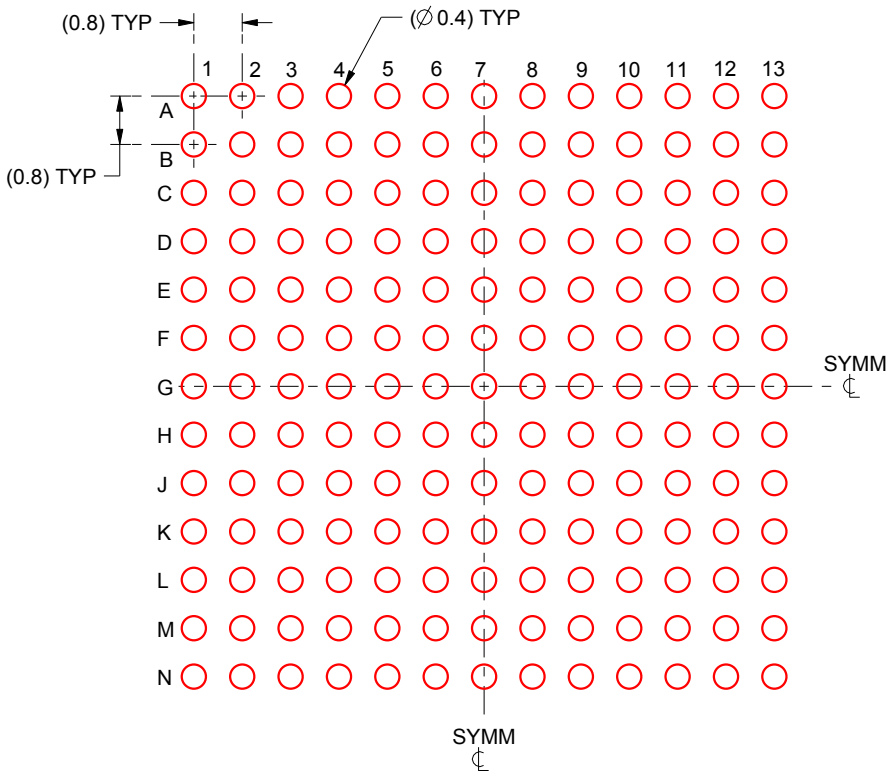


SOLDER MASK DETAILS
NOT TO SCALE

4221886/B 09/2015

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SSZA002 (www.ti.com/lit/ssza002).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4221886/B 09/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
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Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
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