UC1842/3/4/5;UC2842/3/4/5;UC3842/3/4/5

Current Mode PWM Controller

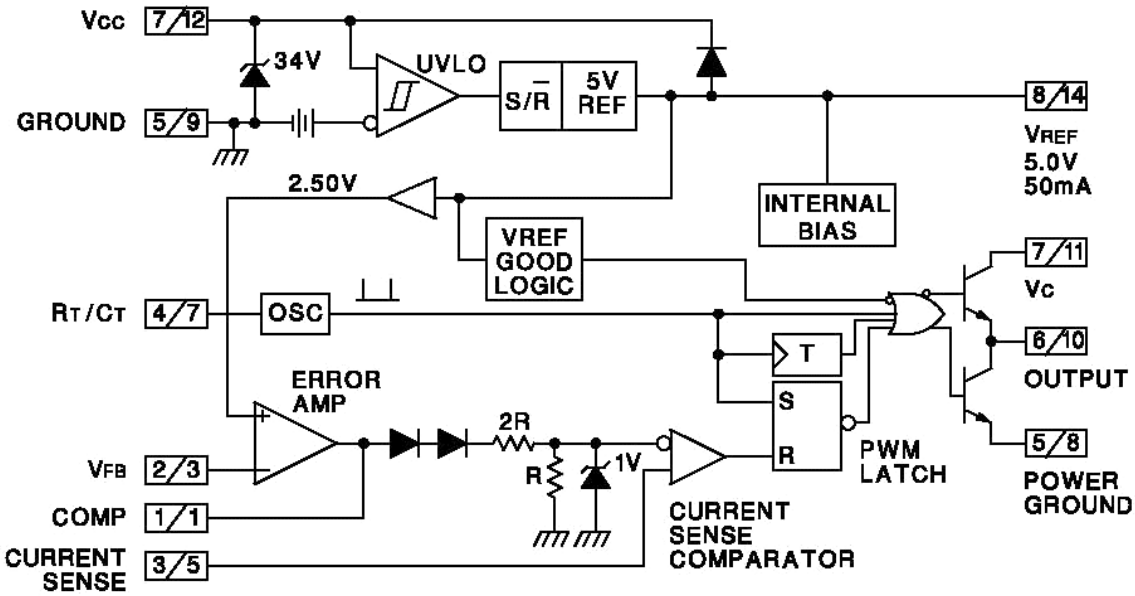
FEATURES

- Optimized For Off-line And DC TO DC Converters
- Low Start Up Current (<1mA)
- Automatic Feed Forward Compensation
- Pulse-by-pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500-khz Operation
- Low Ro Error Amp

DESCRIPTION

The UC1842/3/4/5 family of control devices provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less that 1mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-channel MOSFETs, is low in the off state. Differences between members of this family are the under-Voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of $16V_{ON}$ and $10V_{OFF}$, ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.4V and 7.6V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

BLOCK DIAGRAM



Note 1: A/B A = DIL-8 Pin Number. B = SO-14 and CFP-14 Pin Number.
Note 2: Toggle flip flop used only in 1844 and 1845.

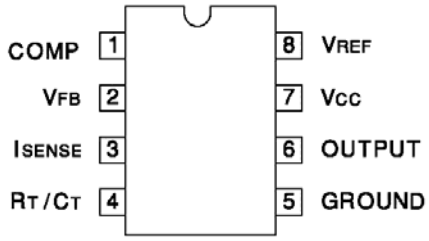
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Low Impedance Source)……..30V
Supply Voltage (Icc<30mA)……Self Limiting
Output Current…….. …±1A
Output Energy (Capacitive Load)……5μJ
Analog Inputs (Pins 2,3)…….-0.3V to +6.3V
Error Amp Output Sink Current……10mA
Power Dissipation at TA≤25°C (DIL -8)……..1W
Power Dissipation at TA≤25°C(SOIC-14)…….725mW
Power Dissipation at TA≤25°C(SOIC-8)……650mW
Storage Temperature Range…….....-65°C to +150°C
Junction Temperature Range……-55°C to +150°C
Lead Temperature (soldering, 10 seconds)……300°C
Note 1: All voltage are with respect to Pin 5.
All currents are positive into the specified terminal.
Consult Packaging Section of Databook for thermal
Limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-8,SOIC-8 (TOP VIEW)

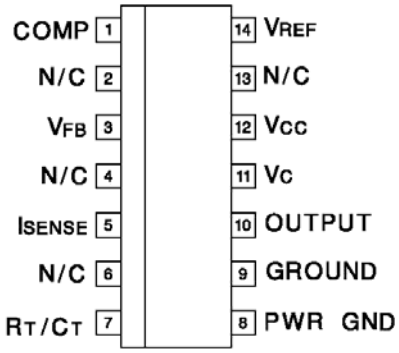
N or J Package, D8 Package



SOIC-14, CFP-14.

D or W Package

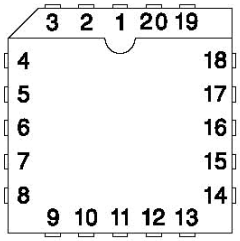
(TOP VIEW)



NC-No internal connection

PLCC-20 (TOP VIEW)

Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
COMP	2
N/C	3
N/C	4
VFB	5
N/C	6
ISENSE	7
N/C	8
N/C	9
RT/CT	10
N/C	11
PWR GND	12
GROUND	13
N/C	14
OUTPUT	15
N/C	16
VC	17
VCC	18
N/C	19
VREF	20

DISSIPATION RATING TABLE

Package	T_A≤25°C Power Rating	Derating Factor Above T_A≤25°C	T_A≤70°C Power Rating	T_A≤85°C Power Rating	T_A≤125°C Power Rating
W	700mW	5.5mW/°C	452mW	370mW	150mW

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for -55°C≤TA≤125°C for the UC184X; -40°C≤TA≤85°C for the UC284X; 0°C≤TA≤70°C for the 384X; Vcc=15V (1); R_T=10KΩ; C_T=3.3nF, T_A=T_J.

PARAMETER	TEST CONDITIONS	UC1842/3/4/5 UC2842/3/4/5			UC3842/3/4/5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J=25°C, I_O=1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12≤V_{IN}≤25V		6	20		6	20	mV
Load Regulation	1≤I_0≤20mA		6	25		6	25	mV
Temp. Stability	See (2)(3)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp. (2)	4.9		5.1	4.82		5.18	V
Output Noise Voltage	10 Hz ≤f≤10kHz, T_J=25°C (2)		50			50		μV
Long Term Stability	TA=125°C,1000Hrs. (2)		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Initial Accuracy	TJ=25°C (4)	47	52	57	47	52	57	kHz
Voltage Stability	12≤Vcc≤25V		0.2	1		0.2	1	%
Temp. Stability	T_{MIN} ≤ T_A≤ T_{MAX} (2)		5			5		%
Amplitude	V_{PIN} 4 peak to peak (2)		1.7			1.7		V
Error Amp Section								
Input Voltage	$V_{PIN\ 1}$ =2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	μA
A_{VOL}	2≤V_O≤4V	65	90		65	90		dB
Unity Gain Bandwidth	T_J=25°C (5)	0.7	1		0.7	1		MHz
PSRR	12≤V_{CC}≤25V	60	70		60	70		dB
Output Sink Current	$V_{PIN\ 2}$ =2.7V, $V_{PIN\ 1}$ =1.1V	2	6		2	6		mA
Output Source Current	$V_{PIN\ 2}$ =2.3V, $V_{PIN\ 1}$ =5V	-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} High	$V_{PIN\ 2}$ =2.3V, R_L=15k to ground	5	6		5	6		V
V_{OUT} Low	$V_{PIN\ 2}$ =2.7V, R_L=15k to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	See(6)(7)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	V_{PIN1}=5V (6)	0.9	1	1.1	0.9	1	1.1	V
PSRR	12≤V_{CC}≤25V (5)(6)		70			70		dB
Input Bias Current			-2	-10		-2	-10	μA
Delay to output	V_{PIN3}=0V to 2V (5)		150	300		150	300	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for -55°C≤TA≤125°C for the UC184X; UC184X; -40°C≤TA≤85°C for the UC284X; 0°C≤TA≤70°C for the 384X; Vcc=15V (Note5); R_T=10K; C_T=3.3nF, T_A=T_J.

PARAMETER	TEST CONDITIONS	UC1842/3/4/5 UC2842/3/4/5			UC3842/3/4/5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Section								
Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
	I_{SINK}=200mA		1.5	2.2		1.5	2.2	V
Output High Level	I_{SOURCE}=20mA	13	13.5		13	13.5		V
	I_{SOURCE}=200mA	12	13.5		12	13.5		V
Rise Time	T_J=25°C, C_L=1nF(5)		50	150		50	150	ns
Fall Time	T_J=25°C, C_L=1nF(5)		50	150		50	150	ns
Under-voltage Lockout Section								
Start Threshold	X842/4	15	16	17	14.5	16	17.5	V
	X843/5	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operating Voltage After Turn On	X842/4	9	10	11	8.5	10	11.5	V
	X843/5	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section								
Maximum Duty Cycle	X842/3	95	97	100	95	97	100	%
	X844/5	46	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current			0.5	1		0.5	1	mA
Operating Supply Current	$V_{PIN\ 2}$=$V_{PIN\ 3}$=0V		11	17		11	17	mA
Vcc Zener Voltage	Icc=25mA	30	34		30	34		V

(1) Adjust Vcc above the start threshold before setting at 15V.

(2) These parameters, although guaranteed, are not 100% tested in production.

(3): Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$Temp\ Stability = \frac{V_{REF}\ (max) - VREF\ (min)}{TJ\ (max) - TJ\ (min)}$$

V_{REF}(max) and V_{REF} (min) are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.

(4): Output frequency equals oscillator frequency for the UC1842 and UC1843.
Output frequency is one half oscillator frequency for the UC1844 and UC1845.

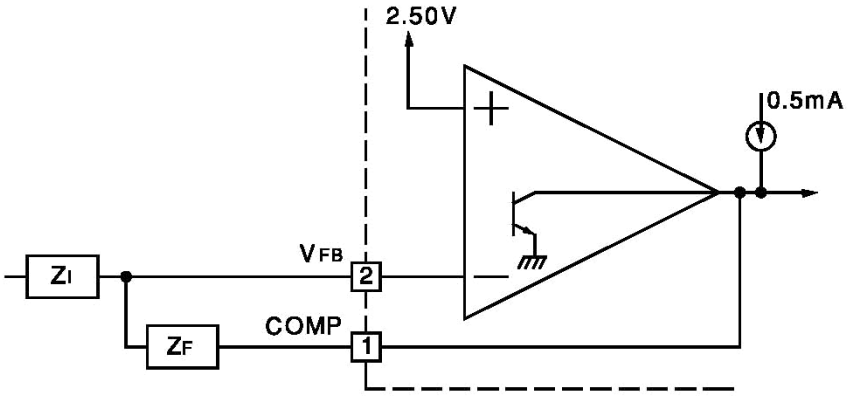
(5)These parameters, although specified, are not 100% tested in production.

(6) Parameter measured at trip point of latch with V_{PIN2}=0.

(7)Gain defined as

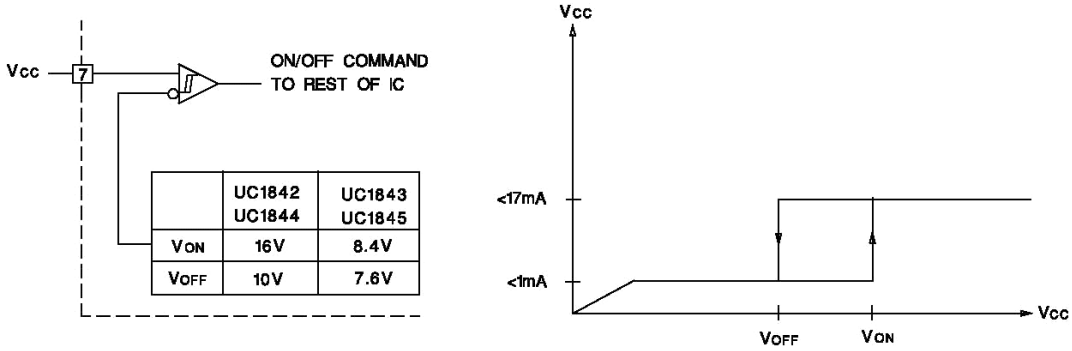
$$A = \frac{\Delta\ VPIN\ 1}{\Delta\ VPIN\ 3},\ 0 \le VPIN\ 3 \le 0.8V$$

ERROR AMP CONFIGURATION



Error Amp can Source or Sink up to 0.5mA

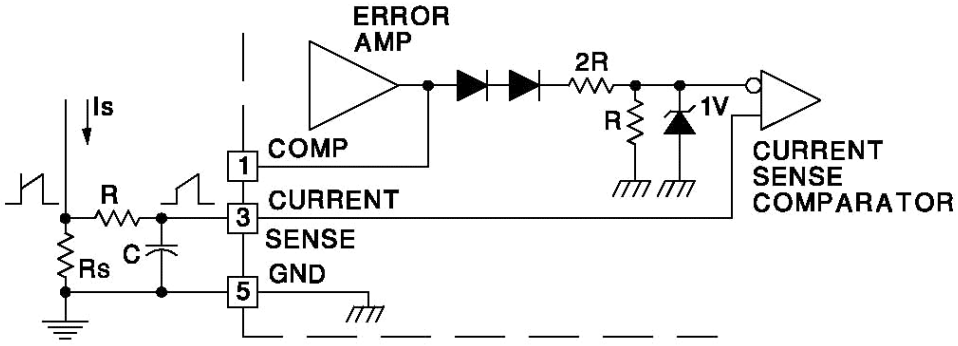
UNDER-VOLTAGE LOCKOUT



During under-voltage lock-out, the output driver is activating the power switch with extraneous leakage biased to sink minor amounts of current. Pin 6 should currents.

Be shunted to ground with a bleeder resistor to prevent.

CURRENT SENSE CIRCUIT

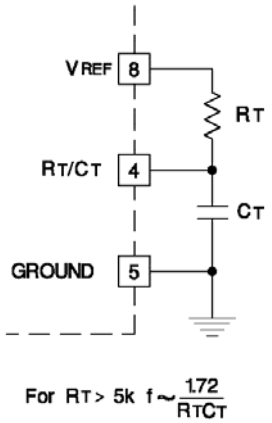


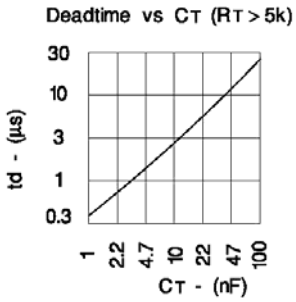
Peak Current (Is) is Determined By The Formula

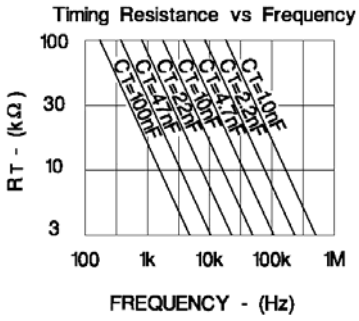
$$I_{SMAX} \approx \frac{1.0V}{RS}$$

A small RC filter may be required to suppress switch transients.

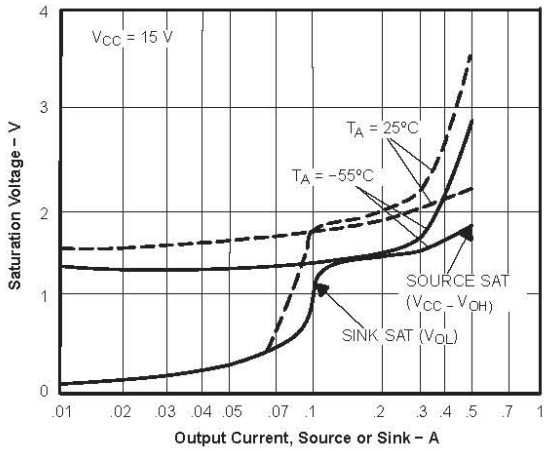
OSCILLATOR SECTION



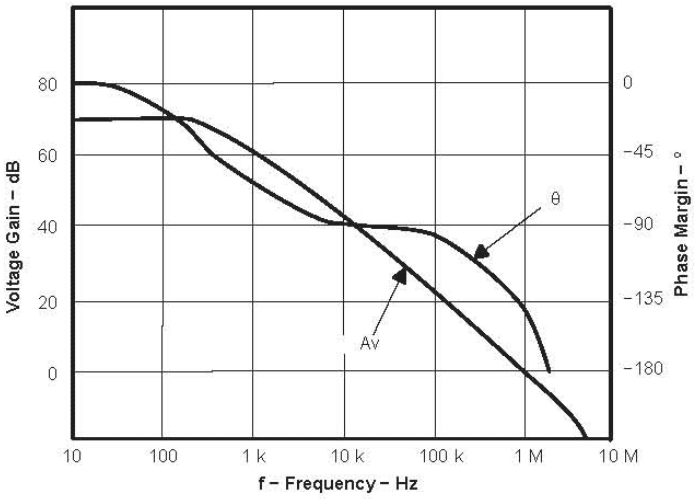




OUTPUT SATURATION CHARACTERISTICS

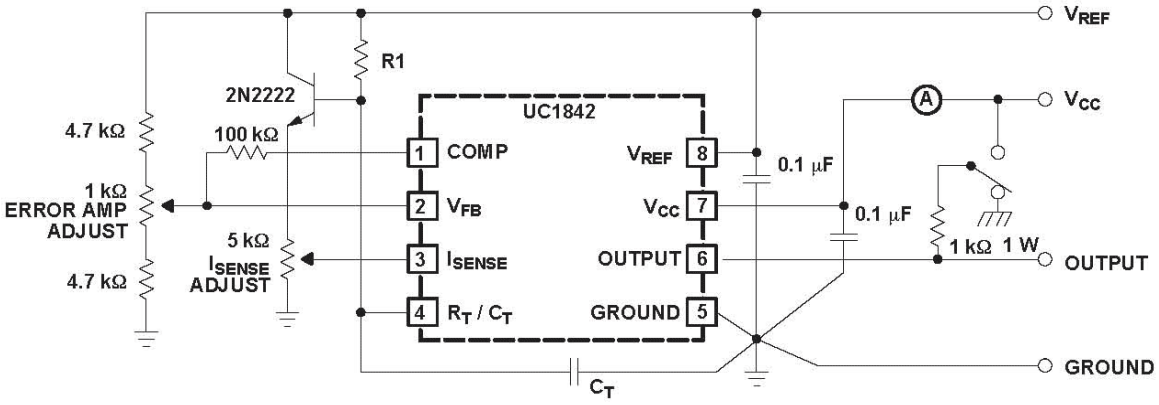


ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE



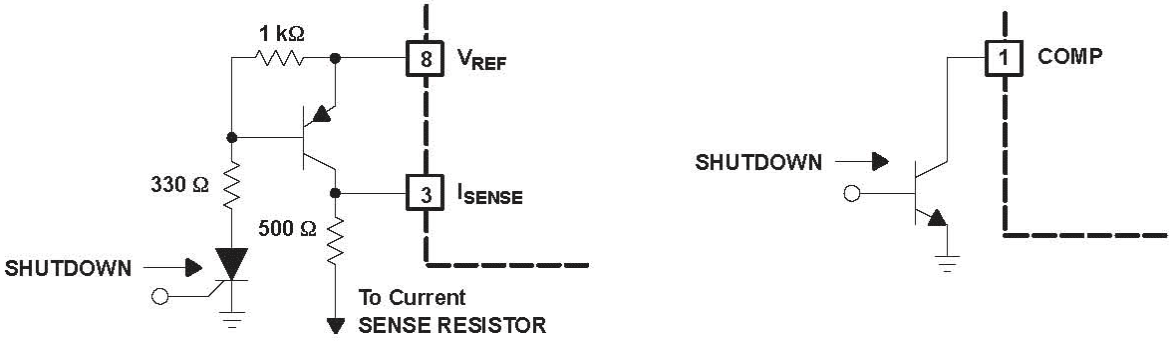
OPEN-LOOP LABORATORY FIXTURE

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5K potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

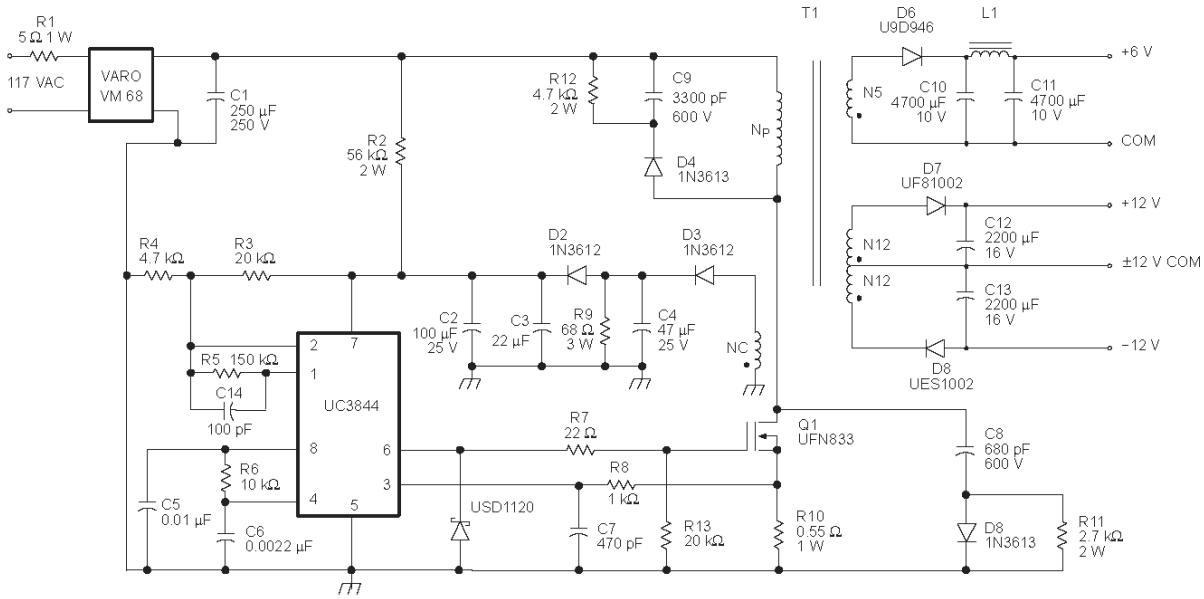


SHUTDOWN TECHNIQUES

Shutdown of the UC1842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that output will remain low until the next clock cycle after the shutdown condition at pin 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling Vcc below the lower UVLO threshold. At this pint the reference turns off, allowing the SCR to reset.



OFFLINE FLYBACK REGULATOR

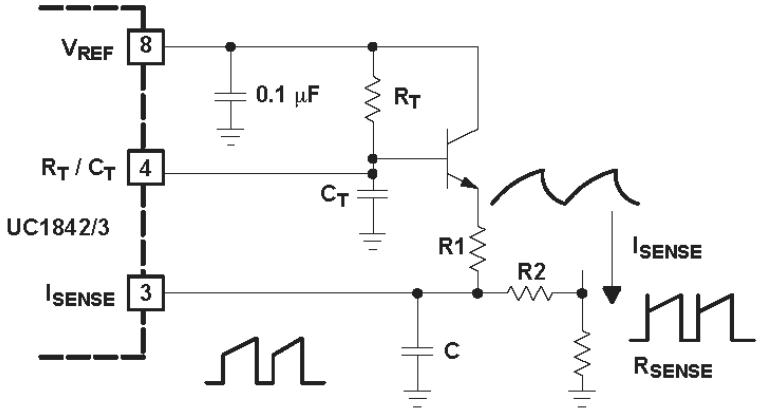


Power Supply Specifications

1. Input Voltages
a. 5VAC to 130VA (50Hz/60Hz)
2.Line Isolation:3750V
3. Switching Frequency:40kHz
4. Efficiency at Full Load 70%
5.Output Voltage:
a. +5V, ±5%; 1A to 4A load
b. +12V, ±3%; 0.1A to 0.3A load
Ripple voltage:100mV P-P Max
C.-12V, ±3%; 0.1A to 0.3A load
Ripple voltage:100mV P-P Max

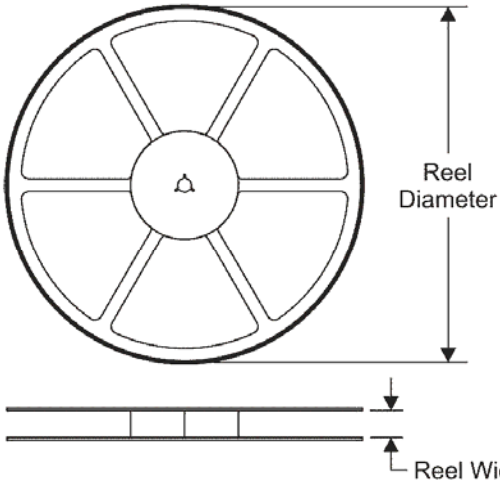
SLOPE COMPENSATION

A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.

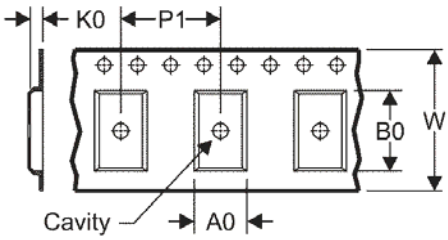


TAPE AND REEL INFORMATION

REEL DIMENSIONS

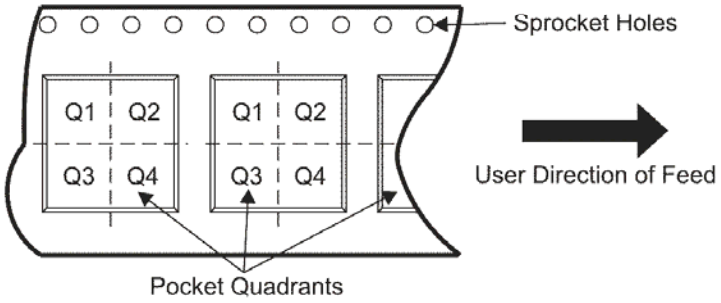


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

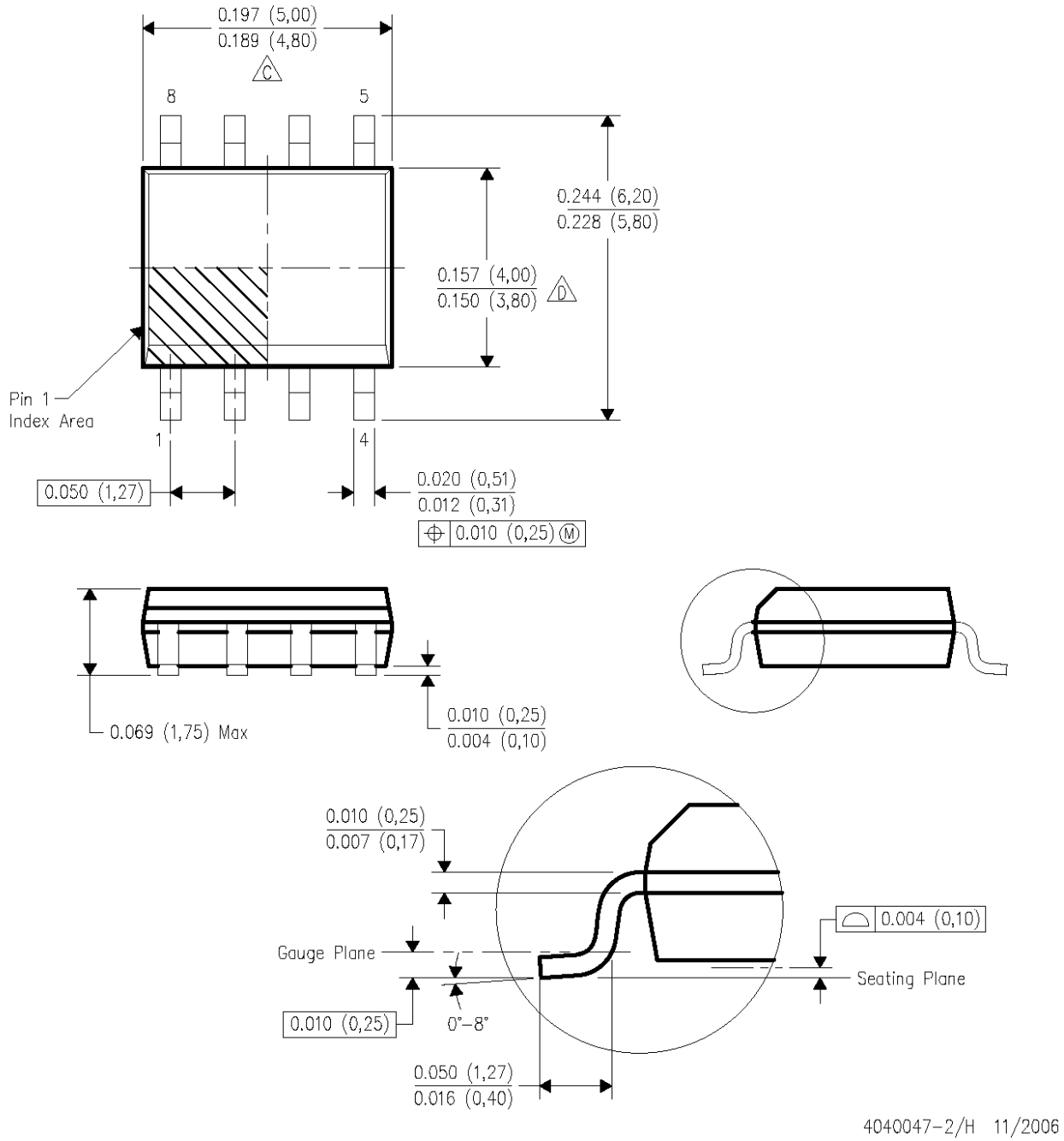
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0(mm)	B0(mm)	K0(mm)	P1(mm)	W(mm)	Pin1 Quadrant
UC2842D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2842DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2843D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2843DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2844D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2844DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2845D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2845DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3842D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3842DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3843D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3843DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3844D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3844DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3845D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3845DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

D(R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

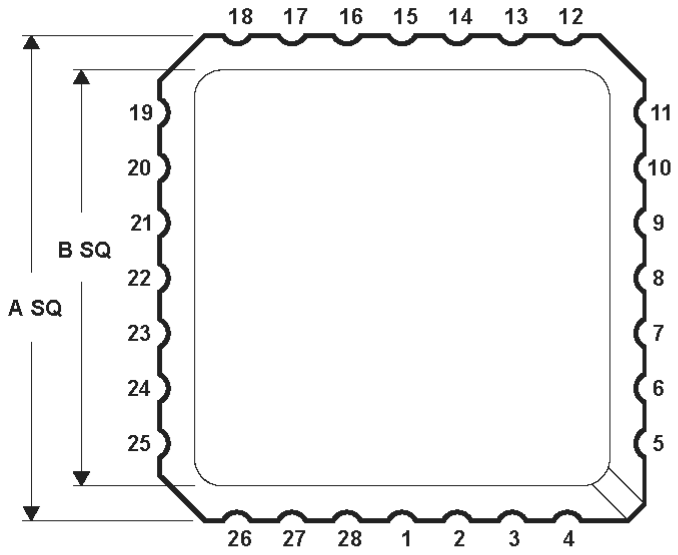
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall note not exceed .006 (0.15) per end.

D Body width does not include interlead flash. Interlead flash shall not exceed .017 (0.43) per side.

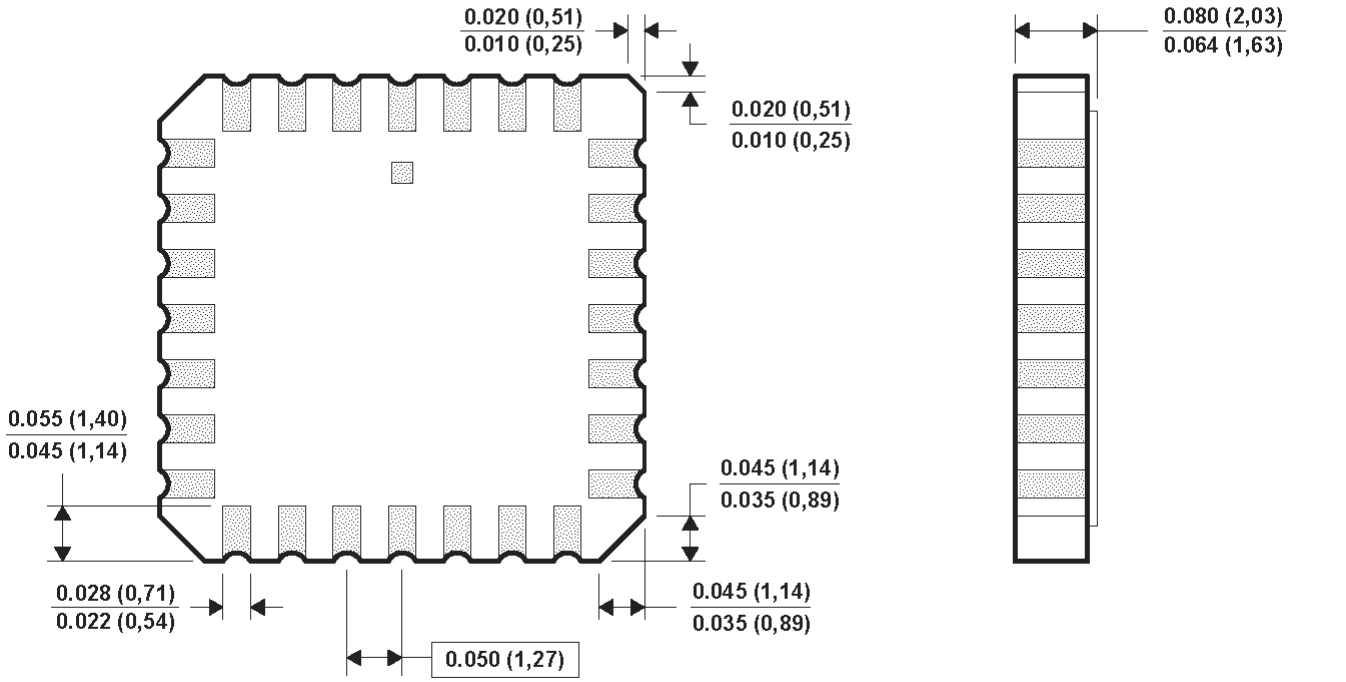
E. Reference JEDEC MS-012 variation AA.

FK(S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).

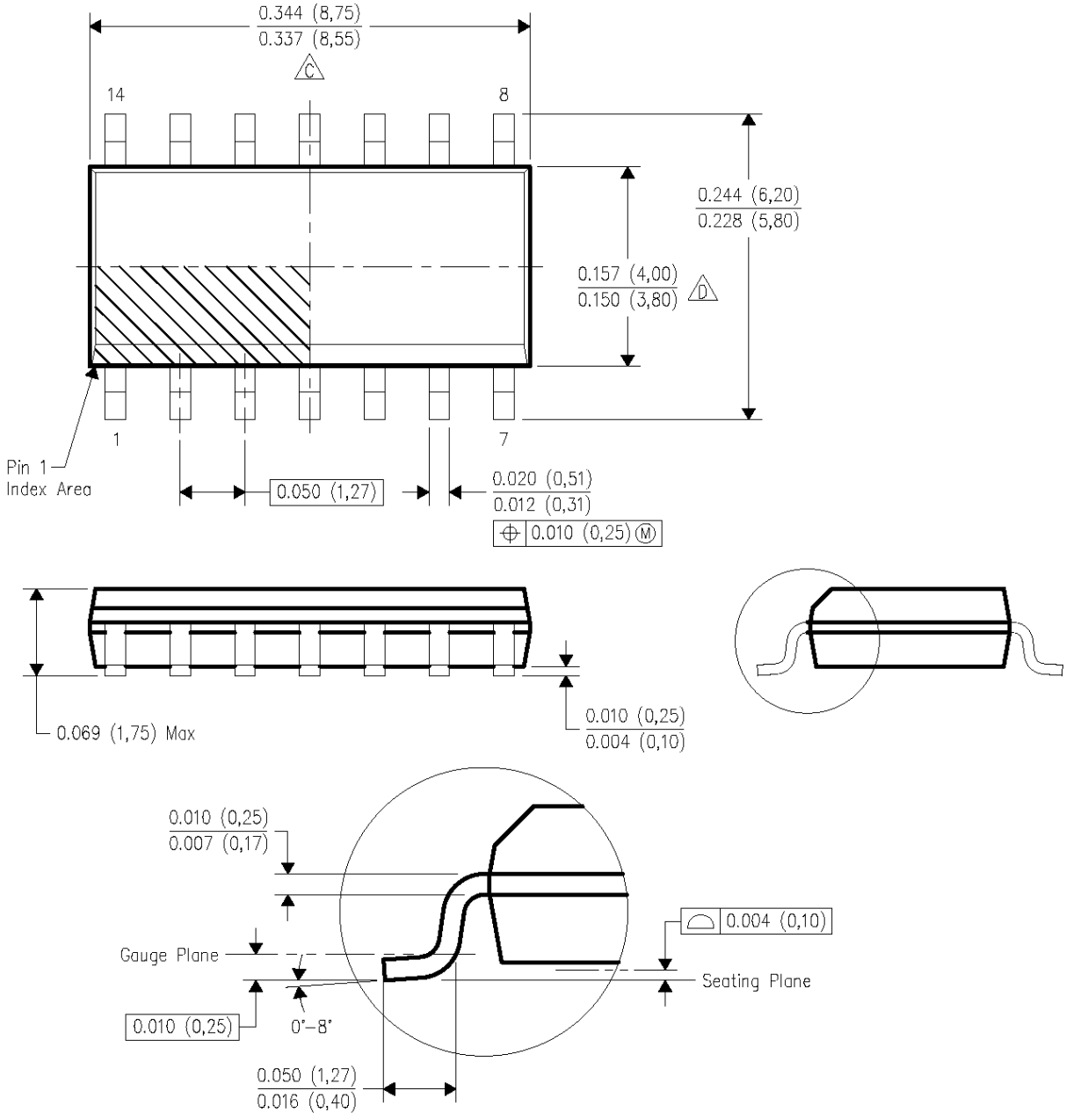
B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

D. The terminals are gold plated.

E. Falls within JEDEC MS-004

D(R-PDSO-G14) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

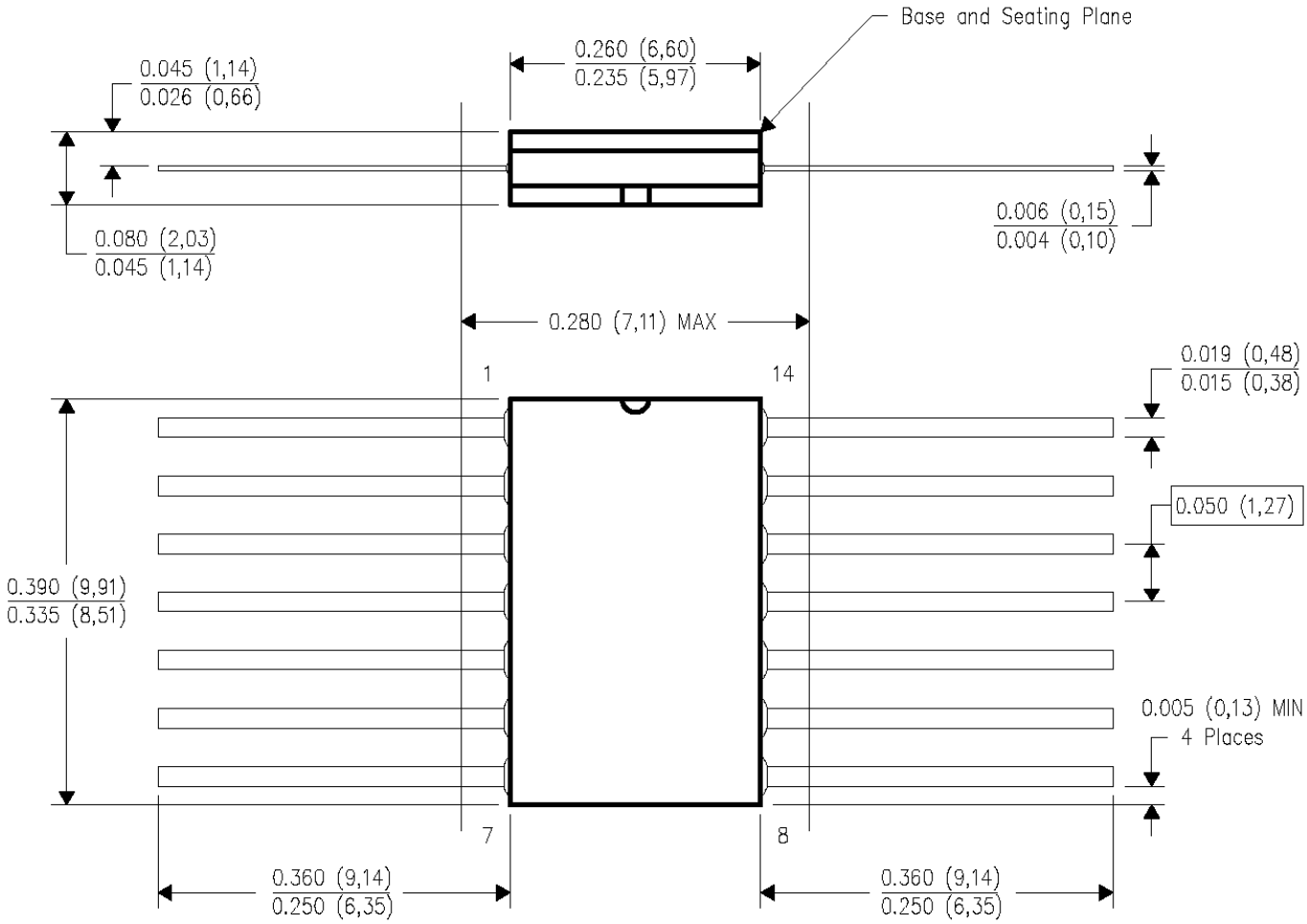
B. This drawing is subject to change without notices.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

D Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AB.

W (R-GDFP-F14) **CERAMIC DUAL FLATPACK**



4040180-2/D 07/03

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

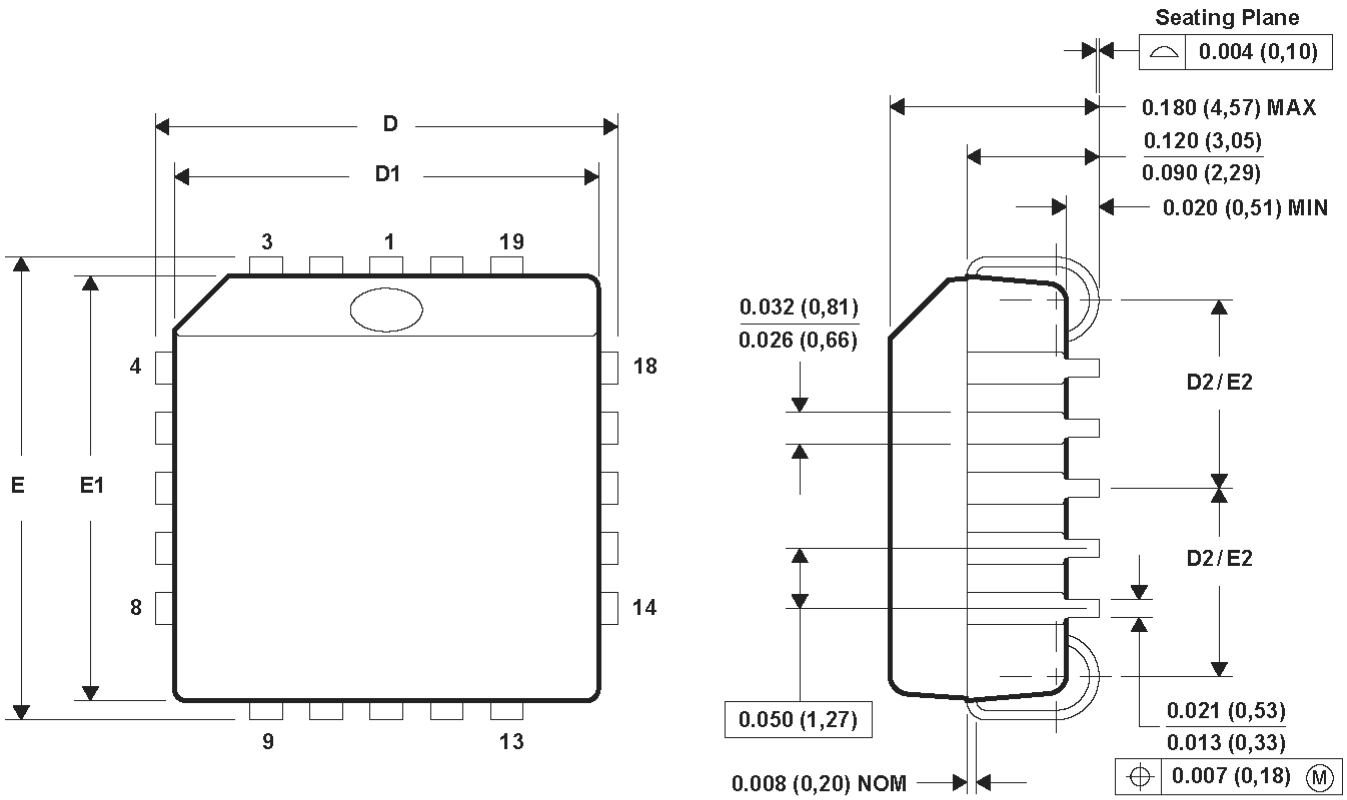
C. This package can be hermetically sealed with a ceramic lid using glass frit.

D. Index point is provided on cap for terminal identification only.

E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FN(S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



NO. OF PINS **	D / E		D1 / E1		D2 / E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

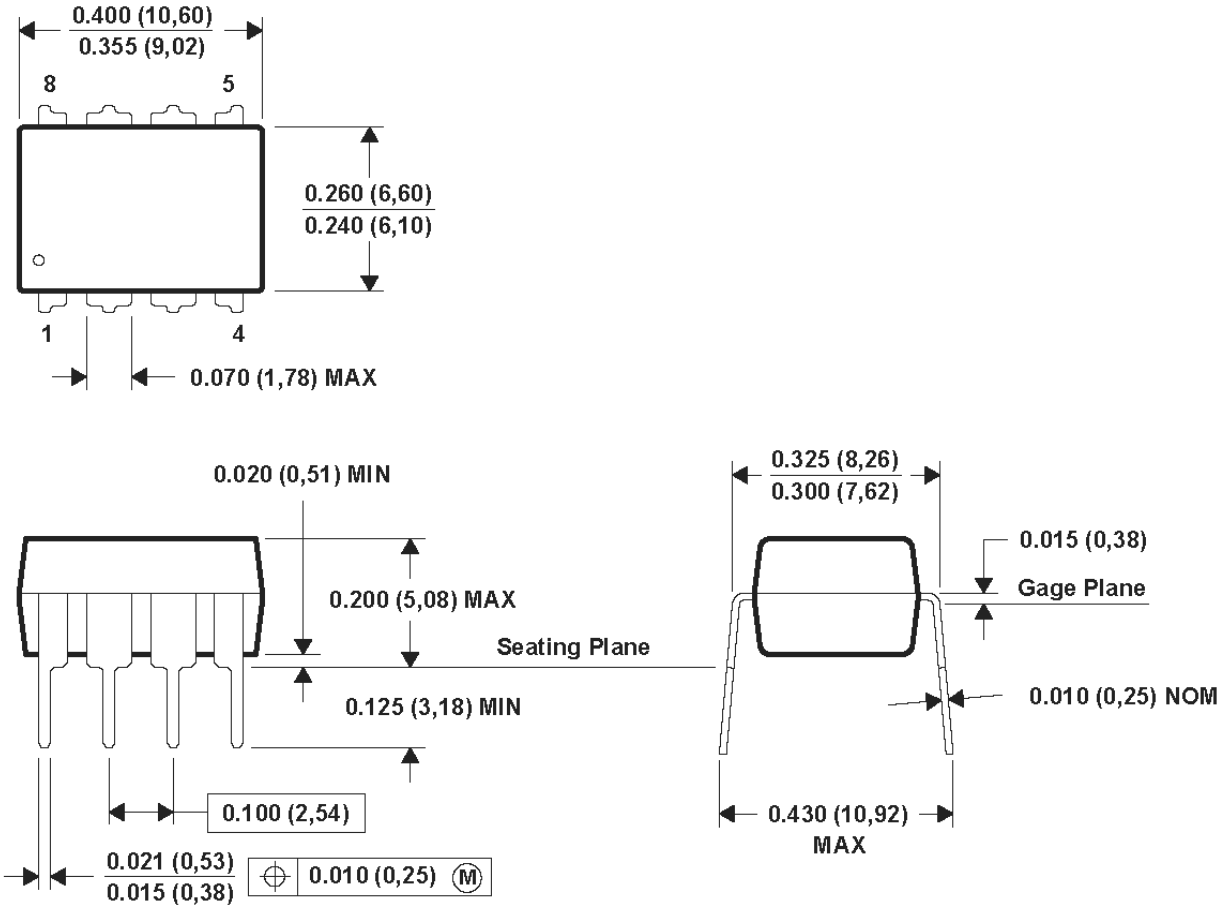
4040005 / B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-018

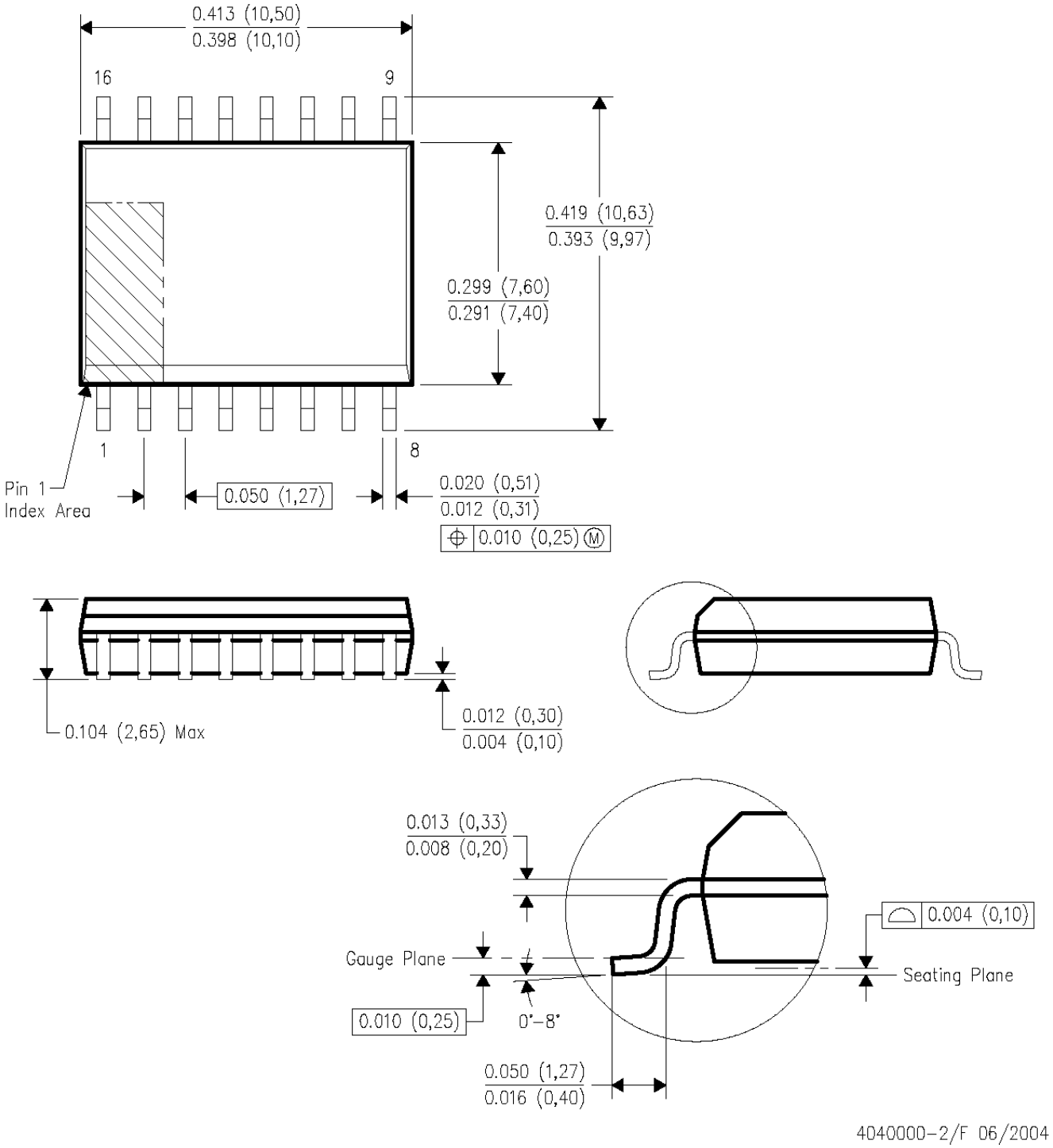
P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



4040082/D 05/98

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

DW (R-PDSO-G16) **PLASTIC SMALL-OUTLINE PACKAGE**



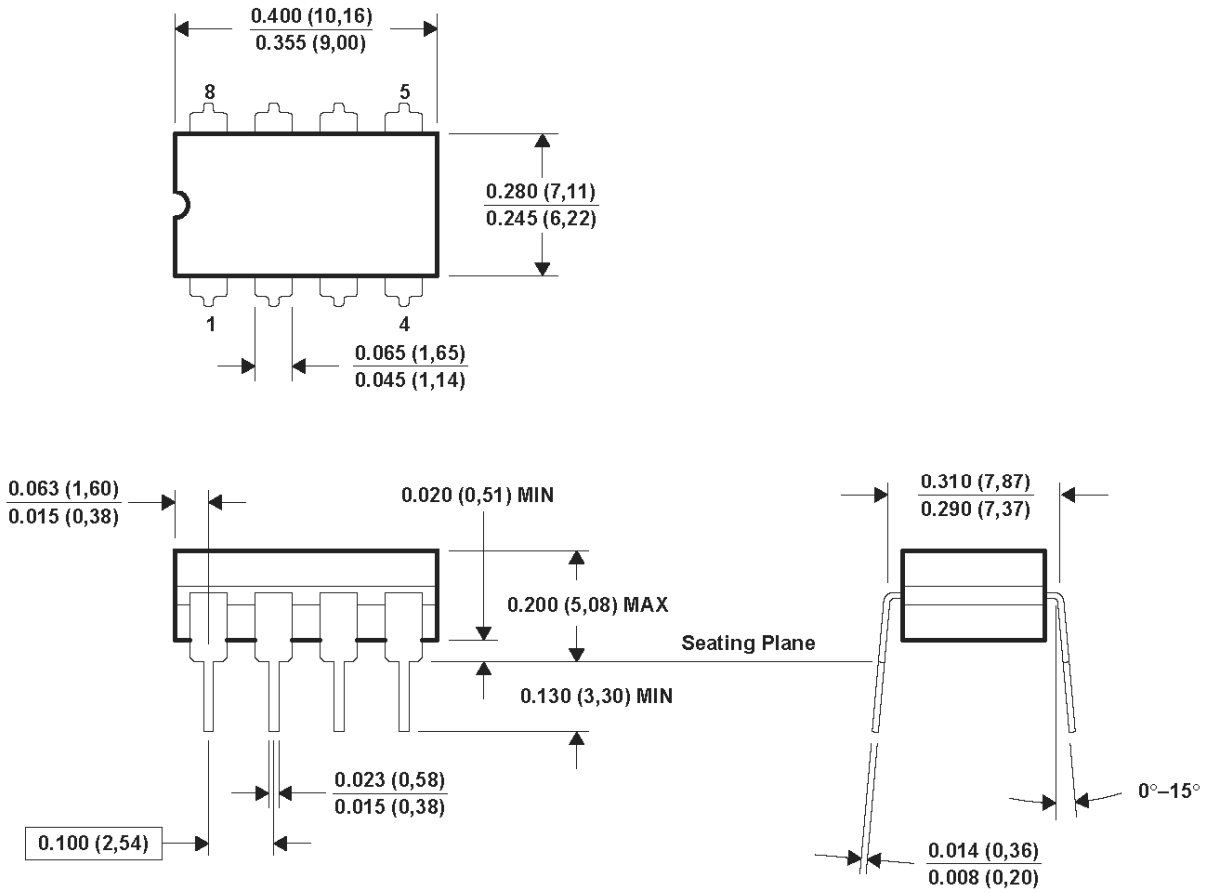
NOTES: A. All linear dimensions are in inches (millimeters)

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).

D. Falls within JEDEC MS-013 variation AA.

JG (R-GDIP –T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a ceramic lid using glass frit.

D. Index point is provided on cap for terminal identification.

E. Falls within MIL STD 1835 GDIP1-T8.