TEXAS INSTRUMENTS

TVP5150

Low-Power VIdeo Decoder With Scaling

Data Manual

September 2002 *DAV Digital Video/Speaker*

SLES043

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1 Introduction

The TVP5150 is a highly integrated low-power video processor, with full video decoding functionality and scaling and audio support. The optimized architecture of the TVP5150 allows for low power consumption.

The high quality single-chip digital video decoder on the TVP5150 converts base-band analog NTSC, PAL, and SECAM video into digital YUV 4:2:2 component video. Y/C composite and S-video inputs are also supported. Digital inputs are supported for YUV 4:2:2, which can then be digitally processed for output on the output YUV databus. The TVP5150 includes one 9-bit A/D converters with 2x sampling. Sampling is square-pixel or ITU-R BT.601 (27 MHz) and is line-locked for correct pixel alignment. The output formats can be 8-bit 4:2:2 or 8-bit ITU-R BT.656 with embedded syncs.

The TVP5150 utilizes Texas Instruments' patented technology for locking to weak, noisy, or unstable signals, and a chroma frequency control output is generated for synchronizing downstream video encoders.

Complementary three-line or four-line adaptive comb filtering is available for both the luma and chroma data paths to reduce both cross-luma and cross-chroma artifacts; a chroma trap filter is also available.

The TVP5150 allows scaling of the input image to various other formats. The scaling can be done in the horizontal and vertical directions. A windowing (cropping) function allows zooming into any desired area in the captured image.

Video characteristics including hue, contrast, and saturation may be programmed using the I^2C high-speed bus interface. The TVP5150 generates synchronization, blanking, field, lock, and clock signals in addition to digital video outputs. The TVP5150 includes methods for advanced vertical blanking interval (VBI) data retrieval. The VBI data processor slices, parses, and performs error checking on Teletext, closed caption, and other data in several formats.

The device has an internal ROM to execute programs.

The TVP5150 detects copy protected input signals according to Macrovision standard.

The main blocks of the TVP5150 include:

- A/D converter with analog processor
- Y/C separation
- Chrominance processor
- Luminance processor
- Scaling/windowing functionality
- Video clock/timing processor and power-down control
- Output formatter
- Host port interface
- VBI data processor
- Macrovision™ detection

1.1 Features

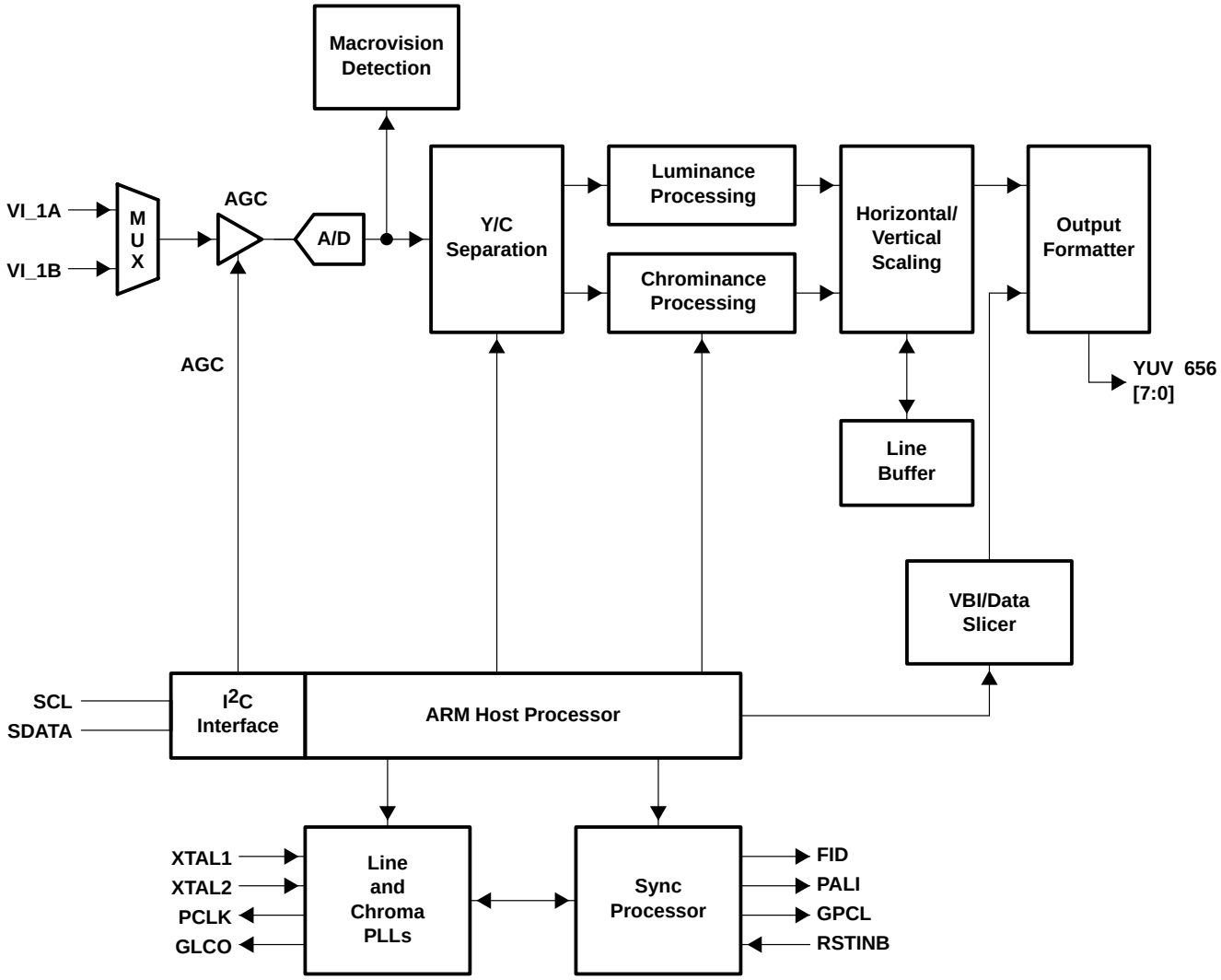
- Accepts NTSC(M), PAL (B,D,G,H,I,M,N) , PAL60 Video Data
- Supports ITU-R BT.601 Standard, Square Pixel Sampling
- High Speed 9-bit A/D Converter
- Two Composite Inputs, One S-Video Input
- Fully Differential CMOS Analog Preprocessing Channels With Clamping and AGC for Best S/N Performance
- Low Power Consumption: < 150 mW

- 32-Pin TQFP Package
- Power-Down Mode
- Brightness, Contrast, Saturation, and Hue Control Through the Host Port
- Complementary 4-Line (3-H delay) Adaptive Comb Filters for Both Cross-Luminance and Cross-Chrominance Noise Reduction
- Patented Architecture for Locking to Weak, Noisy, or Unstable Signals
- Single 14.31818-MHz Crystal for All Standards
- Internal PLL for Line-Locked Clock and Sampling
- Programmable Output Data Rates:
  - 12.2727-MHz Square-Pixel (NTSC)
  - 14.75-MHz Square-Pixel (PAL)
  - 13.5 MHz ITU-R BT.601 (NTSC and PAL)
- Subcarrier Genlock Output for Synchronizing Color Subcarrier of External Encoder. Standard Programmable Video Output Formats:
  - ITU-R BT.656, 8 bit 4:2:2 With Embedded Syncs
  - 8-Bit 4:2:2 With Discrete Syncs
- Macrovision™ Copy Protection Detection
- Advanced Programmable Video Output Formats:
  - 2x Oversampled Raw VBI Data During Active Video
  - Sliced VBI data During Horizontal Blanking or Active Video
  - Teletext (NABTS, WST) Closed-Caption Decode with FIFO
  - Wide Screen Signaling , Video Program System, CGMS, and Vertical Interval Time Code
  - Custom Configuration Mode Allows the User to Program the Slice Engine for Unique VBI Data Signals
- Internal Programmable Host Processor. Programmed Using I^2C:
  - Internal ROM (Program), With Partial RAM Support
  - 3.3-V Tolerant Digital I/O Port
- Scaling Function:
  - Provides Horizontal Scaling in the Range: Down to 1/32x. Pixel Based Adjustment of Number of Pixels Per Line
  - Provides Vertical Scaling in the Range: Down to 1/32x. Pixel Based Adjustment for Number of Lines/Field or Frame
  - Scaler has an Integrated Anti-Aliasing Low-Pass Filter
  - Brightness, Saturation, and Contrast Control for the Scaled Output Data
- Temporal Decimation to Allow Lower Frame Rates, Which Facilitates Compression Algorithms on Low BW Devices
- Power-On Reset

1.2 Applications

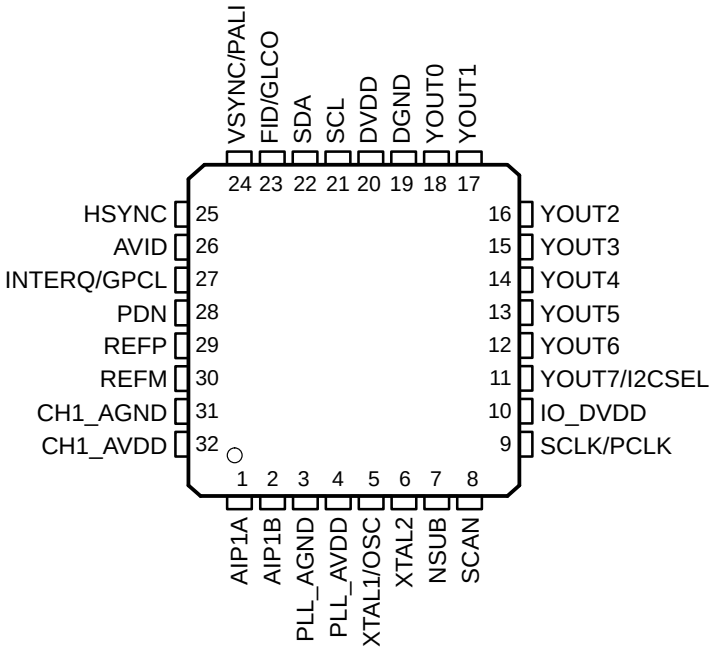
- PDA
- Cell Phones
- Multimedia Applications
- MPEG4 Players
- Internet Appliances/Web Pads
- Portable Games

1.3 Functional Block Diagram



1.4 Terminal Assignments

TQFP PACKAGE
(TOP VIEW)



1.5 Terminal Functions

Table 1–1. Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ANALOG SECTION			
AIP1A	1	I	Analog input
AIP1B	2	I	Analog input
CH1_AGND	31	I	Analog grounds
CH1_AVDD	32	I	Analog supply. Connect to 1.8-V analog supply
NSUB	7		Substrate
PLL_AGND	3	I	PLL ground. Connect to analog ground
PLL_AVDD	4	I	PLL supply. Connect to 1.8-V analog supply
REFM	30	I	A/D reference ground. Connect to analog ground
REFP	29	I	A/D reference supply. Connect to 1.8-V analog
DIGITAL SECTION			
AVID	26	I/O	Active video indicator. This signal is high during the horizontal active time of the video output on the Y and UV terminals. AVID continues to toggle during vertical blanking intervals. This terminal may be placed in a high-impedance state. During reset, AVID is an input, used to program the behavior of Y[7:0], HSYN, VSYN, AVID, and FID immediately after the completion of reset. If AVID is pulled up during reset, Y[7:0], HSYN, VSYN, AVID, and FID are actively driving after reset . If AVID is pulled down during reset, Y[7:0], HSYN, VSYN, AVID, and FID remain in high-impedance state after reset.
DGND	19	I	Digital grounds
DVDD	20	I	Digital supply. Connect to 1.8 V
FID/GLCO	23	I/O	FID: Odd/even field indicator or vertical lock indicator. For odd/even indicator, a logic 1 indicates the odd field. GLCO: This serial output carries color PLL information. A slave device can decode the information to allow chroma frequency control to the TVP5150. Data is transmitted at the SCLK rate.
HSYNC	25	O	Horizontal synchronization

Table 1–1. Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DIGITAL SECTION (CONTINUED)			
INTREQ/GPCL	27	I/O	INTREQ: interrupt request. GPCL: General-purpose control logic. This terminal has three functions: 1. General-purpose output. In this mode the state of GPCL is directly programmed via the host port. 2. Vertical blank output. In this mode the GPCL terminal is used to indicate the vertical blanking interval of the output video. The beginning and end times of this signal are programmable via the host port control. 3. Sync lock control input. In this mode when GPCL is high, the output clock frequencies and the sync timing are forced to nominal values.
IO_DVDD	10	I	IO digital supply. Either 1.8 V or 3.3 V depending on requirements.
PDN	28	I	Power-down pin. Puts device in standby mode. Preserves the value of the registers, but PLL, analog channel, and all the digital circuitry are shut down.
SCAN	8		Scan test input
SCL	21	I/O	I^2C serial clock
SCLK/PCLK	9	O	System clock outputs with twice the frequency of the pixel clock (PCLK). Pixel clock for the data
SDA	22	I/O	I^2C serial data
VSYNC/PALI	24	O	VSYNC: vertical synchronization PALI: PAL line indicator or horizontal lock indicator. For PAL line indicator, a logic 1 indicates a noninverted line, and a logic 0 indicates an inverted line.
XTAL1/OSC XTAL2	5 6	I	External clock reference. The user may connect XTAL1 to a TTL-compatible oscillator or to one terminal of a crystal oscillator. The user may connect XTAL2 to the other terminal of the crystal oscillator or not connect XTAL2 at all. One single 14.31818-MHz crystal or oscillator is needed for square pixel sampling and ITU-R BT.601 sampling.
YOUT(6:0)*	12–18	O	Output decoded ITU-R BT656 output/YUV 422 output.
YOUT(7)/I2CSEL	11	I/O	I2CSEL: Determines address for I^2C (sampled at startup) Logic 1: Address = xxH, Logic 0: Address: yyH YOUT7: MSB of Output decoded ITU-R BT656 output/YUV 422 output.

2 Detailed Description

2.1 Input Multiplexers and Buffers

The TVP5150 has an analog input channel that can accept two CVBS video inputs, ac-coupled through 0.1-µF capacitors. The two analog input ports can be connected as follows.

- Two selectable composite video inputs
- One S-video input

The internal video multiplexers can be configured via the host port. The internal nodes are grounded for zero channel crosstalk. The input buffers are continuous time amplifiers, which allow an input range of up to 0.75 V. This allows the decoder to support input ranges of 0.5 V to 1.5 V with an input attenuation of 1/2. The selection is done by register settings.

2.2 Clamp

An internal clamping circuit restores the ac-coupled video signal to a fixed dc level. The clamping circuit provides line-by-line restoration of the video sync level to a fixed dc reference voltage. Two modes of clamping are provided, coarse and fine.

- In coarse mode, the most negative portion of the input signal (typically the sync tip) is clamped to a fixed dc level and remains on. Typically, this level is the sync tip. This mode is used while the timing processor is searching for the horizontal sync.
- Fine clamp mode is enabled after the horizontal lock is achieved. This is enabled to prevent spurious level shifting caused by noise more negative than the sync tip on the input signal. If fine clamp mode is selected, clamping is only enabled during the sync period.

- When in bottom level mode fine, the sync tip of the input signal will be set to output code 0 of the ADC.
- When in mid level mode, fine clamp restores the dc level of the signal to the mid range of the ADC.

S-video requires fine clamp mode on the chroma channel for proper operation. The clamp can be completely disabled using software registers.

2.3 Programmable Gain Amplifier (PGA) Automatic Gain Control (AGC)

The programmable gain amplifier (PGA) and the automatic gain control (AGC) work together to make sure that the input signal is amplified enough to ensure the proper input range for the ADC. The gain is controlled by a 4-bit gain code, separately controllable for the two channels. The PGA transfer function is different depending on the CLAMP mode. In the bottom-level mode, it is (VINP–VINM) x gain –0.5, so that the output range is ±0.5. In the mid-level mode, it is (VINP–VINM) x gain. This ensures that the signal is in the center of the ADC range regardless of the CLAMP mode.

Input video signal amplitude may vary significantly from the nominal level of 1 VPP (140 IRE). An AGC adjusts the signal amplitude to utilize the maximum range of the A/D converter without clipping. The AGC adjusts gain to achieve desired sync amplitude. Some nonstandard video signals contain peak white levels that saturate the A/D converter. In these cases, AGC automatically cuts back gain to avoid clipping. The AGC has a range of 0 dB to 12 dB as shown in Figure 2–1.

2.4 Analog-to-Digital Converters (ADC)

The ADC has 9 bits of resolution and runs at a maximum speed of 30 MHz. The clock input for the ADC comes from the PLL. The data is aligned to the pixel clock supplied from the DLL and matched in delay.

2.5 Composite Processing Block Diagram

The composite processing block process NTSC/PAL/SECAM signals into the YCbCr color space. The following block diagram explains the basic architecture of this processing block.

The following figure illustrates the luminance/chrominance (Y/C) separation process in the TVP5150. The 9-bit composite video is multiplied by subcarrier signals in the quadrature modulator to generate color difference signals U and V. U and V are then low-pass filtered to achieve the desired bandwidth by the color low-pass filters described in the later section.

An adaptive 4-line comb filter separates UV from Y based on the unique property of color phase shift from line to line. Chroma is remodulated through another quadrature modulator and subtracted from line-delayed composite video to generate luma. This form of Y/C separation is completely complementary, thus loses no information. However, in some applications it is desirable to limit the U/V bandwidth to avoid crosstalk. In that case, notch filters can be turned on. To accommodate some viewing preferences, a peaking filter is also available in the luma path. The Y/C separation is bypassed for S-video input. Contrast, brightness, hue, and saturation are programmable via the host port.

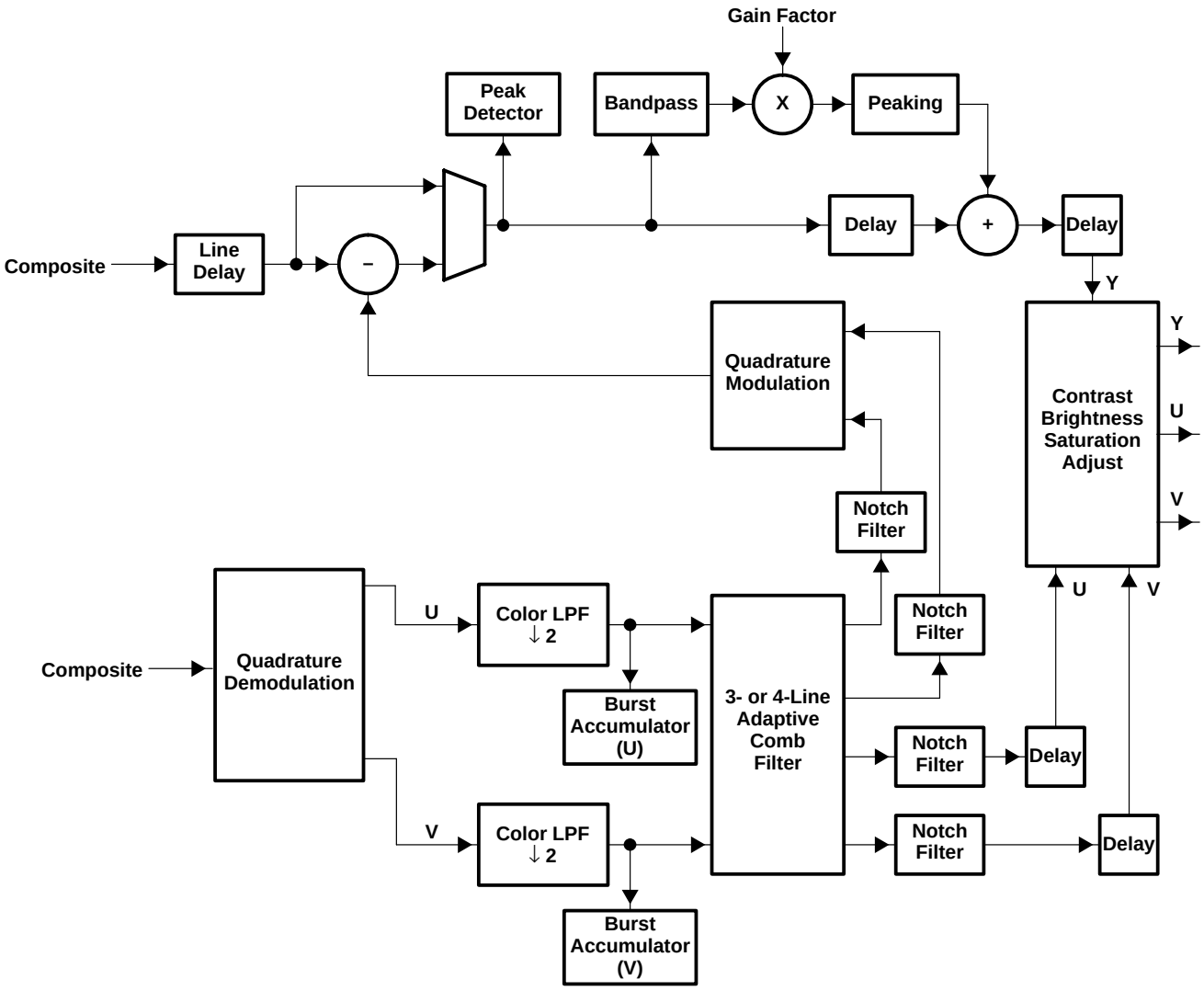


Figure 2–1. Composite Processing Block Diagram

2.5.1 Adaptive Comb Filtering

Y/C separation may be done using adaptive 4-line or 3-line (3-H or 2-H delay), fixed 3-line, fixed 2-line comb filters, or a chroma trap filter as shown. Adaptive comb filtering is available for both luminance and chrominance. The adaptive comb filter algorithm computes the vertical and horizontal contours of color based on a block of 3x3 pixels.

If there is a sharp color transition, comb filtering is applied to the two lines that have less color changes. If there is no color transition, 3-line comb filtering is used with a choice of filter coefficients [1/4, 1/2, 1/4] or [1/2, 0, 1/2] programmable via the host port. Characteristics of 2-line and 3-line comb filters are also shown. The filter frequency plots show that both 2-line and 3-line (with filter coefficients [1/4, 1/2, 1/4]) comb filters have zeros at 1/2 of the horizontal line frequency to separate the interleaved Y/C spectrum in NTSC. The 3-line comb filter has less cross-luma and cross-chroma noise due to slightly sharper filter cutoff. The 3-line comb filter with filter coefficients [1/2, 0, 1/2] has two zeros at 1/4 and 3/4 of the horizontal line frequency. This should be used for PAL only because of its 90 degree U/V phase shifting from line to line. The comb filter can be selectively bypassed in the luma or chroma path. If the comb filter is bypassed in the luma path, then chroma notch filters are used (next section). TI's patented adaptive comb filter algorithm reduces artifacts, such as hanging dots at the color boundary, and detects and properly handles false colors in high-frequency luminance images such as a multiburst pattern or circle pattern. Adaptive comb filtering is the recommended mode of operation.

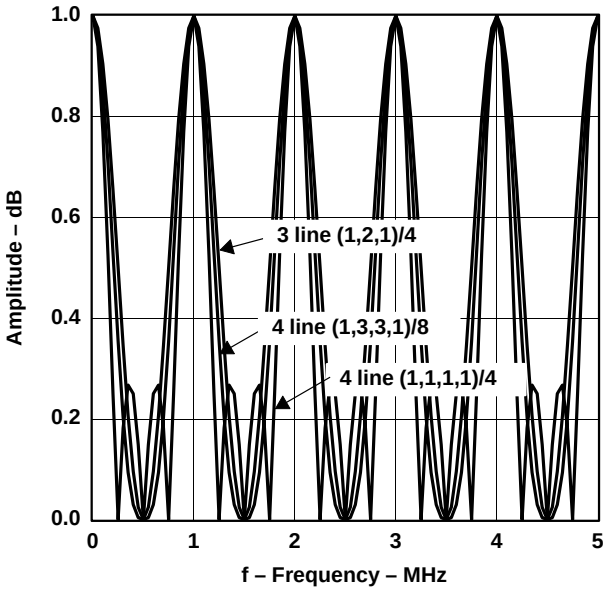


Figure 2–2. Comb Filters Frequency Response

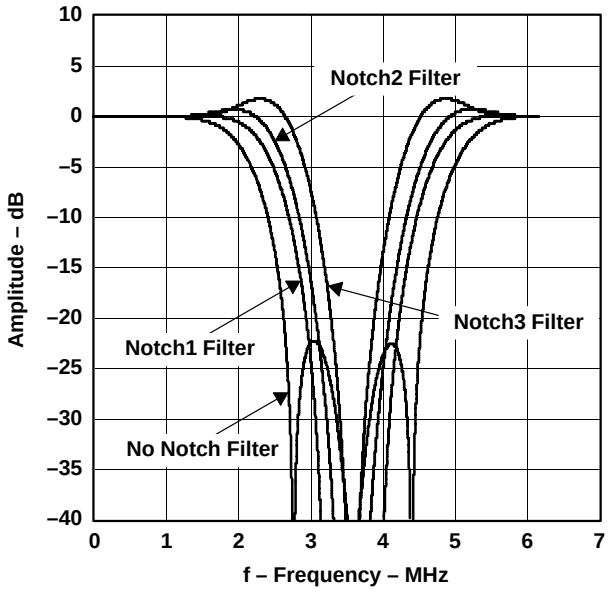


Figure 2–3. Chroma Trap Filter Frequency Response, NTSC Square Pixel Sampling

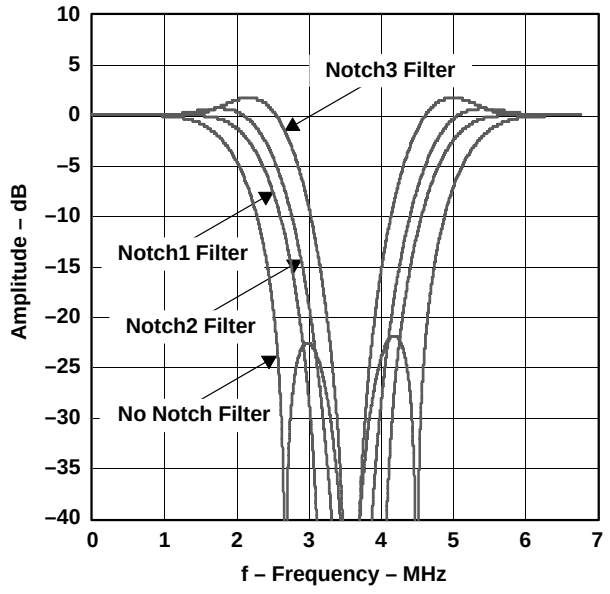


Figure 2–4. Chroma Trap Filter Frequency Response, 13.5-MHz Sampling

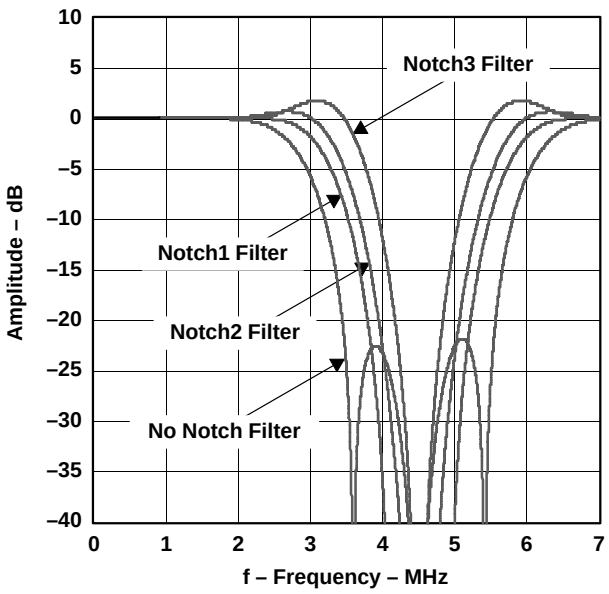


Figure 2–5. Chroma Trap Filter Frequency Response, PAL Square Pixel Sampling

2.5.2 Color Low-Pass Filter

In some applications, it is desirable to limit the U/V bandwidth to avoid crosstalk. This is especially true in case of nonstandard video signals that have asymmetrical U/V sidebands. In this case, notch filters are provided that limits the bandwidth of the U/V signals.

Notch filters are needed when the comb filtering turns off due to extreme color transitions in the input image. The response of these notch filters is shown in Figure 2–6 through Figure 2–9. The notch filters have three options that allow three different frequency responses based on the color frequency characteristics of the input video.

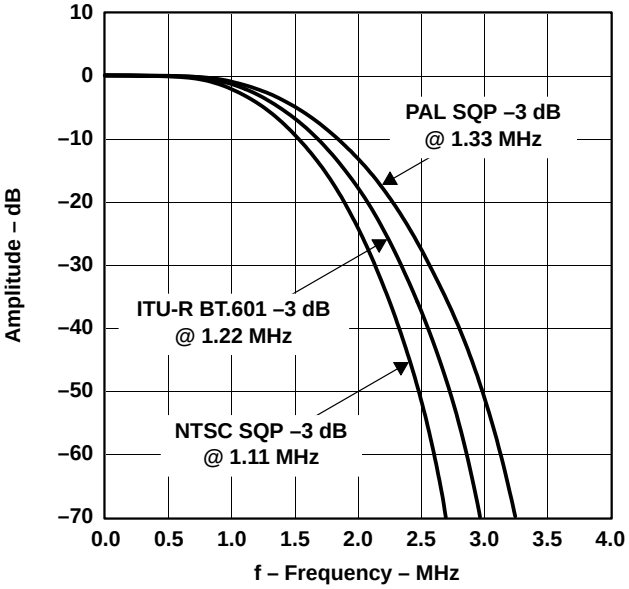


Figure 2–6. Color Low-Pass Filter Frequency Response

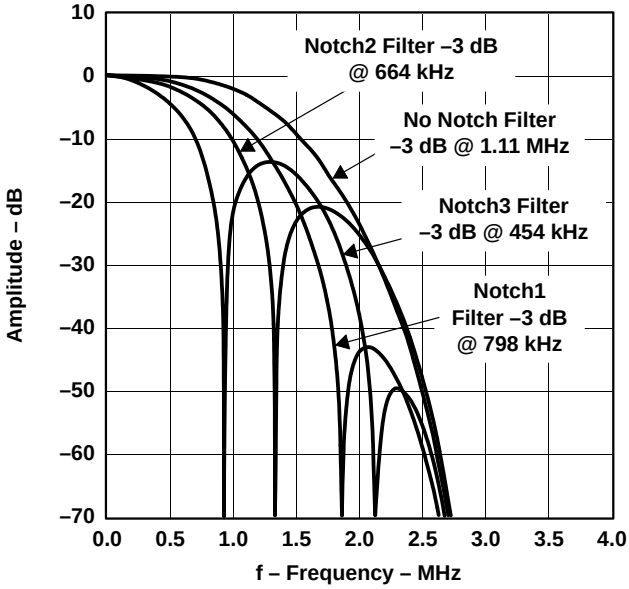


Figure 2–7. Color Low-Pass Filter With Notch Filter Frequency Response, NTSC, and PAL-M Square Pixel Sampling

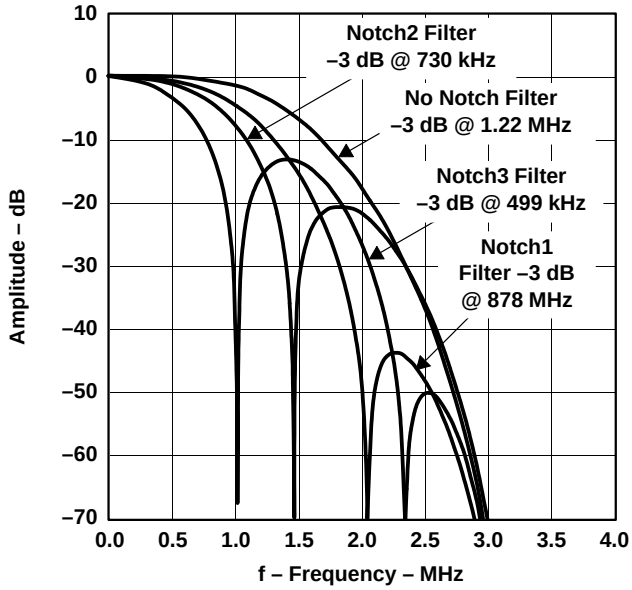


Figure 2–8. Color Low-Pass Filter With Notch Filter Characteristics, 13.5-MHz Sampling

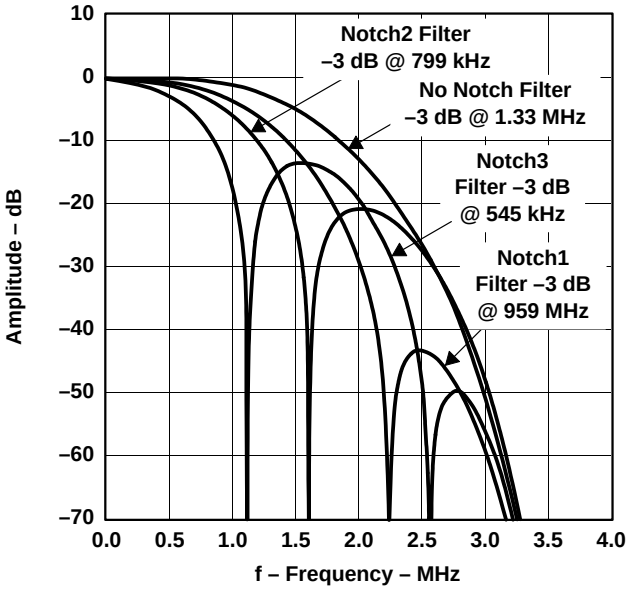


Figure 2–9. Color Low-Pass Filter With Notch Filter Characteristics and PAL Square Pixel Sampling

2.5.3 Luma Processing

The luma component is derived from the composite signal by subtracting the remodulated chroma information. A line delay exists in this path to compensate for the line delay in the adaptive comb filter in the color processing chain. The luma information is then fed into the peaking circuit, which enhances the high frequency components of the signal as shown below.

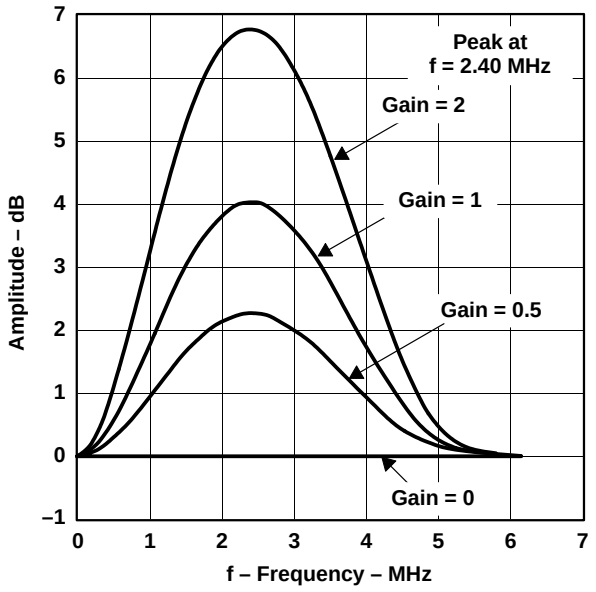


Figure 2–10. Peaking Filter Response, NTSC Square Pixel Sampling

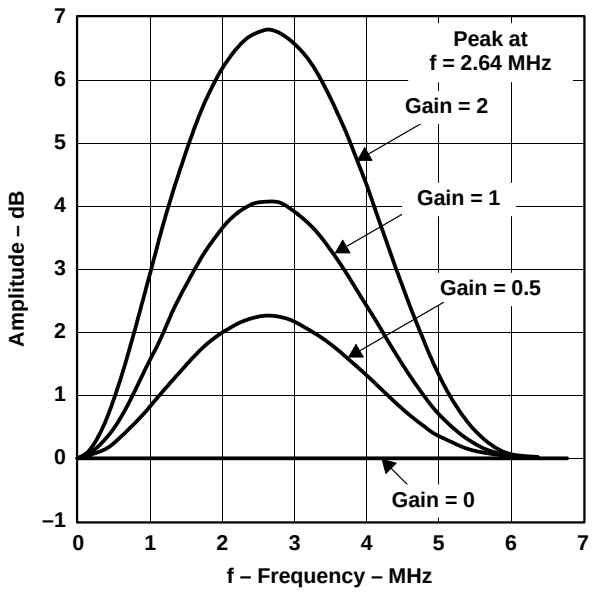


Figure 2–11. Peaking Filter Response, NTSC/PAL ITU-R BT.601 Sampling

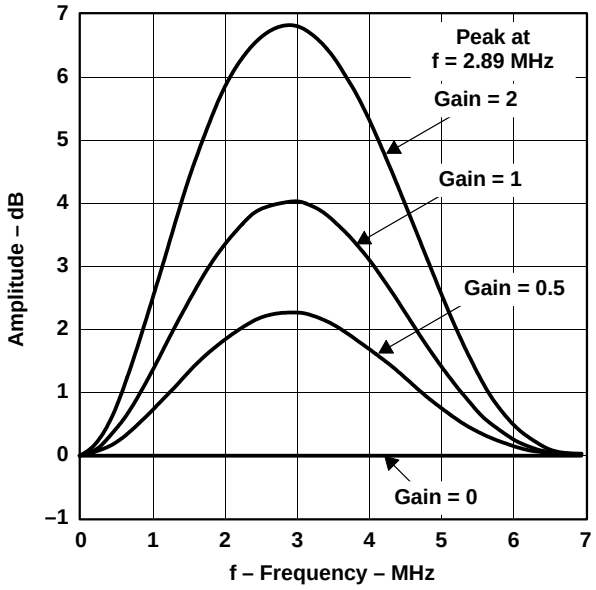


Figure 2–12. Peaking Filter Response, PAL Square Pixel Sampling

2.5.4 Chroma Processing

For PAL/NTSC formats, the color processing begins with a quadrature demodulator extracting U and V components from the composite signal. The U/V signals then pass through the gain control stage for chroma saturation adjustment. An adaptive comb filter is applied to both U and V to eliminate cross-chrominance noise. Hue control is achieved with phase shift of the digitally controlled oscillator. An automatic color killer circuit is also included in this block. The color killer suppresses the chroma processing when the color burst of the video signal is weak or not present.

2.5.5 Timing Processor

The timing processor is a combination of hardware and software running in the microprocessor that serves to control horizontal lock to the input sync pulse edge, AGC, offset adjustment in the analog front end, vertical sync detection, and Macrovision™ detection.

The sync input is filtered by a FIR filter for noise reduction. Coarse lock detects the falling or rising edge of the filtered sync input by comparing pixels against a threshold. The coarse phase error is read by the microprocessor and used to make coarse adjustments to the horizontal DTO frequency. After coarse lock has moved the sync edge within the fine lock window, the fine lock is enabled to make fine adjustments to the horizontal DTO frequency such that the edge is centered within the window to sub pixel accuracy.

The gain and offset of the AFE is adjusted such that the sync height and back porch levels achieve target values. Filtered samples of the sync tip and back porch are read and processed by the microprocessor. The gain that is applied to the sync input is also applied to the chroma input. Filtered samples of the chroma blanking level are read and processed by the microprocessor to adjust the chroma offset to set the blanking level to the midpoint of the ADC range.

The vertical sync is detected at the input by comparing half line accumulated pixel values against an adaptive threshold. Sequential patterns of half line-accumulated results are used to detect odd and even field syncs.

The presence of Macrovision is detected by the presence of pseudosyncs by coarse lock. A counter tracks the number of edges detected after the horizontal sync edge has been detected.

2.5.6 VBI Data Processor

The TVP5150 vertical blank interval (VBI) data processor (VDP) slices various data services like Teletext (WST, NABST), closed caption (CC), wide screen signaling (WSS) etc. These services are acquired by programming the VDP to enable a standard(s) in the VBI. The results are stored in a FIFO and/or registers. The Teletext results are stored in a FIFO only. Table 2–1 gives a summary of the types of VBI data supported according to the video standard. It supports both square pixel and ITU-R BT. 601 sampling for each standard. The 26 standard modes are currently supported. Nevertheless, the TVP5150 VDP can be used for custom modes. TI may provide the RAM content of custom modes when the customer asks with a full custom VBI spec. One configuration for a standard consists of 15 bytes of data. However, addressing of the RAM has steps of 16 bytes for a convenience.

Table 2–1. Data Types Supported by the VDP

LINE MODE REGISTER (D0h–FBh) Bit[3:0]	SAMPLING RATE (0Dh) Bit 7	NAME	DESCRIPTION
0000b	X	X	Reserved
0000b	X	X	Reserved
0001b	0	WST PAL B S	Teletext, PAL, system B, square
0001b	1	WST PAL B 6	Teletext, PAL, system B, ITU-R BT 601
0010b	0	WST PAL C S	Teletext, PAL, system C, square
0010b	1	WST PAL C 6	Teletext, PAL, system C, ITU-R BT 601
0011b	0	WST, NTSC B S	Teletext, NTSC, system B, square
0011b	1	WST, NTSC B 6	Teletext, NTSC, system B, ITU-R BT 601
0100b	0	NABTS, NTSC C S	Teletext, NTSC, system C, square
0100b	1	NABTS, NTSC C 6	Teletext, NTSC, system C, ITU-R BT 601
0101b	0	TTX, NTSC D S	Teletext, NTSC, system D (Japan), square
0101b	1	TTX, NTSC D 6	Teletext, NTSC, system D (Japan), ITU-R BT 601
0110b	0	CC, PAL S	Closed caption PAL square
0110b	1	CC, PAL 6	Closed caption PAL ITU-R BT 601
0111b	0	CC. NTSC S	Closed caption NTSC, square
0111b	1	CC, NTSC 6	Closed caption NTSC, ITU-R BT 601

Table 2–1. Data Types Supported by the VDP (Continued)

LINE MODE REGISTER (D0h–FBh) Bit[3:0]	SAMPLING RATE (0Dh) Bit 7	NAME	DESCRIPTION
1000b	0	WSS, PAL S	Wide screen signal, PAL square
1000b	1	WSS, PAL 6	Wide screen signal, PAL ITU-R BT 601
1001b	0	WSS, NTSC S	Wide screen signal, NTSC, square
1001b	1	WSS, NTSC 6	Wide screen signal, NTSC, ITU-R BT 601
1010b	0	VITC, PAL S	Vertical interval timecode, PAL square
1010b	1	VITC, PAL 6	Vertical interval timecode PAL ITU-R BT 601
1011b	0	VITC, NTSC S	Vertical interval timecode, NTSC, square
1011b	1	VITC, NTSC 6	Vertical interval timecode, NTSC, ITU-R BT 601
1100b	0	VPS, PAL S	Video program system, PAL, square
1100b	1	VPS, PAL 6	Video program system, PAL, ITU-R BT 601
1101b	Custom		Custom
1110b	Custom		Custom
1111b	x	Active video	Active video/full field

At power up, the host interface is required to program the VDP-configuration RAM (VDP-CRAM) contents with the lookup table. This is done through port address C3h. Each read or write from to this address auto increments an internal counter to the next RAM location. To access the VDP-CRAM, the line mode registers (D0h–FCh) must be programmed with FFh to avoid a conflict with the microprocessor and the VDP in both writing and reading. Full field mode must also be disabled.

Available VBI lines are from line 6 to line 27 of both field 1 and field 2. Theoretically, each line can be any VBI mode because the VDP processes VBI data in a line by line. When changing modes, the VDP must allow the current transaction to complete through the delays of the VDP before switching the line mode register's contents. It must also complete the loading of the line mode registers before the next line starts processing. The switch pixel number is set through registers CBh and CCh. Output data is available either through the VBI-FIFO (B0h) or through dedicated registers at 90h–AFh, both of which are available from the host port.

2.6 VBI FIFO and Ancillary Data in Video Stream

Sliced VBI data can be output as ancillary data in the video stream in ITU-R BT.656 mode. VBI data is output during the horizontal blanking period following the line from which the data was retrieved. The following table shows the header format and sequence of the ancillary data inserted into the video stream. This format is also used to store any VBI data into the FIFO. The size of FIFO is 512 bytes. Therefore, the FIFO can store up to 11 lines of Teletext data with NTSC NABST standard.

Table 2–2. Ancillary Data Format and Sequence

BYTE NO.	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	DESCRIPTION	
0	0	0	0	0	0	0	0	0	Ancillary data preamble	
1	1	1	1	1	1	1	1	1		
2	1	1	1	1	1	1	1	1		
3	NEP	EP	0	1	0	DID2	DID1	DID0	Data ID (DID)	
4	NEP	EP	F5	F4	F3	F2	F1	F0	Secondary data ID (SDID)	
5	NEP	EP	N5	N4	N3	N2	N1	N0	Number of 32 bit data (NN)	
6	Video line # [7:0]								Internal data ID0 (IDID0)	
7	0	0	0	Data error	Match #1	Match #2	Video line # [9:8]		Internal data ID1 (IDID1)	
8	1. Data								Data byte	First word
9	2. Data								Data byte	
10	3. Data								Data byte	
11	4. Data								Data byte	
:	:								:	
	m–1. Data								Data byte	N^{th} word
	m. Data								Data byte	
	NEP	EP	CS[5:0]						Checksum	
4(N+2)	1	0	0	0	0	0	0	0	Fill byte	

EP Even parity for D0–D5

NEP Not even parity

DID 91h sliced data of VBI lines of first field
53h sliced data of line 24 to end of first field
55h sliced data of VBI lines of second field
97h sliced data of line 24 to end of second field

SDI: This field holds the data format taken from the line mode register of the corresponding line.

NN Number of Dwords beginning with byte 8 through 4(N+2). Note this value is the number of Dwords where each Dword is 4 bytes.

IDID0 Transaction video line number [7:0]

IDID1 Bit 0/1 – Transaction video line number [9:8]
Bit 2 – Match 2 flag
Bit 3 – Match 1 flag
Bit 4 – 1 if an error was detected in the EDC block. 0 if not.

CS Sum of D0–D7 of DID through last data byte.

2.6.1 Raw Video Data Output

The TVP5150 can output raw A/D video data at 2x sampling rate for external VBI slicing. This is transmitted as an ancillary data block, a bit differently from the way the sliced VBI data is transmitted in FIFO format, as described in the previous section. First, the samples are transmitted during the active portion of the line. The ITU-R BT.656 spec requires that a preamble code of 00h FFh FFh ZZh be transmitted where, if ZZh is anything other that 15h, it indicates the presence of ancillary data immediately following the preamble. Also, a preamble of 00h FFh FFh 15h should be inserted after the ancillary data to indicate that the remainder of the line is available for the insertion of further ancillary signals.

2.6.2 Output Formatter

The YUV digital output can be programmed as 8-bit 4:2:2 or 8-bit ITU-R BT.656 parallel interface standard. This circuit also detects pseudo sync pulses, AGC pulses, and color striping in copy protected material according to Macrovision specification and retrieves VBI information. S-video bypasses the Y/C separation block.

The different formats that are supported and the corresponding sampling frequencies are listed in Table 2–3.

Table 2–3. Output Formatter Supported Formats

MODES	DATA CLOCK FREQUENCY	PINS	EMBEDDED SYNCS, VBI DATA, RAW DATA	STANDARDS SUPPORTED
8-bit ITU-R BT.656	2xPCLK (SCLK)	Ch(7-0) YCbCr	Syncs optional VBI optional (edge prog) Raw data optional	NTSC/PAL YUV output
8-bit 4:2:2	2xPCLK (SCLK)	Ch(7-0) YCbCr	Syncs optional VBI optional (edge prog) Raw data optional	Any standard YUV output

Figure 2–13 explains the different modes.

NOTE:8-bit mode uses only eight MSBs of output ports.

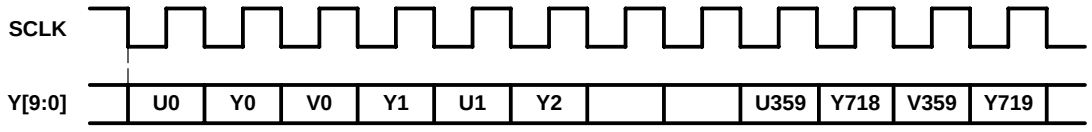


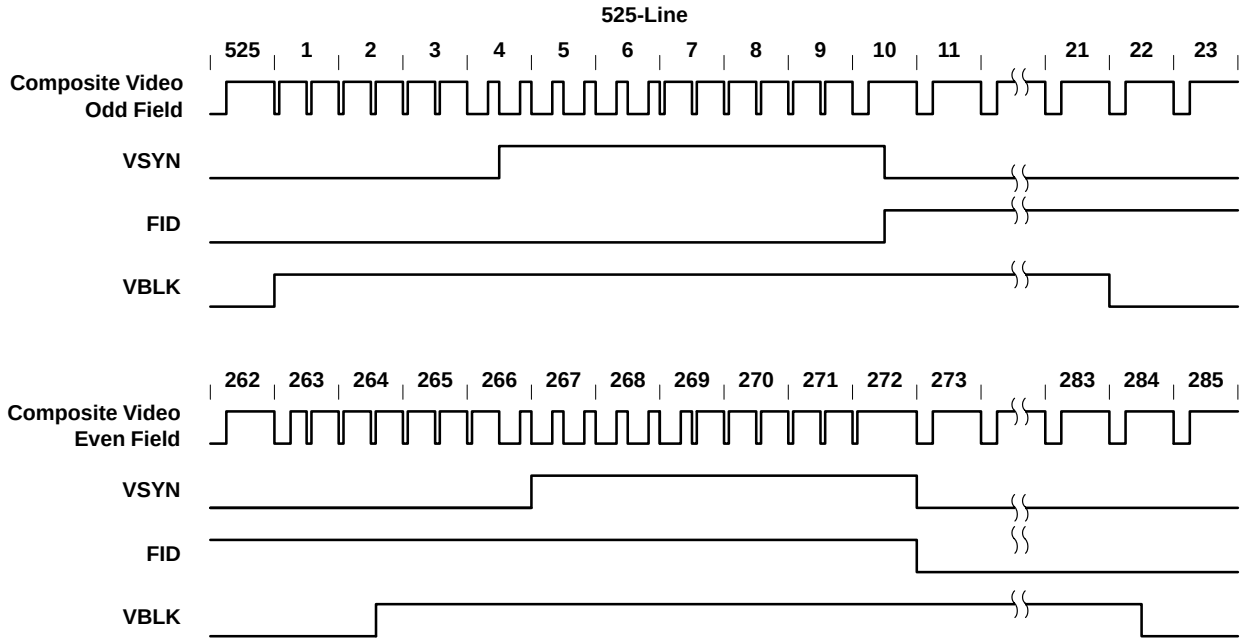
Figure 2–13. 8-Bit YCbCr 4:2:2 Mode

2.7 Synchronization Signals

Non-data stream embedded syncs are provided via the following signals:

- VSYNC (vertical sync)
- FID/VLK (field indicator or vertical lock indicator)
- GPCL/VBLK (general-purpose IO or vertical blanking indicator)
- PALI/HLK (PAL switch indicator or horizontal lock indicator)
- HSYN (horizontal sync)
- AVID (active video indicator)

In hardware, VSYN, FID, PALI, and VBLK are software set and double buffered to an independent programmable SCLK pixel count. This allows any possible alignment to the internal pixel count and line count. The proper settings for a 525-line video output are given as an example below.



Note 1. Line numbering conforms to ITU-R BT.470

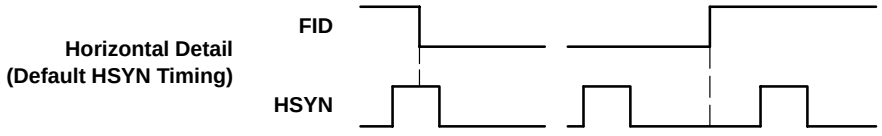
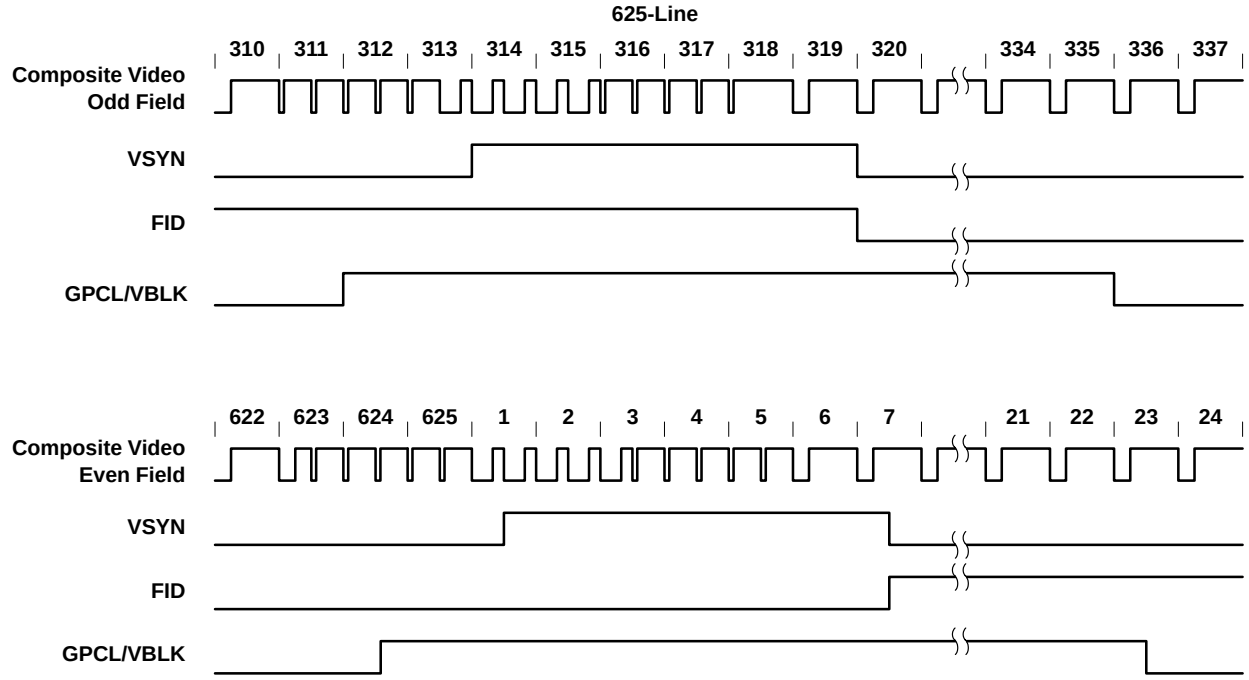


Figure 2–14. 525-Line Vertical Synchronization Signal

HSYN is start (SCLK) pixel programmable with a fixed duration of 128 SCLK's. AVID has both start and stop pixels programmable and can be programmed to be inactive during the VBI, which is the default mode of operation. Note that when using embedded syncs AVID occurs four pixels before the first active pixel, aligning with the SAV code.

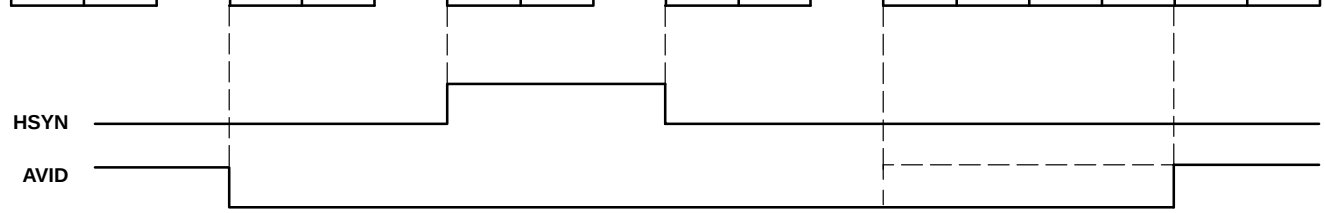


Note 1. Line numbering conforms to ITU-R BT.470

Figure 2–15. 625-Line Vertical Synchronization Signal

8-bit 4:2:2 timing with 2x pixel clock (SCLK) reference. Shown with and without embedded syncs.

NTSC 601	1438	1439	1440	...	1471	1472	...	1599	1600	...	1711	1712	1713	1714	1715	0	1
8-Bit	Cr	Y	Cb	...	Y	Cb	...	Y	Cb	...	Y	Cb	Y	Cr	Y	Cb 0	Y 0
ITU 656	Cr 359	Y 719	FF EAV	...	10	80	...	10	80	...	10	FF SAV	00	00	XX	Cb 0	Y 0



NOTE: The AVID rising edge occurs 4 SCLK cycles early when in the ITU-R BT.656 output mode.

Figure 2–16. Horizontal Synchronization Signals

2.7.1 Embedded Syncs

Standards with embedded syncs insert SAV and EAV codes into the data stream on the rising and falling edge of AVID. These codes contain the V and F bits, which also define vertical timing. F and V are software programmable and change after SAV but before EAV, so that the new value always appears on EAV first. Table 2–4 gives the format of the SAV and EAV codes.

H = 1 always indicates EAV. H = 0 always indicates SAV. The alignment of V and F to the line and field counter varies depending on the standard.

Table 2–4. Format of the SAV and EAV Codes

	D7	D6	D5	D4	D3	D2	D1	D0
Preamble	1	1	1	1	1	1	1	1
Preamble	0	0	0	0	0	0	0	0
Preamble	0	0	0	0	0	0	0	0
Status word	1	F	V	H	P3	P2	P1	P0

The P bits are protection bits:

P3 = V xor H; P2 = F xor H; P1 = F xor V; P0 = F xor V xor H

2.7.2 HLK and VLK

HLK and VLK outputs can be selected to replace PALI and FID respectively. These signals are quasi-static. They only change state when out of horizontal or vertical lock.

2.7.3 Clock Circuits

An internal line-locked PLL generates the system and pixel clocks. Figure 2–17 shows a simplified clock circuit diagram. The digital control oscillator (DCO) generates the reference signal for the horizontal PLL. A 14.318-MHz clock is required to drive the DCO. This may be input to TVP5150 at TTL level on the XTAL1 terminal, or a crystal of 14.318-MHz fundamental resonant frequency may be connected across terminals XTAL1 and XTAL2. The next figure shows the reference clock configurations. For the example crystal circuit shown, (a parallel-resonant crystal with 14.328-MHz fundamental frequency), the external capacitors must have the following relationship:

CL1 = CL2 = 2CL – C(stray)

Where C(stray) is the terminal capacitance with respect to ground. Note that with the crystal oscillator an external 4.53-kΩ resistor is required across XTAL1 and XTAL2 terminals.

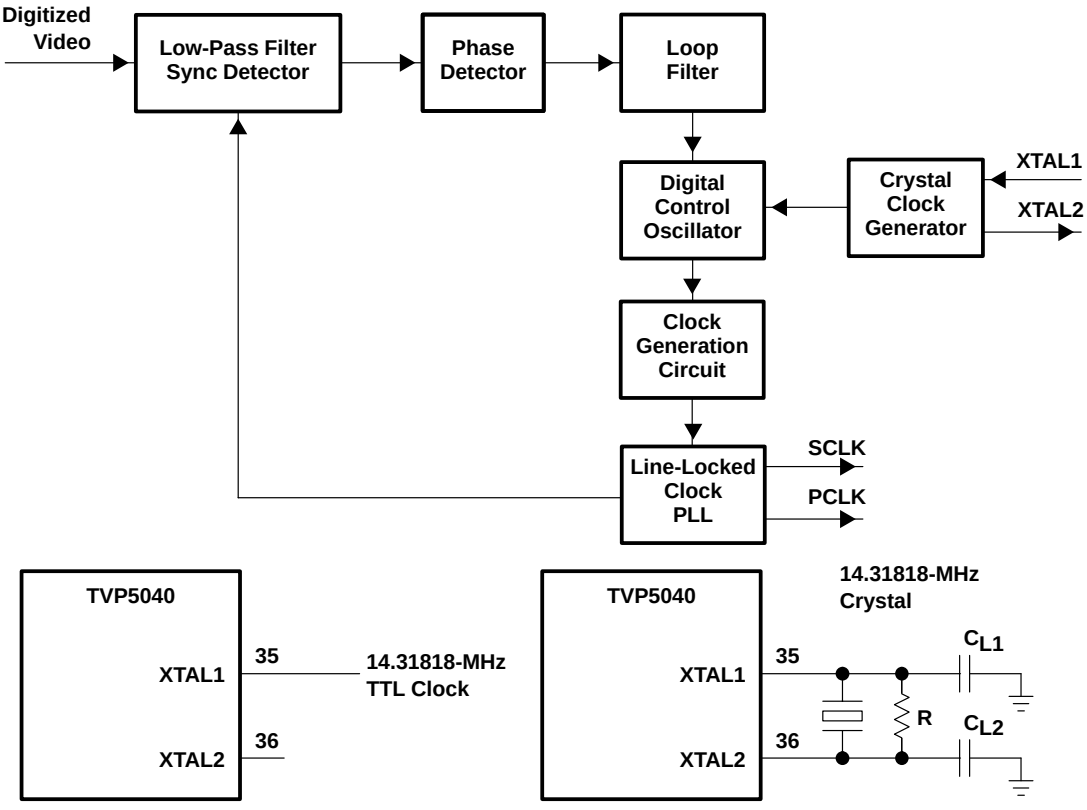


Figure 2–17. Reference Clock Configurations

2.7.4 Phase-Locked Loop

The PLL provides the device with the necessary clocks. Clocks are provided to the ADC, for luma and chroma processing, audio block, and the scaling blocks.

The self-biasing PLL minimizes jitter and processes environmental variability. It is capable of operating off a single crystal frequency with a high supply rejection ratio.

2.7.5 Genlock

A Genlock control function is provided to support a standard video encoder to synchronize its internal color phase DCO for a clean video line and color lock. The Genlock is compatible with the Phillips RTC and the TI proprietary Genlock schemes.

2.7.6 TVP5150 Genlock Control Interface

The frequency control word of the internal color subcarrier digital control oscillator (DCO) and the subcarrier phase reset bit are transmitted via the GLCO terminal. The frequency control word is a 23-bit binary number. The frequency of the DCO can be calculated from the following equation:

$$Fdco = \frac{Fctrl}{223} \times Fsclk$$

Where Fdco is the frequency of the DCO, Fctrl is the 23-bit DCO frequency control, and Fsclk is the frequency of the SCLK. The last bit (bit 0) of the DCO frequency control is always 0.

A write of 1 to bit 4 of the chrominance control register at HOST PORT sub-address 1Ah causes the sub-carrier DTO phase reset bit to be sent on the next scan line on GLCO. The active low reset bit occurs 7 SCLK's after the transmission of the last bit of DCO frequency control. Upon the transmission of the reset bit, the phase of the TVP5150 internal subcarrier DCO is reset to zero.

This interface provides a method to signal a subcarrier DTO phase reset on the next scan line.

A genlocking slave device can be connected to the GLCO terminal and use the information on GLCO to synchronize ins internal color phase DCO to achieve clean line and color lock.

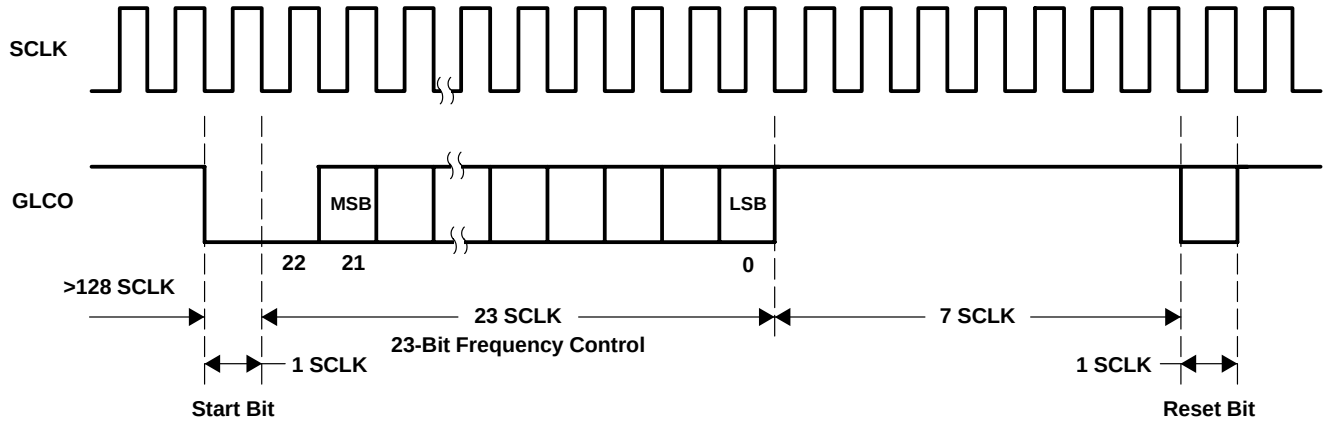


Figure 2–18. GCLO Timing

2.8 Scaling/Windowing Functionality

2.8.1 Scaling

Scaling can be done vertically and horizontally. The device is able to scale by ratios of:

	DOWNSCALE
Vertically	1/32x
Horizontally	1/32x

The device does not allow changing frame rates. Only the number of lines per frame or field and the number of pixels per line can be changed. The change takes place on a frame or field basis.

For the horizontal scaling, an optimized 32 phase 5 tap polyphase filter is used for both chroma and luma. This filter acts as an anti-aliasing interpolation filter. The filter has different settings allowing it to change based on the scaling ratio.

For the vertical filter a novel algorithm is developed. This algorithm allows for different settings of the length and filter coefficients based on the scaling ratio. This change of the settings is transparent to the user.

The scaler allows the user to define the desired scaled image size with a resolution of 2 pixels horizontally and vertically. Registers are provided for the user to allow this control of the horizontal and vertical size.

The interface to the user is the number of horizontal pixels and vertical lines that are to be used. The input to the scaler is from the windowing interface (explained in the next section).

2.8.2 Windowing

The device also supports windowing, which basically allows the user to decide the active video window within the original video data. The user has control over the starting (top left corner) and end point (bottom right corner) of the window. An external signal (AVID) is active during the time when the valid video data, based on the window defined, is output from the device.

The windowing takes place before the data is scaled. The user could define the area of interest and then scale it to the desired resolution.

2.8.3 Temporal Decimation

To reduce the frame rate coming out the device, it is necessary to drop frames/fields depending on the user input. Normally this feature is used when the bandwidth of the backend processor is not able to handle real time video. In this case, the number of frames per second output by the device can be configured.

If the backend processor handles the dropping of frames, then there is a possibility of the output being bursty. The TVP5150 ensures an equal distribution of frame dropping from the maximum set of frames available.

The TVP5150 can be configured to drop frames either on a frame or field basis. The user can also configure the device to start at either odd or even frame boundaries, or to suppress selectively only odd or even fields.

AVID determines whether the data is active or not. Hence, it is disabled (high) when the field/frame is dropped.

2.9 Interfacing to the DSC24, TI DSP

2.9.1 Audio

When the DSC24 needs to communicate with an audio codec, the interface would just require an audio clock. This clock is provided by the audio interface available on the TVP5150.

2.9.2 Video

The DSC24has a standard interface for video signals. It accepts YUV4:2:2 16-bit component input data, along with the pixel clock and the horizontal and vertical syncs. Table 2–5 shows the pin descriptions and the corresponding pins on the TVP5150.

Table 2–5. Pin Descriptions

TYP5150 PIN NAME	DSC24 PIN NAME	I/O ON TVP4150	DESCRIPTION
PCLK	PCLK	O	Pixel clock for the data
YOUT(7:0)†	YIN(7:0)	O	ITU 656 output from TVP5150
HSYNC	HDIN	O	Horizontal synchronization to the DSC24
VSYNC	VDIN	O	Vertical synchronization to the DSC24

† The 8 MSB's of the 9-bit bus

3 Electrical Specifications

3.1 Absolute Maximum Ratings†

Digital power supply voltage, DV_{DD} . . . . . –0.3 V to TBD V
Analog power supply voltage, AV_{DD} . . . . . –0.5 V to TBD V
Digital input voltage, V_I . . . . . –0.3 V to DV_{DD}+0.3 V
Operating free-air temperature, T_A . . . . . 0°C to 70°C
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Maximum total power dissipation, P_D . . . . . 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
DV_{DD}	Digital supply voltage		1.8		V
AV_{DD}	Analog supply voltage		1.8		V
$IODV_{DD}$	Digital I/O supply voltage		1.8/3.3		V
$V_{I(PP)}$	Analog input voltage (ac-coupling necessary)	0.5		1.26	V
V_{IH}	Digital input voltage high	2			V
V_{IL}	Digital input voltage low			0.8	V
V_{IH} (I^2C)	Input voltage high, VC0 and VC1 in I^2C mode	2.3			V
V_{IL} (I^2C)	Input voltage low, VC0 and VC1 in I^2C mode			1	V
I_{OH}	Output current, V_{out} = 2.4 V	–4	–8		mA
I_{OL}	Output current, V_{out} = 0.4 V	6	8		mA
T_A	Operating free-air temperature	0		70	°C

3.2.1 Crystal Specifications

CRYSTAL/CLOCK SPECIFICATIONS	MIN	NOM	MAX	UNIT
Frequency		14.31818		MHz
Frequency tolerance			±50	ppm

3.3 Electrical Characteristics

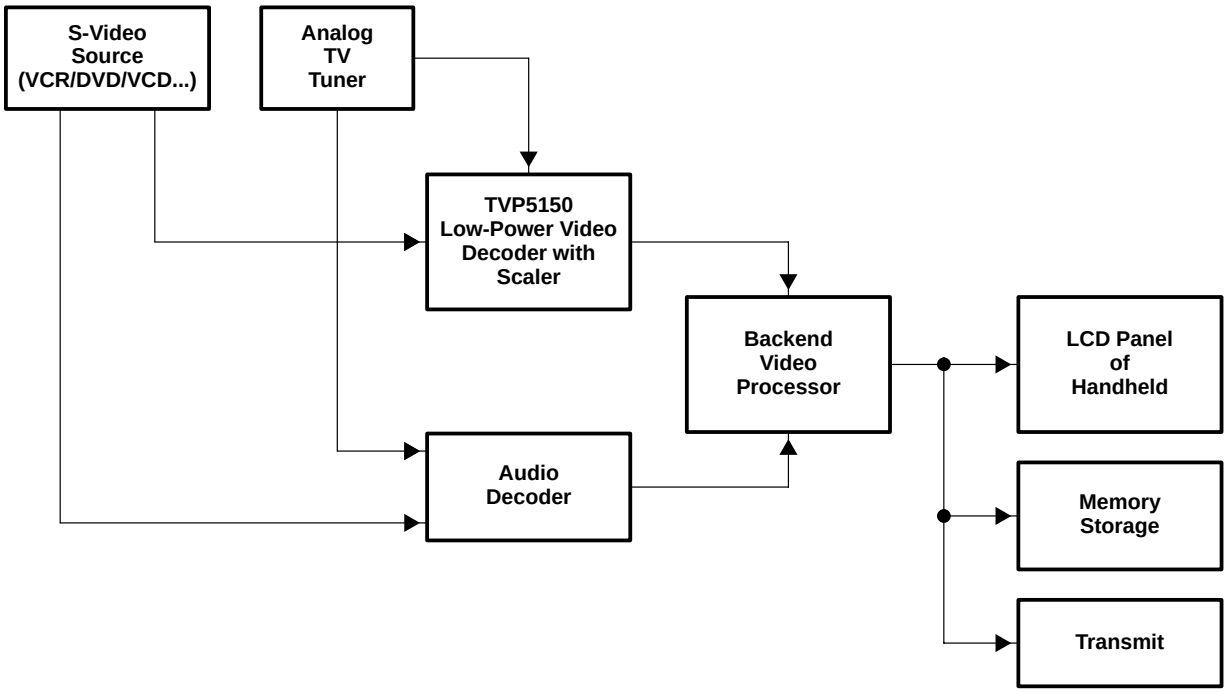
Test conditions: DV_{DD} = 1.8 V, AV_{DD} = 1.8 V, T_A = 70°C (unless otherwise specified)

3.3.1 DC Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DI_{DD}	Digital supply current			35		mA
AI_{DD}	Analog supply current			30		mA
I_{lkg}	Input leakage current			TBD		µA
C_i	Input capacitance	By design		TBD		pF
V_{OH}	High-level output voltage			TBD		V
V_{OL}	Low-level output voltage			TBD		V

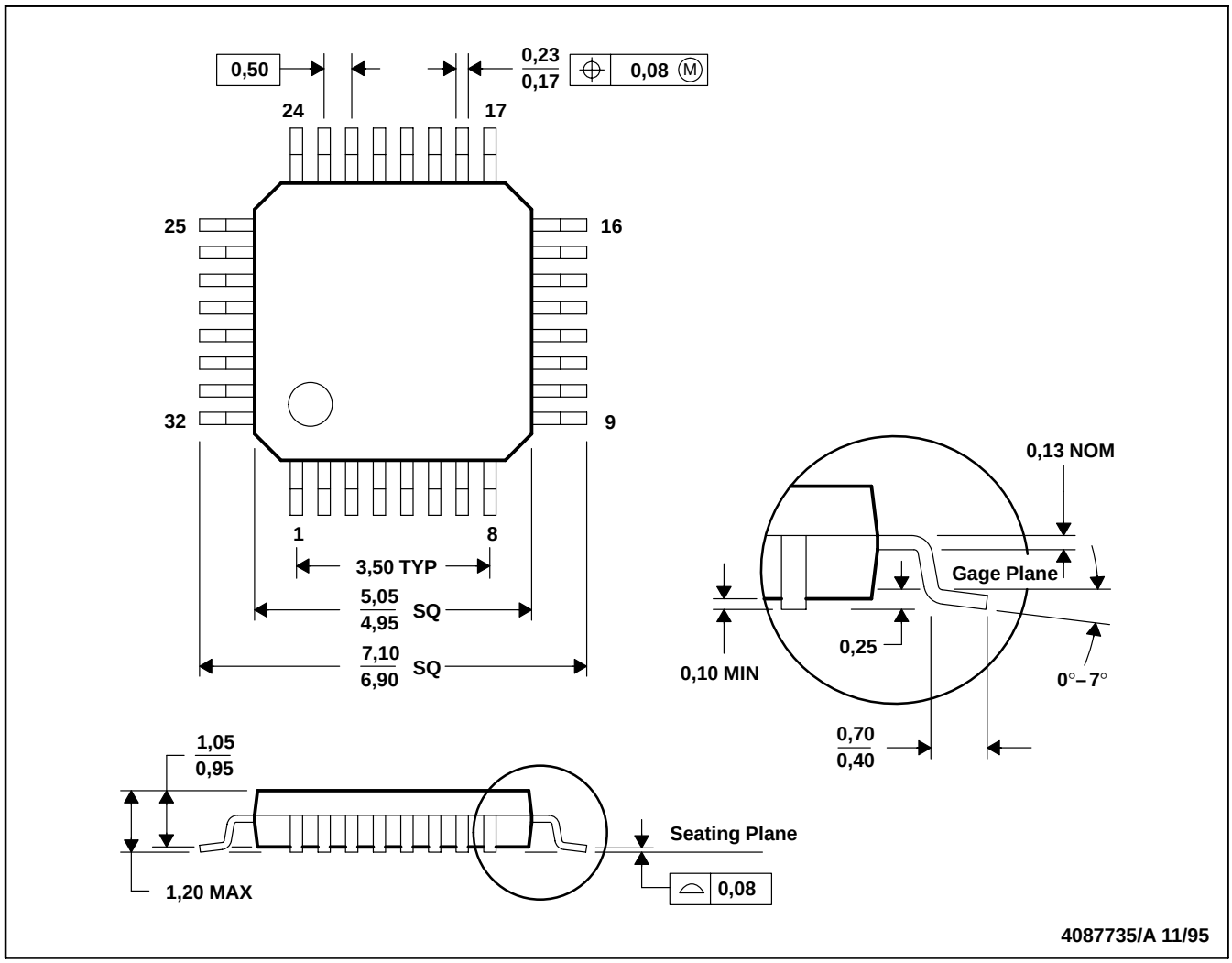
NOTE: Measured with a load of 10 kΩ in parallel to 15 pF.

4 Application Information



5 Mechanical Data

PBS (S-PQFP-G32)
PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.