10-Ω SPDT ANALOG SWITCH
SINGLE-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER

FEATURES

- 2.25-V to 5.5-V Single-Supply Operation
- Low ON-State Resistance (10 Ω Max at V_+ = 5V)
- Specified Break-Before-Make Switching
- Low Power Consumption
- TTL/CMOS Compatible Control Input
- Low Input/Output Capacitance
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Control Inputs Are 5.5-V Tolerant
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)

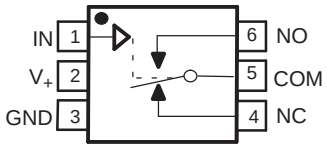
APPLICATIONS

- Cell Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- Sample-and-Hold Circuits

DESCRIPTION

The TS5A9411 is a single-pole double-throw (SPDT) analog switch that is designed to operate from 2.25 V to 5.5 V. The device offers low ON-state resistance, low leakage, and low power with a break-before-make feature. These features make this device suitable for portable and battery-powered applications.

DCK PACKAGE
(TOP VIEW)



FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	SOT (SC-70) – DCK	Tape and reel	TS5A9411DCKR	32_

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) DCK: The actual top-side marking has one additional character that designates the assembly/test site.

SUMMARY OF CHARACTERISTICS(1)

Configuration	2:1 Multiplexer/ Demultiplexer (1 × SPDT)
Number of channels	1
ON-state resistance (r_{ON})	5.3 Ω
ON-state resistance match (Δr_{ON})	0.03 Ω
ON-state resistance flatness $r_{ON(flat)}$)	2 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	9 ns/7 ns
Break-before-make time (t_{BBM})	1 ns
Charge injection (Q_C)	12.5 pC
Bandwidth (BW)	100 MHz
OFF isolation (O_{ISO})	–84 dB at 1 MHz
Crosstalk (X_{TALK})	–85 dB at 1 MHz
Total harmonic distortion (THD)	0.03%
Leakage current ($I_{NO(OFF)}$/$I_{NC(OFF)}$)	±3 nA
Power-supply current (I_+)	0.01 µA
Package options	6-pin DCK

(1) V_+ = 5 V, T_A = 25°C

ABSOLUTE MINIMUM AND MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(3)		–0.3	6	V
V_{NO} V_{NC} V_{COM}	Analog voltage range(3)(4)(5)		–0.3	V_+ + 0.3	V
I_K	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0	–50		mA
I_{NO} I_{NC} I_{COM}	On-state switch current	V_{NO}, V_{NC}, V_{COM} = 0 to V_+	–50	50	mA
	On-state peak switch current(6)		–200	200	
V_I	Digital input voltage range(3)(4)		–0.5	V_+ + 0.3	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration < 10% duty cycle

THERMAL IMPEDANCE RATINGS

				UNIT
θ_{JA}	Package thermal impedance(1)	DCK package	259	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY(1)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{ON}	V_{NO} or V_{NC} = 3 V, I_{COM} = –10 mA,	Switch ON, See Figure 6	25°C	4.5 V		5.3	9	Ω
				Full				10	
ON-state resistance match between channels	Δr_{ON}	V_{NO} or V_{NC} = 3 V, I_{COM} = –10 mA,	Switch ON, See Figure 6	25°C	4.5 V		0.03	0.3	Ω
				Full				0.3	
ON-state resistance flatness	$r_{ON(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –10 mA,	Switch ON, See Figure 6	25°C	4.5 V		2		Ω
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = 1 V to 4.5 V, or V_{NC} or V_{NO} = 4.5 V, V_{COM} = 1 V,	Switch OFF, See Figure 7	25°C	5.5 V	–500		500	pA
				Full		–3		3	nA
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = 1 V V_{NC} or V_{NO} = 4.5 V, V_{COM} = 4.5 V,	Switch ON, See Figure 8	25°C	5.5 V	–500		500	pA
				Full		–3		3	nA
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 1 V, or V_{NC} or V_{NO} = Open, V_{COM} = 4.5 V,	Switch ON, See Figure 8	25°C	5.5 V	–500		500	pA
				Full		–3		3	nA
Digital Input (IN)									
Input logic high	V_{IH}			Full	4.5 V to 5.5 V	2.4		5.5	V
					4.5 V	2		5.5	
Input logic low	V_{IL}			Full	4.5 V to 5.5 V	0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	5.5 V	–0.05		0.05	µA
				Full		–0.05		0.05	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 10	25°C	5 V			9	ns
				Full	4.5 V to 5.5 V			10	
Turn-off time	t_{OFF}	V_{COM} = 3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 10	25°C	5 V			7	ns
				Full	4.5 V to 5.5 V			7.5	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = 3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 11	25°C	5 V	1			ns
				Full		0.9			
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 15	25°C	5 V		12.5		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, f = 1 MHz,	Switch OFF, See Figure 9	25°C	5 V		3.5		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, f = 1 MHz,	See Figure 9	25°C	5 V		8.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, f = 1 MHz,	Switch ON, See Figure 9	25°C	5 V		8.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND, f = 1 MHz,	See Figure 9	25°C	5 V		25		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 12	25°C	5 V		100		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz,	Switch OFF, See Figure 13	25°C	5 V		–84		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz,	Switch ON, See Figure 14	25°C	5 V		–85		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 16	25°C	5 V		0.03		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	5.5 V		0.01		µA
				Full				0.5	

ELECTRICAL CHARACTERISTICS FOR 3-V SUPPLY(1)

V_+ = 2.7 V to 3.3 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{ON}	V_{NO} or V_{NC} = 1.5 V, I_{COM} = –10 mA,	Switch ON, See Figure 6	25°C	2.7 V		11.5	15	Ω
				Full				20	
ON-state resistance match between channels	Δr_{ON}	V_{NO} or V_{NC} = 1.5 V, I_{COM} = –10 mA,	Switch ON, See Figure 6	25°C	2.7 V		0.05	0.3	Ω
				Full				0.3	
ON-state resistance flatness	$r_{ON(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –10 mA,	Switch ON, See Figure 6	25°C	3 V		2		Ω
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = 1 V to 3 V, or V_{NC} or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 7	25°C	3.3V	–400		400	pA
				Full		–2		2	nA
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = 1 V V_{NC} or V_{NO} = 3 V, V_{COM} = 3 V,	Switch ON, See Figure 8	25°C	3.3 V	–400		400	pA
				Full		–2		2	nA
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 1 V, or V_{NC} or V_{NO} = Open, V_{COM} = 3 V,	Switch ON, See Figure 8	25°C	3.3 V	–400		400	pA
				Full		–2		2	nA
Digital Input (IN)									
Input logic high	V_{IH}			Full		2		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V	–0.05		0.05	µA
				Full		–0.05		0.05	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

ELECTRICAL CHARACTERISTICS FOR 3-V SUPPLY (continued)

V_+ = 2.7 V to 3.3 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 10	25°C	3 V			13	ns
				Full	2.7 V to 3.3 V			15	
Turn-off time	t_{OFF}	V_{COM} = 3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 10	25°C	3.3 V			7.5	ns
				Full	2.7 V to 3.3 V			8.5	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = 3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 11	25°C	3.3 V	1			ns
				Full		0.9			
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 15	25°C	3 V		6		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, f = 1 MHz,	Switch OFF, See Figure 9	25°C	3 V		3.5		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, f = 1 MHz,	Switch OFF, See Figure 9	25°C	3 V		8.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, f = 1 MHz,	Switch OFF, See Figure 9	25°C	3 V		8.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND, f = 1 MHz,	See Figure 9	25°C	3 V		2.5		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 12	25°C	3 V		100		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 13	25°C	3 V		–84		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 14	25°C	3 V		–85		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 16	25°C	3 V		0.09		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V		0.01		µA
				Full				0.5	

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY(1)

V_+ = 2.25 V to 2.75, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{ON}	V_{NO} or V_{NC} = 1 V, I_{COM} = –10 mA,	Switch ON, See Figure 6	25°C	2.25 V		15	25	Ω
				Full				28	
ON-state resistance match between channels	Δr_{ON}	V_{NO} or V_{NC} = 1 V, I_{COM} = –10 mA,	Switch ON, See Figure 6	25°C	2.25 V		0.06	0.3	Ω
				Full				0.3	
ON-state resistance flatness	$r_{ON(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –10 mA,	Switch ON, See Figure 6	25°C	2.25 V		4		Ω
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 1.5 V, V_{COM} = 0.5 V to 1.5 V, or V_{NC} or V_{NO} = 1.5 V, V_{COM} = 1.5 V,	Switch OFF, See Figure 7	25°C	2.75 V	–300		300	pA
				Full		–1		1	nA
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 1.5 V, V_{COM} = 0.5 V to 1.5 V V_{NC} or V_{NO} = 1.5 V, V_{COM} = 1.5 V,	Switch ON, See Figure 8	25°C	2.75 V	–300		300	pA
				Full		–1		1	nA
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0.5 V, or V_{NC} or V_{NO} = Open, V_{COM} = 1.5 V,	Switch ON, See Figure 8	25°C	2.75 V	–300		300	pA
				Full		–1		1	nA
Digital Input (IN)									
Input logic high	V_{IH}			Full		2		5.5	V
Input logic low	V_{IL}			Full		0		0.4	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0 V		25°C	2.75 V	–0.05		0.05	µA
				Full		–0.05		0.05	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY (continued)

V_+ = 2.25 V to 2.75, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 10	25°C	2.5 V			18	ns
				Full	2.25 V to 2.75 V			20	
Turn-off time	t_{OFF}	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 10	25°C	2.5 V			8	ns
				Full	2.25 V to 2.75 V			9.5	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 11	25°C	2.5 V	1			ns
				Full		0.9			
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 15	25°C	2.5 V		4.5		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, f = 1 MHz,	Switch OFF, See Figure 9	25°C	2.5 V		3.5		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, f = 1 MHz,	Switch OFF, See Figure 9	25°C	2.5 V		8.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, f = 1 MHz,	Switch OFF, See Figure 9	25°C	2.5 V		8.5		pF
Digital input capacitance	C_i	V_I = V_+ or GND, f = 1 MHz,	See Figure 9	25°C	2.5 V		2.5		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 12	25°C	2.5 V		100		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 13	25°C	2.5 V		–84		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 14	25°C	2.5 V		–84		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 16	25°C	2.5 V		0.15		%
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.75 V		0.01		µA
				Full				0.5	

TYPICAL PERFORMANCE

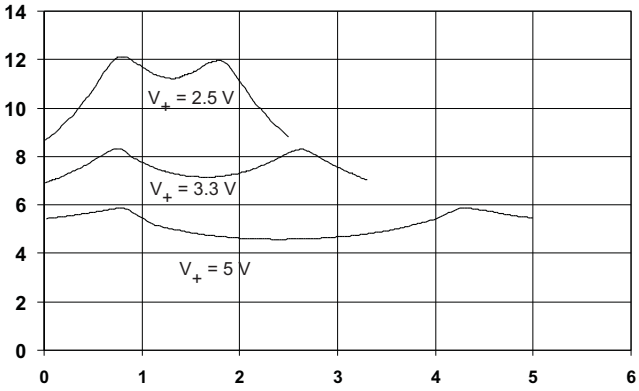


Figure 1. r_{ON} vs V_{IN}

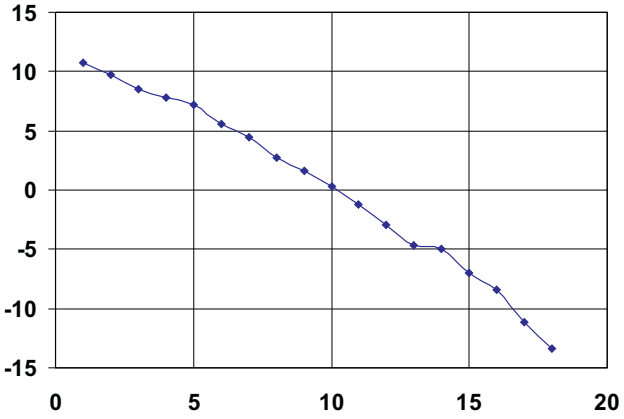


Figure 2. Charge Injection (Q_C) vs V_{COM}

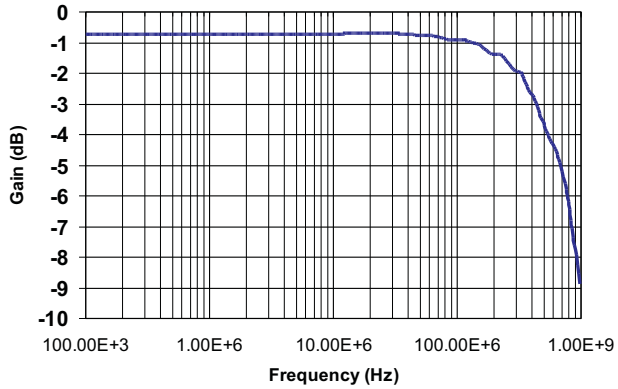


Figure 3. Bandwidth (V_+ = 3 V)

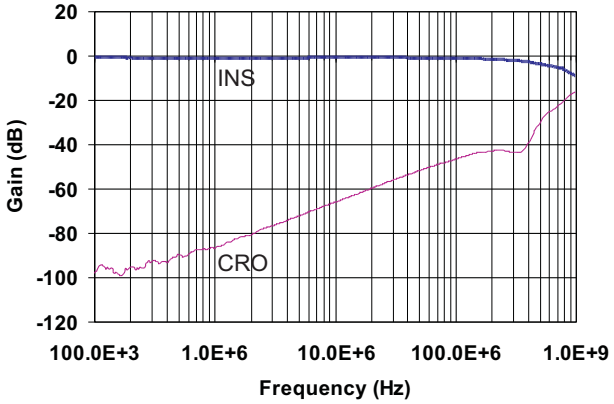


Figure 4. OFF Isolation vs Crosstalk (V_+ = 3 V)

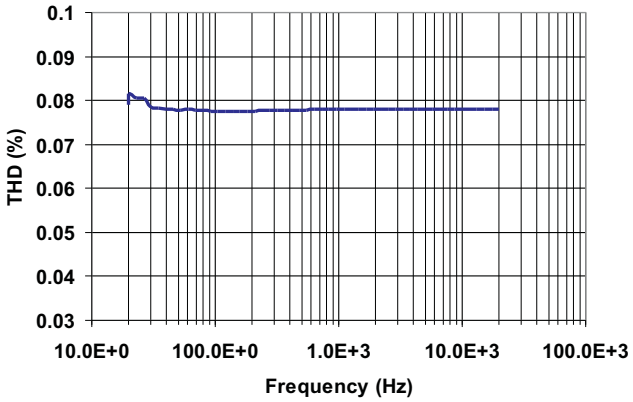


Figure 5. Total Harmonic Distortion vs Frequency

PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	IN	Digital control to connect COM to NO
2	V_+	Power supply
3	GND	Digital ground
4	NC	Normally closed
5	COM	Common
6	NO	Normally open

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{ON}	Resistance between COM and NC or COM and NO ports when the channel is ON
Δr_{ON}	Difference of r_{on} between channels
$r_{ON(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) being open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) being open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) being open
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at IN
I_{IH}, I_{IL}	Leakage current measured at IN
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM, NC, or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM, NC, or NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_O$, C_L is the load capacitance and ΔVO is the change in analog output voltage.

PARAMETER DESCRIPTION (continued)

SYMBOL	DESCRIPTION
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio or root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

PARAMETER MEASUREMENT INFORMATION

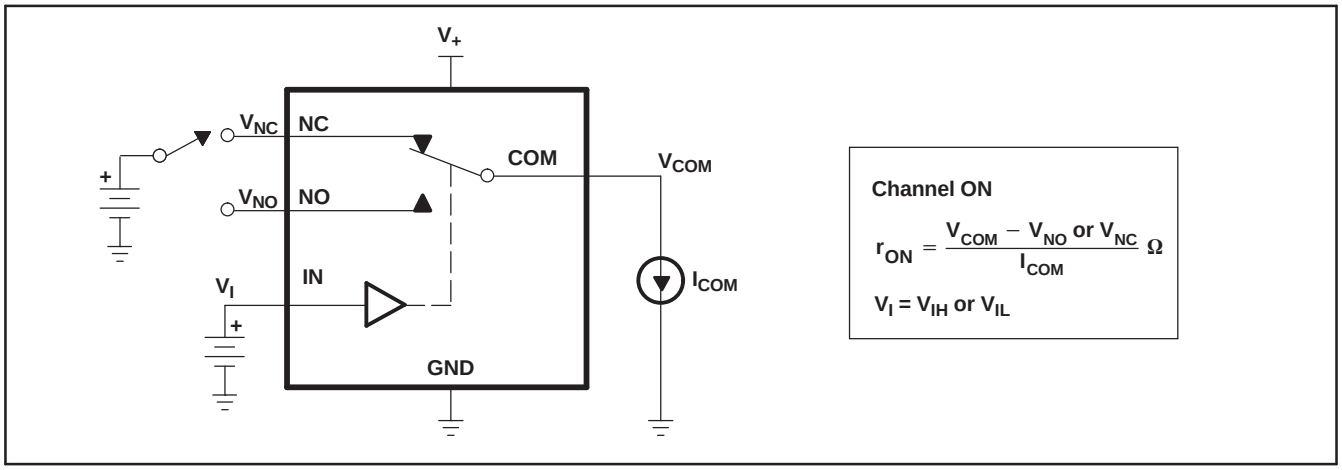


Figure 6. ON-State Resistance (r_{ON})

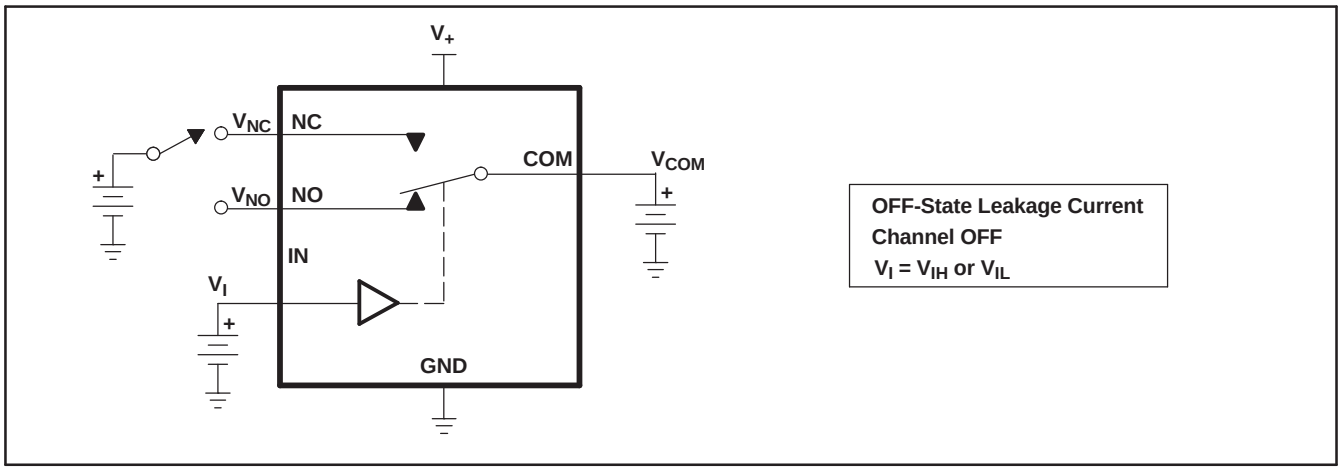


Figure 7. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

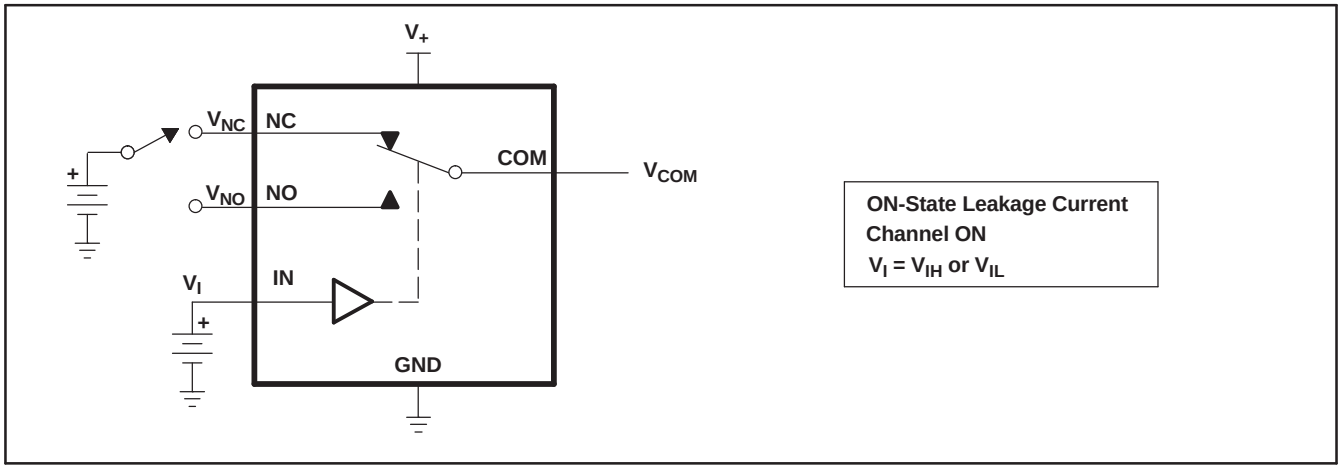


Figure 8. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

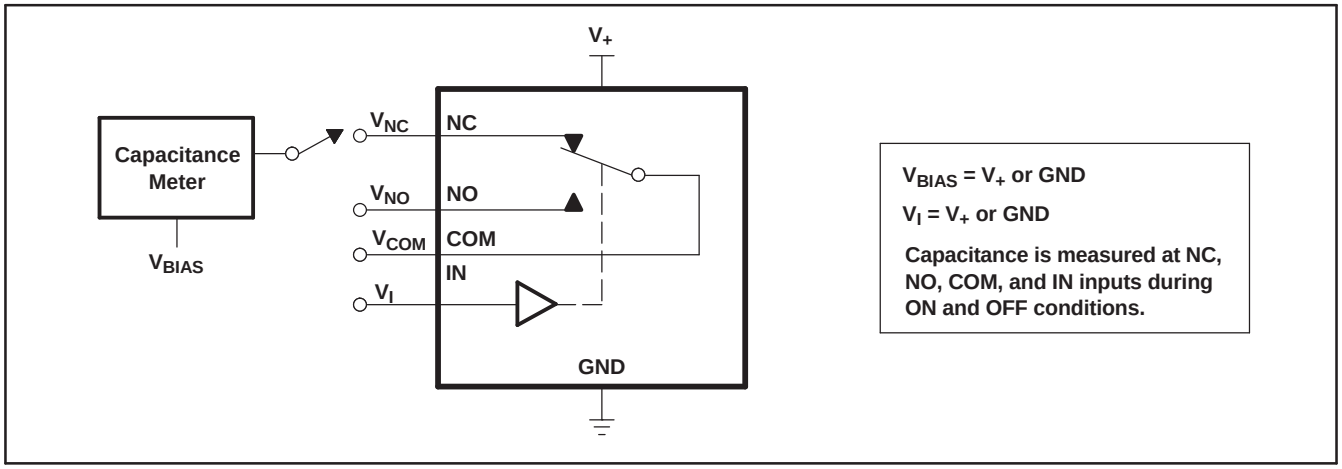
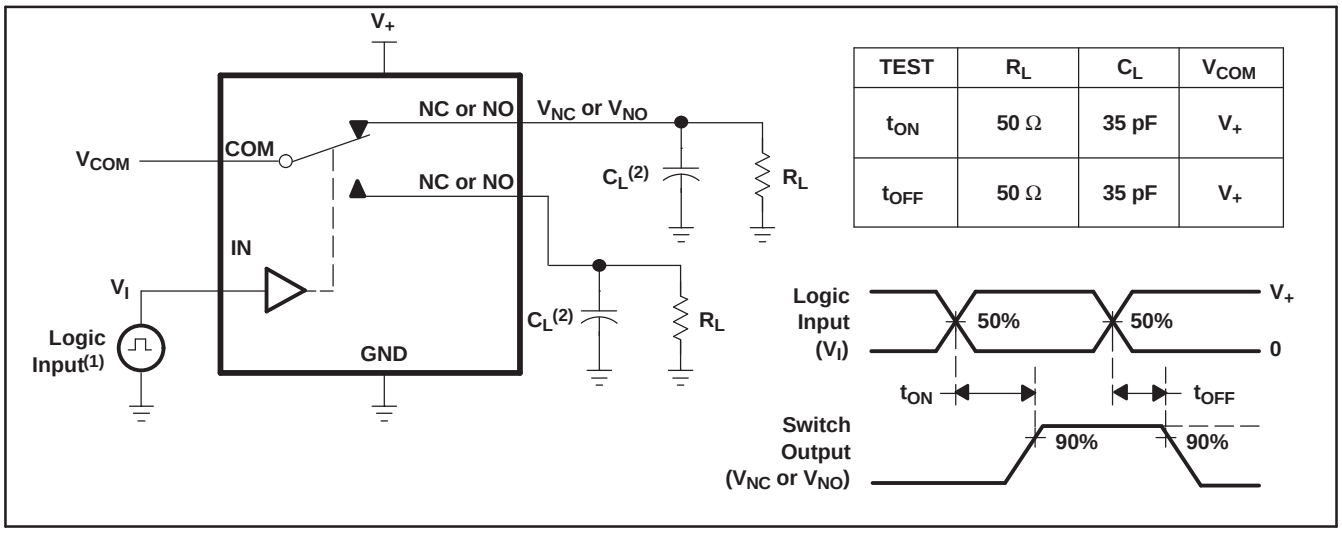


Figure 9. Capacitance (C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

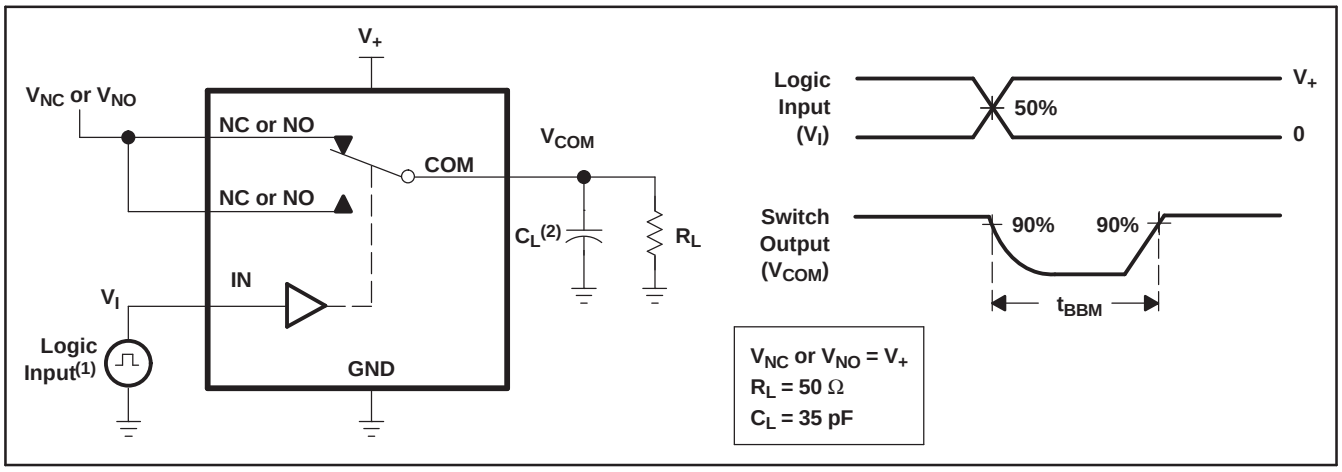


TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_+
t_{OFF}	50 Ω	35 pF	V_+

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 10. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 11. Break-Before-Make Time (t_{BBM})

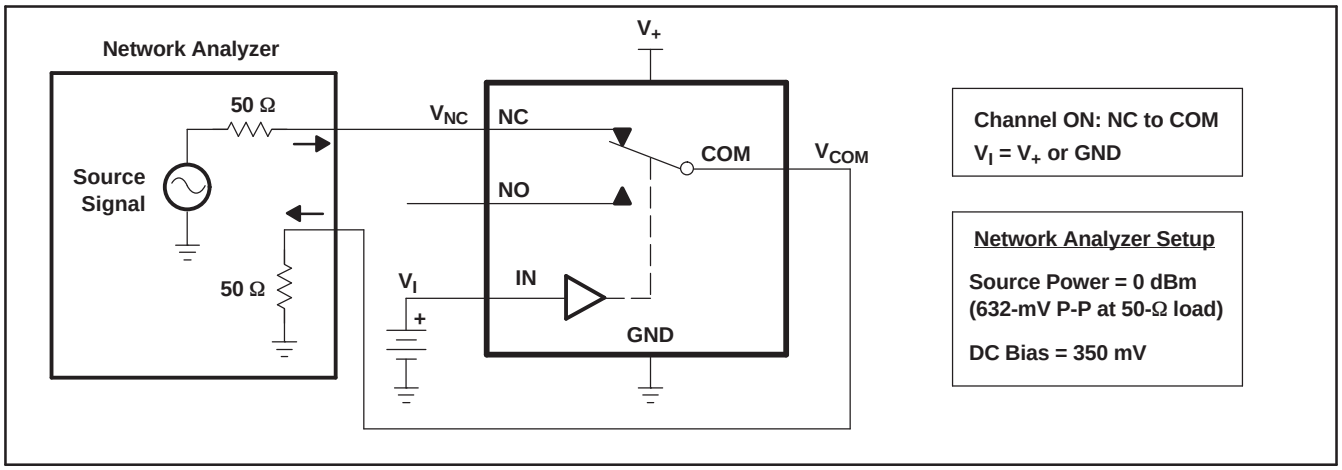


Figure 12. Bandwidth (BW)

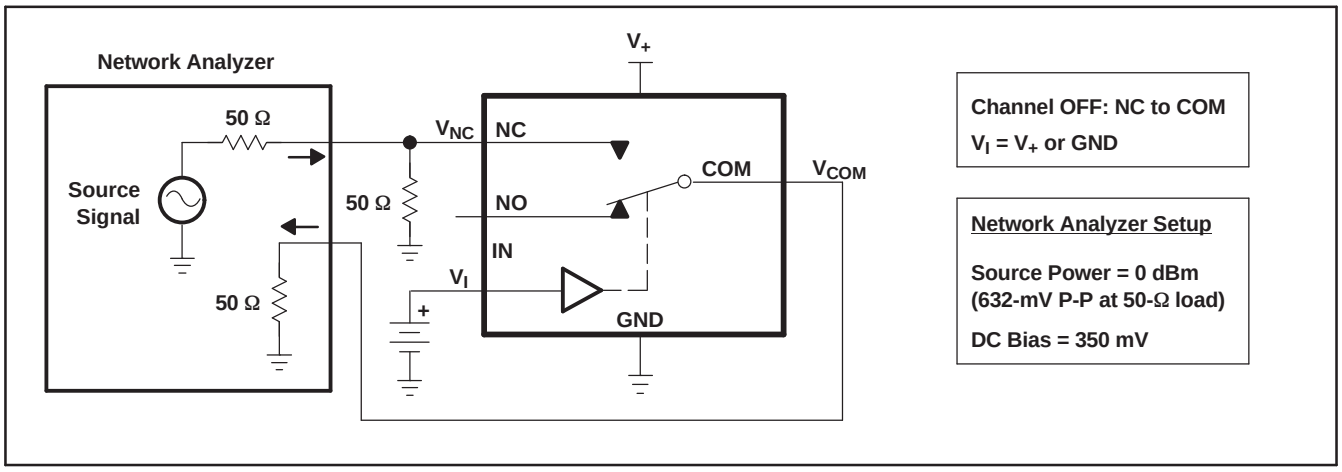


Figure 13. OFF Isolation (O_{ISO})

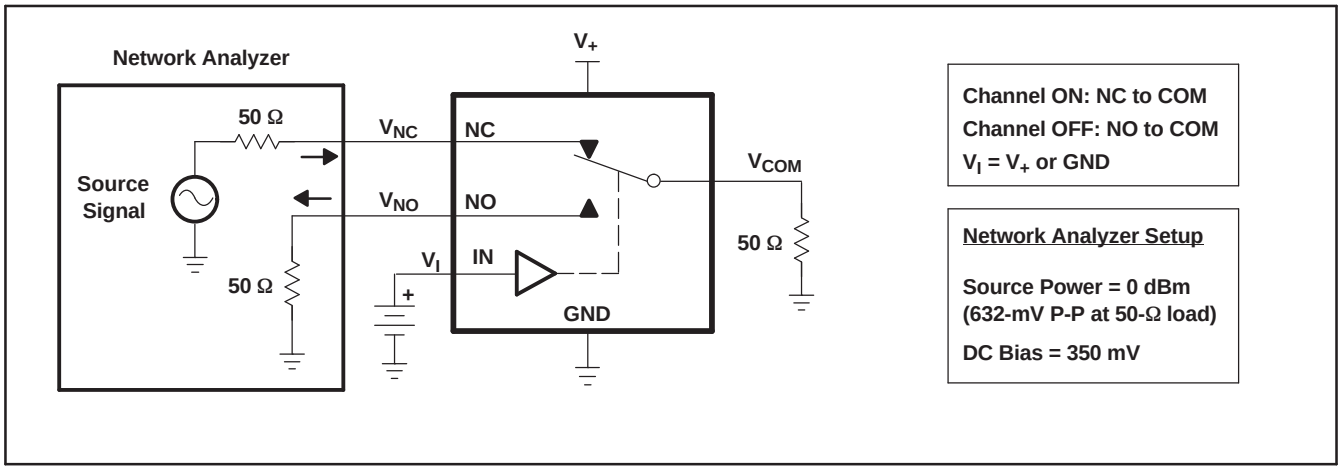
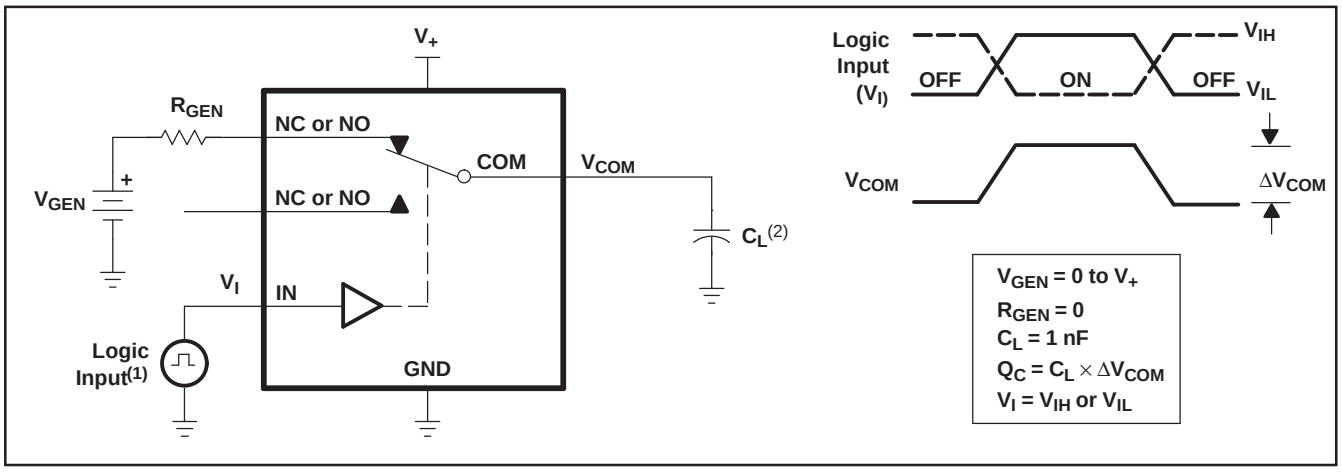


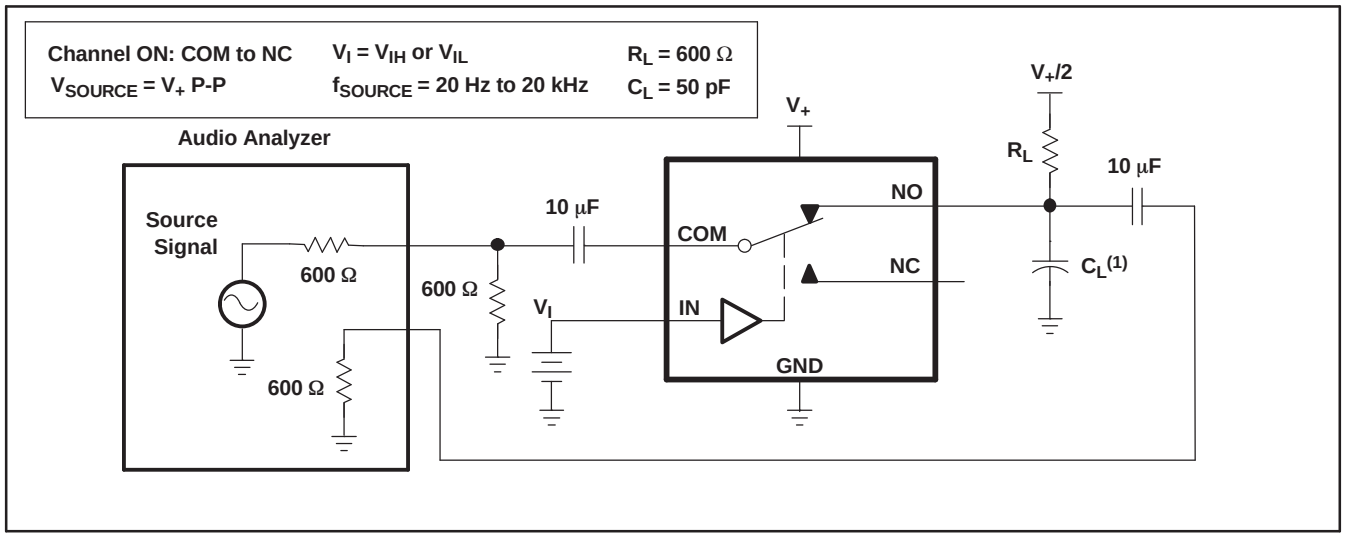
Figure 14. Crosstalk (X_{TALK})



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 15. Charge Injection (Q_C)



A. C_L includes probe and jig capacitance.

Figure 16. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A9411DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(32F ~ 32R)	Samples
TS5A9411DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(32F ~ 32R)	Samples
TS5A9411DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(32F ~ 32R)	Samples
TS5A9411DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(32F ~ 32R)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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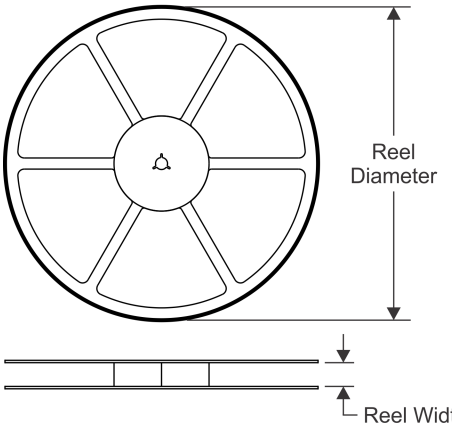
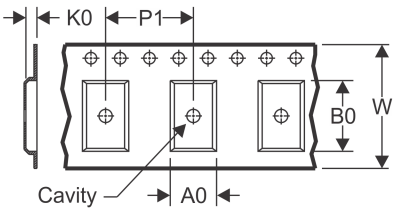
TAPE AND REEL INFORMATION

REEL DIMENSIONS

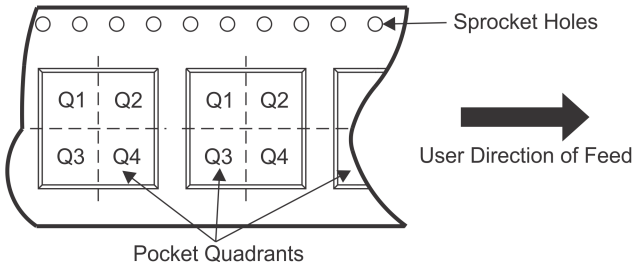


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

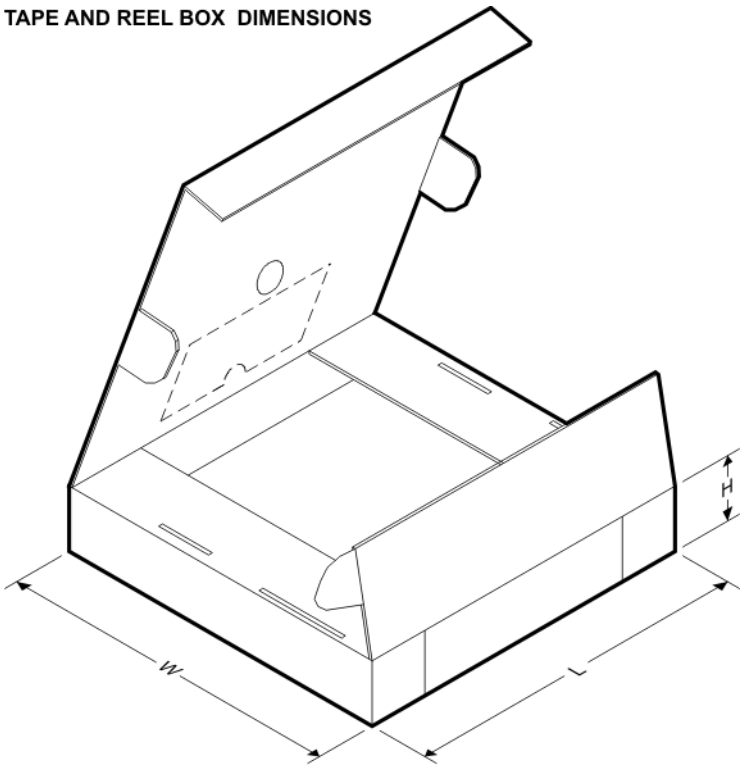
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A9411DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TS5A9411DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3

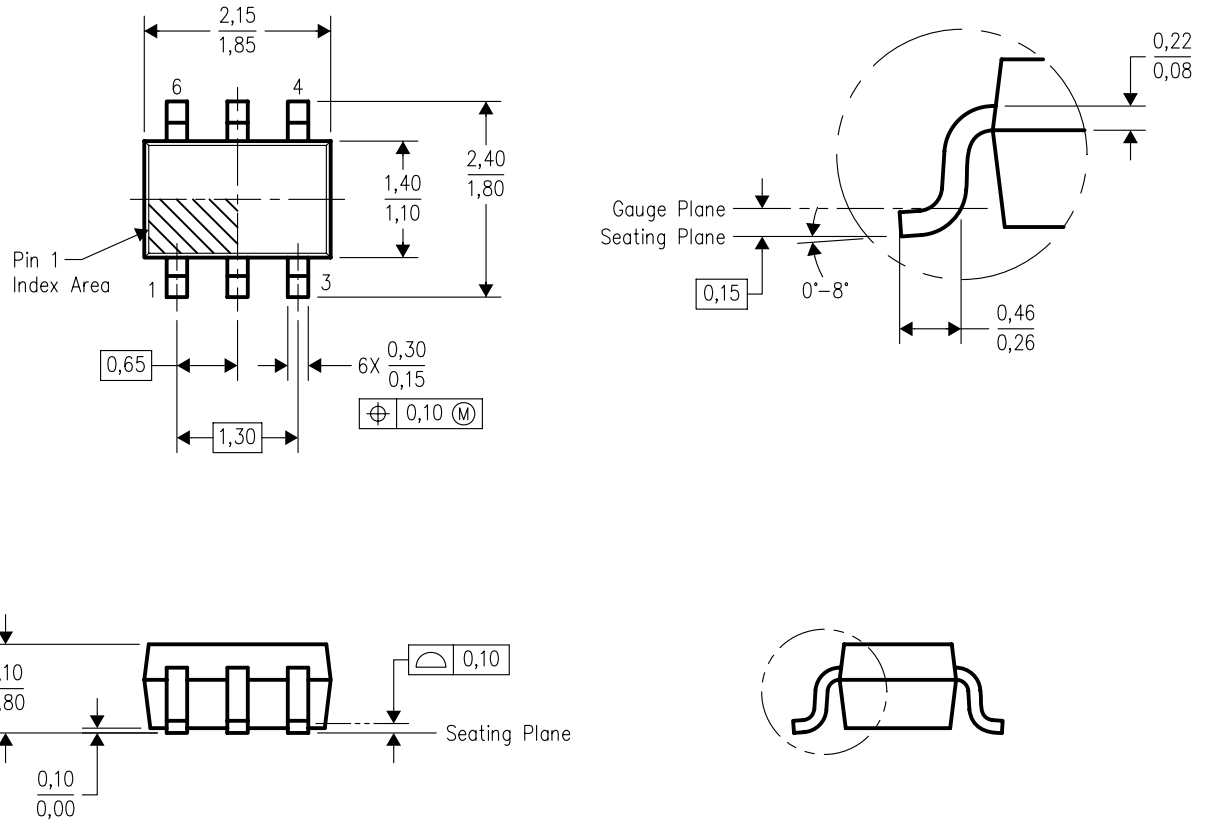
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A9411DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
TS5A9411DCKT	SC70	DCK	6	250	202.0	201.0	28.0

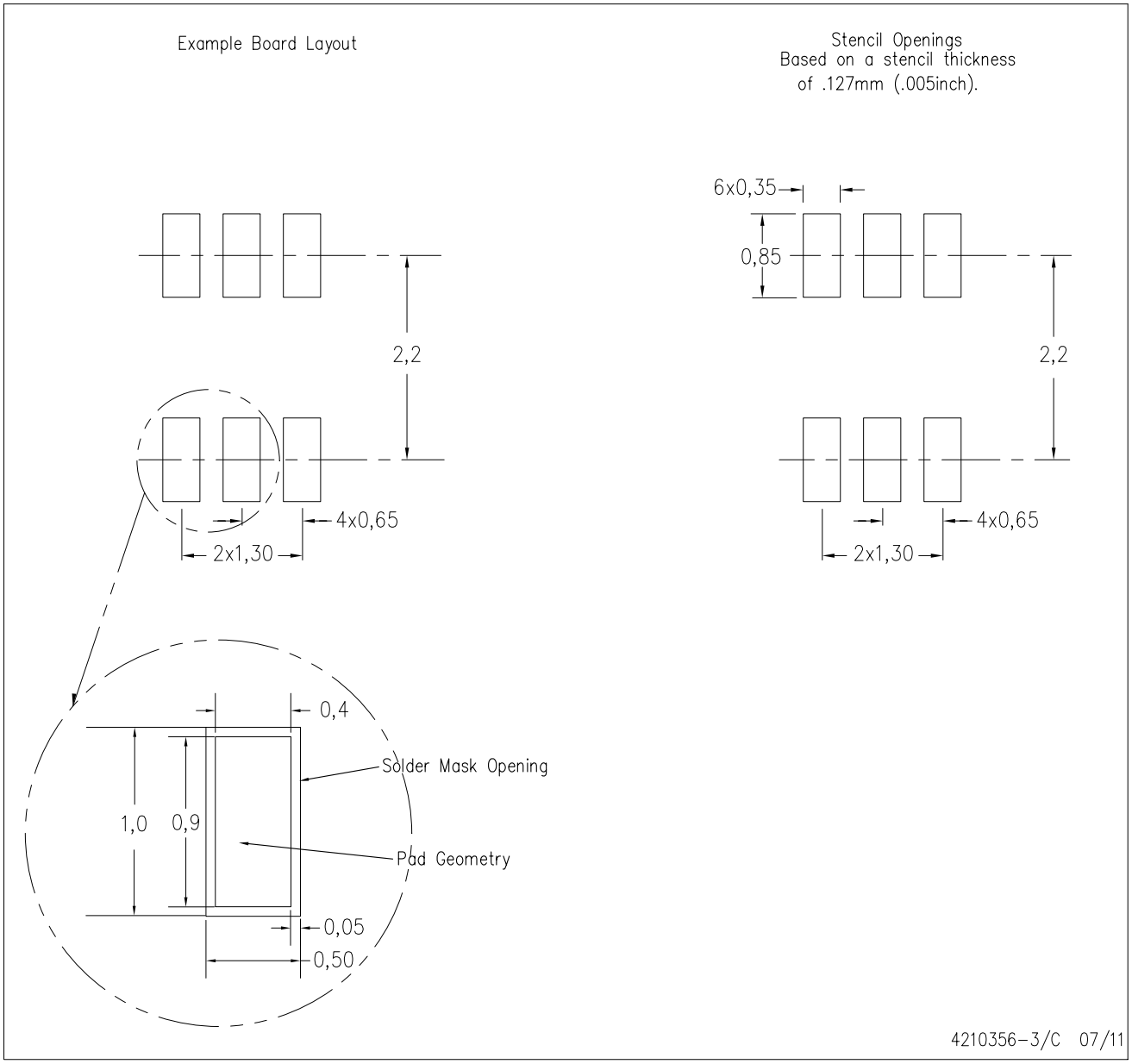
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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