0.9-Ω LOW-VOLTAGE SINGLE-SUPPLY QUAD SPST ANALOG SWITCH

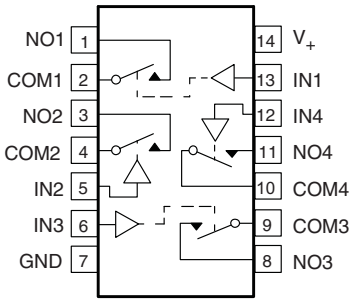
FEATURES

- Low ON-State Resistance (r_{ON})
  - 0.9 Ω Max (3-V Supply)
  - 1.5 Ω Max (1.8-V Supply)
- r_{ON} Flatness: 0.4 Ω Max (3-V)
- r_{ON} Matching
  - 0.05 Ω Max (3-V Supply)
  - 0.25 Ω Max (1.8-V Supply)
- 1.6-V to 3.6-V Single-Supply Operation
- 1.8-V CMOS Logic Compatible (3-V Supply)
- High Current-Handling Capacity (100 mA Continuous)
- Fast Switching: t_{ON} = 14 ns, t_{OFF} = 9 ns
- ESD Protection Exceeds JESD-22
  - 4000-V Human Body Model (A114-A)
  - 300-V Machine Model (A115-A)
  - 1000-V Charged Device Model (C101)

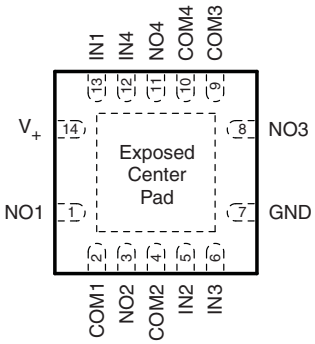
APPLICATIONS

- Power Routing
- Battery Powered Systems
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communications Circuits
- PCMCIA Cards
- Cellular Phones
- Modems
- Hard Drives

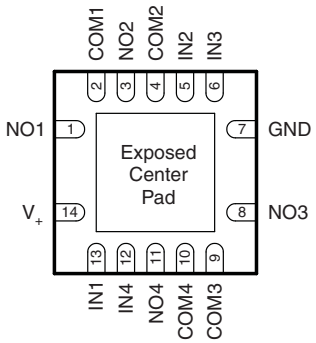
PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)

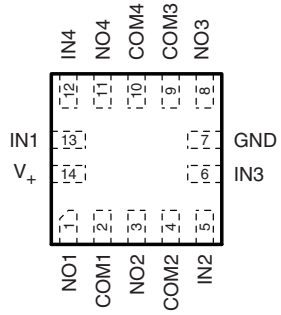


RGY PACKAGE
(BOTTOM VIEW)

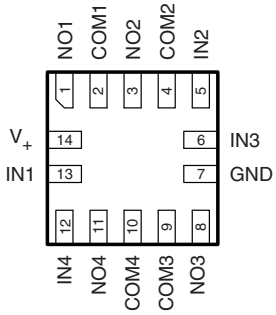


If the exposed center pad is used, it must be connected as a secondary ground or left electrically open.

RUC PACKAGE
(TOP VIEW)



RUC PACKAGE
(BOTTOM VIEW)



DESCRIPTION/ORDERING INFORMATION

The TS3A4751 is a low ON-state resistance (r_{on}), low-voltage, quad, single-pole/single-throw (SPST) analog switch that operates from a single 1.6-V to 3.6-V supply. This device has fast switching speeds, handles rail-to-rail analog signals, and consumes very low quiescent power.

The digital input is 1.8-V CMOS compatible when using a 3-V supply.

The TS3A4751 has four normally open (NO) switches. The TS3A4751 is available in a 14-pin thin shrink small-outline package (TSSOP) and in space-saving 14-pin SON (RGY) and micro QFN (RUC) packages.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SON – RGY	Reel of 2000	TS3A4751RGYR	YC751
	micro QFN – RUC	Reel of 2000	TS3A4751RUCR	3M
	TSSOP – PW	Reel of 2000	TS3A4751PWR	YC751

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLE

IN	NO TO COM, COM TO NO
L	OFF
H	ON

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range referenced to GND(2)		–0.3	4	V
V_{NO} V_{COM} V_{IN}	Analog and digital voltage range		–0.3	V_+ + 0.3	V
I_{NO} I_{COM}	On-state switch current	V_{NO}, V_{COM} = 0 to V_+	–100	100	mA
I_+ I_{GND}	Continuous current through V_+ or GND			±100	mA
	Peak current pulsed at 1 ms, 10% duty cycle	COM, $V_{I/O}$		±200	mA
T_A	Operating temperature range		–40	85	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Signals on COM or NO exceeding V_+ or GND are clamped by internal diodes. Limit forward diode current to maximum current rating.

PACKAGE THERMAL IMPEDANCE

				UNIT
θ_{JA}	Package thermal impedance(1)	PW package	88	°C/W
		RGY package	91.6	
		RUC package	216.7	

(1) The package thermal impedance is measured in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS FOR 3-V SUPPLY(1)(2)

V_+ = 2.7 V to 3.6 V, T_A = –40°C to 85°C, V_{IH} = 1.4 V, V_{IL} = 0.5 V (unless otherwise noted).

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	MIN	TYP(3)	MAX	UNIT
Analog Switch								
Analog signal range	V_{COM}, V_{NO}				0		V_+	V
ON-state resistance	r_{on}	V_+ = 2.7 V, I_{COM} = –100 mA, V_{NO} = 1.5 V		25°C		0.7	0.9	Ω
				Full			1.1	
ON-state resistance match between channels(4)	Δr_{on}	V_+ = 2.7 V, I_{COM} = –100 mA, V_{NO} = 1.5 V		25°C		0.03	0.05	Ω
				Full			0.15	
ON-state resistance flatness(5)	$r_{on(flat)}$	V_+ = 2.7 V, I_{COM} = –100 mA, V_{NO} = 1 V, 1.5 V, 2 V		25°C		0.23	0.4	Ω
				Full			0.5	
NO OFF leakage current(6)	$I_{NO(OFF)}$	V_+ = 3.6 V, V_{COM} = 0.3 V, 3 V, V_{NO} = 3 V, 0.3 V		25°C	–2	1	2	nA
				Full	–18		18	
COM OFF leakage current(6)	$I_{COM(OFF)}$	V_+ = 3.6 V, V_{COM} = 0.3 V, 3 V, V_{NO} = 3 V, 0.3 V		25°C	–2	1	2	nA
				Full	–18		18	
COM ON leakage current(6)	$I_{COM(ON)}$	V_+ = 3.6 V, V_{COM} = 0.3 V, 3 V, V_{NO} = 0.3 V, 3 V, or floating		25°C	–2.5	0.01	2.5	nA
				Full	–5		5	
Dynamic								
Turn-on time	t_{ON}	V_{NO} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 14		25°C		5	14	ns
				Full			15	
Turn-off time	t_{OFF}	V_{NO} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 14		25°C		4	9	ns
				Full			10	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, See Figure 15		25°C		3		pC
NO OFF capacitance	$C_{NO(OFF)}$	f = 1 MHz, See Figure 16		25°C		23		pF
COM OFF capacitance	$C_{COM(OFF)}$	f = 1 MHz, See Figure 16		25°C		20		pF
COM ON capacitance	$C_{COM(ON)}$	f = 1 MHz, See Figure 16		25°C		43		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON		25°C		125		MHz
OFF isolation(7)	O_{ISO}	R_L = 50 Ω, C_L = 5 pF, See Figure 17	f = 10 MHz	25°C		–40		dB
			f = 1 MHz			–62		
Crosstalk	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, See Figure 17	f = 10 MHz	25°C		–73		dB
			f = 1 MHz			–95		
Total harmonic distortion	THD	f = 20 Hz to 20 kHz, V_{COM} = 2 V_{P-P}	R_L = 32 Ω	25°C		0.04		%
			R_L = 600 Ω			0.003		
Digital Control Inputs (IN1–IN4)								
Input logic high	V_{IH}			Full	1.4			V
Input logic low	V_{IL}			Full			0.5	V
Input leakage current	I_{IN}	V_I = 0 or V_+		25°C		0.5	1	nA
				Full	–20		20	
Supply								
Power-supply range	V_+				1.6		3.6	V
Positive-supply current	I_+	V_+ = 3.6 V, V_{IN} = 0 or V_+		25°C			0.075	µA
				Full			0.75	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Parts are tested at 85°C and specified by design and correlation over the full temperature range.
(3) Typical values are at V_+ = 3 V, T_A = 25°C.
(4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$
(5) Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal ranges.
(6) Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at T_A = 25°C.
(7) OFF isolation = $20_{log}10$ (V_{COM}/V_{NO}), V_{COM} = output, V_{NO} = input to OFF switch

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY(1)(2)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C, V_{IH} = 1 V, V_{IL} = 0.4 V (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	MIN	TYP(3)	MAX	UNIT
Analog Switch								
Analog signal range	V_{COM}, V_{NO}				0		V_+	V
ON-state resistance	r_{on}	V_+ = 1.8 V, I_{COM} = –10 mA, V_{NO} = 0.9 V		25°C		1	1.5	Ω
				Full			2	
ON-state resistance match between channels(4)	Δr_{on}	V_+ = 1.8 V, I_{COM} = –10 mA, V_{NO} = 0.9 V		25°C		0.09	0.15	Ω
				Full			0.25	
ON-state resistance flatness(5)	$r_{on(flat)}$	V_+ = 1.8 V, I_{COM} = –10 mA, 0 ≤ V_{NO} ≤ V_+		25°C		0.7	0.9	Ω
				Full			1.5	
NO OFF leakage current(6)	$I_{NO(OFF)}$	V_+ = 1.95 V, V_{COM} = 0.15 V, 1.65 V, V_{NO} = 1.8 V, 0.15 V		25°C	–1	0.5	1	nA
				Full	–10		10	
COM OFF leakage current(6)	$I_{COM(OFF)}$	V_+ = 1.95 V, V_{COM} = 0.15 V, 1.65 V, V_{NO} = 1.65 V, 0.15 V		25°C	–1	0.5	1	nA
				Full	–10		10	
COM ON leakage current(6)	$I_{COM(ON)}$	V_+ = 1.95 V, V_{COM} = 0.15 V, 1.65 V, V_{NO} = 0.15 V, 1.65 V, or floating		25°C	–1	0.01	1	nA
				Full	–3		3	
Dynamic								
Turn-on time	t_{ON}	V_{NO} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 14		25°C		6	18	ns
				Full			20	
Turn-off time	t_{OFF}	V_{NO} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 14		25°C		5	10	ns
				Full			12	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, See Figure 15		25°C		3.2		pC
NO OFF capacitance	$C_{NO(OFF)}$	f = 1 MHz, See Figure 16		25°C		23		pF
COM OFF capacitance	$C_{COM(OFF)}$	f = 1 MHz, See Figure 16		25°C		20		pF
COM ON capacitance	$C_{COM(ON)}$	f = 1 MHz, See Figure 16		25°C		43		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON		25°C		123		MHz
OFF isolation(7)	O_{ISO}	R_L = 50 Ω, C_L = 5 pF, See Figure 17	f = 10 MHz	25°C		–61		dB
			f = 100 MHz			–36		
Crosstalk	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, See Figure 17	f = 10 MHz	25°C		–95		dB
			f = 100 MHz			–73		
Total harmonic distortion	THD	f = 20 Hz to 20 kHz, V_{COM} = 2 V_{P-P}	R_L = 32 Ω	25°C		0.14		%
			R_L = 600 Ω			0.013		
Digital Control Inputs (IN1–IN4)								
Input logic high	V_{IH}			Full	1			V
Input logic low	V_{IL}			Full			0.4	V
Input leakage current	I_{IN}	V_I = 0 or V_+		25°C		0.1	5	nA
				Full	–10		10	
Supply								
Power-supply range	V_+				1.6		3.6	V
Positive-supply current	I_+	V_I = 0 or V_+		25°C			0.05	µA
				Full			0.5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Parts are tested at 85°C and specified by design and correlation over the full temperature range.
(3) Typical values are at T_A = 25°C.
(4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$
(5) Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal ranges.
(6) Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at T_A = 25°C.
(7) OFF isolation = $20_{log}10$ (V_{COM}/V_{NO}), V_{COM} = output, V_{NO} = input to OFF switch

TYPICAL PERFORMANCE

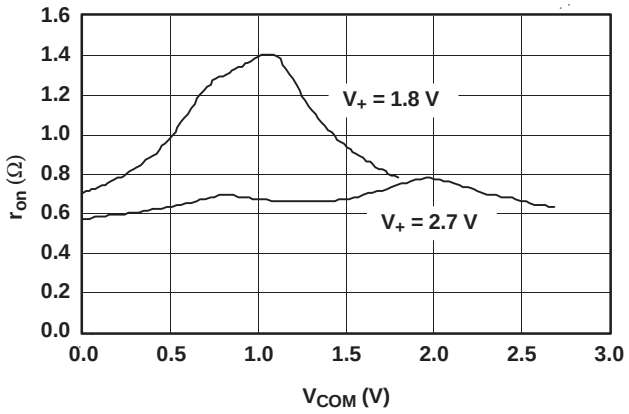


Figure 1. r_{on} vs V_{COM}

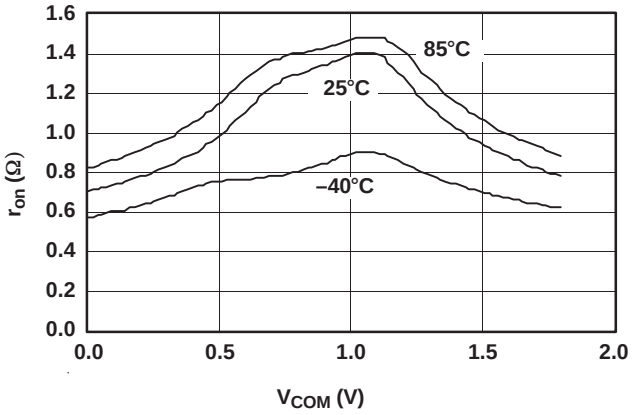


Figure 2. r_{on} vs V_{COM} (V_+ = 1.8 V)

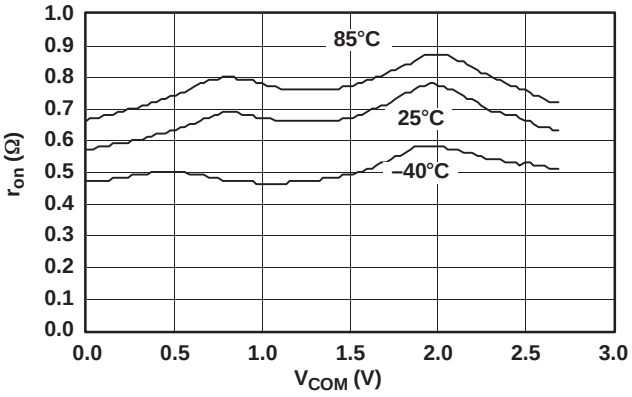


Figure 3. r_{on} vs V_{COM} (V_+ = 2.7 V)

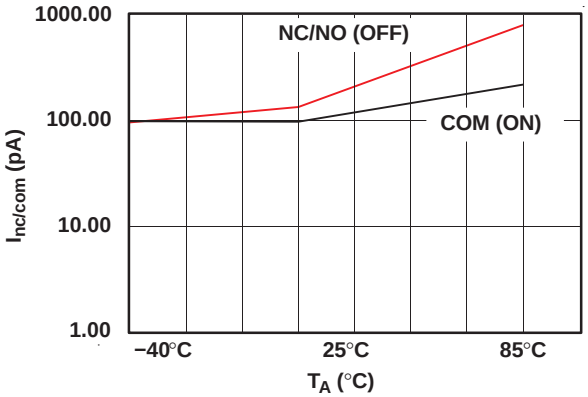


Figure 4. I_{ON} and I_{OFF} vs Temperature (V_+ = 3.6 V)

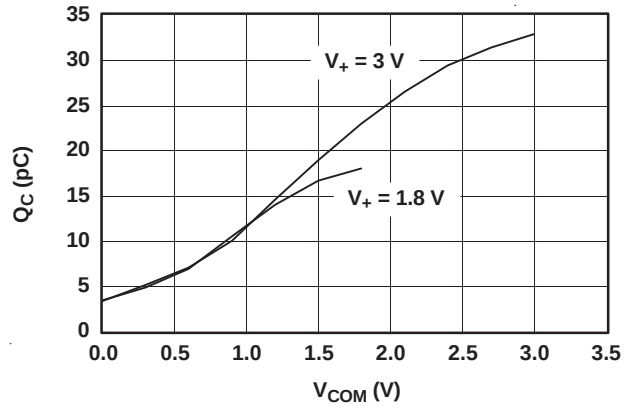


Figure 5. Q_C vs V_{COM}

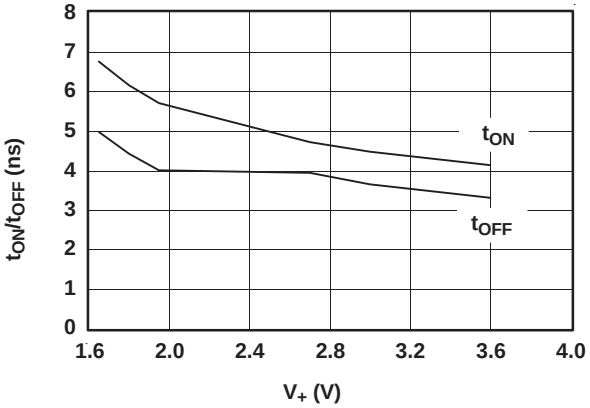


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

TYPICAL PERFORMANCE (continued)

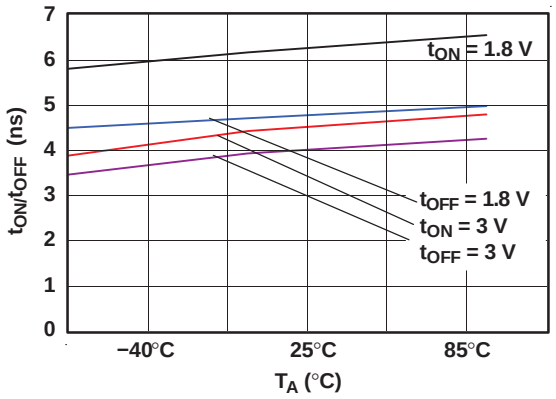


Figure 7. t_{ON} and t_{OFF} vs Temperature

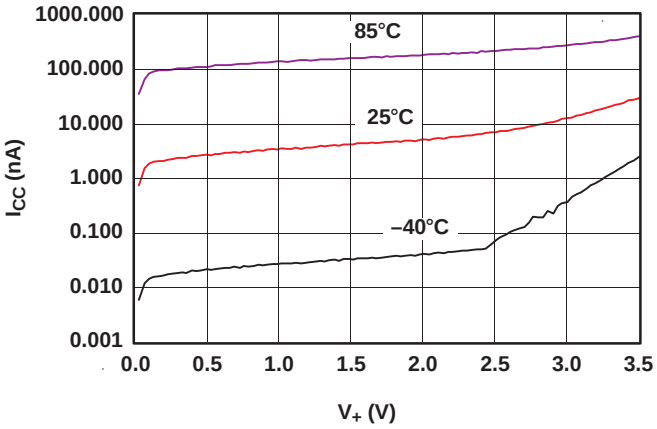


Figure 8. I_{CC} vs V_+

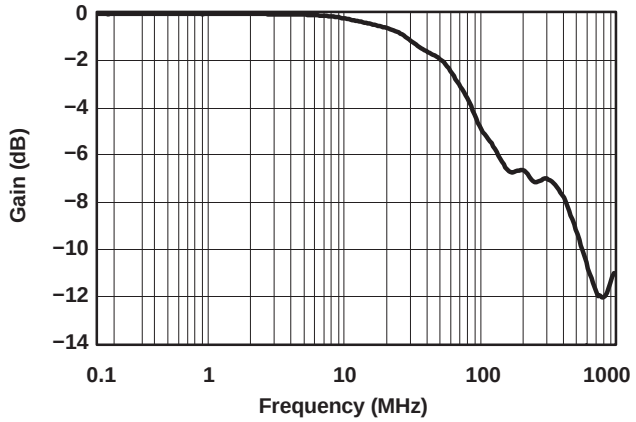


Figure 9. Gain vs Frequency (V_+ = 3 V)

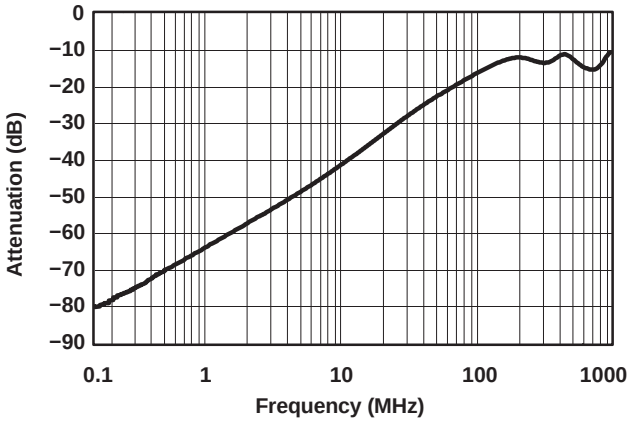


Figure 10. OFF Isolation vs Frequency (V_+ = 3 V)

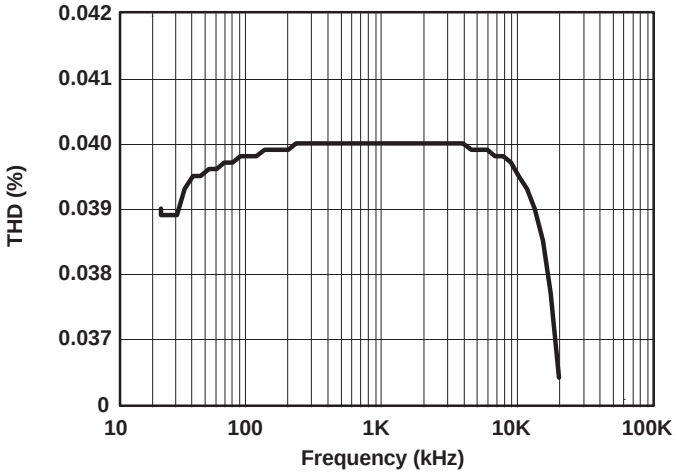


Figure 11. Total Harmonic Distortion vs Frequency (R_L = 32 Ω)

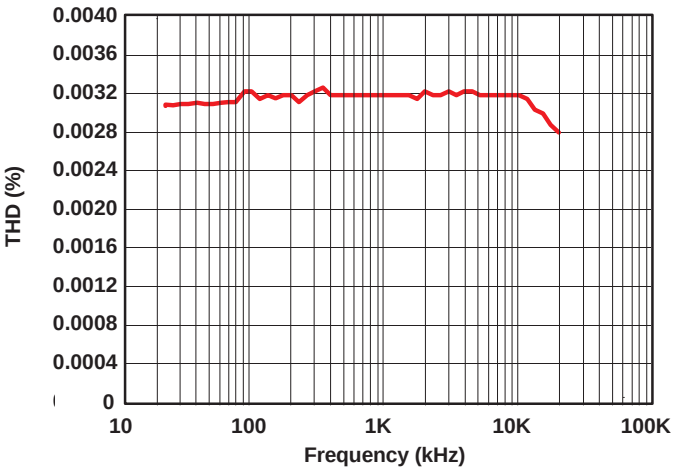


Figure 12. Total Harmonic Distortion vs Frequency (R_L = 600 Ω)

TYPICAL PERFORMANCE (continued)

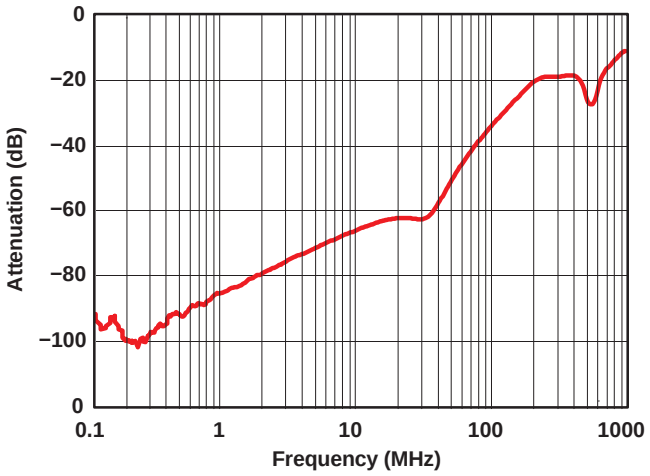


Figure 13. Crosstalk vs Frequency (V_+ = 3 V)

PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1, 3, 8, 11	NO1, NO2, NO3, NO4	Normally open
2, 4, 9, 10	COM1, COM2, COM3, COM4	Common
7	GND	Ground
13, 5, 6, 12	IN1, IN2, IN3, IN4	Logic control inputs
14	V_+	Positive supply voltage

APPLICATION INFORMATION

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_+ on first, followed by NO or COM.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_+ supply to other components. A 0.1-µF capacitor, connected from V_+ to GND, is adequate for most applications.

Logic Inputs

The TS3A4751 logic inputs can be driven up to 3.6 V, regardless of the supply voltage. For example, with a 1.8-V supply, IN may be driven low to GND and high to 3.6 V. Driving IN rail to rail minimizes power consumption.

Analog Signal Levels

Analog signals that range over the entire supply voltage (V_+ to GND) can be passed with very little change in r_{on} (see Typical Operating Characteristics). The switches are bidirectional, so NO and COM can be used as either inputs or outputs.

Layout

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

TEST CIRCUITS/TIMING DIAGRAMS

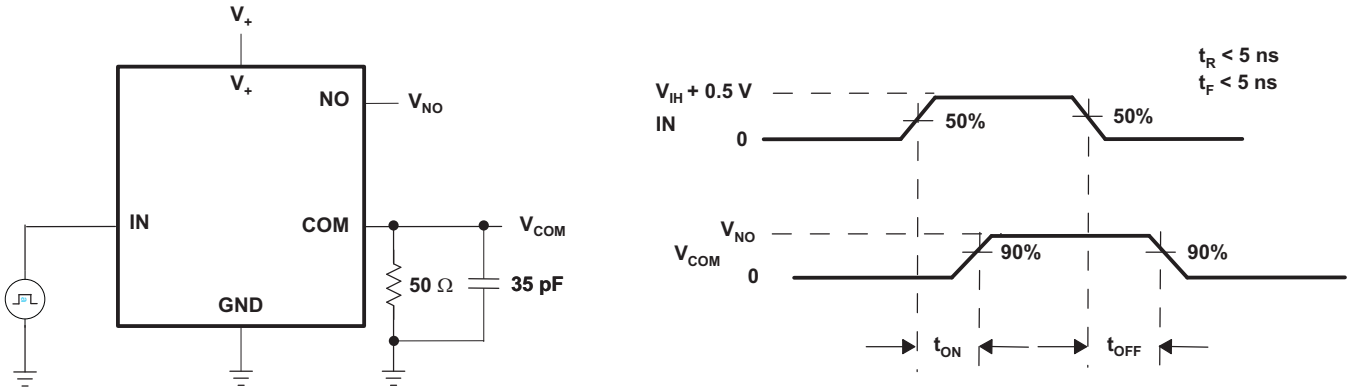


Figure 14. Switching Times

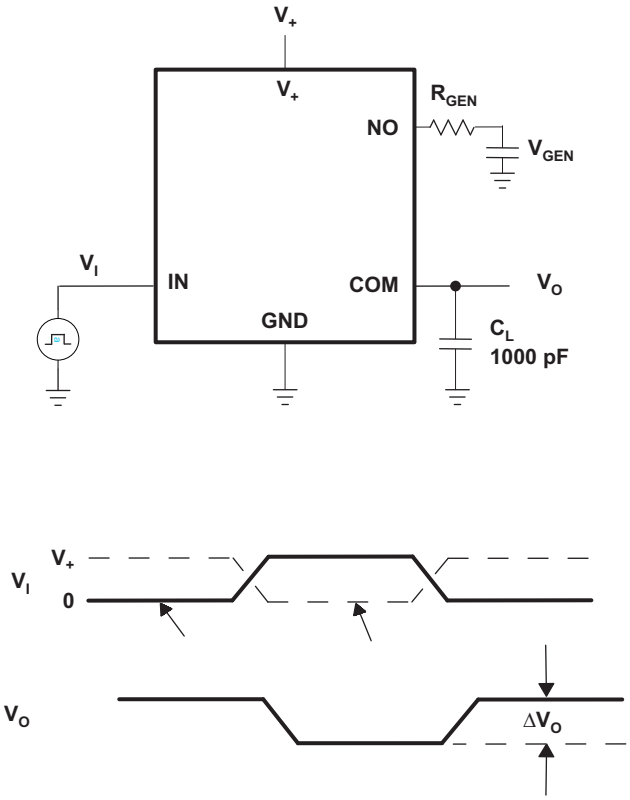


Figure 15. Charge Injection (Q_C)

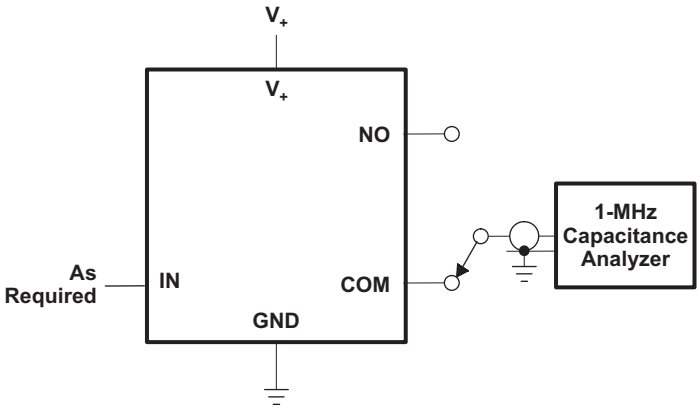
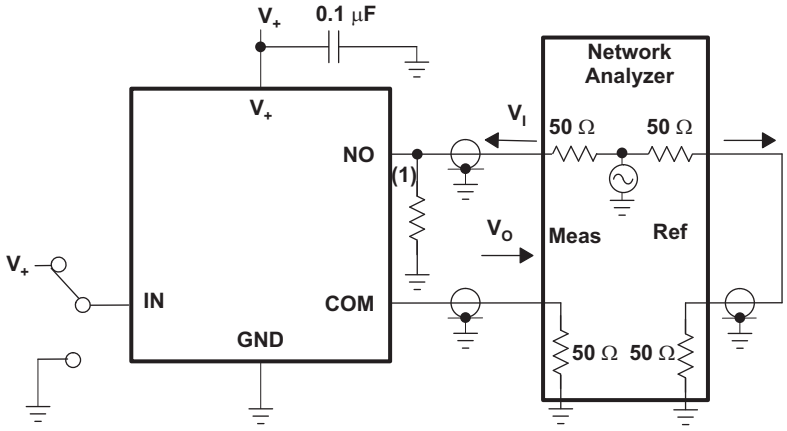


Figure 16. NO and COM Capacitance

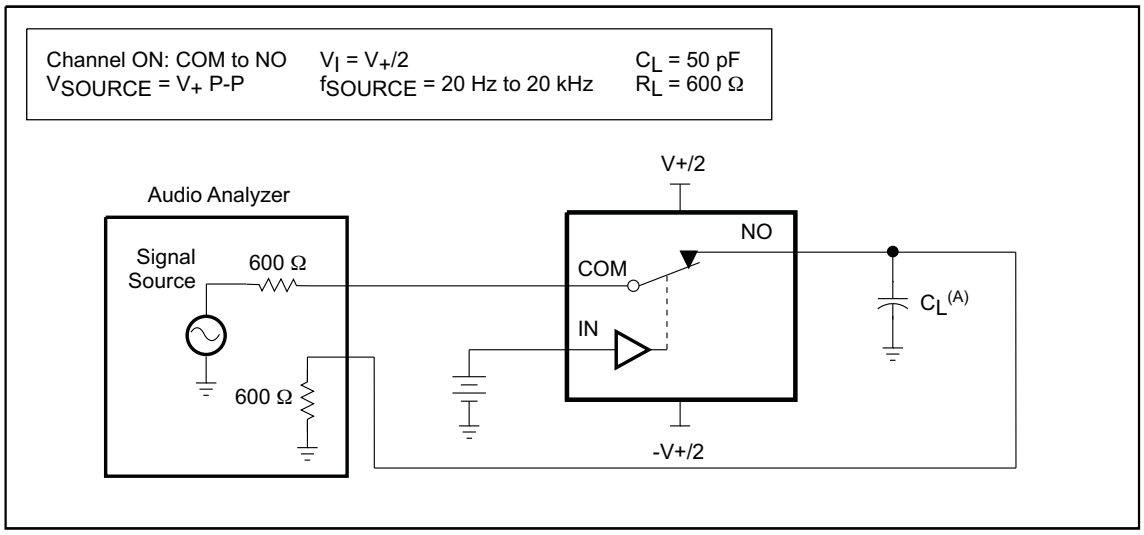


Measurements are standardized against short at socket terminals. OFF isolation is measured between COM and OFF terminals on each switch. Bandwidth is measured between COM and ON terminals on each switch. Signal direction through switch is reversed; worst values are recorded.

OFF isolation = 20 log V_O/V_I

(1) Add 50-Ω termination for OFF isolation

Figure 17. OFF Isolation, Bandwidth, and Crosstalk



A. C_L includes probe and jig capacitance.

Figure 18. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A4751PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YC751	Samples
TS3A4751PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YC751	Samples
TS3A4751RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YC751	Samples
TS3A4751RGYRG4	ACTIVE	VQFN	RGY	14		TBD	Call TI	Call TI	-40 to 85		Samples
TS3A4751RUCR	ACTIVE	QFN	RUC	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3MO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

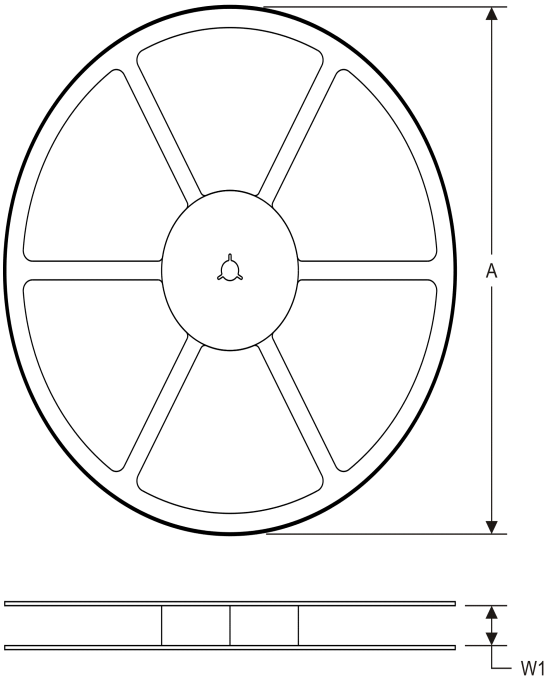
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

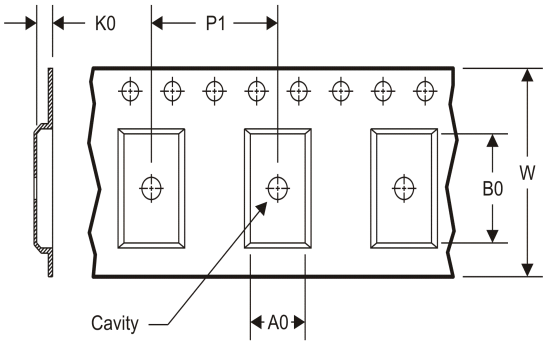
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



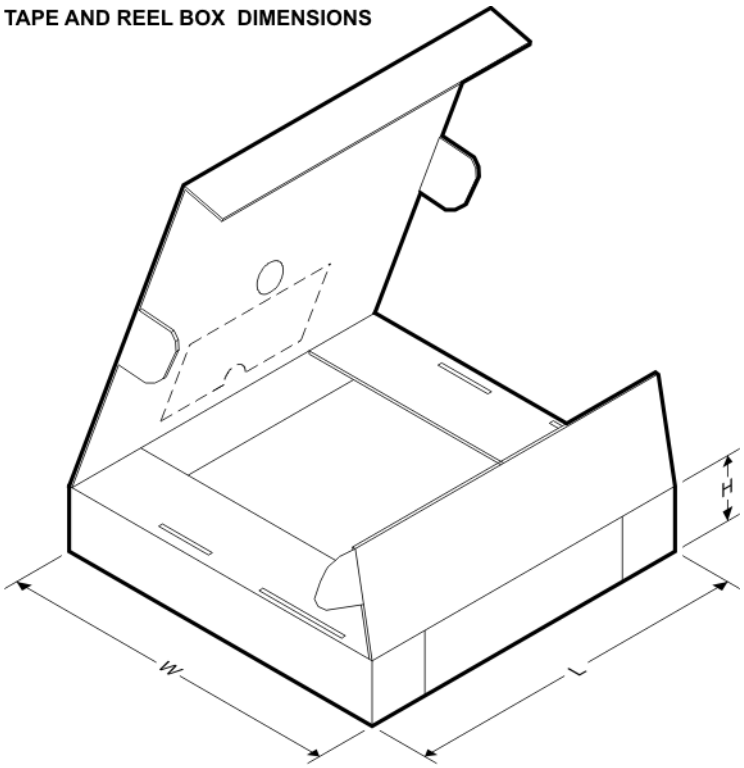
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A4751PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3A4751RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TS3A4751RUCR	QFN	RUC	14	3000	179.0	8.4	2.25	2.25	0.55	4.0	8.0	Q2

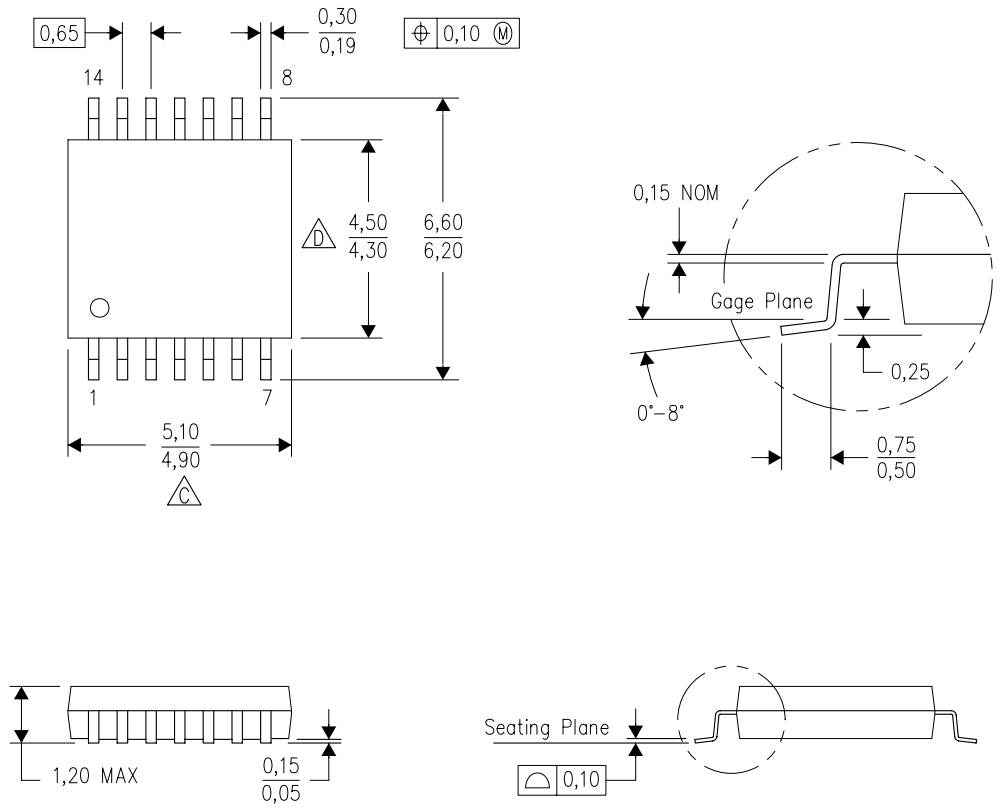
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A4751PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TS3A4751RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0
TS3A4751RUCR	QFN	RUC	14	3000	203.0	203.0	35.0

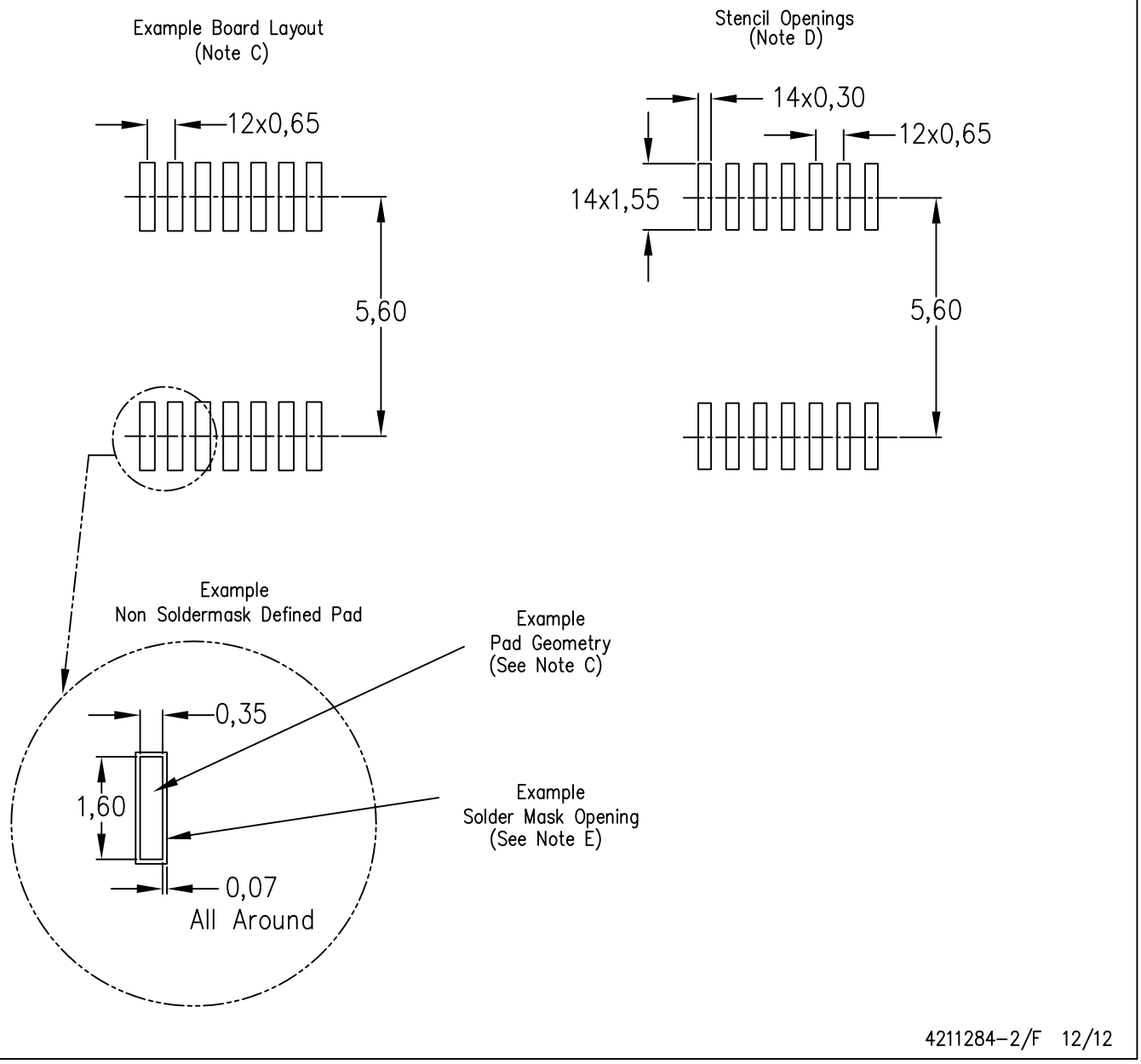
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

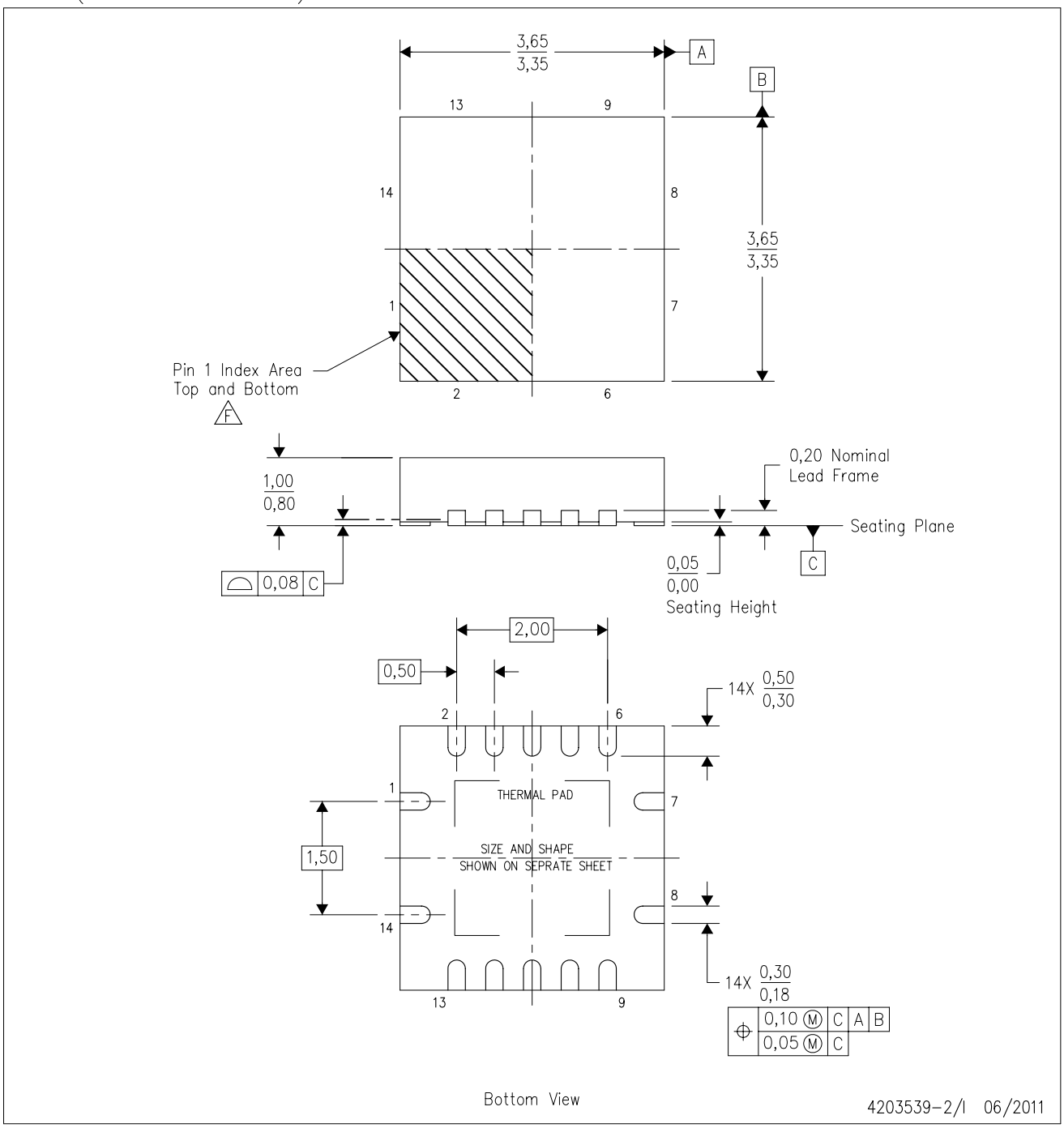
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

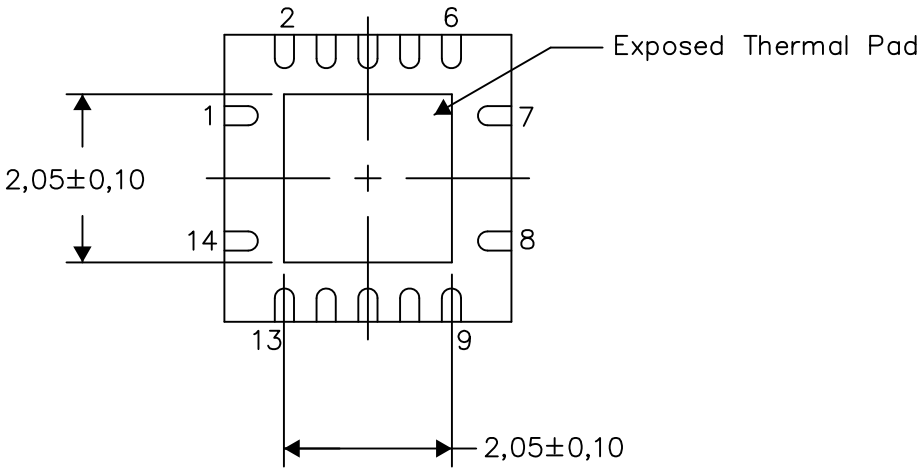
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



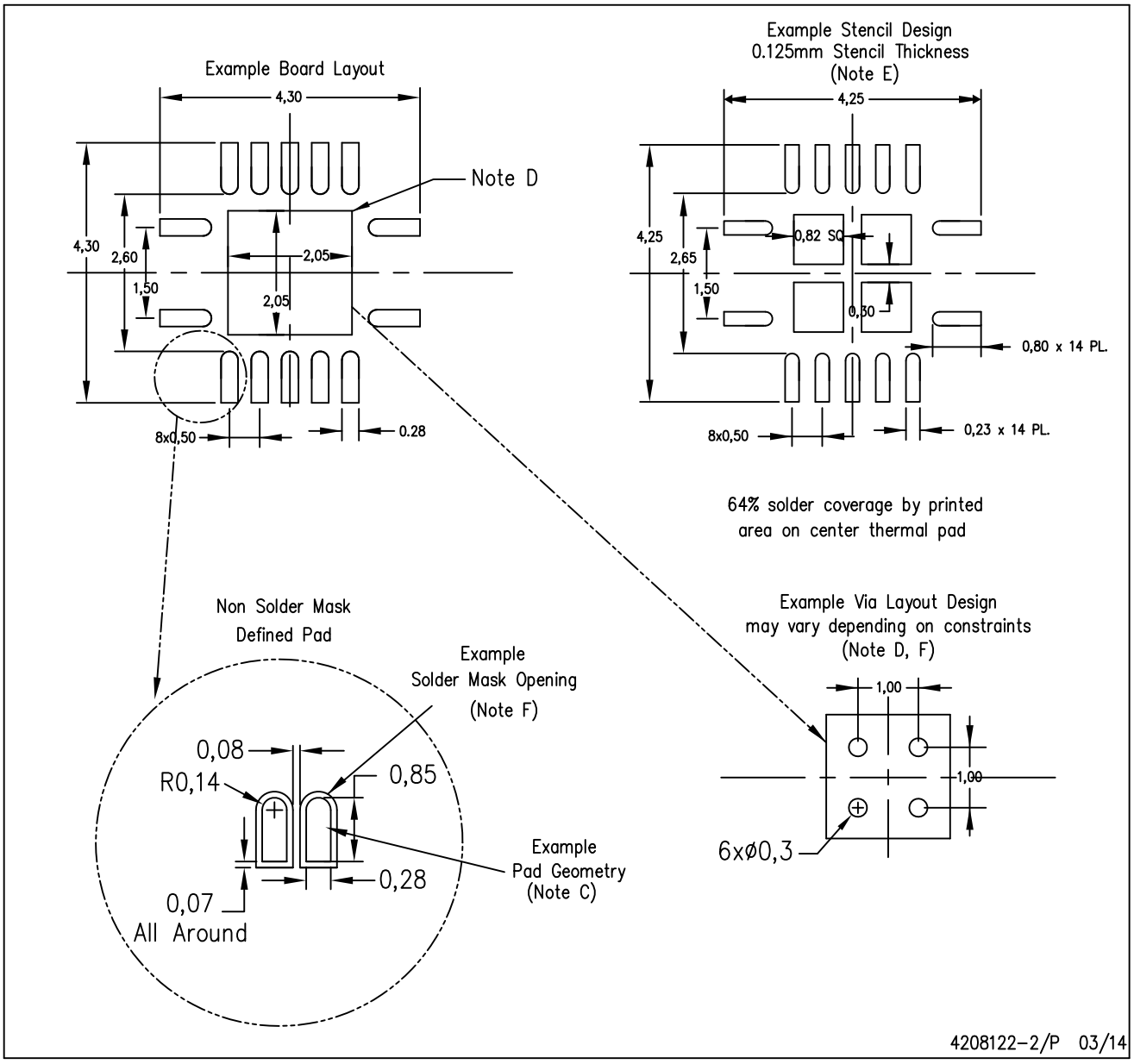
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

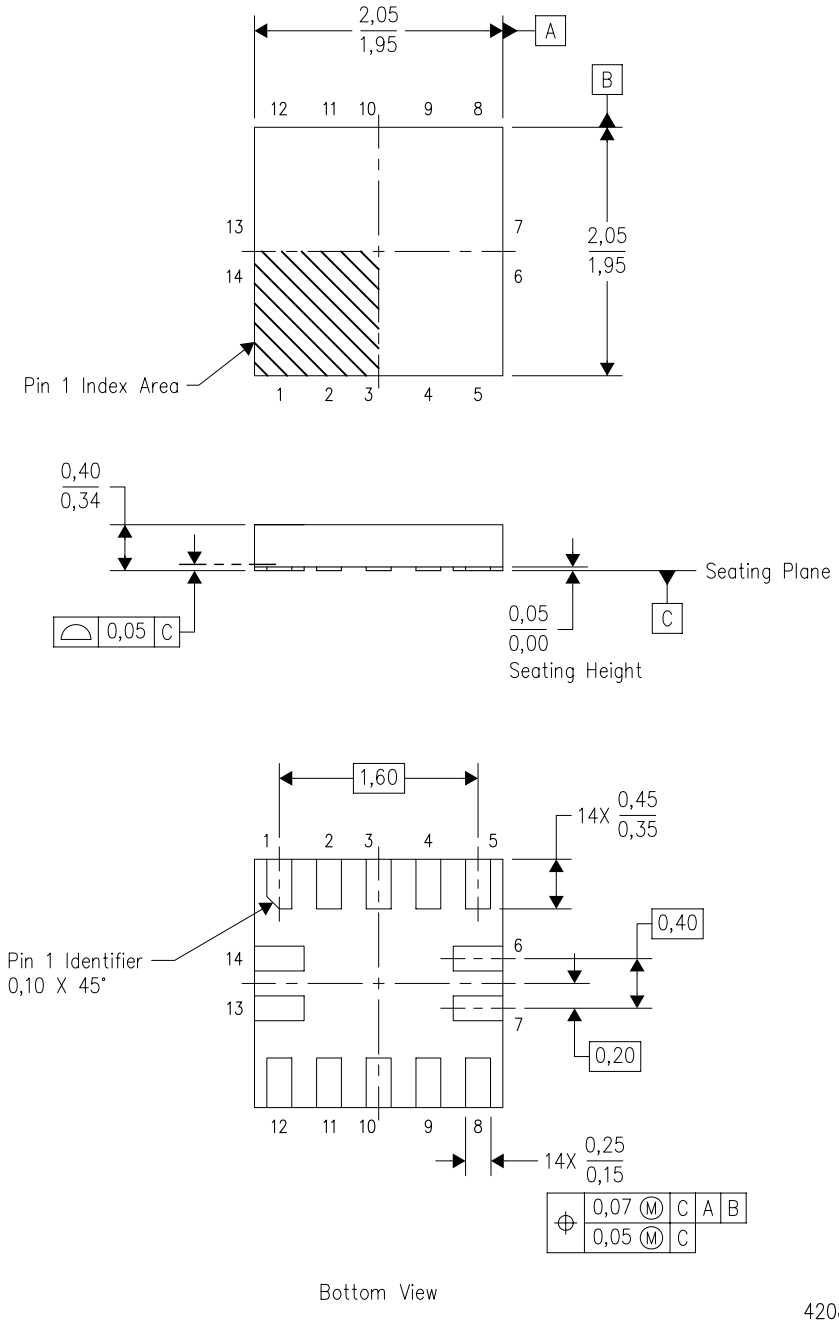
NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RUC (S–PX2QFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

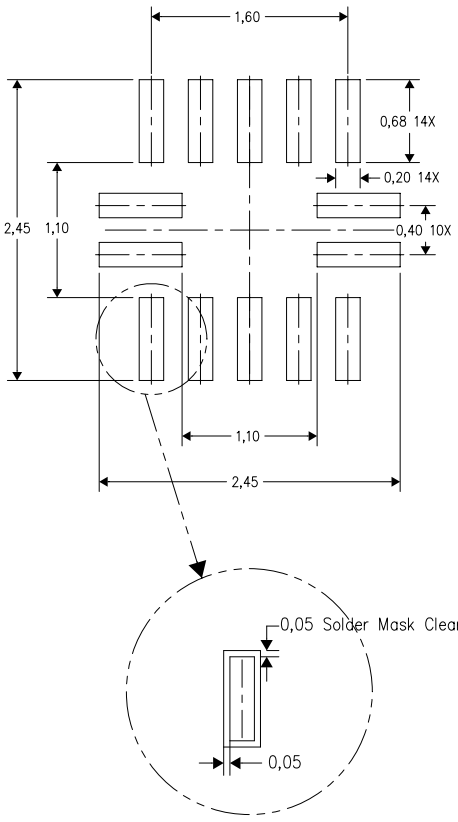


4208447/C 08/2008

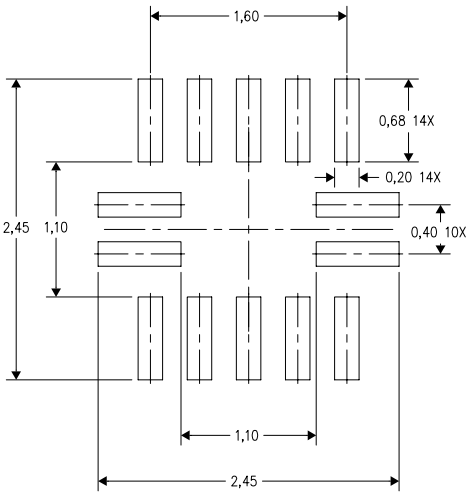
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2GFE.

RUC (S–PX2QFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)



Note D

4211124/A 06/10

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Texas Instruments:

TS3A4751PWR TS3A4751PWRG4 TS3A4751RGYR TS3A4751RGYRG4 TS3A4751RUCR