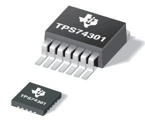


1.5A Ultra-LDO with Programmable Sequencing

FEATURES

- **Track Pin Allows for Flexible Power-Up Sequencing**
- **1% Accuracy Over Line, Load, and Temperature**
- **Supports Input Voltages as Low as 0.9V with External Bias Supply**
- **Adjustable Output (0.8V to 3.6V)**
- **Ultra-Low Dropout: 55mV at 1.5A (typ)**
- **Stable with Any or No Output Capacitor**
- **Excellent Transient Response**
- **Available in 5mm × 5mm × 1mm QFN and DDPAK-7 Packages**
- **Open-Drain Power-Good (5 × 5 QFN)**
- **Active High Enable**

APPLICATIONS

- **FPGA Applications**
- **DSP Core and I/O Voltages**
- **Post-Regulation Applications**
- **Applications with Special Start-Up Time or Sequencing Requirements**

DESCRIPTION

The TPS74301 low-dropout (LDO) linear regulator provides an easy-to-use robust power management solution for a wide variety of applications. The TRACK pin allows the output to track an external supply. This feature is useful in minimizing the stress on ESD structures that are present between the CORE and I/O power pins of many processors. The enable input and power-good output allow easy sequencing with external regulators. This complete flexibility allows the user to configure a solution that meets the sequencing requirements of FPGAs, DSPs, and other applications with special start-up requirements.

A precision reference and error amplifier deliver 1% accuracy over load, line, temperature, and process. Each LDO is stable with low-cost ceramic output capacitors and the device is fully specified from –40°C to +125°C. The TPS74301 is offered in a small (5mm × 5mm) QFN package, yielding a highly compact total solution size. For applications that require additional power dissipation, the DDPAK (KTW) package is also available.

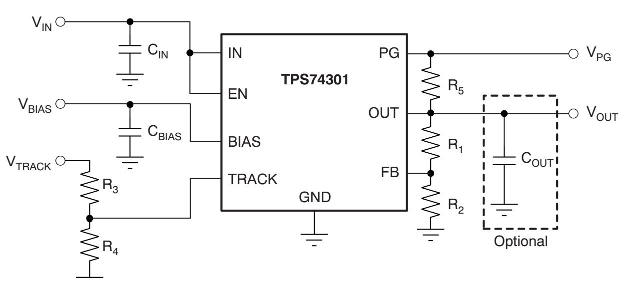


Figure 1. Typical Application Circuit

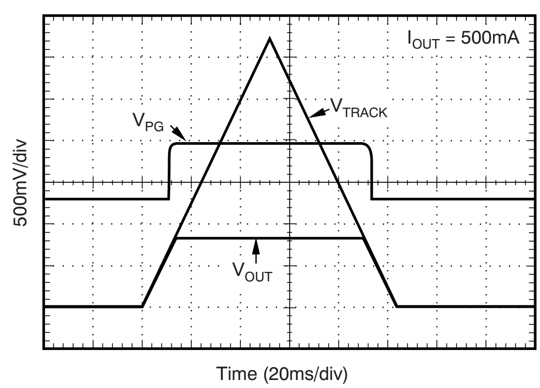


Figure 2. Tracking Response

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}(2)
TPS743**xx*yyyz***	**XX** is nominal output voltage (for example, 12 = 1.2V, 15 = 1.5V, 01 = Adjustable).(3) **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Output voltages from 0.9V to 1.5V in 50mV increments and 1.5V to 3.3V in 100mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.
(3) For fixed 0.8V operation, tie FB to OUT.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –40°C to +125°C, unless otherwise noted. All voltages are with respect to GND.

		TPS74301	UNIT
V_{IN}, V_{BIAS}	Input voltage range	–0.3 to +6	V
V_{EN}	Enable voltage range	–0.3 to +6	V
V_{PG}	Power-good voltage range	–0.3 to +6	V
I_{PG}	PG sink current	0 to +1.5	mA
V_{TRACK}	Track pin voltage range	–0.3 to +6	V
V_{FB}	Feedback pin voltage range	–0.3 to +6	V
V_{OUT}	Output voltage range	–0.3 to V_{IN} + 0.3	V
I_{OUT}	Maximum output current	Internally limited	
	Output short circuit duration	Indefinite	
P_{DISS}	Continuous total power dissipation	See Dissipation Ratings Table	
T_J	Operating junction temperature range	–40 to +125	°C
T_{STG}	Storage junction temperature range	–55 to +150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	θ_{JA}	θ_{JC}	T_A < +25°C POWER RATING	DERATING FACTOR ABOVE T_A = +25°C
RGW (QFN)(1)	36.5°C/W	4.05°C/W	2.74W	27.4mW/°C
KTW (DDPAK)(2)	18.8°C/W	2.32°C/W	5.32W	53.2mW/°C

(1) See Figure 31 for PCB layout description.
(2) See Figure 34 for PCB layout description.

ELECTRICAL CHARACTERISTICS

At V_{EN} = 1.1V, V_{IN} = V_{OUT} + 0.3V, C_{IN} = C_{BIAS} = 0.1μF, C_{OUT} = 10μF, I_{OUT} = 50mA, V_{BIAS} = 5.0V, and T_J = –40°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS	TPS74301 MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		V_{OUT} + V_{DO}		5.5	V
V_{BIAS}	Bias pin voltage range		2.375		5.25	V
V_{REF}	Internal reference (Adj.)	T_J = +25°C	0.796	0.8	0.804	V
V_{OUT}	Output voltage range	V_{IN} = 5V, I_{OUT} = 1.5A, V_{BIAS} = 5V	V_{REF}		3.6	V
	Accuracy(1)	2.375V ≤ V_{BIAS} ≤ 5.25V, 50mA ≤ I_{OUT} ≤ 1.5A	–1	±0.2	1	%
V_{OUT}/V_{IN}	Line regulation	$V_{OUT (NOM)}$ + 0.3 ≤ V_{IN} ≤ 5.5V, QFN		0.0005	0.05	%/V
		$V_{OUT (NOM)}$ + 0.3 ≤ V_{IN} ≤ 5.5V, DDPAK		0.0005	0.06	
V_{OUT}/I_{OUT}	Load regulation	0mA ≤ I_{OUT} ≤ 50mA		0.013		%/mA
		50mA ≤ I_{OUT} ≤ 1.5A		0.04		%/A
V_{DO}	V_{IN} dropout voltage(2)	I_{OUT} = 1.5A, V_{BIAS} – $V_{OUT (NOM)}$ ≥ 1.62V, QFN		55	100	mV
		I_{OUT} = 1.5A, V_{BIAS} – $V_{OUT (NOM)}$ ≥ 1.62V, DDPAK		60	120	
	V_{BIAS} dropout voltage(2)	I_{OUT} = 1.5A, V_{IN} = V_{BIAS}			1.4	V
I_{CL}	Current limit	V_{OUT} = 80% × $V_{OUT (NOM)}$	1.8		4	A
I_{BIAS}	Bias pin current	I_{OUT} = 0mA to 1.5A		2	4	mA
I_{SHDN}	Shutdown supply current (V_{IN})	V_{EN} ≤ 0.4V		1	100	μA
I_{FB}	Feedback pin current(3)	I_{OUT} = 50mA to 1.5A	–250	68	250	nA
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V		73		dB
		800kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V		42		
	Power-supply rejection (V_{BIAS} to V_{OUT})	1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V		67		dB
		800kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V		50		
Noise	Output noise voltage	100Hz to 100kHz, I_{OUT} = 1.5A		25 × V_{OUT}		$μV_{RMS}$
V_{TRAN}	%V_{OUT} droop during load transient	I_{OUT} = 50mA to 1.5A at 1A/μs, C_{OUT} = none		3.5		%V_{OUT}
t_{STR}	Minimum startup time	V_{TRACK} > 0.8V		40		μs
T_{ACC}	Track pin accuracy	0.2V ≤ V_{TRACK} ≤ 0.7V, V_{OUT} = 0.8V	–60		60	mV
I_{TR}	Track pin current	V_{TRACK} = 0.4V		0.1	1	μA
$V_{EN, HI}$	Enable input high level		1.1		5.5	V
$V_{EN, LO}$	Enable input low level		0		0.4	V
$V_{EN, HYS}$	Enable pin hysteresis			50		mV
$V_{EN, DG}$	Enable pin deglitch time			20		μs
I_{EN}	Enable pin current	V_{EN} = 5V		0.1	1	μA
V_{IT}	PG trip threshold	V_{OUT} decreasing	86.5	90	93.5	%V_{OUT}
V_{HYS}	PG trip hysteresis			3		%V_{OUT}
$V_{PG, LO}$	PG output low voltage	I_{PG} = 1mA (sinking), V_{OUT} < V_{IT}			0.3	V
$I_{PG, LKG}$	PG leakage current	V_{PG} = 5.25V, V_{OUT} > V_{IT}		0.3	1	μA
T_J	Operating junction temperature		–40		+125	°C
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+155		°C
		Reset, temperature decreasing		+140		

(1) Adjustable devices tested at 0.8V; external resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from the input to V_{OUT} when V_{OUT} is 2% below nominal.
(3) I_{FB} current flow is out of the device.

BLOCK DIAGRAM

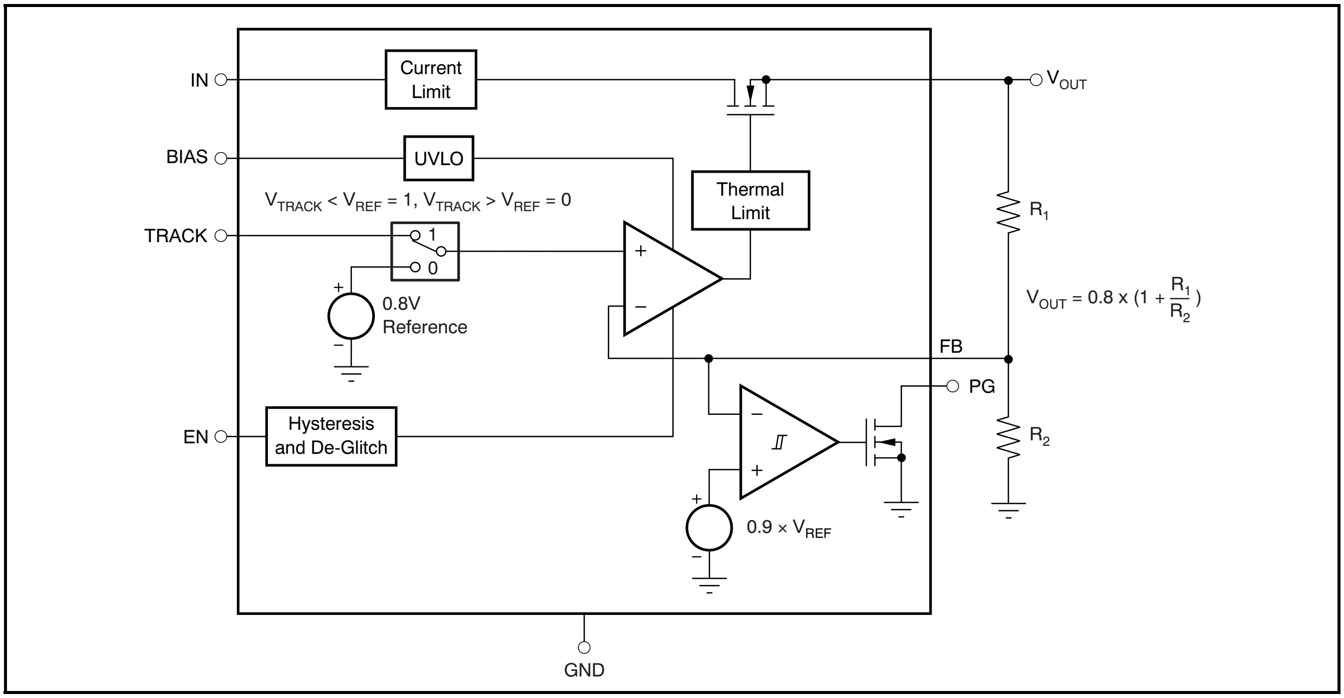
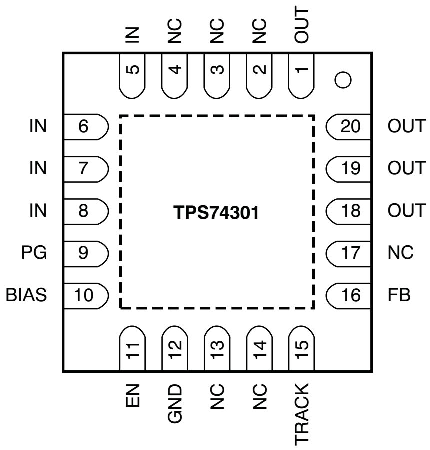


Table 1. Standard 1% Resistor Values for Programming the Output Voltage(1)

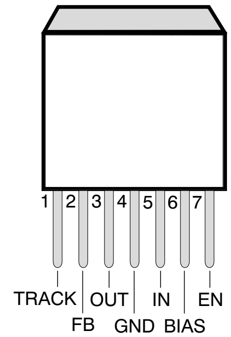
R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1.0
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

(1) $V_{OUT} = 0.8 \times (1 + R1/R2)$

5 × 5 QFN (RGW)
Package — Top View



7-Lead
DDPAK (KTW)
Surface-Mount



PIN DESCRIPTIONS

NAME	KTW (DDPAK)	RGW (QFN)	DESCRIPTION
IN	5	5–8	Unregulated input to the device.
EN	7	11	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.
TRACK	1	15	Tracking pin. Connect this pin to the center tap of a resistor divider off of an external supply to program the device to track an external supply.
BIAS	6	10	Bias input voltage for error amplifier, reference, and internal control circuits.
PG	N/A	9	Power-Good (PG) is an open-drain, active-high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold the pin is driven to a low-impedance state. A pull-up resistor from 10kΩ to 1MΩ should be connected from this pin to a supply up to 5.5V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.
FB	2	16	This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
OUT	3	1, 18–20	Regulated output voltage. No capacitor is required on this pin for stability.
NC	N/A	2–4, 13, 14, 17	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
GND	4	12	Ground
PAD/TAB			Should be soldered to the ground plane for increased thermal performance.

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(TYP)}$ + 0.3V, V_{BIAS} = 3.3V, I_{OUT} = 50mA, EN = V_{IN}, C_{IN} = 1μF, C_{BIAS} = 4.7μF, and C_{OUT} = 10μF, unless otherwise noted.

LOAD REGULATION

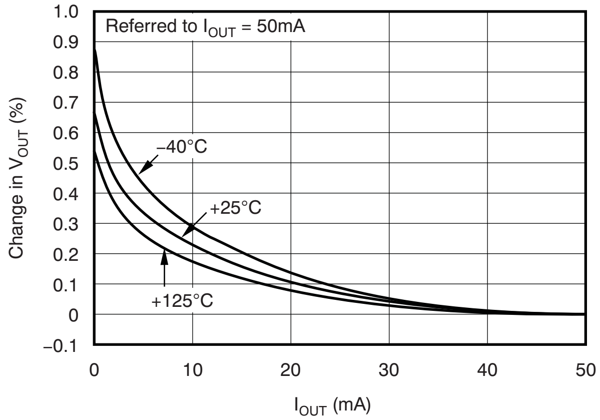


Figure 3.

LOAD REGULATION

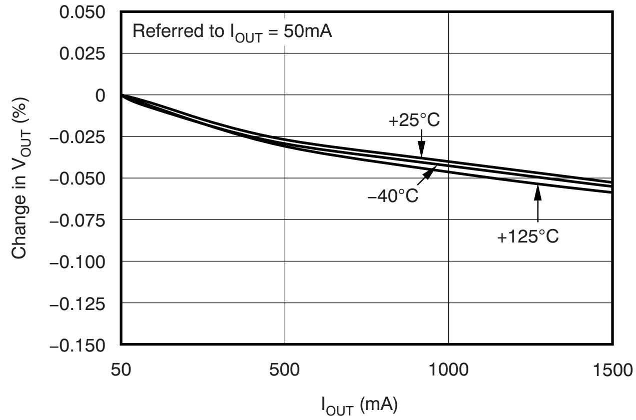


Figure 4.

LINE REGULATION

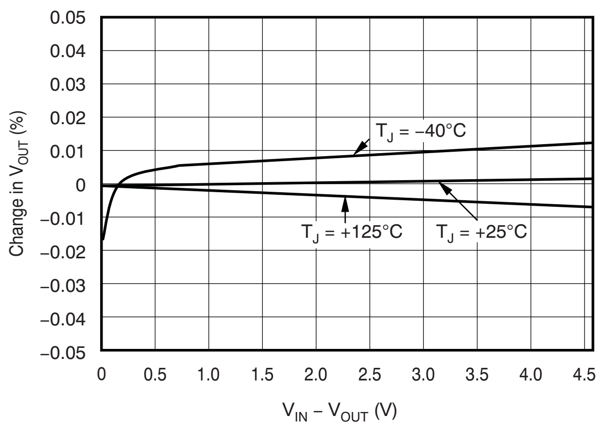


Figure 5.

V_{IN} DROPOUT VOLTAGE vs I_{OUT} AND TEMPERATURE (T_J)

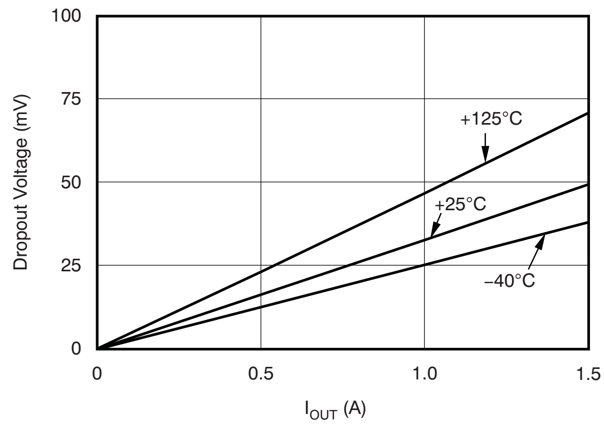


Figure 6.

V_{IN} DROPOUT VOLTAGE vs V_{BIAS} – V_{OUT} AND TEMPERATURE (T_J)

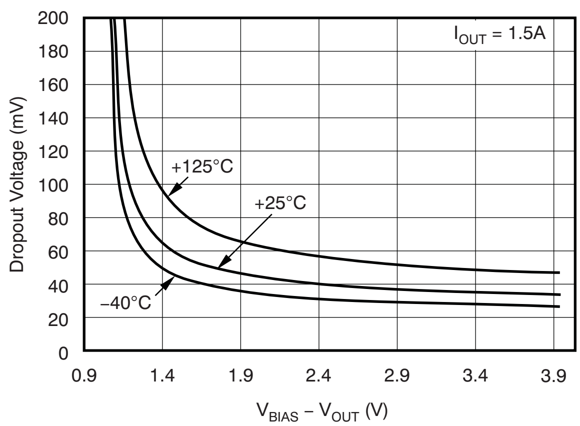


Figure 7.

V_{IN} DROPOUT VOLTAGE vs V_{BIAS} – V_{OUT} AND TEMPERATURE (T_J)

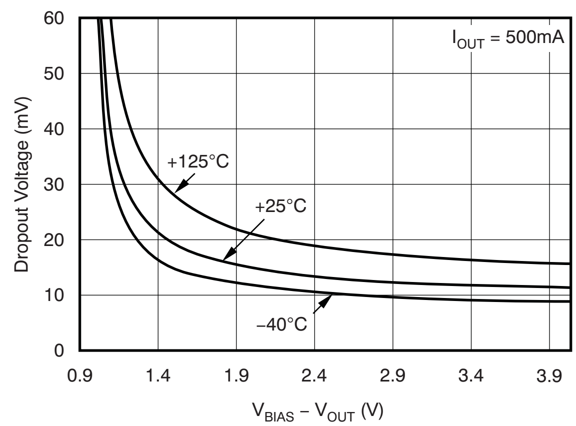


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(TYP)}$ + 0.3V, V_{BIAS} = 3.3V, I_{OUT} = 50mA, EN = V_{IN}, C_{IN} = 1μF, C_{BIAS} = 4.7μF, and C_{OUT} = 10μF, unless otherwise noted.

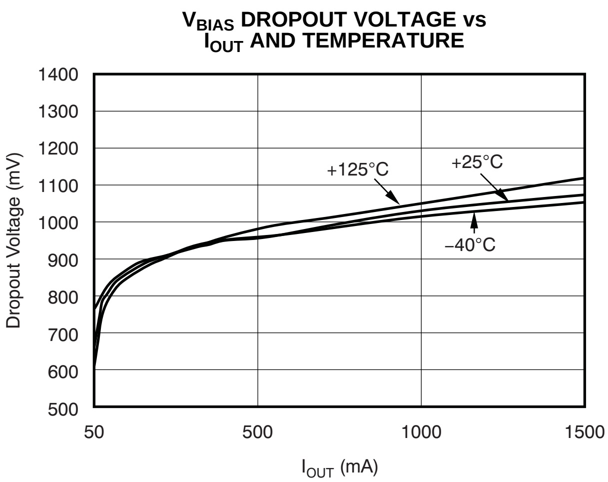


Figure 9.

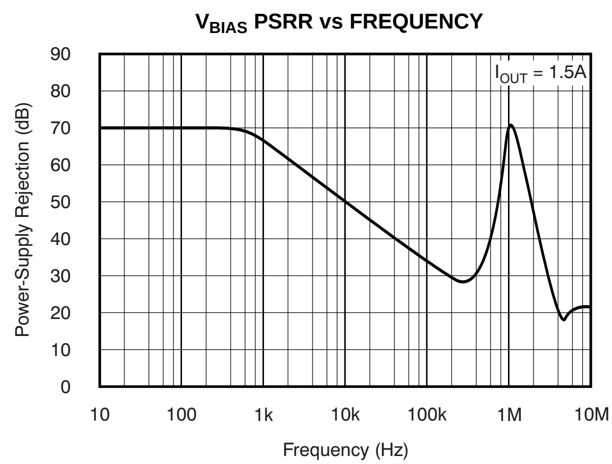


Figure 10.

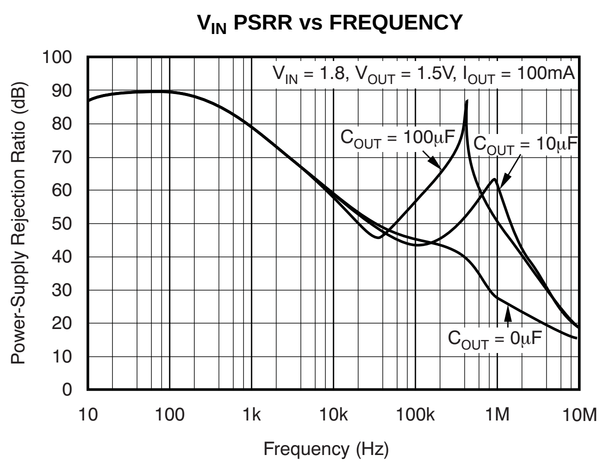


Figure 11.

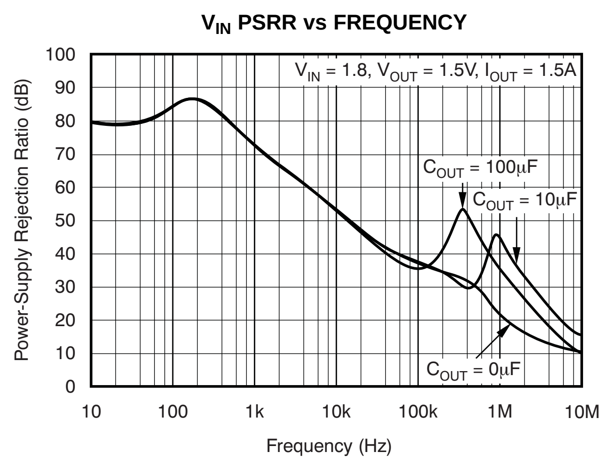


Figure 12.

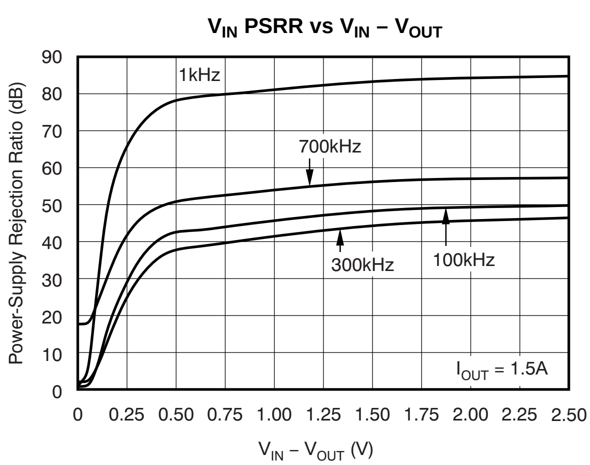


Figure 13.

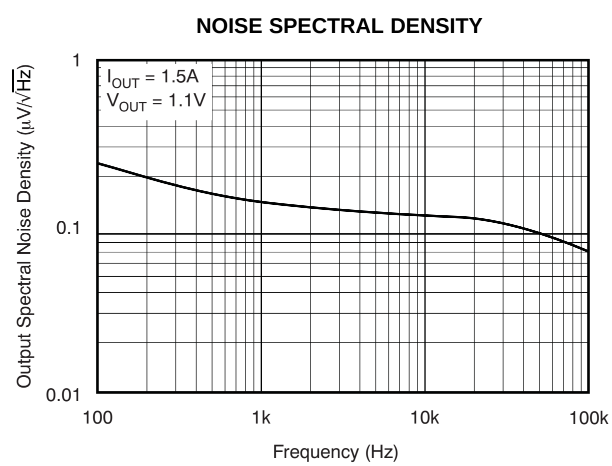


Figure 14.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(TYP)}$ + 0.3V, V_{BIAS} = 3.3V, I_{OUT} = 50mA, EN = V_{IN}, C_{IN} = 1μF, C_{BIAS} = 4.7μF, and C_{OUT} = 10μF, unless otherwise noted.

V_{BIAS} LINE TRANSIENT

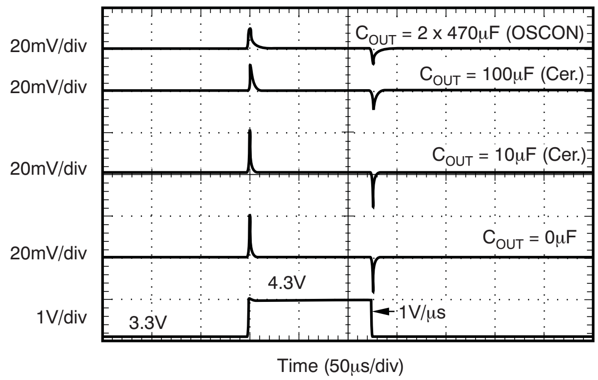


Figure 15.

V_{IN} LINE TRANSIENT (1.5A)

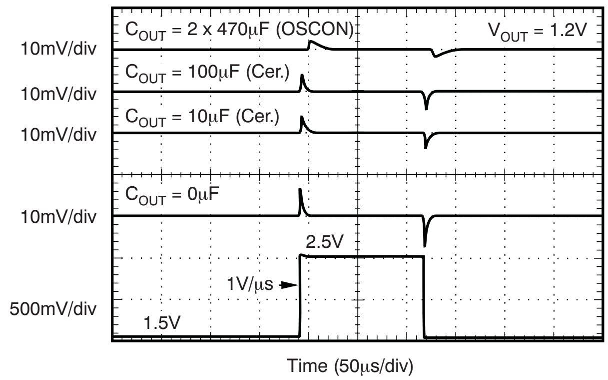


Figure 16.

OUTPUT LOAD TRANSIENT RESPONSE

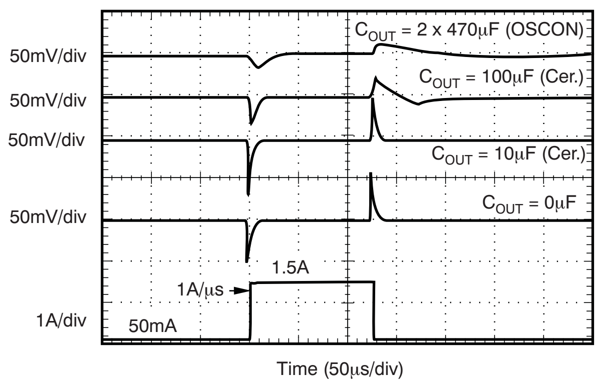


Figure 17.

TRACKING RESPONSE

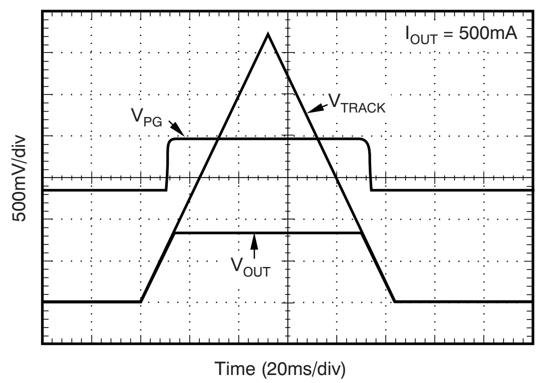


Figure 18.

POWER-UP/POWER-DOWN

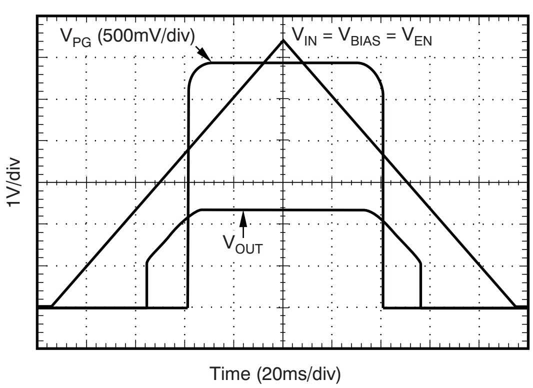


Figure 19.

I_{BIAS} vs I_{OUT} AND TEMPERATURE

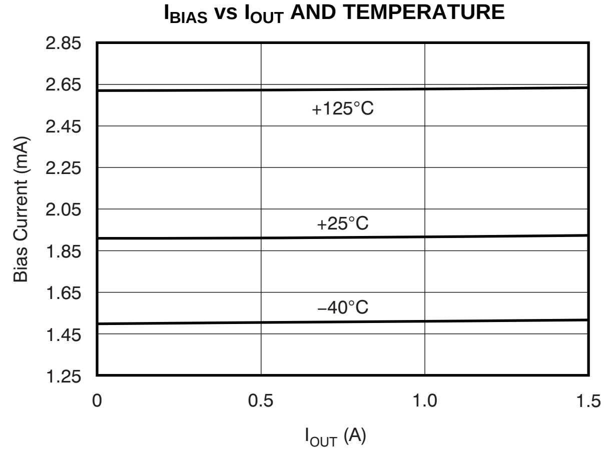


Figure 20.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(TYP)}$ + 0.3V, V_{BIAS} = 3.3V, I_{OUT} = 50mA, EN = V_{IN}, C_{IN} = 1μF, C_{BIAS} = 4.7μF, and C_{OUT} = 10μF, unless otherwise noted.

I_{BIAS} vs V_{BIAS} AND V_{OUT}

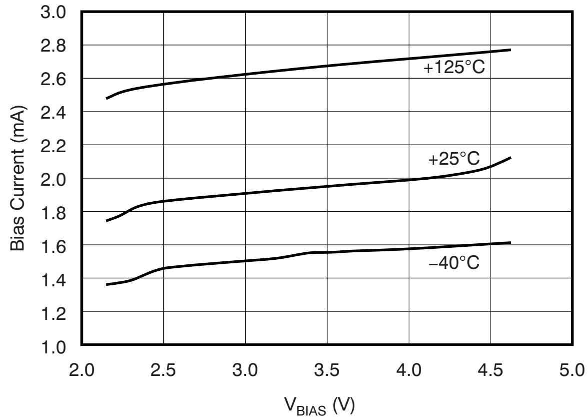


Figure 21.

I_{BIAS} SHUTDOWN vs TEMPERATURE

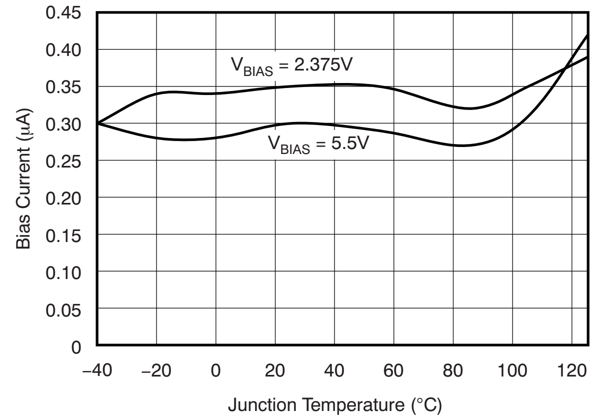


Figure 22.

TURN-ON RESPONSE–QFN PACKAGE

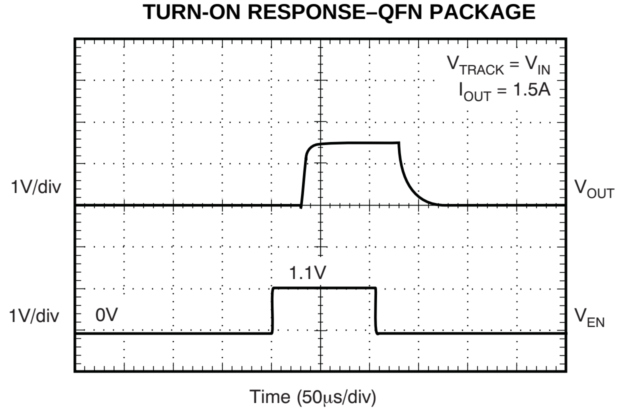


Figure 23.

LOW-LEVEL PG VOLTAGE vs PG CURRENT

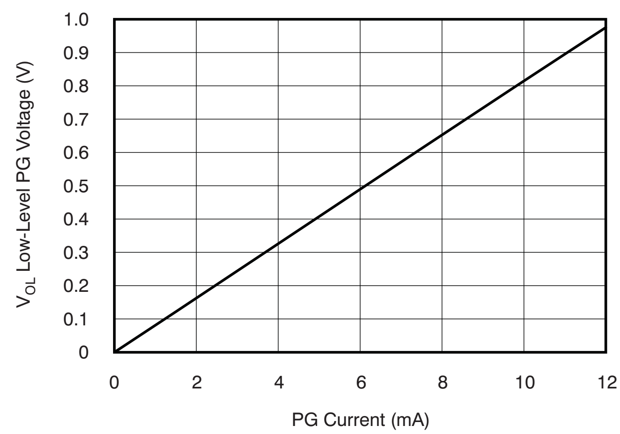


Figure 24.

OUTPUT SHORT-CIRCUIT RECOVERY

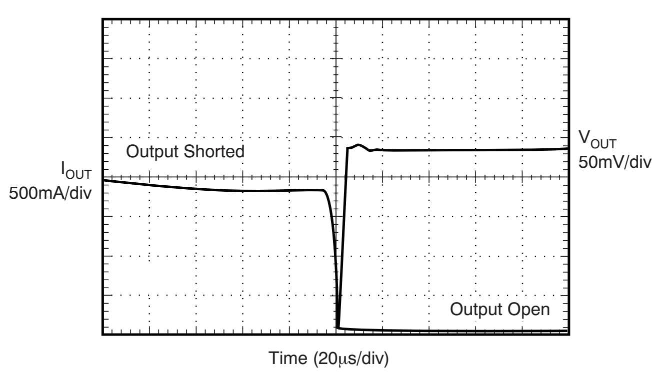


Figure 25.

APPLICATION INFORMATION

The TPS74301 belongs to a family of new generation ultra-low dropout regulators that feature soft-start and tracking capabilities. These regulators use a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS-pass FET offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS74301 to be stable with any or even no output capacitor. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS74301 features a TRACK pin that allows the output to track an external supply. This feature is useful in minimizing the stress on ESD structures that are present between the CORE and I/O power pins of many processors. A power-good (PG) output is also available to allow supply monitoring and sequencing of follow-on supplies. To control the output turn-on, an enable (EN) pin with hysteresis and deglitch is provided to allow slow-ramping signals to be utilized for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor intensive systems.

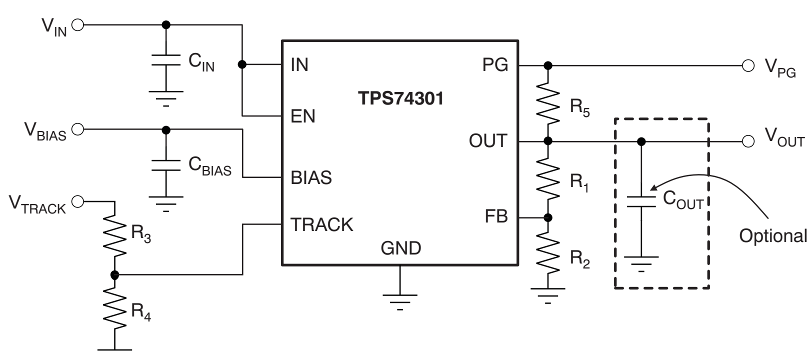
Figure 26 is a typical application circuit for the TPS74301 adjustable device.

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 26. Refer to Table 1 for sample resistor values of common output voltages. In order to achieve the maximum accuracy specifications, R_2 should be ≤ 4.99kΩ.

INPUT, OUTPUT, AND BIAS CAPACITOR REQUIREMENTS

The device does not require any output capacitor for stability. If an output capacitor is needed, the device is designed to be stable for all available types and values of output capacitance. The device is also stable with multiple capacitors in parallel, of any type or value.

The capacitance required on the IN and BIAS pins is strongly dependent on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} and V_{BIAS} is 1μF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7μF. Good quality, low ESR capacitors should be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors should be placed as close the pins as possible for optimum performance.



$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Figure 26. Typical Application Circuit for the TPS74301 (Adjustable)

TRANSIENT RESPONSE

The TPS74301 was designed to have transient response within 5% for most applications without any output capacitor. In some cases, the transient response may be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance would do. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient at the expense of a slightly longer V_{OUT} recovery time. Refer to Figure 17 in the Typical Characteristics section. Since the TPS74301 is stable without an output capacitor, many applications may allow for little or no capacitance at the LDO output. For these applications, local bypass capacitance for the device under power may be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive high-value capacitors at the LDO output.

DROPOUT VOLTAGE

The TPS74301 offers industry-leading dropout performance, making it well-suited for high-current low V_{IN}/low V_{OUT} applications. The extremely low dropout of the TPS74301 allows the device to be used instead of a DC/DC converter and still achieve good efficiencies. This efficiency allows users to rethink the power architecture for their applications to find the smallest, simplest, and lowest cost solution.

There are two different specifications for dropout voltage with the TPS74301. The first specification (as shown in Figure 27) is referred to as *V_{IN} Dropout* and is for users wishing to apply an external bias voltage to achieve low dropout. This specification assumes that V_{BIAS} is at least 1.62V above V_{OUT}, which is the case for V_{BIAS} when powered by a 3.3V rail with 5% tolerance and with V_{OUT} = 1.5V. If V_{BIAS} is higher than $3.3V \times 0.95$ or V_{OUT} is less than 1.5V, V_{IN} dropout is less than specified.

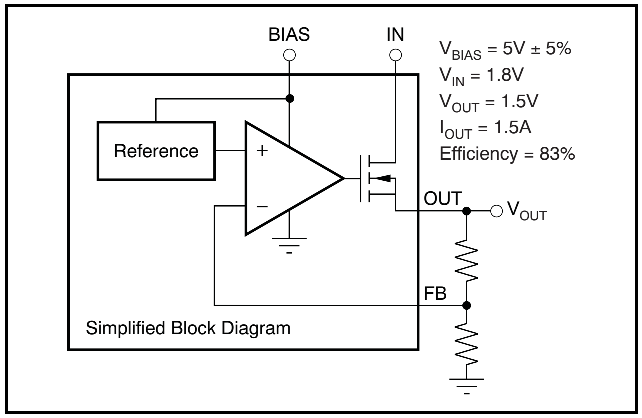


Figure 27. Typical Application of the TPS74301 Using an Auxiliary Bias Rail

The second specification (see Figure 28), referred to as *V_{BIAS} Dropout*, is for users who wish to tie IN and BIAS together. This option allows the device to be used in applications where an auxiliary bias voltage is unavailable or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass FET, and therefore must be 1.4V above V_{OUT}.

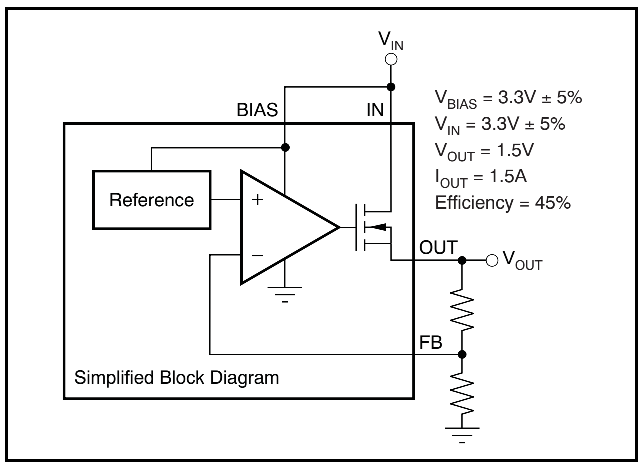


Figure 28. Typical Application of the TPS74301 Without an Auxiliary Bias

PROGRAMMABLE SEQUENCING WITH TRACK

The TPS74301 features a track pin that allows the output to track an external supply at start-up. While the TRACK input is below 0.8V, the error amplifier regulates the FB pin to the TRACK input. Properly choosing the resistor divider network (R_1 and R_2) as shown in Figure 29 enables the regulator output to track the external supply to obtain a simultaneous or ratiometric start-up. Once the TRACK input reaches 0.8V, the error amplifier regulates the FB pin to the 0.8V internal reference. Further increases to the TRACK input have no effect.

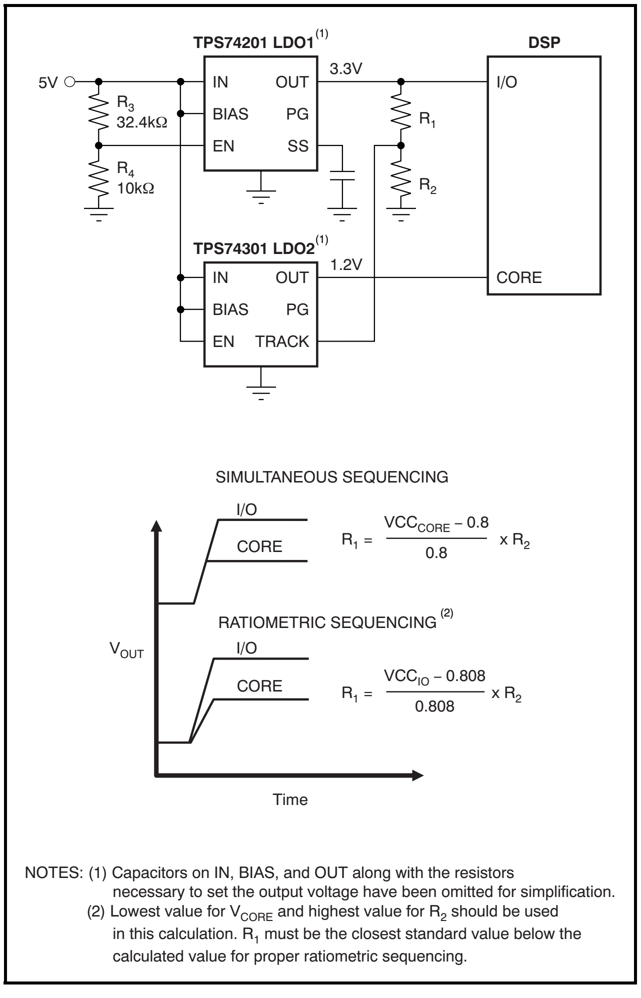


Figure 29. Various Sequencing Methods Using the TRACK Pin

The maximum recommended value for R_2 is 100kΩ. Once R_2 is selected, R_1 is calculated using one of the equations given in Figure 29.

SEQUENCING REQUIREMENTS

The device can have V_{IN}, V_{BIAS}, V_{EN}, and V_{TRACK} sequenced in any order without causing damage to the device. However, for the track function to work as intended, certain sequencing rules must be applied. V_{BIAS} must be present and the device enabled before the track signal starts to ramp. V_{IN} should ramp up faster than the external supply being tracked so that the tracking signal will not drive the device into V_{IN} dropout as V_{OUT} ramps up. The preferred method to sequence the tracking device is to have V_{IN}, V_{BIAS}, and V_{EN} above the minimum required voltages before enabling the master supply to initiate the startup sequence. This method is illustrated in Figure 29. Resistors R_3 and R_4 disable the master supply until the input voltage is above 3.52V (typical).

If the TRACK pin is not needed it should be connected to V_{IN}. Configured in this way, the device starts up typically within 40µs, which may result in large inrush current that could cause the input supply to droop. If soft-start is needed, consider the TPS74201 or TPS74401 devices.

OUTPUT NOISE

The TPS74301 provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 0.001µF soft-start capacitor, the output noise is reduced by half and is typically $30\mu V_{RMS}$ for a 1.2V output (10Hz to 100kHz). Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. The RMS noise with a 0.001µF soft-start capacitor is given in Equation 1.

$$V_N(\mu V_{RMS}) = 25\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (1)$$

The low output noise of the TPS74301 makes it a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

ENABLE/SHUTDOWN

The enable (EN) pin is active high and is compatible with standard digital signaling levels. V_{EN} below 0.4V turns the regulator off, while V_{EN} above 1.1V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slow-ramping analog signals. This configuration allows the TPS74301 to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50mV of hysteresis and a deglitch circuit to help avoid on-off cycling because of small glitches in the V_{EN} signal.

The enable threshold is typically 0.8V and varies with temperature and process variations. Temperature variation is approximately –1mV/°C; therefore, process variation accounts for most of the variation in the enable threshold. If precise turn-on timing is required, a fast rise-time signal should be used to enable the TPS74301.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, it should be connected as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

POWER-GOOD (QFN Package Only)

The power-good (PG) pin is an open-drain output and can be connected to any 5.5V or lower rail through an external pull-up resistor. This pin requires at least 1.1V on V_{BIAS} in order to have a valid output. The PG output is high-impedance when V_{OUT} is greater than V_{IT} + V_{HYS}. If V_{OUT} drops below V_{IT} or if V_{BIAS} drops below 1.9V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of PG pin sink current is up to 1mA, so the pull-up resistor for PG should be in the range of 10kΩ to 1MΩ. PG is only provided on the QFN package. If output voltage monitoring is not needed, the PG pin can be left floating.

INTERNAL CURRENT LIMIT

The TPS74301 features a factory-trimmed, accurate current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 1.8A and maintain regulation. The current limit responds in about 10µs to reduce the current during a short-circuit fault. Recovery from a short-circuit condition is well-controlled and results in very little output overshoot when the load is removed. See Figure 25 in the Typical Characteristics section for output short-circuit recovery performance.

The internal current limit protection circuitry of the TPS74301 is designed to protect against overload conditions. It is not intended to allow operation above the rated current of the device. Continuously running the TPS74301 above the rated current degrades device reliability.

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +155°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +30°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS74301 is designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TPS74301 into thermal shutdown degrades device reliability.

LAYOUT RECOMMENDATIONS AND POWER DISSIPATION

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage droop on the input of the device during load transients, the capacitance on IN and BIAS should be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can therefore improve stability. To achieve optimal transient performance and accuracy, the top side of R_1 in Figure 26 should be connected as close as possible to the load. If BIAS is connected to IN, it is recommended to connect BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage droop on BIAS during transient conditions and can improve the turn-on response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation. Power dissipation of the device depends on input voltage and load conditions, and can be calculated using Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On both the QFN (RGW) and DDPAK (KTW) packages, the primary conduction path for heat is through the exposed pad or tab to the printed circuit board (PCB). The pad or tab can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device, and can be calculated using Equation 3:

$$R_{\theta JA} = \frac{(+125^{o}C - T_A)}{P_D} \qquad (3)$$

Knowing the maximum $R_{\theta JA}$ and system air flow, the minimum amount of PCB copper area needed for appropriate heatsinking can be calculated using Figure 30 through Figure 34.

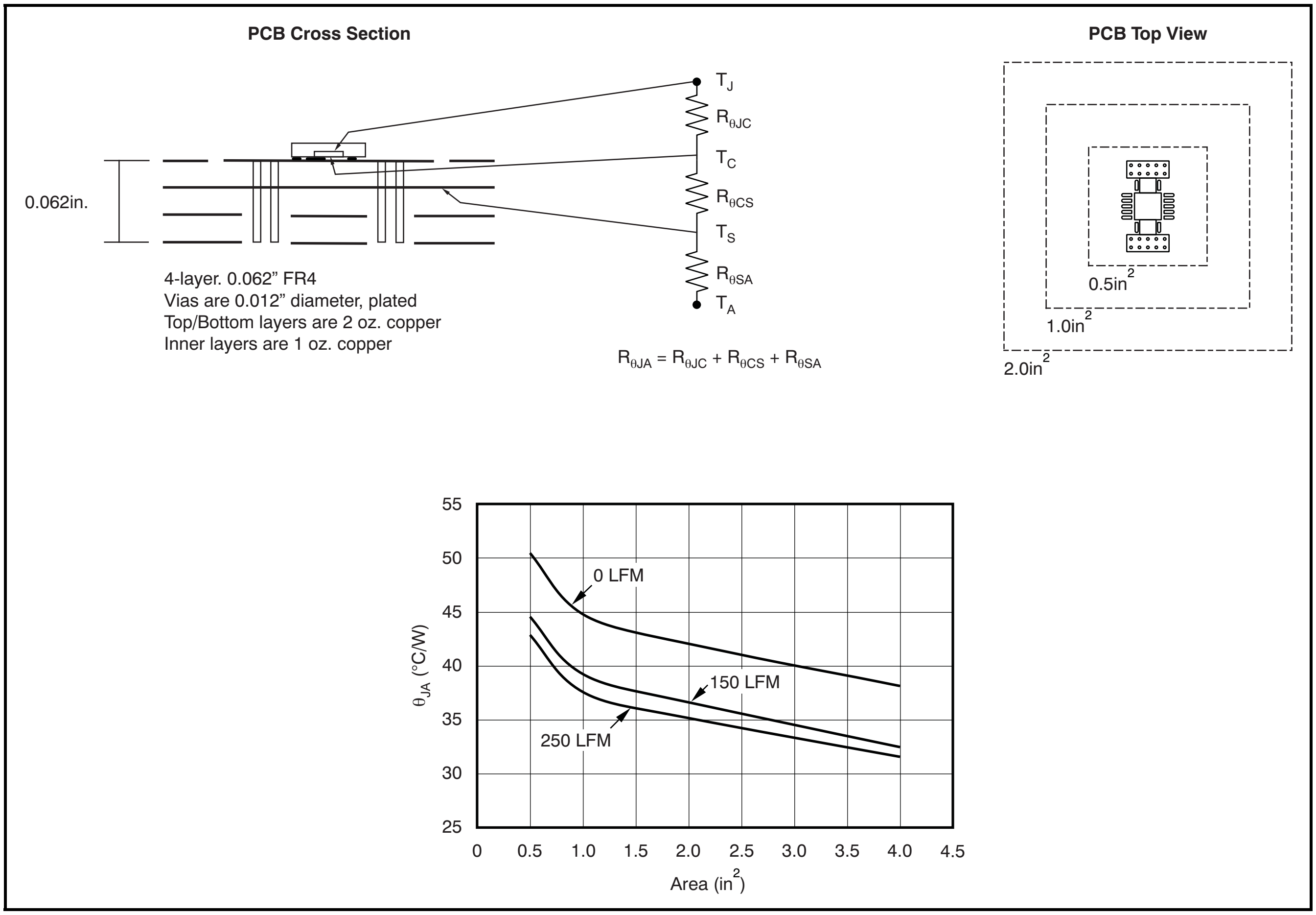


Figure 30. PCB Layout and Corresponding $R_{\theta JA}$ Data, Buried Thermal Plane, No Vias Under Thermal Pad

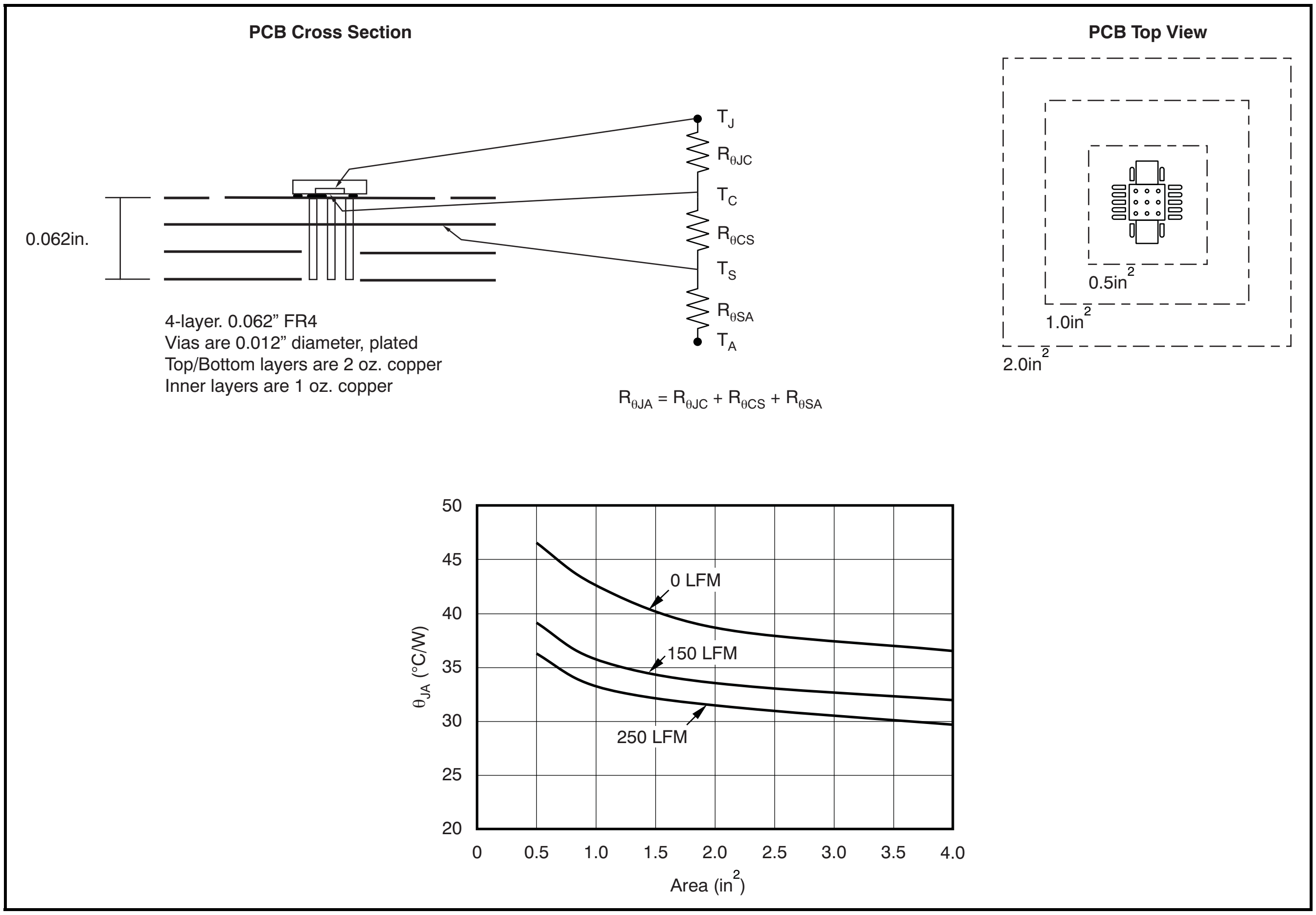


Figure 31. PCB Layout and Corresponding $R_{\theta JA}$ Data, Buried Thermal Plane, Vias Under Thermal Pad

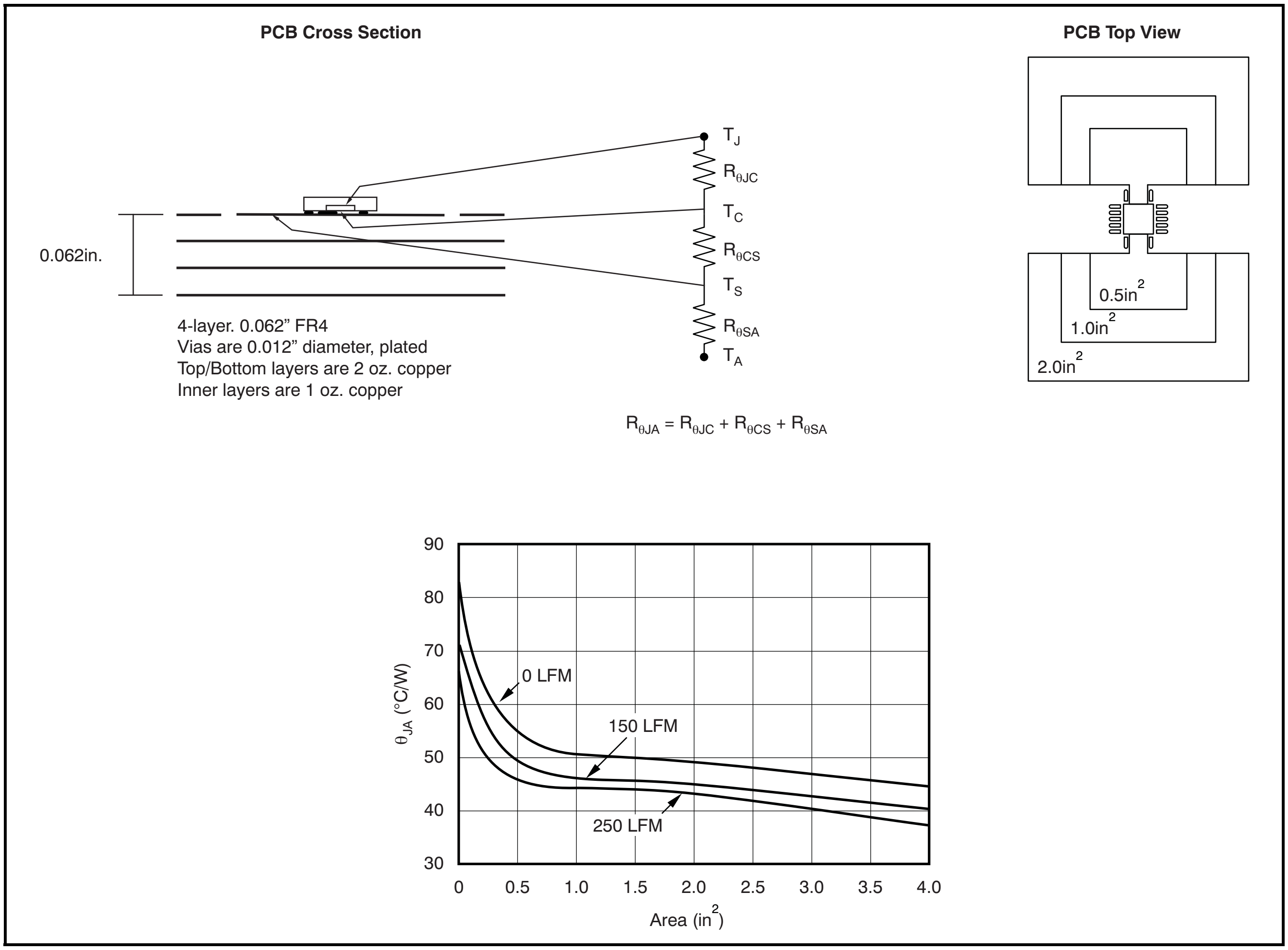


Figure 32. PCB Layout and Corresponding $R_{\theta JA}$ Data, Top Layer Thermal Plane

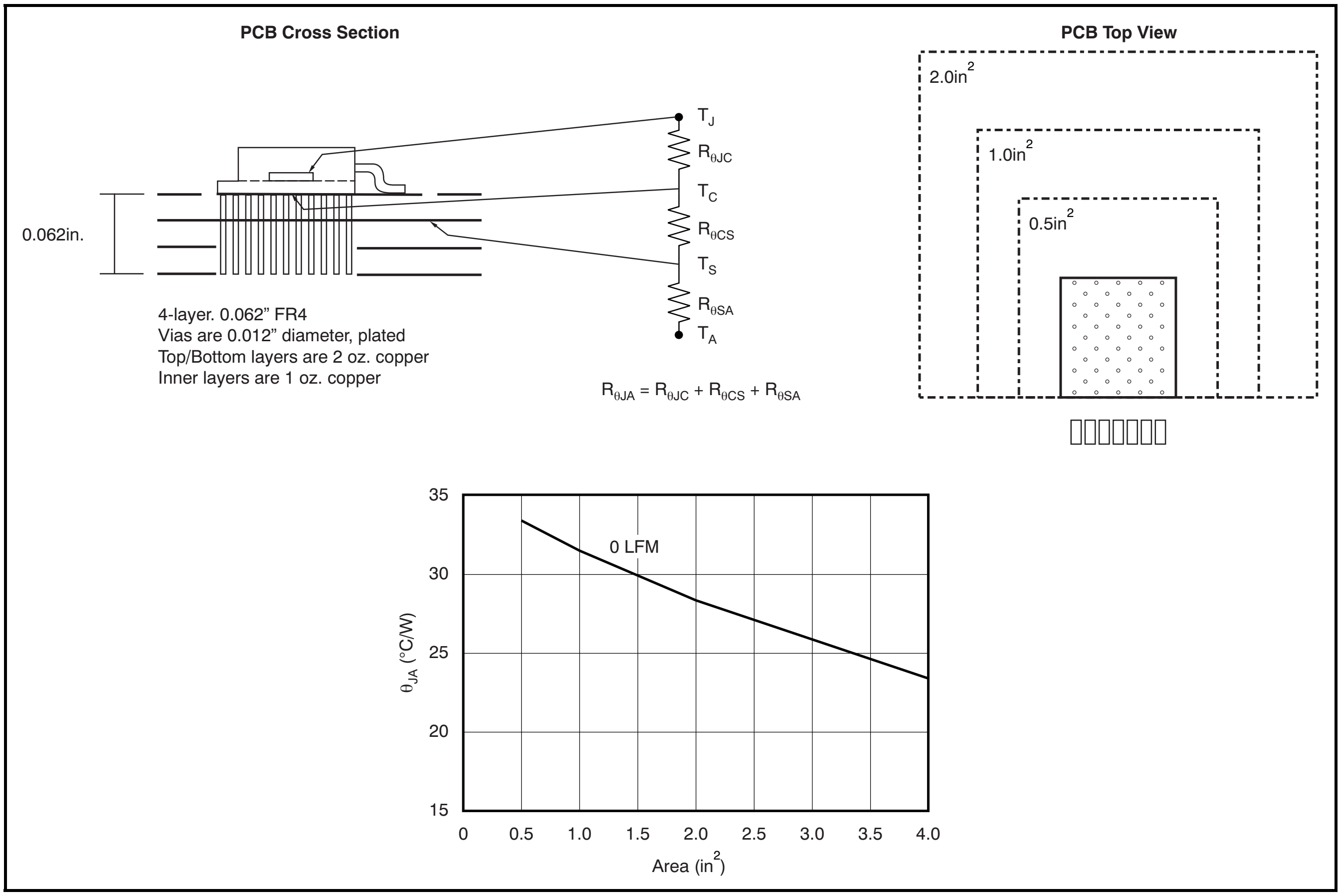


Figure 33. PCB Layout and Corresponding $R_{\theta JA}$, Buried Thermal Plane

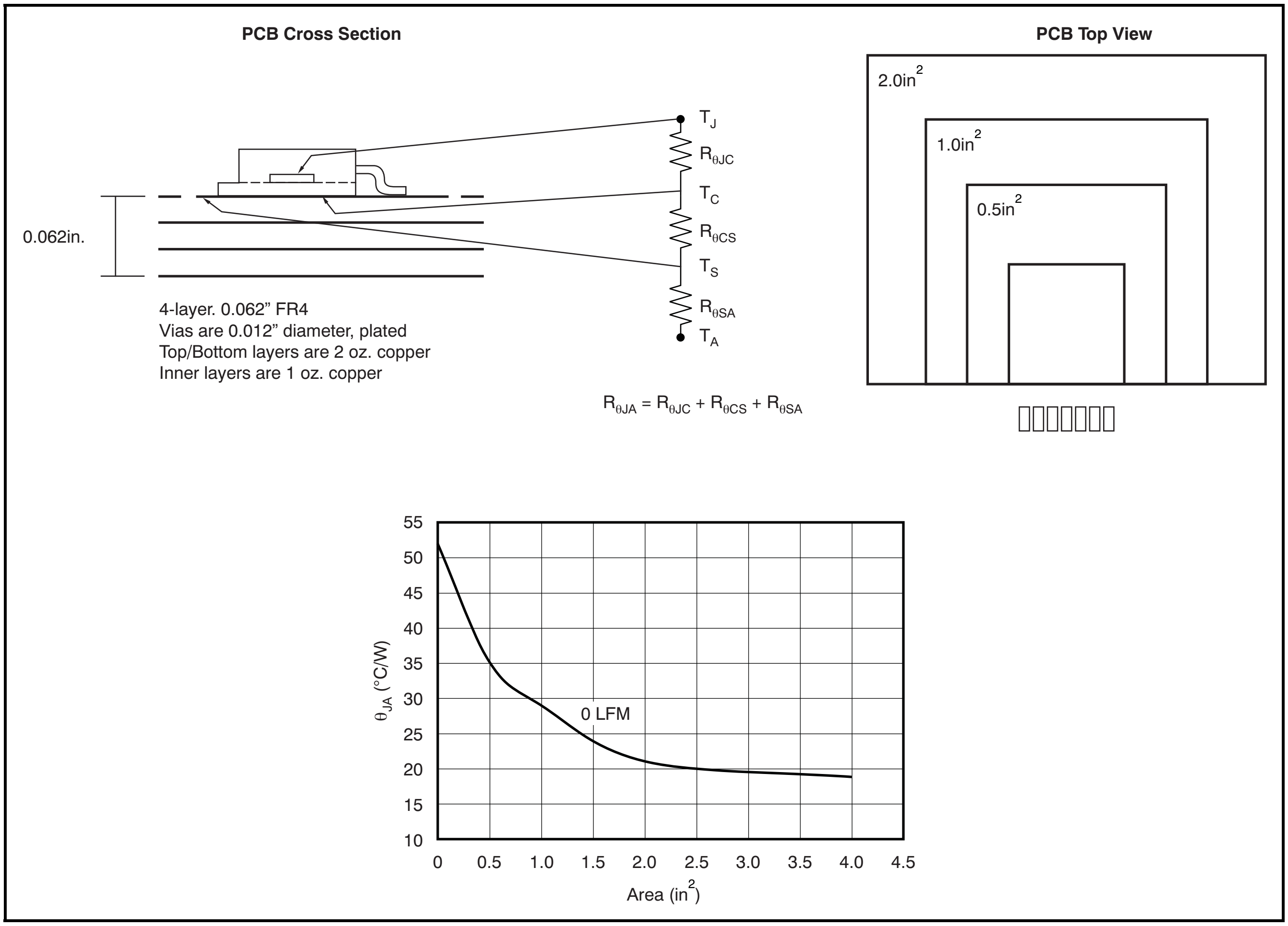


Figure 34. PCB Layout and Corresponding $R_{\theta JA}$, Top Layer Thermal Plane

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS74301KTWR	ACTIVE	DDPAK	KTW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR
TPS74301KTWRG3	ACTIVE	DDPAK	KTW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR
TPS74301KTWT	ACTIVE	DDPAK	KTW	7	50	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR
TPS74301KTWTG3	ACTIVE	DDPAK	KTW	7	50	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR
TPS74301RGWR	ACTIVE	QFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS74301RGWRG4	ACTIVE	QFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS74301RGWT	ACTIVE	QFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS74301RGWTG4	ACTIVE	QFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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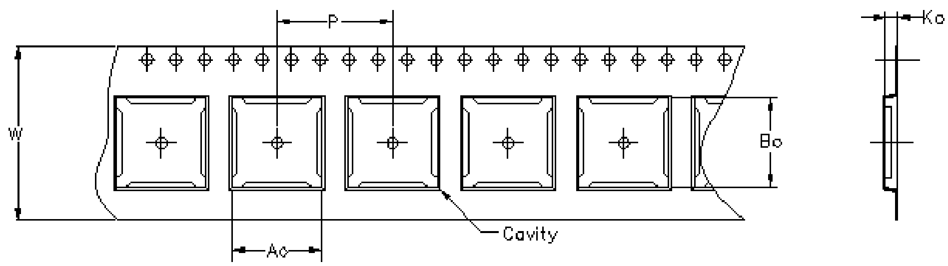
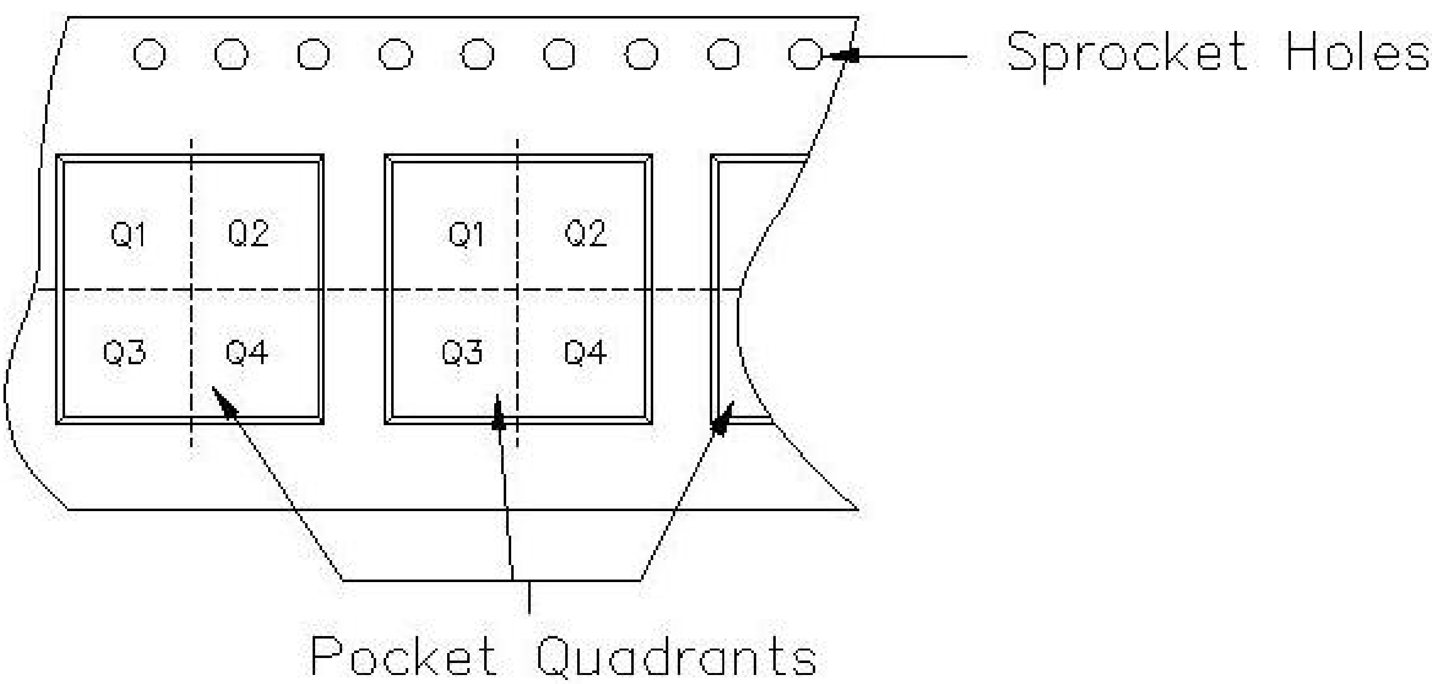


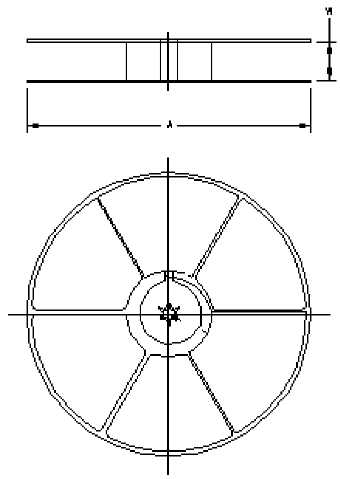
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao =	Dimension designed to accommodate the component width.
Bo =	Dimension designed to accommodate the component length.
Ko =	Dimension designed to accommodate the component thickness.
W =	Overall width of the carrier tape.
P =	Pitch between successive cavity centers.



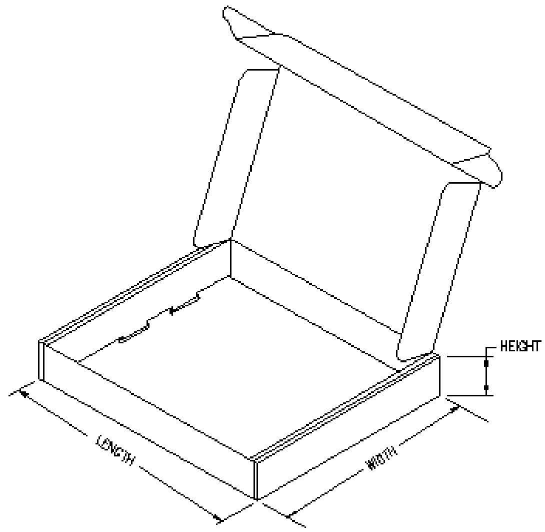
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74301RGWR	RGW	20	MLA	330	12	5.3	5.3	1.5	8	12	PKGORNT2TR-MSP
TPS74301RGWT	RGW	20	MLA	180	12	5.3	5.3	1.5	8	12	PKGORNT2TR-MSP

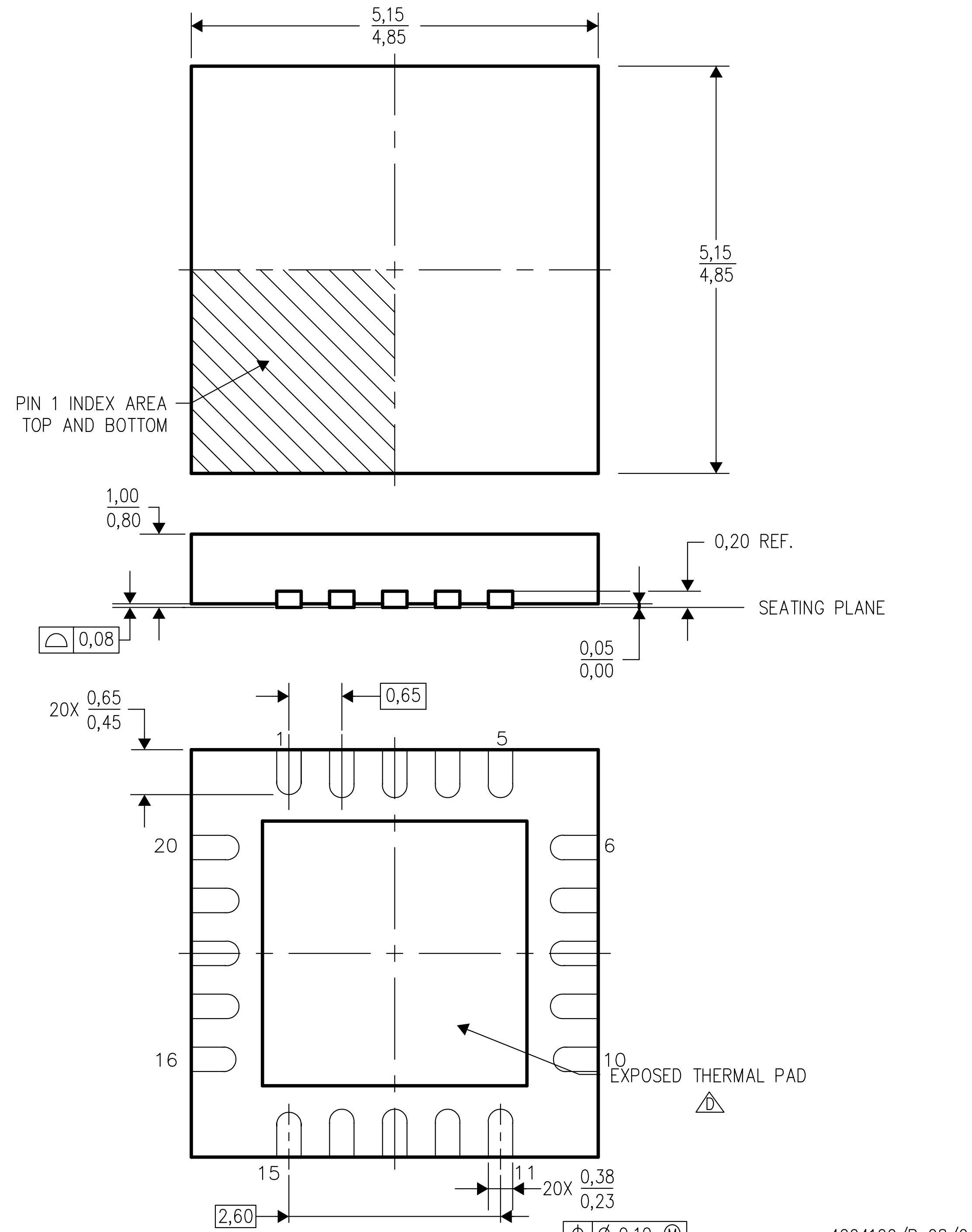


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS74301RGWR	RGW	20	MLA	346.0	346.0	29.0
TPS74301RGWT	RGW	20	MLA	190.0	212.7	31.75


HEIGHT
LENGTH
WIDTH

RGW (S-PQFP-N20) PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flat pack, No-leads (QFN) package configuration
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO-220.

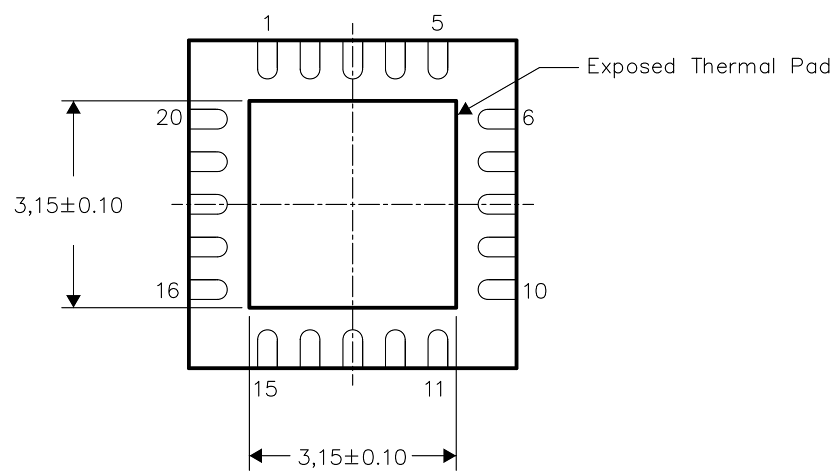
THERMAL PAD MECHANICAL DATA
RGW (S–PQFP–N20)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

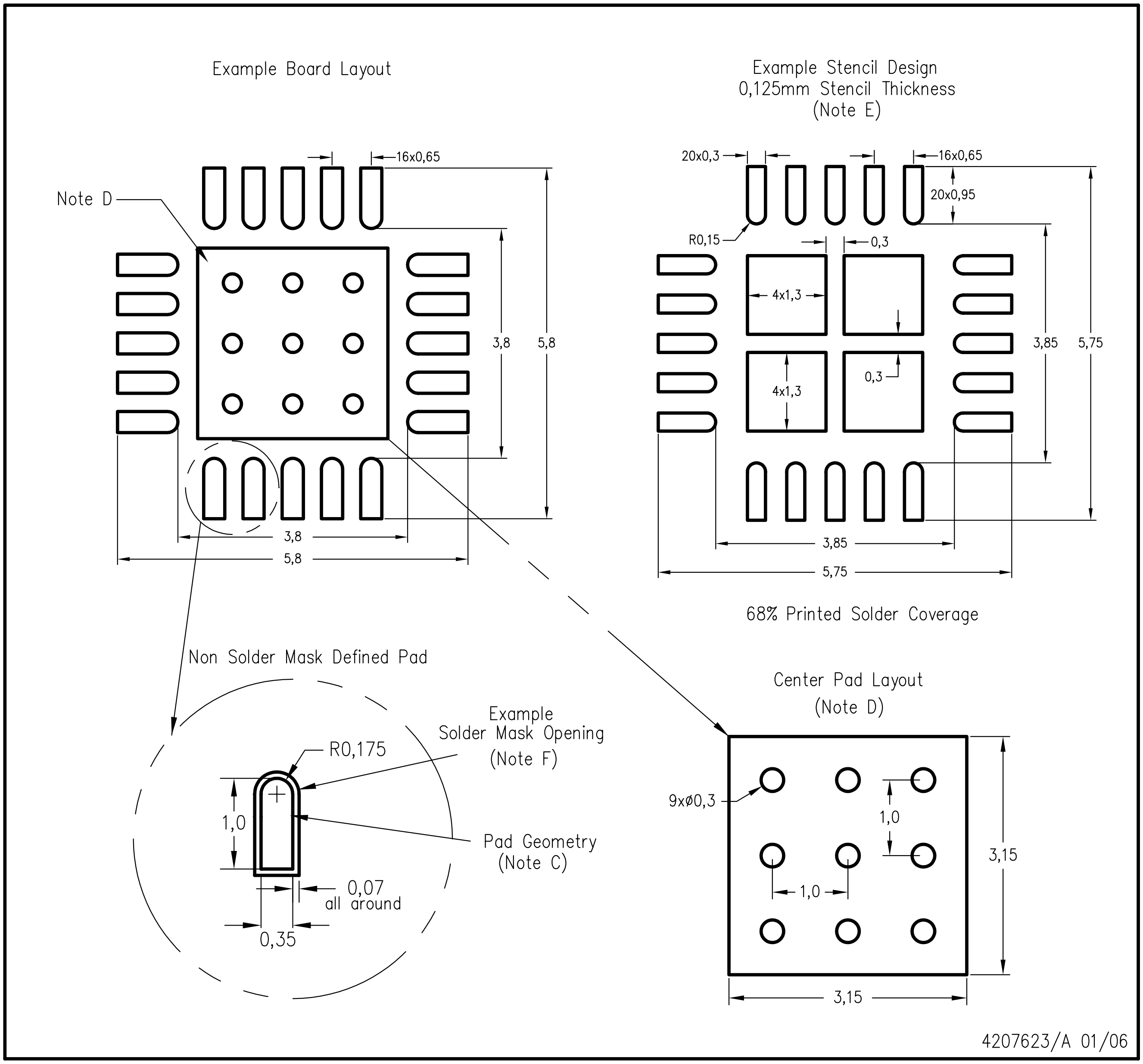


Bottom View

NOTE: All linear dimensions are in millimeters

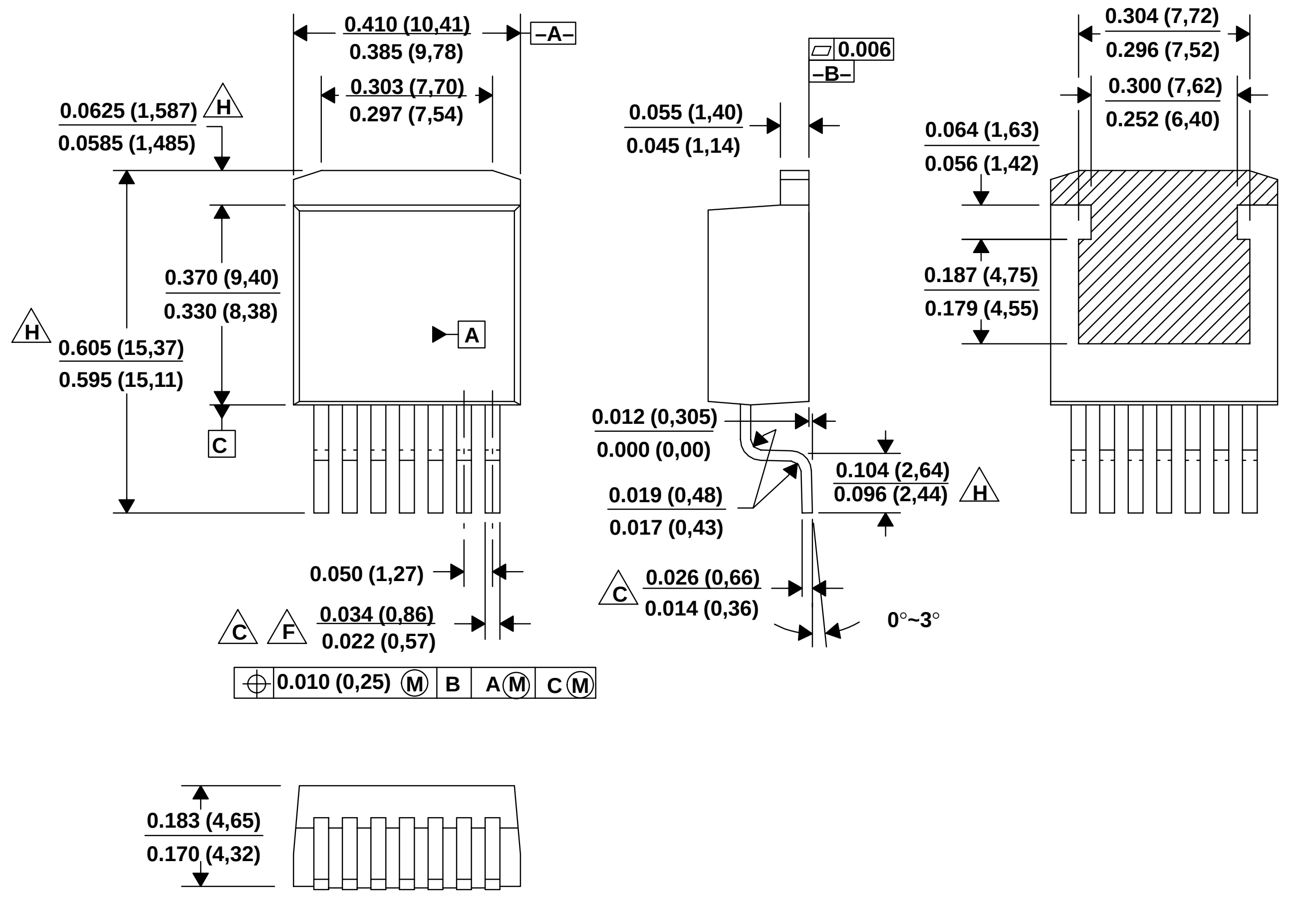
Exposed Thermal Pad Dimensions

RGW (S–PQFP–N20)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

KTW (R-PSFM-G7) **PLASTIC FLANGE-MOUNT**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead width and height dimensions apply to the plated lead.
D. Leads are not allowed above the Datum B.
E. Stand–off height is measured from lead tip with reference to Datum B.
F. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum dimension by more than 0.003”.
G. Cross–hatch indicates exposed metal surface.
H. Falls within JEDEC MO–169 with the exception of the dimensions indicated.

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