500mA, Low-Dropout Voltage Regulator for C2000™

Check for Samples: TPS73534

FEATURES

- **Optimal Output Voltage for I/O Rail of C2000**
- **Good Line/Load Transient Response for MCUs**
- **500mA LDO Voltage Regulator with Enable**
- **Low I_Q: 46μA**
- **Low Shutdown Current: 1μA**
- **Stable with 2μF Ceramic Capacitor**
- **Good PSRR: 60dB at 1kHz**
- **Low Noise: 28μV_{RMS}**
- **2% Overall Accuracy (Load/Line/Temp)**
- **8-Pin 3x3mm SON**

APPLICATIONS

- **C2000 I/O Power Rail Supply**

DESCRIPTION

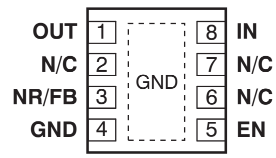
The TPS73534 low-dropout (LDO) voltage regulator is optimized for use with TI's C2000 controller family to meet the I/O power rail tolerance requirement. The device offers very good line and load transient response, even with very low quiescent current of 46μA.

The device also has superior noise and PSRR performance to supply noise sensitive circuit blocks.

In combination with a voltage supervisor such as the TPS3808G01, the TPS73534 can deliver tight V_{IO} voltages and generate accurate power-good signals that meet or exceed power requirements for the C2000.

The TPS73534 is fully specified from T_J = –40°C to +125°C and is offered in a 3mm x 3mm SON package.

DRB PACKAGE
3mm x 3mm SON
(TOP VIEW)



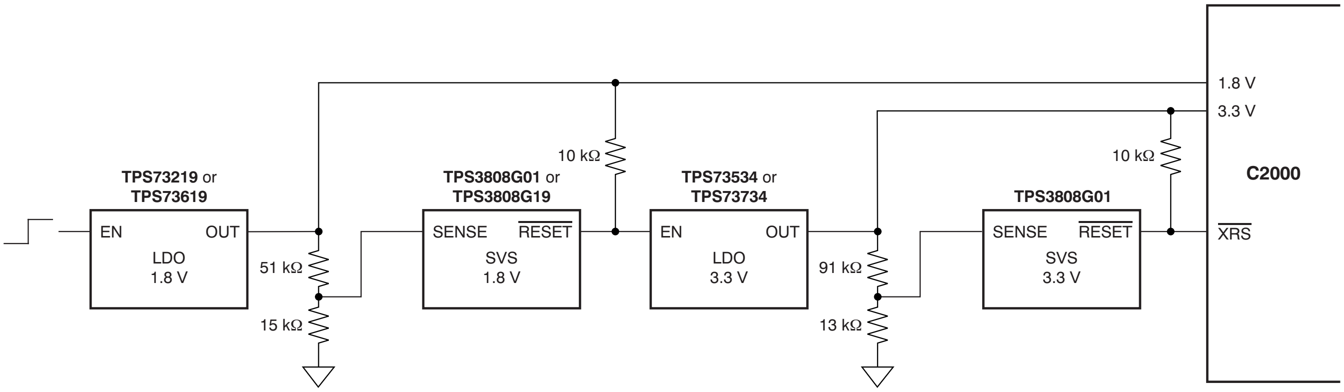


Figure 1. Typical Application

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT} (2)
TPS735**xx** ***yyy z***	**XX** is nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, 01 = Adjustable). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Output voltages from 1.0V to 3.6V in 50mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS

Over operating temperature range (unless otherwise noted).(1)

PARAMETER	TPS73534	UNIT
V_{IN} range	–0.3 to +7.0	V
V_{EN} range	–0.3 to V_{IN} +0.3	V
V_{OUT} range	–0.3 to V_{IN} +0.3	V
V_{FB} range	–0.3 to V_{FB} (TYP) +0.3	V
Peak output current	Internally limited	
Continuous total power dissipation	See *Thermal Information* table	
Junction temperature range, T_J	–55 to +150	°C
Storage temperature range , T_{STG}	–55 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

THERMAL INFORMATION

THERMAL METRIC[1]		TPS73534[2] DRB 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[3]	47.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[4]	83	
θ_{JB}	Junction-to-board thermal resistance[5]	N/A	
ψ_{JT}	Junction-to-top characterization parameter[6]	2.1	
ψ_{JB}	Junction-to-board characterization parameter[7]	17.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[8]	12.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.
(2) Thermal data for the DRB package is derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
  (a) The exposed pad is connected to the PCB ground layer through a 2x2 thermal via array.
  (b) The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
  (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, see the *Power Dissipation* and *Estimating Junction Temperature* sections of this data sheet.
(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(6) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

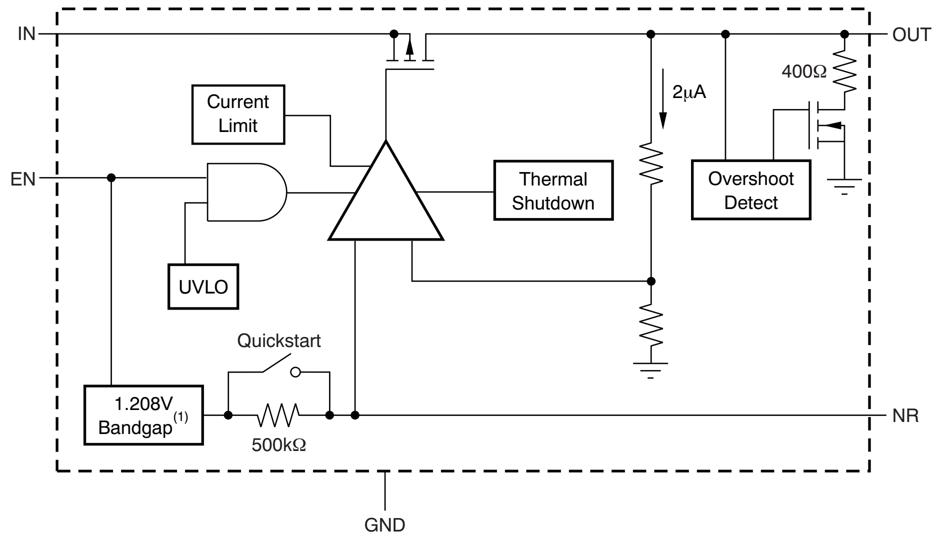
ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = 3.9V; I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{OUT} = 2.2µF, C_{NR} = 0.01µF, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			3.9		6.5	V
V_{OUT}	Output accuracy	Nominal	T_J = +25°C	–1.0		+1.0	%
V_{OUT}	Output accuracy	DRB package over V_{IN}, I_{OUT}, Temp	V_{OUT} + 0.3V ≤ V_{IN} ≤ V_{OUT} > 6.5V 1mA ≤ I_{OUT} ≤ 500mA, V_{OUT} > 2.2V	–2.0	±1.0	+2.0	%
ΔV_{OUT}%/ ΔV_{IN}	Line regulation		$V_{OUT(NOM)}$ + 0.3V ≤ V_{IN} ≤ 6.5V		0.02		%/V
ΔV_{OUT}%/ ΔI_{OUT}	Load regulation		500µA ≤ I_{OUT} ≤ 500mA		0.005		%/mA
V_{DO}	Dropout voltage (V_{IN} = $V_{OUT(NOM)}$ – 0.1V)		I_{OUT} = 500mA		280	500	mV
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(NOM)}$ V_{IN} = $V_{OUT(NOM)}$ + 0.9V, V_{IN} ≥ 2.7V	800	1170	1720	mA
I_{GND}	Ground pin current		500µA ≤ I_{OUT} ≤ 500mA		45	65	µA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4V		0.15	1.0	µA
PSRR	Power-supply rejection ratio V_{IN} = 3.85V, V_{OUT} = 2.85V, C_{NR} = 0.01µF, I_{OUT} = 100mA		f = 100Hz		60		dB
			f = 1kHz		56		dB
			f = 10kHz		41		dB
			f = 100kHz		28		dB
V_N	Output noise voltage BW = 10Hz to 100kHz, V_{OUT} = 2.8V		C_{NR} = 0.01µF		11 x V_{OUT}		μV_{RMS}
			C_{NR} = none		95 x V_{OUT}		μV_{RMS}
T_{STR}	Startup time, V_{OUT}= 0% to 90% V_{OUT} = 2.85V, R_L = 14Ω, C_{OUT} = 2.2µF		C_{NR} = none		45		µs
			C_{NR} = 0.001µF		45		µs
			C_{NR} = 0.01µF		50		µs
			C_{NR} = 0.047µF		50		µs
$V_{EN(HI)}$	Enable high (enabled)			1.2		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)			0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled		V_{EN} = V_{IN} = 6.5V		0.03	1.0	µA
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		165		°C
			Reset, temperature decreasing		145		°C
T_J	Operating junction temperature			–40		+125	°C
UVLO	Under-voltage lock-out		V_{IN} rising	1.90	2.20	2.65	V
	Hysteresis		V_{IN} falling		70		mV

DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM

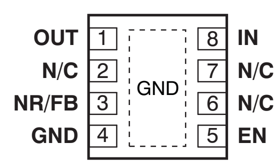


NOTE (1): Fixed voltage versions between 1.0V to 1.2V have a 1.0V bandgap circuit instead of a 1.208V bandgap circuit.

Figure 2. Fixed Voltage Version

PIN CONFIGURATION

DRB PACKAGE
3mm × 3mm SON-6
(TOP VIEW)



PIN DESCRIPTIONS

TPS73534		
NAME	DRB	DESCRIPTION
IN	8	Input supply.
GND	4	Ground. The pad must be tied to GND.
EN	5	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
NR	3	Fixed voltage versions only; connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This allows output noise to be reduced to very low levels.
FB	3	Adjustable version only; this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	1	Output of the regulator. A small capacitor (total typical capacitance ≥ 2.0μF ceramic) is needed from this pin to ground to assure stability.
N/C	2, 6, 7	Not internally connected. This pin must either be left open, or tied to GND.

TYPICAL CHARACTERISTICS

Over operating temperature range (T_J= –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 1mA, V_{EN} = V_{IN},C_{OUT} = 2.2μF, C_{NR} = 0.01μF, unless otherwise noted. Typical values are at T_J = +25°C.

TPS73501 LINE REGULATION

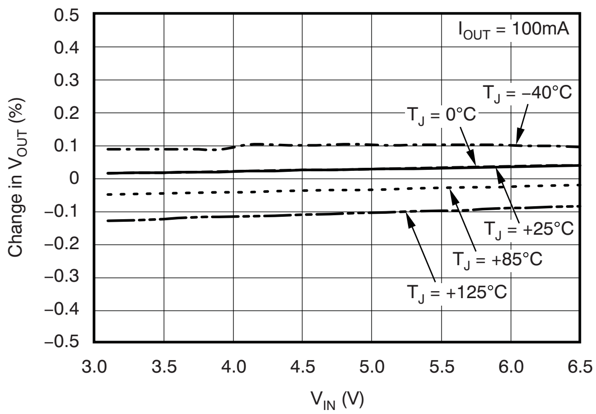


Figure 3.

TPS73525 LINE REGULATION

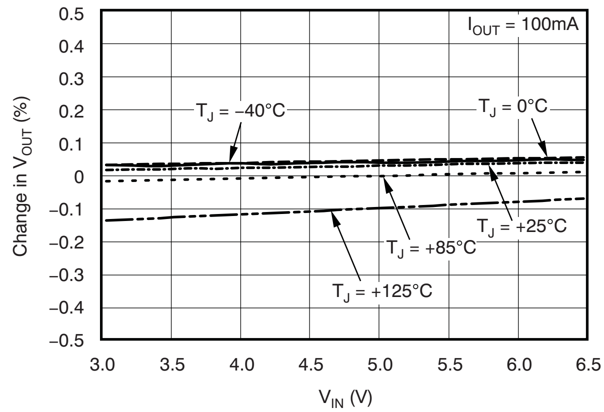


Figure 4.

TPS73501 LOAD REGULATION

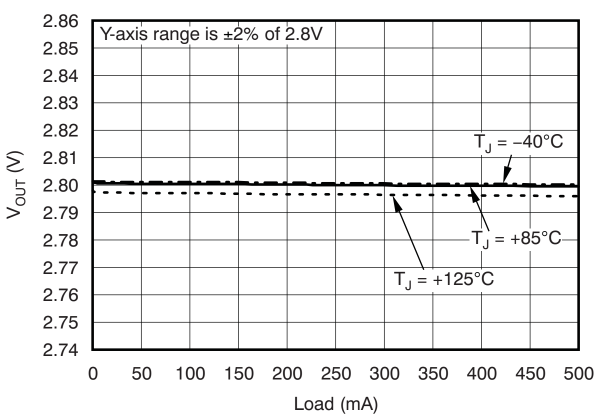


Figure 5.

TPS73525 LOAD REGULATION

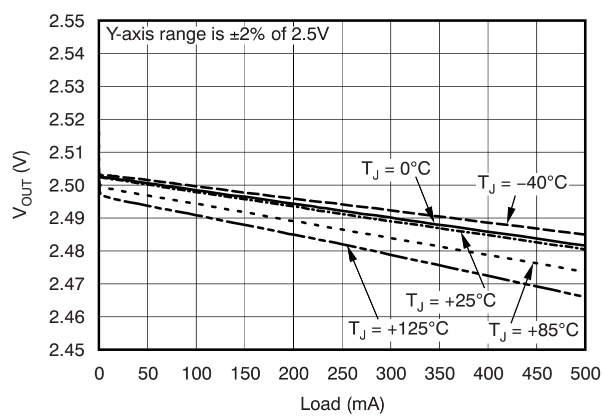


Figure 6.

TPS73525 GROUND PIN CURRENT vs OUTPUT CURRENT

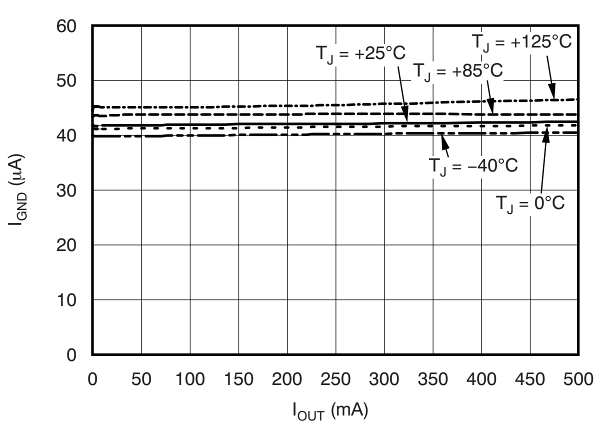


Figure 7.

TPS73525 GROUND PIN CURRENT (DISABLE) vs TEMPERATURE

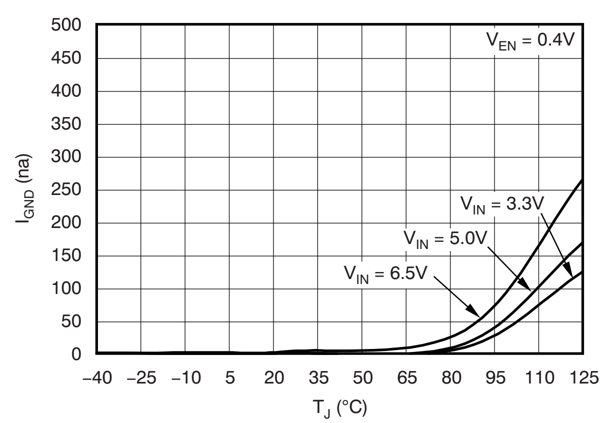


Figure 8.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 1mA, V_{EN} = V_{IN},C_{OUT} = 2.2µF, C_{NR} = 0.01µF, unless otherwise noted. Typical values are at T_J = +25°C.

TPS73501 DROPOUT VOLTAGE vs OUTPUT CURRENT

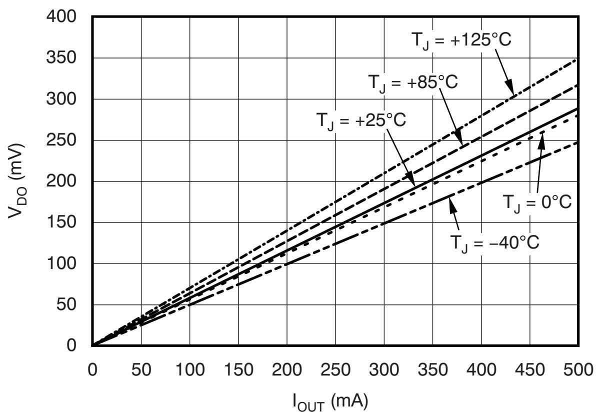


Figure 9.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 1.0V)

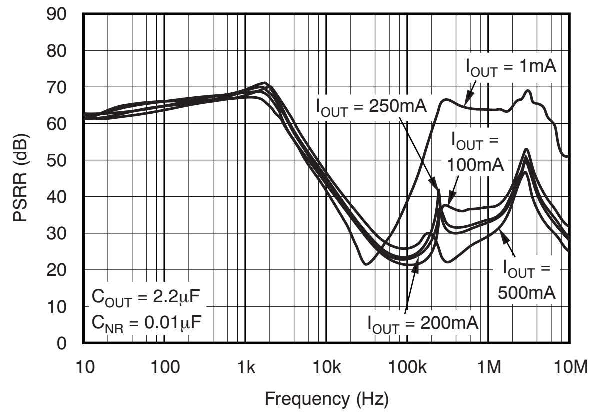


Figure 10.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 0.5V)

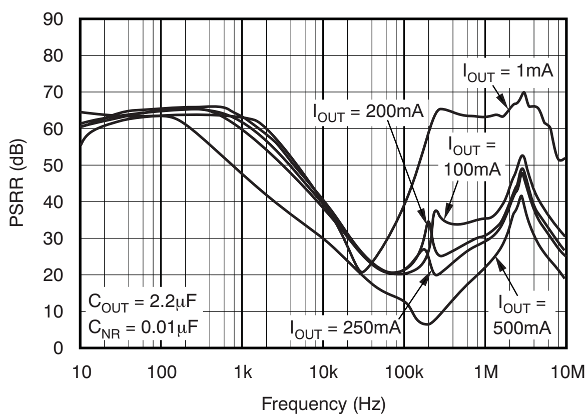


Figure 11.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 0.3V)

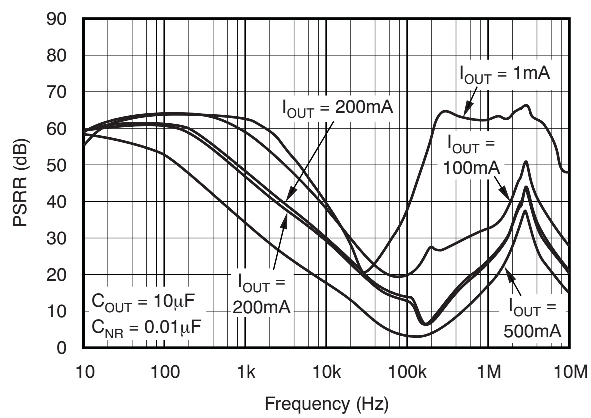


Figure 12.

TPS73525 TOTAL NOISE vs C_{NR}

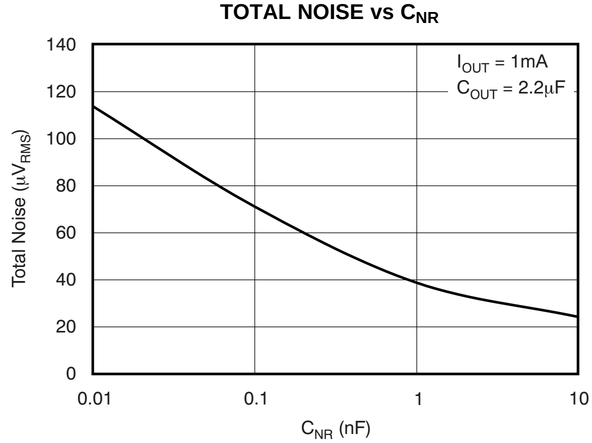


Figure 13.

TPS73525 TOTAL NOISE vs C_{OUT}

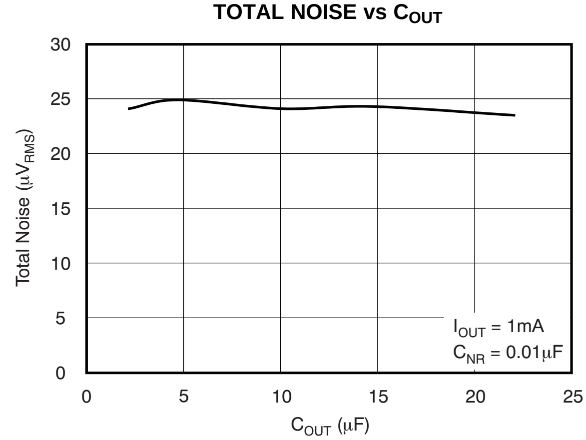


Figure 14.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 1mA, V_{EN} = V_{IN},C_{OUT} = 2.2μF, C_{NR} = 0.01μF, unless otherwise noted. Typical values are at T_J = +25°C.

TPS73525
TURN-ON RESPONSE
(V_{IN} = V_{EN})

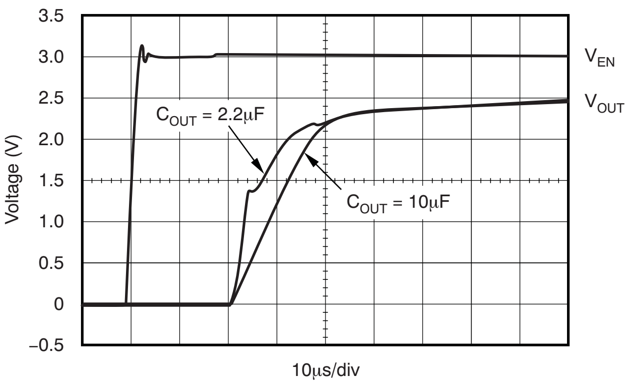


Figure 15.

TPS73525
EN RESPONSE OVER STABLE V_{IN}

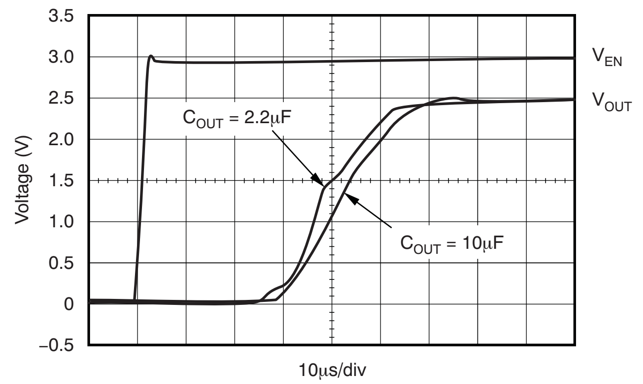


Figure 16.

TPS73525
POWER-UP/POWER-DOWN
(V_{IN} = V_{EN})

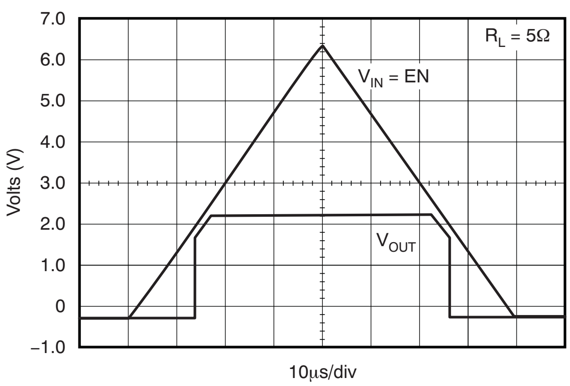


Figure 17.

TPS73525 LOAD TRANSIENT RESPONSE

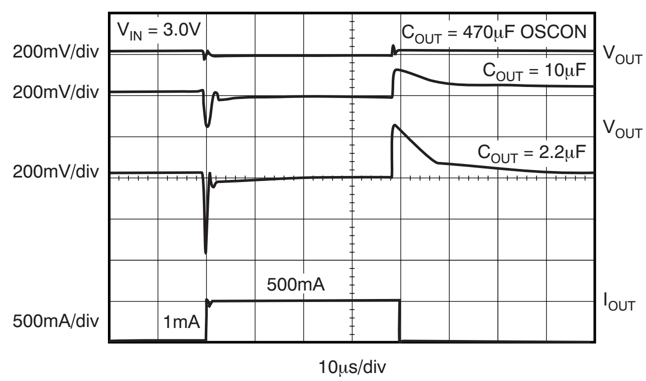


Figure 18.

TPS73525 LINE TRANSIENT RESPONSE

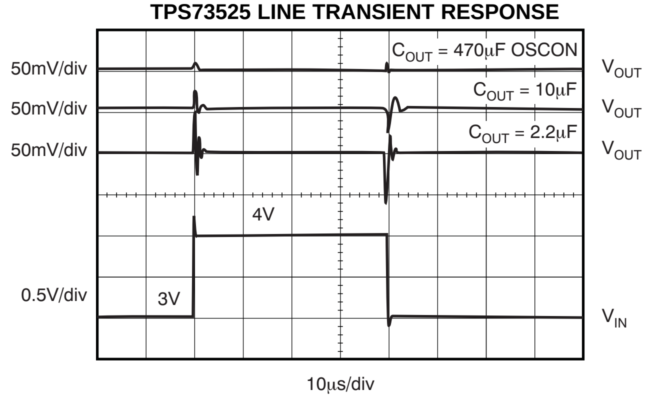


Figure 19.

APPLICATION INFORMATION

The TPS73534 LDO regulators combines the high performance required of many RF and precision analog applications with ultra-low current consumption. High PSRR is provided by a high gain, high bandwidth error loop with good supply rejection at very low headroom (V_{IN} – V_{OUT}). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the bandgap reference and to improve PSRR while a quick-start circuit fast-charges this capacitor at startup. The combination of high performance and low ground current also make the TPS73534 an excellent choice for portable applications. All versions have thermal and over-current protection and are fully specified from –40°C to +125°C.

Figure 20 shows the basic circuit connections for fixed voltage models. R_1 and R_2 can be calculated for any output voltage using the formula in .

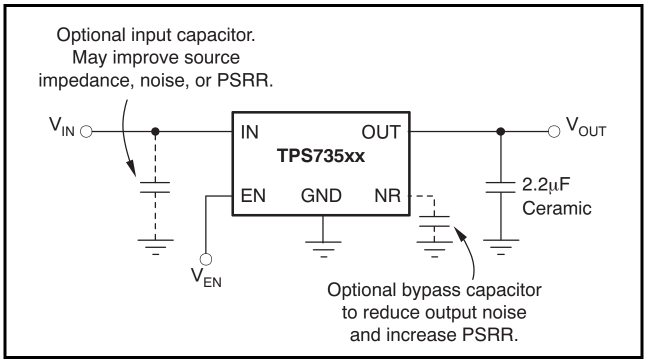


Figure 20. Typical Application Circuit for Fixed Voltage Versions

Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1μF to 1μF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. The ground of this capacitor should be connected as close as the ground of output capacitor; a capacitor value of 0.1μF is enough in this condition. When it is difficult to place these two ground points close together, a 1μF capacitor is recommended. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1μF input capacitor may be necessary to ensure stability.

The TPS73534 is designed to be stable with standard ceramic output capacitors of values 2.2μF or larger. X5R and X7R type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR of the output capacitor should be < 1.0Ω, so output capacitor type should be either ceramic or conductive polymer electrolytic.

Output Noise

In most LDOs, the bandgap is the dominant noise source. If a noise reduction capacitor (C_{NR}) is used with the TPS73534, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01μF noise reduction capacitor; for the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives 2μA of divider current has the same noise performance as a fixed voltage version. To further optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2Ω. This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

Noise can be referred to the feedback point (FB pin) such that with C_{NR} = 0.01μF, total noise is given approximately by Equation 1:

$$V_N = \frac{11\mu V_{RMS}}{V} \times V_{OUT} \quad (1)$$

Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Internal Current Limit

The TPS73534 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in current limit for extended periods of time.

The PMOS pass element in the TPS73534 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

Dropout Voltage

The TPS73534 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS,\ ON}$ of the PMOS pass element. Because the PMOS device behaves like a resistor in dropout, V_{DO} approximately scales with output current.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in the Typical Characteristics section.

Startup and Noise Reduction Capacitor

The TPS73534 uses a quick-start circuit to fast-charge the noise reduction capacitor, C_{NR}, if present (see the Functional Block Diagrams). This architecture allows the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate in this configuration.

Note that for fastest startup, V_{IN} should be applied first, then the enable pin (EN) driven high. If EN is tied to IN, startup is somewhat slower. Refer to the Typical Characteristics section. The quick-start switch is closed for approximately 135µs. To ensure that C_{NR} is fully charged during the quick-start time, a 0.01µF or smaller capacitor should be used.

Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response. In the adjustable version, adding C_{FB} between OUT and FB improves stability and transient response. The transient response of the TPS73534 is enhanced by an active pull-down that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pull-down device behaves like a 400Ω resistor to ground.

Undervoltage Lock-Out (UVLO)

The TPS73534 utilizes an undervoltage lock-out circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a de-glitch feature so that it typically ignores undershoot transients on the input if they are less than 50µs duration.

Minimum Load

The TPS73534 is stable and well-behaved with no output load. To meet the specified accuracy, a minimum load of 500µA is required. Below 500µA at junction temperatures near +125°C, the output can drift up enough to cause the output pull-down to turn on. The output pull-down limits voltage drift to 5% typically but ground current could increase by approximately 50µA. In typical applications, the junction cannot reach high temperatures at light loads because there is no appreciable dissipated power. The specified ground current would then be valid at no load in most applications.

Thermal Information

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS73534 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS73534 into thermal shutdown degrades device reliability.

Package Mounting

Solder pad footprint recommendations for the TPS73534 are available from the Texas Instruments web site at www.ti.com.

Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current time the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \quad (2)$$

Note: When the device is used in a condition of higher input and lower output voltages with the DRV and DRB packages, P_D exceeds the package rating at room temperature. This equation shows an example of the DRB package:

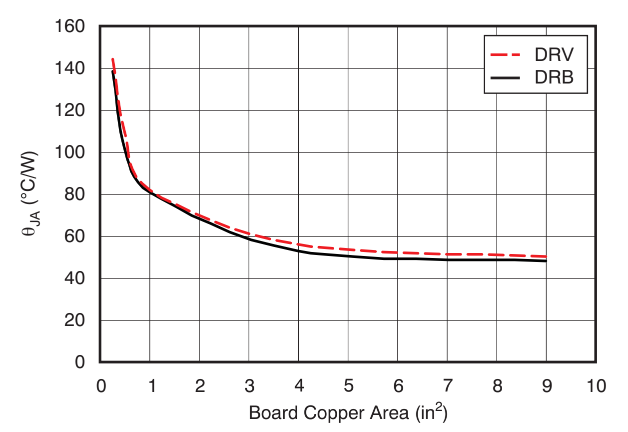
P_D = (6.5V – 1.0V) × 500mA = 2.75W, which is greater than 2.5W at +25°C.

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On both SON (DRB) and SON (DRV) packages, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 3:

$$R_{\theta JA} = \frac{(+125^{o}C - T_A)}{P_D} \quad (3)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 21.



Note: θ_{JA} value at board size of $9in^2$ (that is, 3in × 3in) is a JEDEC standard.

Figure 21. θ_{JA} vs Board Size

Figure 21 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

NOTE: When the device is mounted on an application PCB, it is strongly recommended to use Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

ESTIMATING JUNCTION TEMPERATURE

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 4). For backwards compatibility, an older θ_{JC},*Top* parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \qquad (4)$$

Where P_D is the power dissipation shown by Equation 2, T_T is the temperature at the center-top of the IC package, and T_B is the PCB temperature measured 1mm away from the IC package *on the PCB surface* (as Figure 23 shows).

NOTE: Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com.

By looking at Figure 22, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 4 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

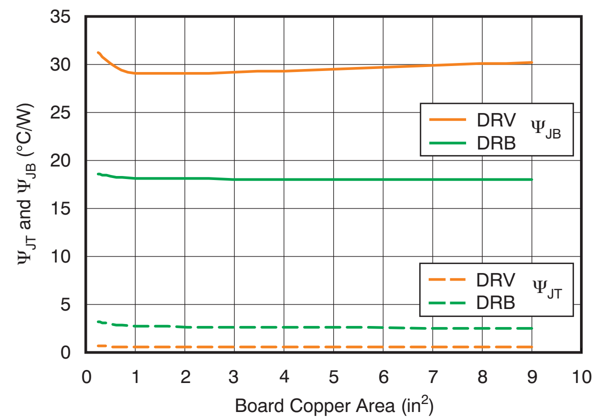
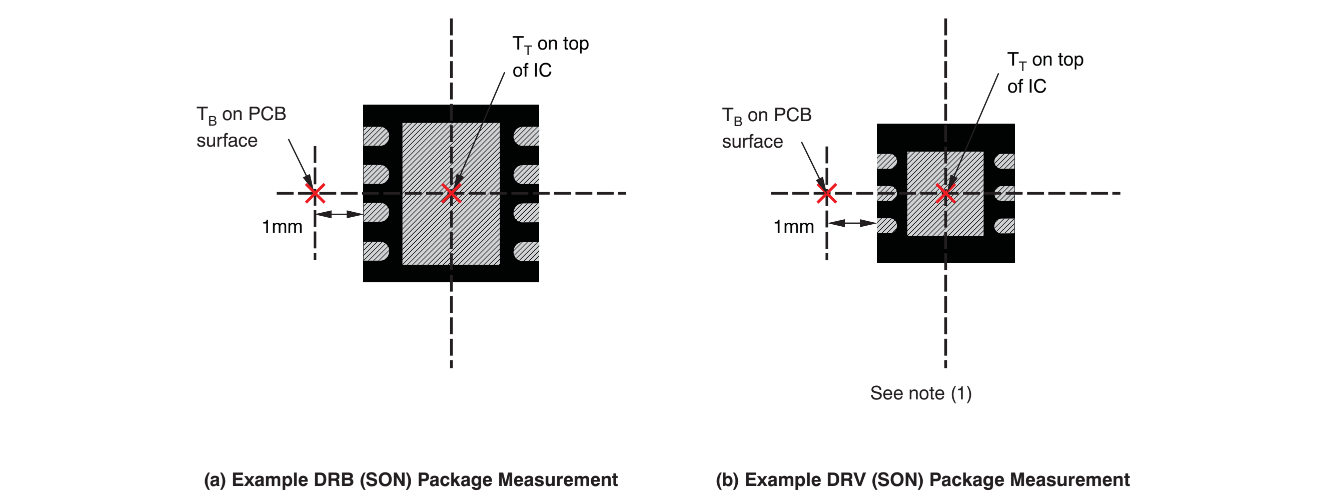


Figure 22. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, refer to application report SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com. For further information, refer to application report SPRA953, *IC Package Thermal Metrics*, also available on the TI website.



(1) Power dissipation may limit operating range. Check *Thermal Information* table.

Figure 23. Measuring Points for T_T and T_B

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS73534DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73534DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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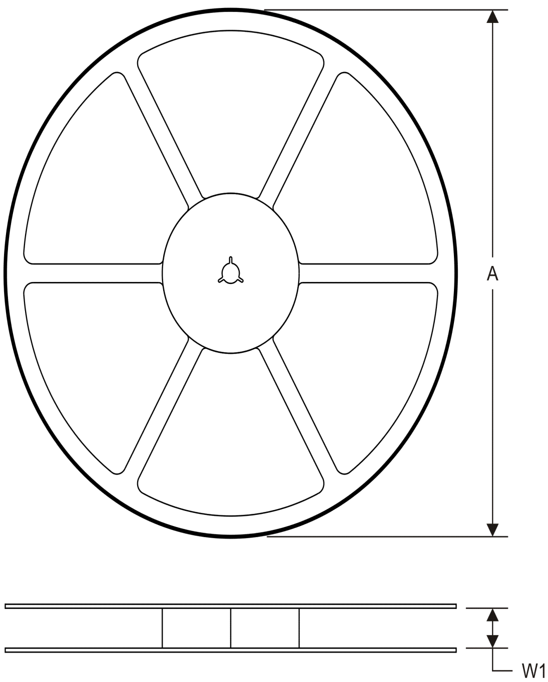
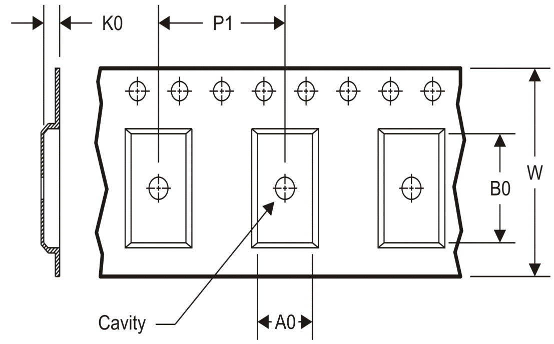
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



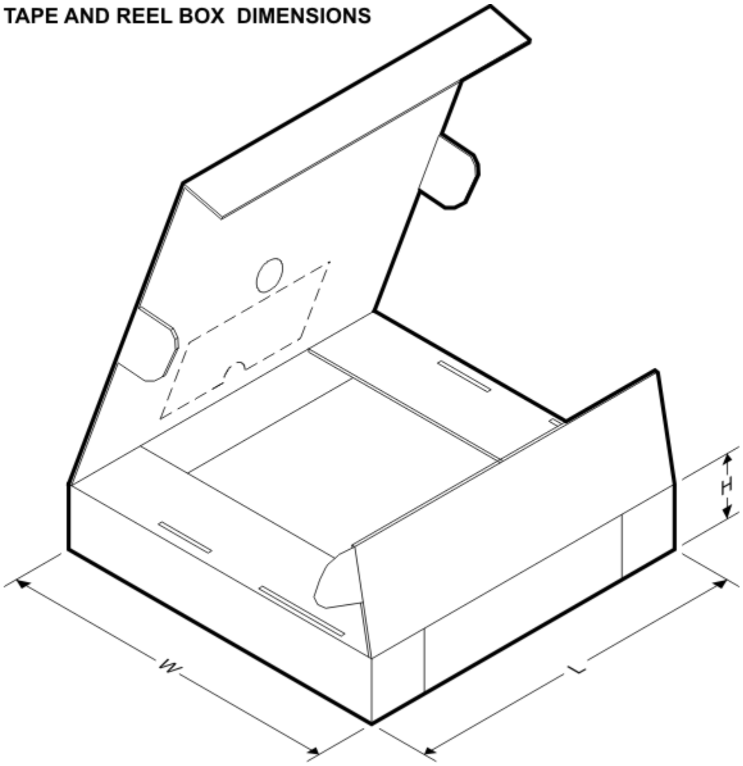
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73534DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73534DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

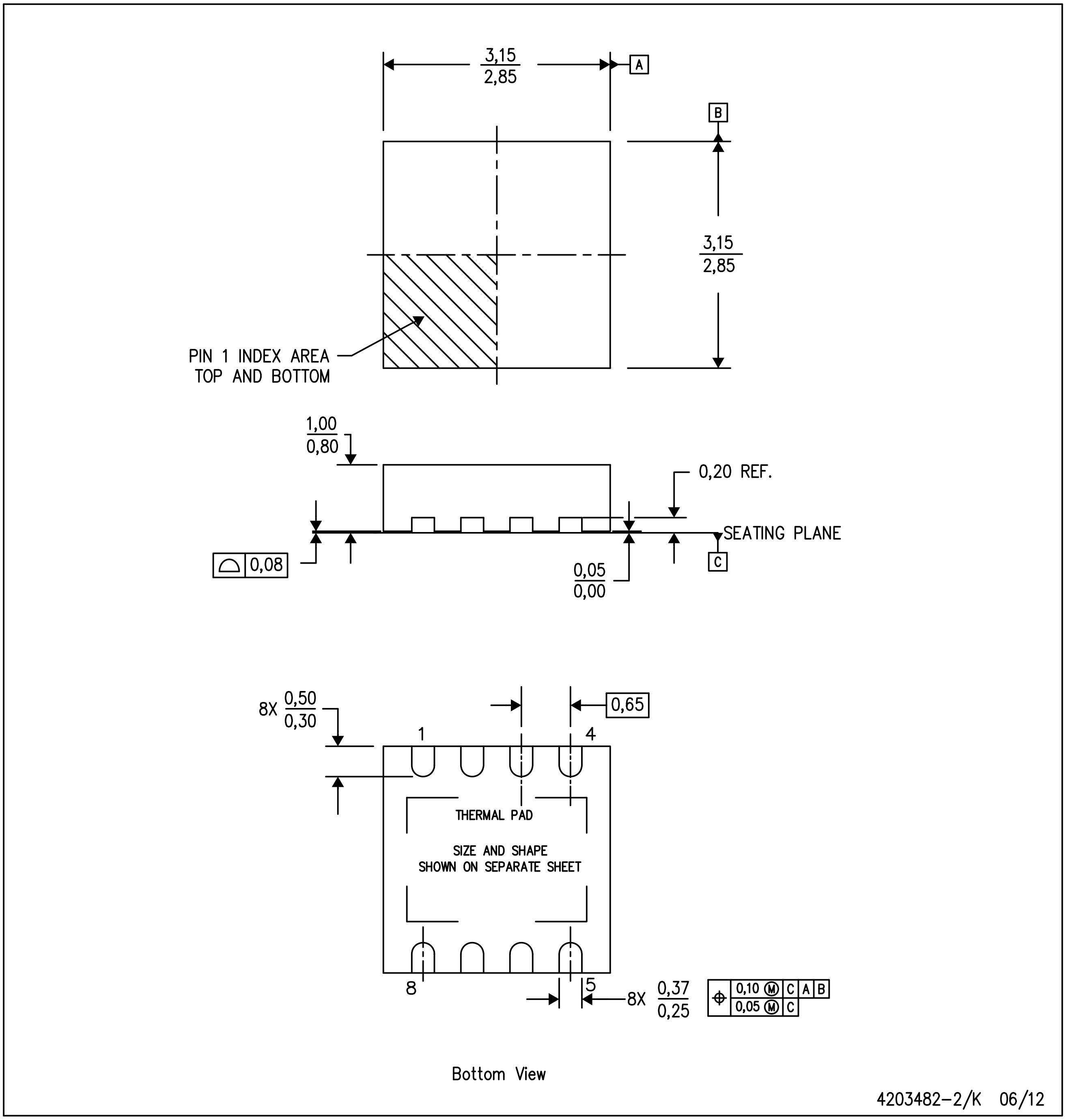
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73534DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS73534DRBT	SON	DRB	8	250	210.0	185.0	35.0

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

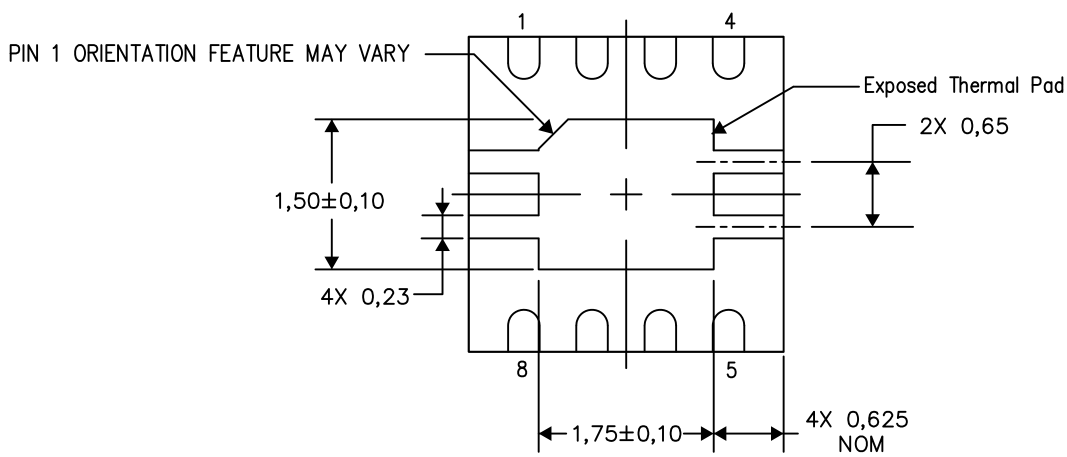
DRB (S-PVSON-N8) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



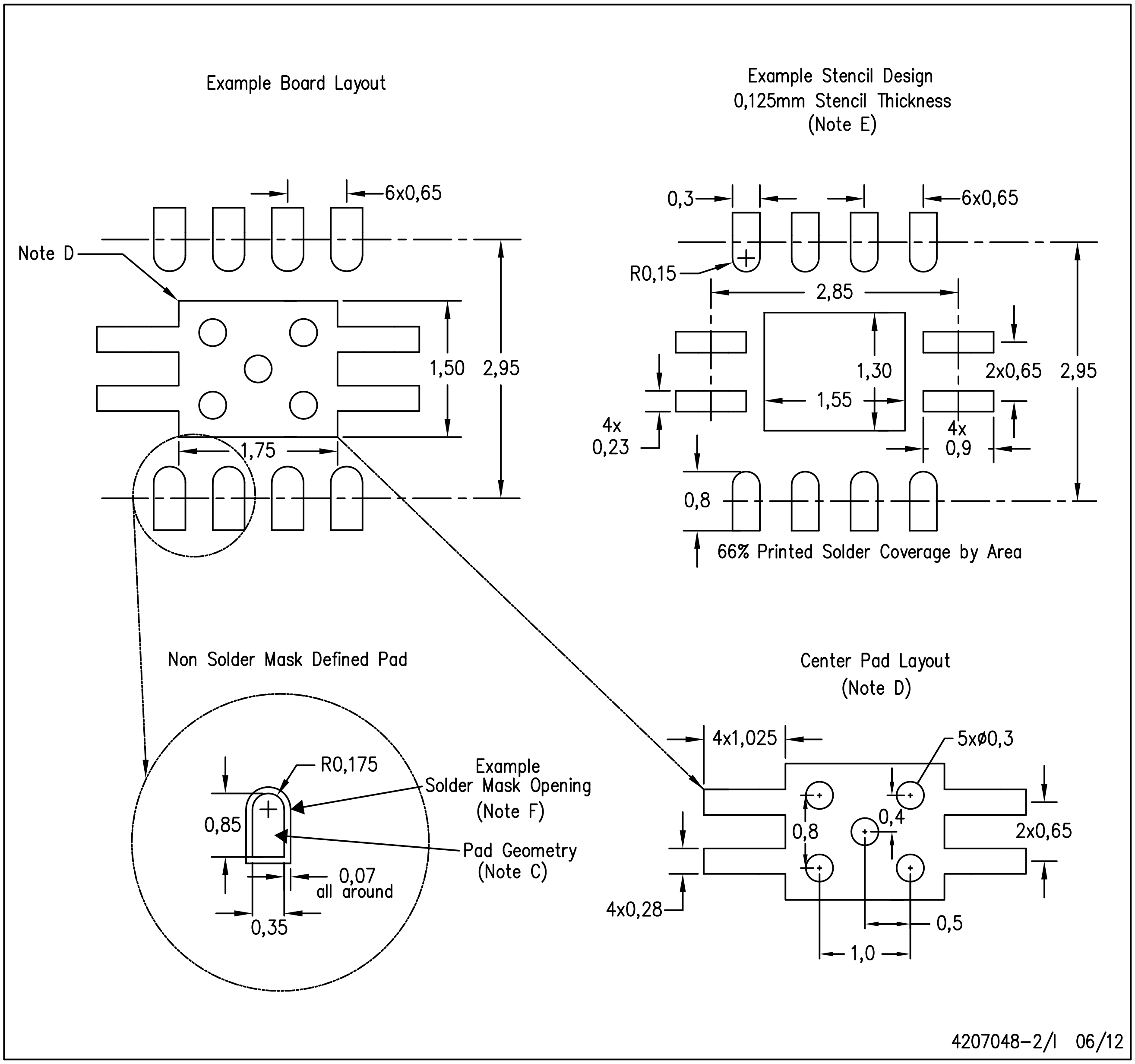
Bottom View

Exposed Thermal Pad Dimensions

4206340-2/M 06/12

NOTE: All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Publication IPC–7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

F. Customers should contact their board fabrication site for solder mask tolerances.

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