# Dual, 200mA Output, Low Noise, High PSRR Low-Dropout Linear Regulators

## FEATURES

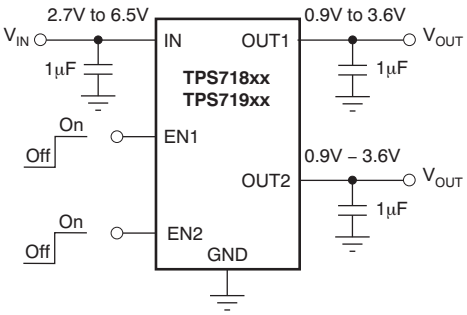
- **Dual, 200mA High-Performance LDOs**
- **Low Total Quiescent Current: 90μA with Both LDOs Enabled**
- **Low Noise: 70μ$V_{RMS}$/V**
- **Active Output Pulldown (TPS719xx)**
- **Independent Enables for Each LDO**
- **PSRR: 65dB at 1kHz, 45dB at 1MHz**
- **Available in Multiple Fixed-Output Voltage Combinations from 0.9V to 3.6V Using Innovative Factory EEPROM Programming**
- **Fast Start-Up Time: 160μs**
- **Over-Current, Over-Temperature and Under-Voltage Protection**
- **Low Dropout: 230mV at 200mA**
- **Stable with 1μF Ceramic Output Capacitor**
- **Available in 2mm × 2mm SON-6 and 6-Ball WCSP Packages**

## APPLICATIONS

- **Digital Cameras and Camera Modules**
- **Cellular Camera and TV Phones**
- **Wireless LAN, Bluetooth®**
- **Handheld Products**

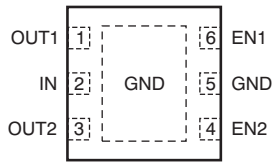
## DESCRIPTION

The TPS718xx and TPS719xx families of low-dropout (LDO) regulators offer a high power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient responses while consuming a very low 90μA (typical) at no load ground current with both LDOs enabled. The TPS719xx also provides an active pulldown circuit to quickly discharge output loads. The TPS718xx and TPS719xx are stable with ceramic capacitors and use an advanced BiCMOS fabrication process to yield a typical dropout voltage of 230mV at 200mA output loads. The TPS718xx and TPS719xx also use a precision voltage reference and feedback loop to achieve 3% overall accuracy over all load, line, process, and temperature variations. Both families of devices are fully specified from $T_J$ = –40°C to +125°C and are offered in 2mm × 2mm SON-6 and 6-ball Wafer Chip-Scale (WCSP) packages that are ideal for applications such as mobile handsets and WLAN that require good thermal dissipation while maintaining a very small footprint.

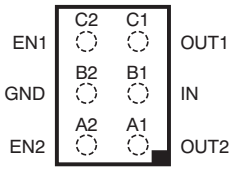



Typical Application Circuit

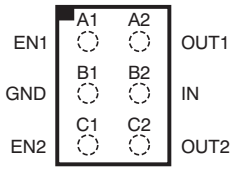
**TPS718xx, TPS719xx**
**DRV Package**
**2mm x 2mm SON-6**
**(Top View)**




**TPS718xx, TPS719xx**
**YZC Package**
**6-BALL WCSP**
**(Top View)**




**TPS718Axx, TPS719Axx**
**YZC Package**
**6-BALL WCSP**
**(Top View)**



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)

| PRODUCT | $V_{OUT}$(2)(3) |
|---|---|
| TPS718***xx-yywwwz***<br>TPS718A***xx-yywwwz***<br>TPS719***xx-yywwwz***<br>TPS719A***xx-yywwwz*** | **A** denotes device with rotated pin 1 orientation of wafer-chipscale package.<br>**XX** is nominal output voltage for LDO1 (for example, 28 = 2.8V).<br>**YY** is nominal output voltage for LDO2.<br>**WWW** is package designator.<br>**Z** is tape and reel quantity (R = 3000, T = 250). |
| ***Examples:*** TPS71918–285DRVR<br>TPS719185-33DRVR | **XX** = 18 = 1.8V, **YYY** = 285 = 2.85V<br>**XXX** = 185 = 1.85V, **YY** = 33 = 3.3V<br>**DRV** = 2mm x 2mm SON package<br>**Z** = R = 3000 piece reel |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Both outputs are programmable from 0.9V to 3.6V in 50mV increments.
(3) Output voltages from 0.9V to 3.6V in 50mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating temperature range (unless otherwise noted). All voltages are with respect to GND.

| PARAMETER | TPS718xx, TPS719xx | UNIT |
|---|---|---|
| Input voltage range, $V_{IN}$ | –0.3 to +7.0 | V |
| Enable voltage range, $V_{EN1}$ and $V_{EN2}$ | –0.3 to $V_{IN}$ + 0.3V | V |
| Output voltage range, $V_{OUT}$ | –0.3 to +7.0 | V |
| Peak output current | Internally limited | |
| Output short-circuit duration | Indefinite | |
| Junction temperature range, $T_J$ | –55 to +150 | °C |
| Storage temperature range , $T_{STG}$ | –55 to +150 | °C |
| Total continuous power dissipation, $P_{DISS}$ | See Dissipation Ratings Table | |
| ESD rating, HBM | 2 | kV |
| ESD rating, CDM | 500 | V |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

## DISSIPATION RATINGS

| BOARD | PACKAGE | $R_{\theta JC}$ | $R_{\theta JA}$ | DERATING FACTOR ABOVE $T_A$ = +25°C | $T_A$ < +25°C | $T_A$ = +70°C | $T_A$ = +85°C |
|---|---|---|---|---|---|---|---|
| High-K(1) | DRV | 20°C/W | 95°C/W | 10.53mW/°C | 1053mW | 579mW | 421mW |
| High-K(1) | YZC | 27°C/W | 190°C/W | 5.3mW/°C | 530mW | 295mW | 215mW |

(1) The JEDEC high-K (2s2p) board used to derive this data was a 3in × 3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

## ELECTRICAL CHARACTERISTICS

Over operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; $I_{OUT}$ = 0.5mA, $V_{EN1}$ = $V_{EN2}$ = $V_{IN}$, $C_{OUT}$ = 1.0µF, unless otherwise noted. Typical values are at $T_J$ = +25°C.

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range(1) | | | 2.7 | | 6.5 | V |
| $V_{OUT1}$, $V_{OUT2}$ | Output voltage range | | | 0.9 | | 3.6 | V |
| $V_{OUT1}$, $V_{OUT2}$ | Output accuracy | Nominal | $T_J$ = +25°C | | ±2.5 | | mV |
| | | Over $V_{IN}$, $I_{OUT}$, Temp | $V_{OUT}$ + 0.5V ≤ $V_{IN}$ ≤ 6.5V<br>0mA ≤ $I_{OUT}$ ≤ 200mA | –3.0 | | +3.0 | % |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line regulation | | $V_{OUT(NOM)}$ + 0.5V ≤ $V_{IN}$ ≤ 6.5V,<br>$I_{OUT}$ = 5mA | | 130 | | µV/V |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation | | 0mA ≤ $I_{OUT}$ ≤ 200mA | | 75 | | µV/mA |
| $V_{DO}$ | Dropout voltage(2)<br>($V_{IN}$ = $V_{OUT(NOM)}$ – 0.1V) | | $I_{OUT}$ = 200mA | | 230 | 400 | mV |
| $I_{CL}$ | Output current limit (per output) | | $V_{OUT}$ = 0.9 × $V_{OUT(NOM)}$ | 240 | 340 | 575 | mA |
| $I_{GND}$ | Ground pin current | | $I_{OUT1}$ = $I_{OUT2}$ = 0.1mA | | 90 | 160 | µA |
| | | | $I_{OUT1}$ = $I_{OUT2}$ = 200mA | | 250 | | µA |
| $I_{SHDN}$ | Shutdown current ($I_{GND}$) | | $V_{EN1,2}$ ≤ 0.4V, 2.7V ≤ $V_{IN}$ < 4.5V,<br>$T_J$ = –40°C to +85°C | | 0.3 | 3.0 | µA |
| | | | $V_{EN1,2}$ ≤ 0.4V, 4.5V ≤ $V_{IN}$ ≤ 6.5V,<br>$T_J$ = –40°C to +85°C | | 1.8 | | µA |
| PSRR | Power-supply rejection ratio<br>$V_{IN}$ = 3.8V, $V_{OUT}$ = 2.8V,<br>$I_{OUT}$ = 200mA | | f = 100Hz | | 63 | | dB |
| | | | f = 1kHz | | 63 | | dB |
| | | | f = 10kHz | | 72 | | dB |
| | | | f = 100kHz | | 58 | | dB |
| | | | f = 1MHz | | 44 | | dB |
| $V_N$ | Output noise voltage<br>BW = 100Hz to 100kHz | | | | 70 × $V_{OUT}$ | | $\mu V_{RMS}$ |
| $T_{STR}$ | Startup time(3) | | $R_L$ = 14Ω, $V_{OUT}$ = 2.8V,<br>$C_{OUT}$ = 1.0µF | | 160 | | µs |
| $T_{SHUT}$ | Shutdown time(4), (5)<br>(TPS719xx only) | | $R_L$ = ∞, $C_{OUT}$ = 1.0µF,<br>$V_{OUT}$ = 2.8V | | 180 | | µs |
| $V_{EN(HI)}$ | Enable high (enabled)<br>(EN1 and EN2) | | $V_{IN}$ ≤ 5.5V | 1.2 | | 6.5 | V |
| | | | 5.5V < $V_{IN}$ ≤ 6.5V | 1.25 | | 6.5 | V |
| $V_{EN(LO)}$ | Enable low (shutdown)<br>(EN1 and EN2) | | | 0 | | 0.4 | V |
| $I_{EN}$ | Enable pin current, enabled<br>(EN1 and EN2) | | EN1 = EN2 = 6.5V | | 0.04 | 1.0 | µA |
| UVLO | Undervoltage lockout | | $V_{IN}$ rising | 2.38 | 2.45 | 2.52 | V |
| | Hysteresis | | $V_{IN}$ falling | | 150 | | mV |
| $T_{SD}$ | Thermal shutdown temperature | | Shutdown, temperature increasing | | +160 | | °C |
| | | | Reset, temperature decreasing | | +140 | | °C |
| $T_J$ | Operating junction temperature | | | –40 | | +125 | °C |

(1) Minimum $V_{IN}$ = $V_{OUT}$ + $V_{DO}$ or 2.7V, whichever is greater.
(2) $V_{DO}$ is not measured for devices with $V_{OUT(NOM)}$ < 2.8V because minimum $V_{IN}$ = 2.7V.
(3) Time from $V_{EN}$ = 1.25V to $V_{OUT}$ = 95% ($V_{OUT(NOM)}$).
(4) Time from $V_{EN}$ = 0.4V to $V_{OUT}$ = 5% ($V_{OUT(NOM)}$).
(5) See *Shutdown* section in the Applications Information for more details.

## DEVICE INFORMATION

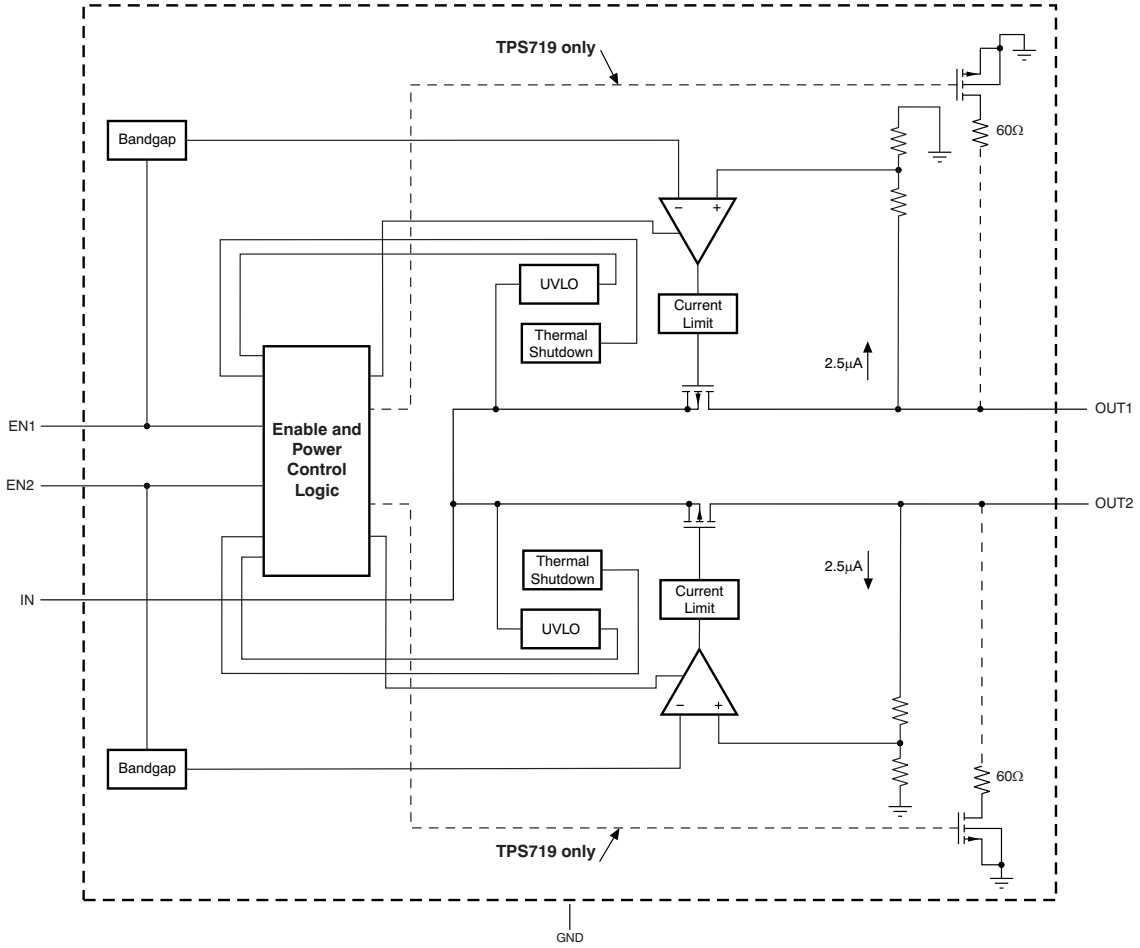
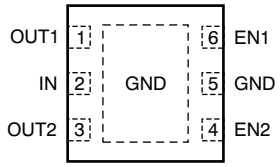
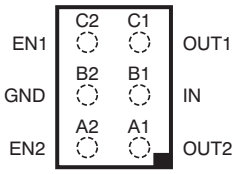



**Figure 1. Functional Block Diagram**

**DRV PACKAGE**
**SON-6**
**(TOP VIEW)**

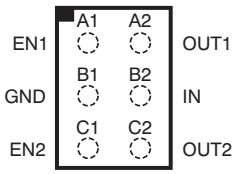



**YZC PACKAGE**
**6-BALL WCSP**
**(TOP VIEW)**




**TPS718xx**
**TPS719xx**

**YZC PACKAGE**
**6-BALL WCSP**
**(TOP VIEW)**




**TPS718Axx**
**TPS719Axx**

## PIN DESCRIPTIONS

| TPS718xx TPS719xx | | | TPS718Axx(1) TPS719Axx(1) | |
|---|---|---|---|---|
| **NAME** | **DRV** | **YZC** | **YZC** | **DESCRIPTION** |
| OUT1 | 1 | C1 | A2 | Output of Regulator 1. A small ceramic capacitor (typically ≥ 1μF) is needed from this pin to ground to assure stability. |
| IN | 2 | B1 | B2 | Input supply to both regulators. |
| OUT2 | 3 | A1 | C2 | Output of Regulator 2. A small ceramic capacitor (typically ≥ 1μF) is needed from this pin to ground to assure stability. |
| EN2 | 4 | A2 | C1 | Enable pin for Regulator 2. Driving the Enable pin (EN2) high turns on Regulator 2. Driving this pin low puts Regulator 2 into shutdown mode, reducing operating current. |
| GND | 5 | B2 | B1 | Ground. DRV thermal pad should also be connected to ground. |
| EN1 | 6 | C2 | A1 | Enable pin for Regulator 1. Driving the Enable pin (EN1) high turns on Regulator 1. Driving this pin low puts Regulator 1 into shutdown mode, reducing operating current. |

(1) **A** option denotes devices with rotated Pin 1 orientation on Wafer Chipscale packages.

## TYPICAL CHARACTERISTICS

Over operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; $I_{OUT}$ = 0.5mA, $V_{EN1}$ = $V_{EN2}$ = $V_{IN}$, $C_{OUT}$ = 1.0µF, unless otherwise noted. Typical values are at $T_J$ = +25°C.

**LINE REGULATION**

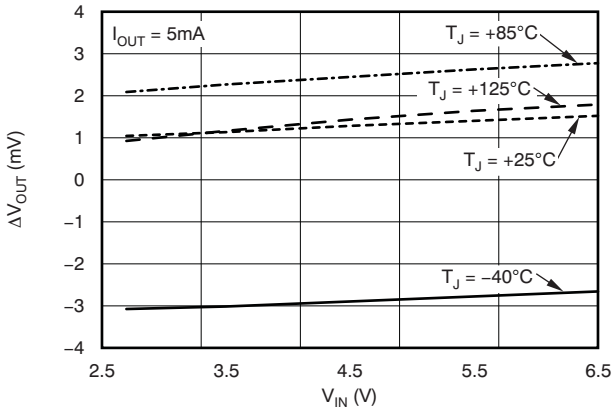



**Figure 2.**

**LINE REGULATION**

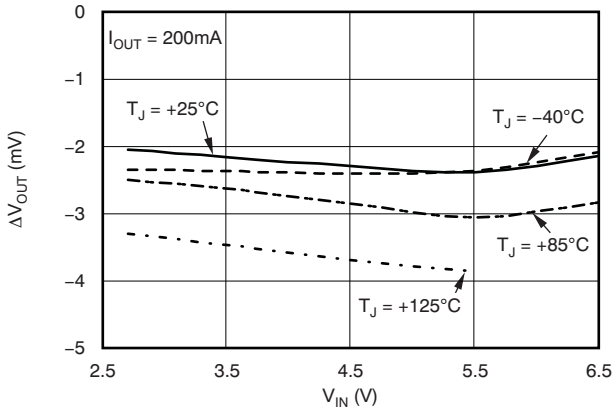



**Figure 3.**

**LOAD REGULATION UNDER LIGHT LOADS**

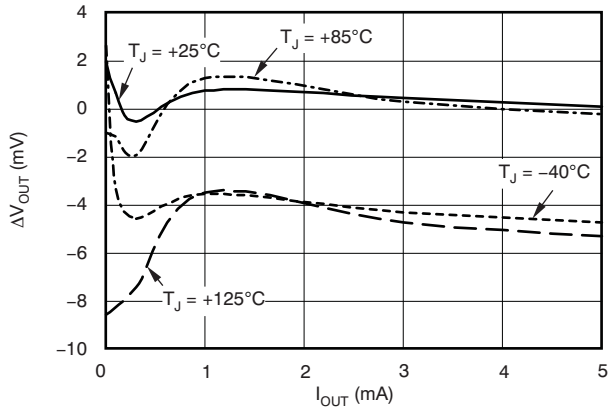



**Figure 4.**

**LOAD REGULATION**

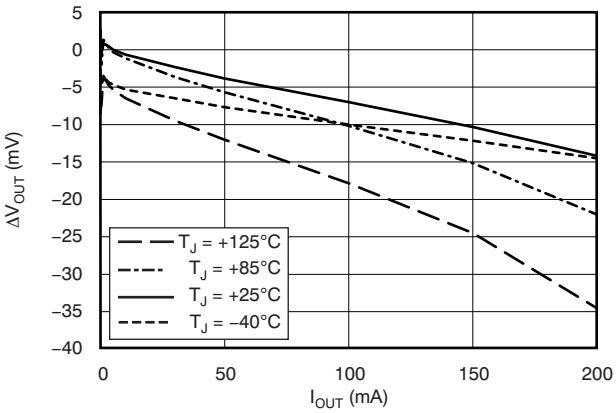



**Figure 5.**

**OUTPUT VOLTAGE vs TEMPERATURE**

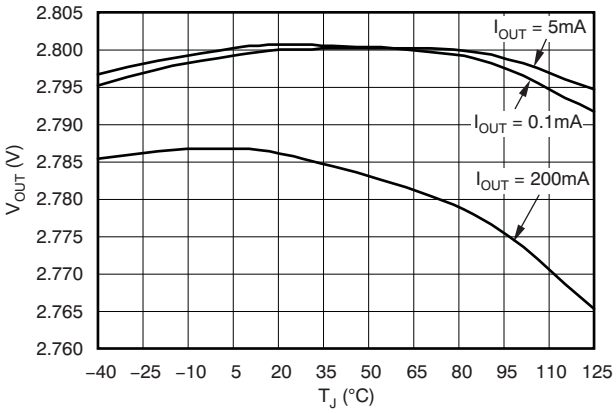



**Figure 6.**

**DROPOUT VOLTAGE vs OUTPUT CURRENT**

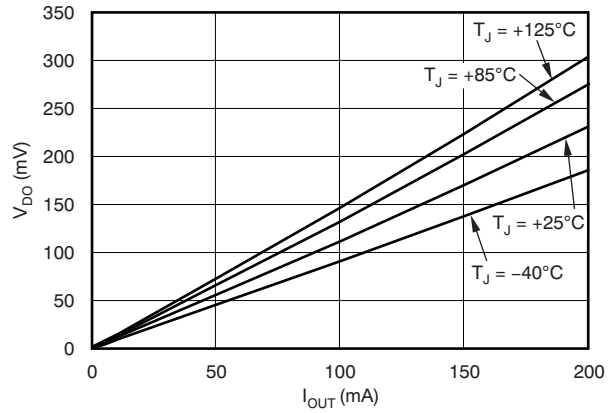



**Figure 7.**

## TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; $I_{OUT}$ = 0.5mA, $V_{EN1}$ = $V_{EN2}$ = $V_{IN}$, $C_{OUT}$ = 1.0µF, unless otherwise noted. Typical values are at $T_J$ = +25°C.

**GROUND PIN CURRENT vs OUTPUT CURRENT**

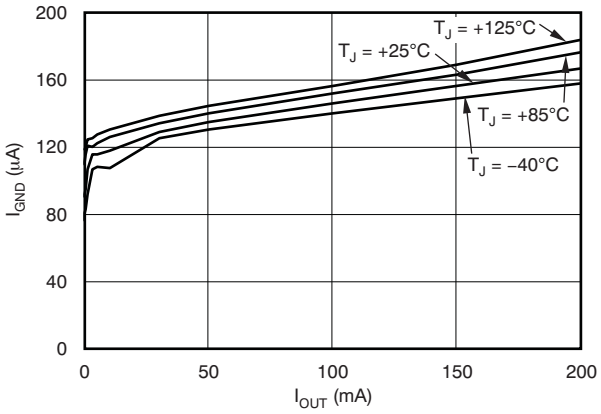



**Figure 8.**

**GROUND PIN CURRENT vs INPUT VOLTAGE**

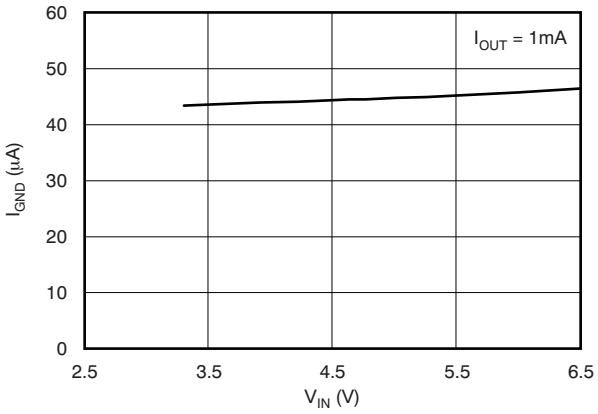



**Figure 9.**

**GROUND PIN CURRENT vs TEMPERATURE (BOTH LDOs ENABLED)**

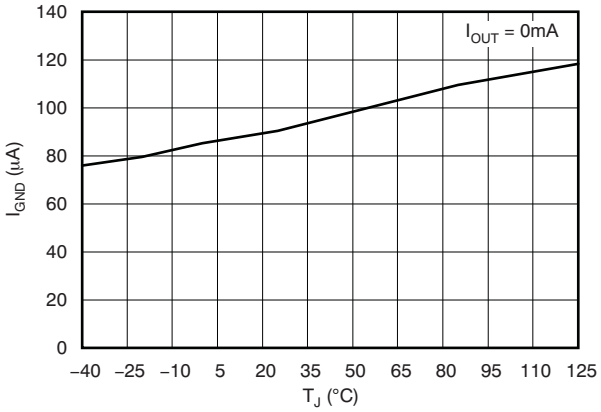



**Figure 10.**

**SHUTDOWN CURRENT vs INPUT VOLTAGE**

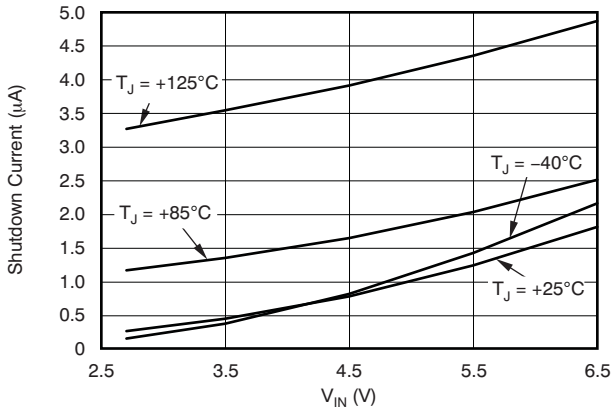



**Figure 11.**

**CURRENT LIMIT vs INPUT VOLTAGE**

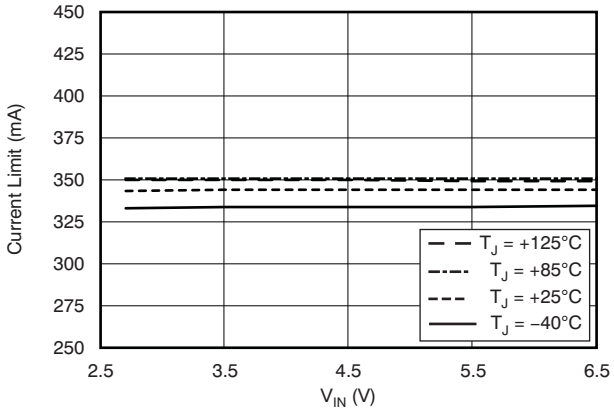



**Figure 12.**

**POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY ($V_{IN}$ – $V_{OUT}$ = 0.5V)**

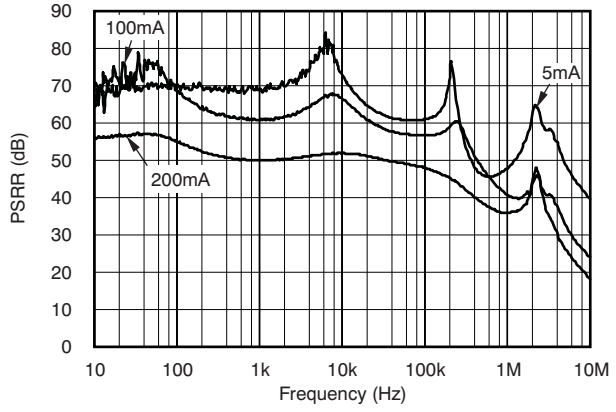



**Figure 13.**

## TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; $I_{OUT}$ = 0.5mA, $V_{EN1}$ = $V_{EN2}$ = $V_{IN}$, $C_{OUT}$ = 1.0µF, unless otherwise noted. Typical values are at $T_J$ = +25°C.

**POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY ($V_{IN}$ – $V_{OUT}$ = 1V)**

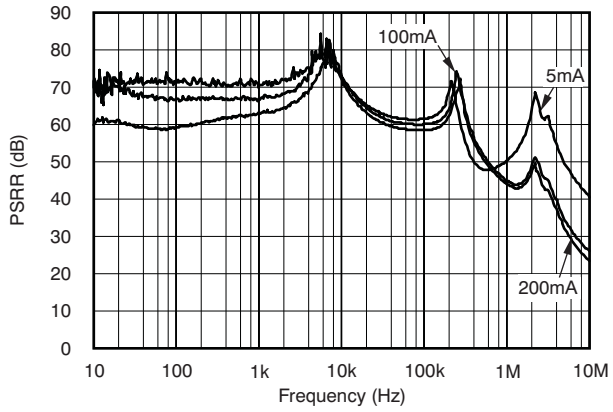



**Figure 14.**

**POWER-SUPPLY RIPPLE REJECTION vs INPUT VOLTAGE**

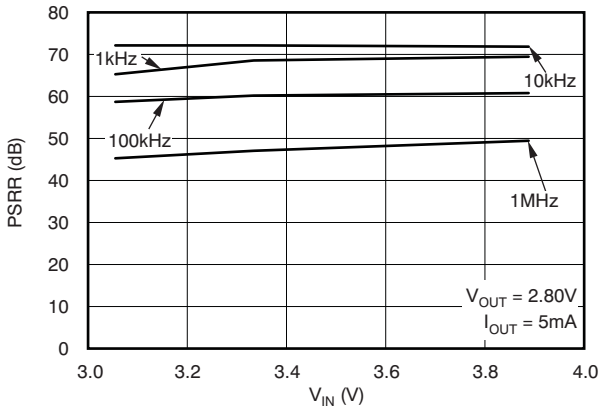



**Figure 15.**

**POWER-SUPPLY RIPPLE REJECTION vs INPUT VOLTAGE**

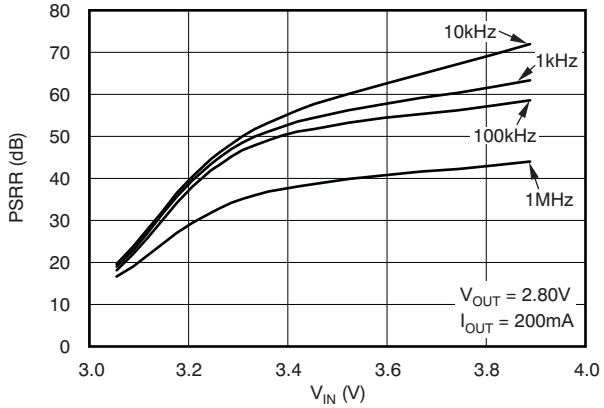



**Figure 16.**

**OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY**

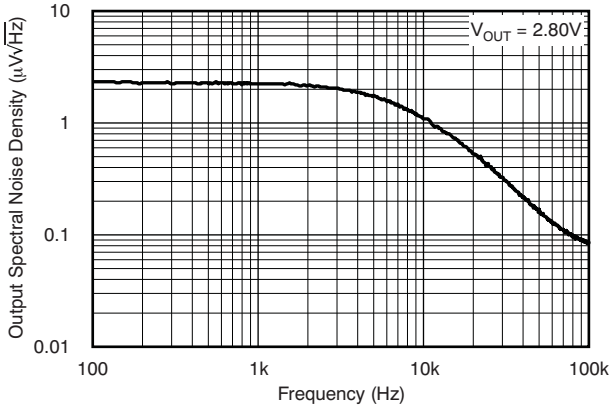



**Figure 17.**

**LINE TRANSIENT RESPONSE**

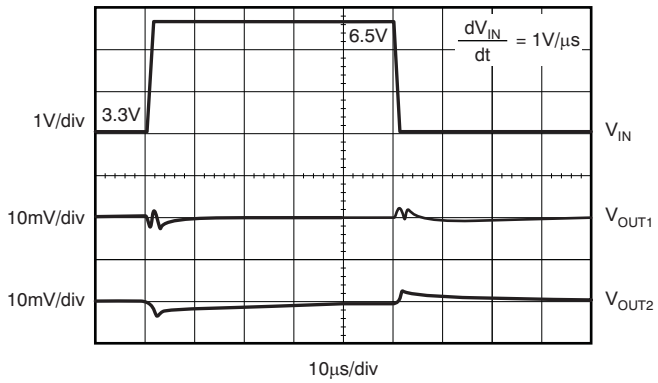



**Figure 18.**

**LOAD TRANSIENT RESPONSE**

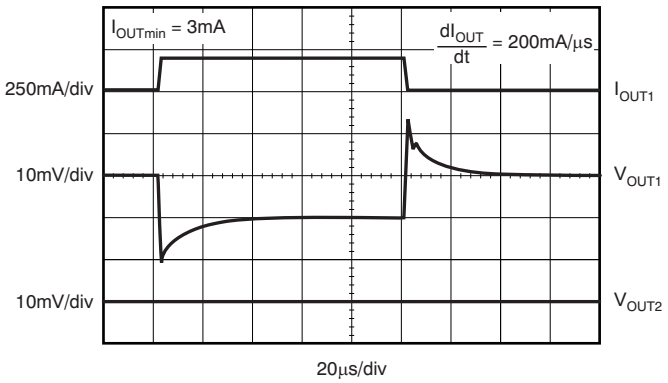



**Figure 19.**

## TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; $I_{OUT}$ = 0.5mA, $V_{EN1}$ = $V_{EN2}$ = $V_{IN}$, $C_{OUT}$ = 1.0µF, unless otherwise noted. Typical values are at $T_J$ = +25°C.

**TPS719 ENABLE RESPONSE**

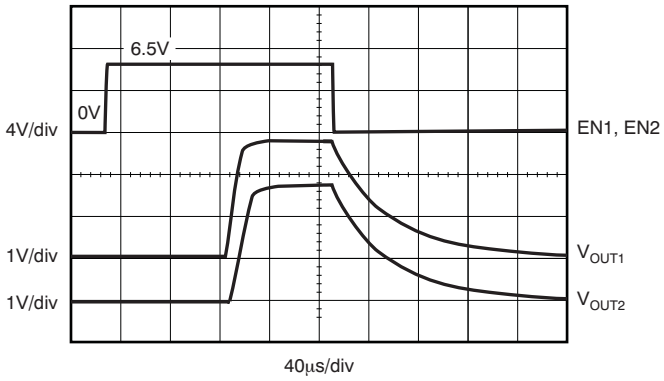



**Figure 20.**

**POWER-UP/POWER-DOWN**

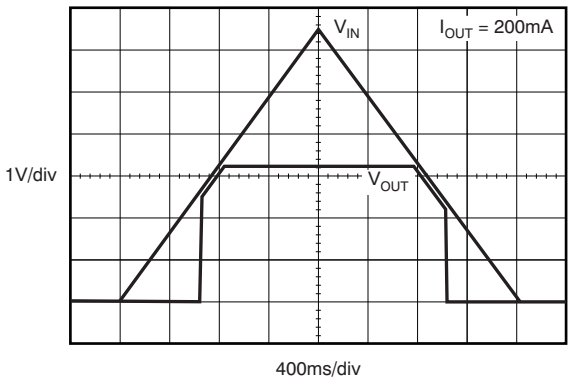



**Figure 21.**

## APPLICATION INFORMATION

The TPS718xx/TPS719xx belong to a family of new generation LDO regulators that use innovative circuitry to achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR (up to 1MHz) at very low headroom ($V_{IN}$ – $V_{OUT}$). These features, combined with low noise, two independent enables, low ground pin current and ultra-small packaging, make this part ideal for portable applications. This family of regulators offer sub-bandgap output voltages, current limit and thermal protection, and is fully specified from –40°C to +125°C.

Figure 22 shows the basic circuit connections.

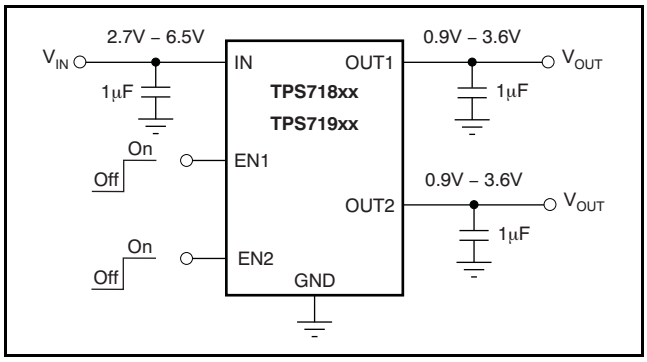



**Figure 22. Typical Application Circuit**

### Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 1.0µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located close to the power source. If source impedance is not sufficiently low, a 0.1µF input capacitor may be necessary to ensure stability.

The TPS718xx/TPS719xx are designed to be stable with standard ceramic capacitors of values 1.0µF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be <1.0Ω.

### Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for $V_{IN}$ and $V_{OUT}$, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device. High ESR capacitors may degrade PSRR.

### Internal Current Limit

The TPS718xx/TPS719xx internal current limits help protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TPS718xx/TPS719xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current may be appropriate.

### Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN. The TPS719 with internal active output pulldown circuitry discharges the output with a time constant (*t*) of:

$$t = 3\left(\frac{60 \times R_L}{60 + R_L}\right) \times C_{OUT}$$

with:

$R_L$ = output load resistance

$C_{OUT}$ = output capacitance

### Dropout Voltage

The TPS718xx/TPS719xx use a PMOS pass transistor to achieve low dropout. When ($V_{IN}$ – $V_{OUT}$) is less than the dropout voltage ($V_{DO}$), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. $V_{DO}$ approximately scales with output current because the PMOS device behaves like a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as ($V_{IN}$ – $V_{OUT}$) approaches dropout. This effect is shown in Figure 13 and Figure 14 in the Typical Characteristics section.

### Transient Response

As with any regulator, increasing the size of the output capacitor will reduce over/undershoot magnitude but increase duration of the transient response.

### Undervoltage Lock-Out (UVLO)

The TPS718xx/TPS719xx utilize an undervoltage lock-out circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a de-glitch feature so that it typically ignores undershoot transients on the input if they are less than 50μs duration. On the TPS719xx, the active pulldown discharges $V_{OUT}$ when the device is in UVLO off condition. However, the input voltage needs to be greater than 0.8V for active pulldown to work.

### Minimum Load

The TPS718xx/TPS719xx are stable with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS718xx/TPS719xx employ an innovative, low-current mode circuit under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

## THERMAL INFORMATION

### Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS718xx/TPS719xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS718xx/TPS719xx into thermal shutdown degrades device reliability.

### Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Dissipation Ratings* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation ($P_D$) is equal to the product of the output current times the voltage drop across the output pass element ($V_{IN}$ to $V_{OUT}$), as shown in Equation 1:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

### Package Mounting

Solder pad footprint recommendations for the TPS718xx/TPS719xxx are available from the Texas Instruments web site at www.ti.com.

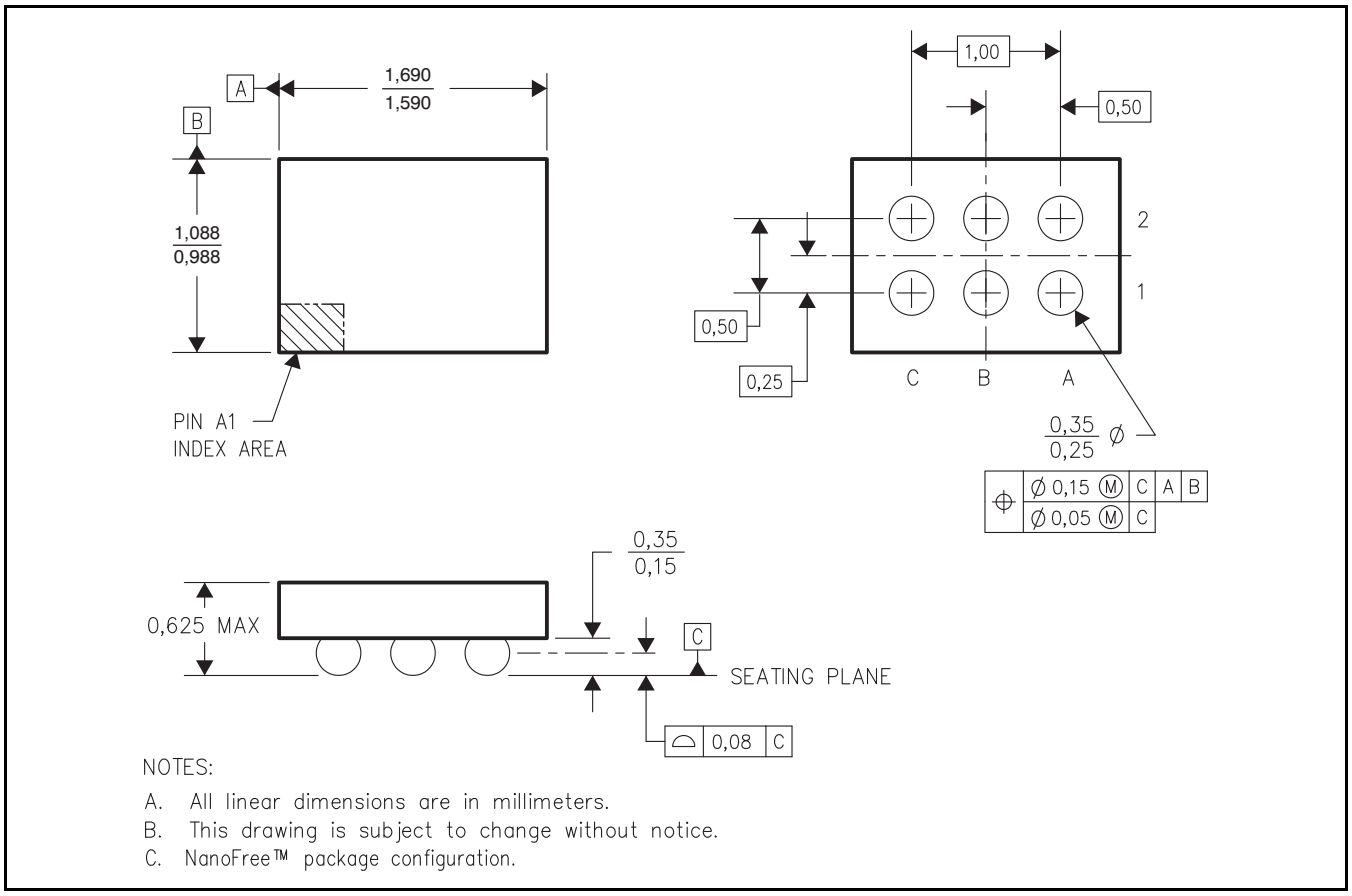



**Figure 23. YZC Wafer Chip-Scale Package Dimensions (in mm)**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS71812-33DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BVC | Samples |
| TPS71812-33DRVT | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BVC | Samples |
| TPS71818-27YZCR | NRND | DSBGA | YZC | 6 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | FX | |
| TPS71818-27YZCT | NRND | DSBGA | YZC | 6 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | FX | |
| TPS71818-33DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OEI | Samples |
| TPS71818-33DRVT | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OEI | Samples |
| TPS71825-12DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BVO | Samples |
| TPS71825-12DRVT | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BVO | Samples |
| TPS71828-28YZCR | NRND | DSBGA | YZC | 6 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | FZ | |
| TPS71828-28YZCT | NRND | DSBGA | YZC | 6 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | FZ | |
| TPS71828-30DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BVX | Samples |
| TPS71828-30DRVT | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BVX | Samples |
| TPS71828-30DRVTG4 | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BVX | Samples |
| TPS71913-28DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BWP | Samples |
| TPS71913-28DRVT | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BWP | Samples |
| TPS71913-28DRVTG4 | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BWP | Samples |
| TPS71918-12DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BWW | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS71918-12DRVT | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BWW | Samples |
| TPS71918-12DRVTG4 | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BWW | Samples |
| TPS71918-28DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ODQ | Samples |
| TPS71918-28DRVT | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ODQ | Samples |
| TPS71921-22DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OBW | Samples |
| TPS71921-22DRVT | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OBW | Samples |
| TPS71926-15DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAJ | Samples |
| TPS71926-15DRVT | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAJ | Samples |
| TPS71926-15DRVTG4 | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAJ | Samples |
| TPS71928-28DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAK | Samples |
| TPS71928-28DRVT | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAK | Samples |
| TPS71928-28DRVTG4 | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAK | Samples |
| TPS719285-285DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OAU | Samples |
| TPS71933-28DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAH | Samples |
| TPS71933-28DRVRG4 | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAH | Samples |
| TPS71933-28DRVT | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAH | Samples |
| TPS71933-28DRVTG4 | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAH | Samples |
| TPS71933-33DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BWL | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS71933-33DRVT | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BWL | Samples |
| TPS71933-33DRVTG4 | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BWL | Samples |
| TPS71936-315DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CVZ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

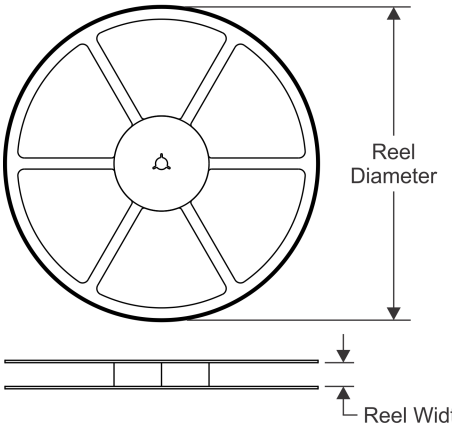
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

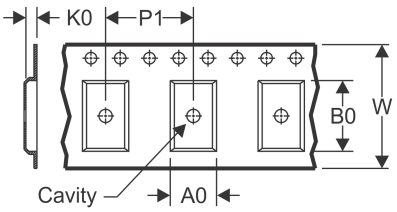
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

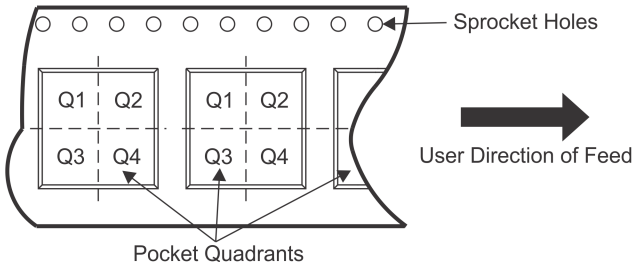



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

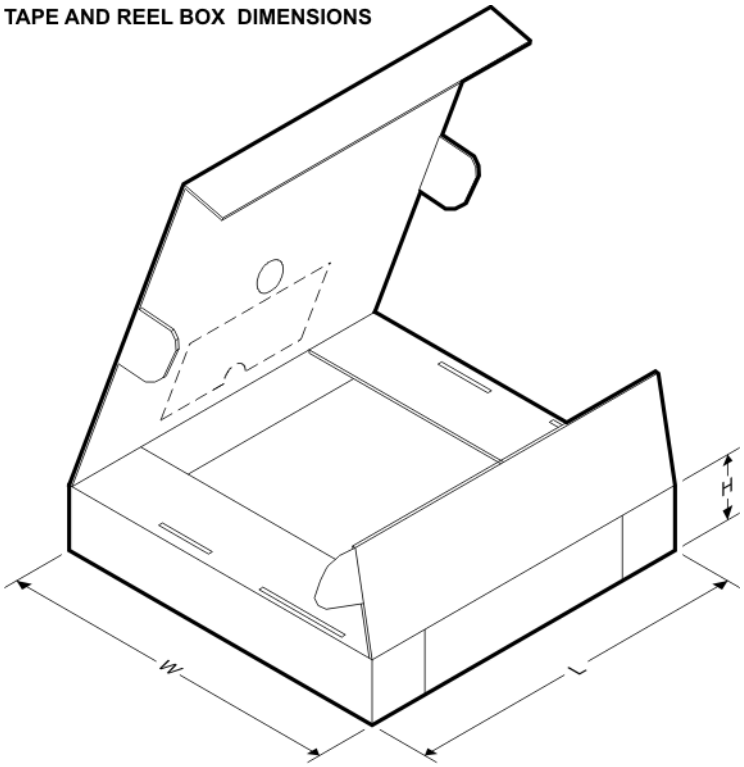



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS71812-33DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71812-33DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71818-33DRVR | WSON | DRV | 6 | 3000 | 178.0 | 8.4 | 2.25 | 2.25 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS71818-33DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71818-33DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71818-33DRVT | WSON | DRV | 6 | 250 | 178.0 | 8.4 | 2.25 | 2.25 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS71825-12DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71825-12DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71828-30DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71828-30DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71913-28DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71913-28DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71918-12DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71918-12DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71918-28DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71918-28DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71921-22DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71921-22DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS71926-15DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71926-15DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71928-28DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71928-28DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS719285-285DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71933-28DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71933-28DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71933-33DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71933-33DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71936-315DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |

**TAPE AND REEL BOX DIMENSIONS**

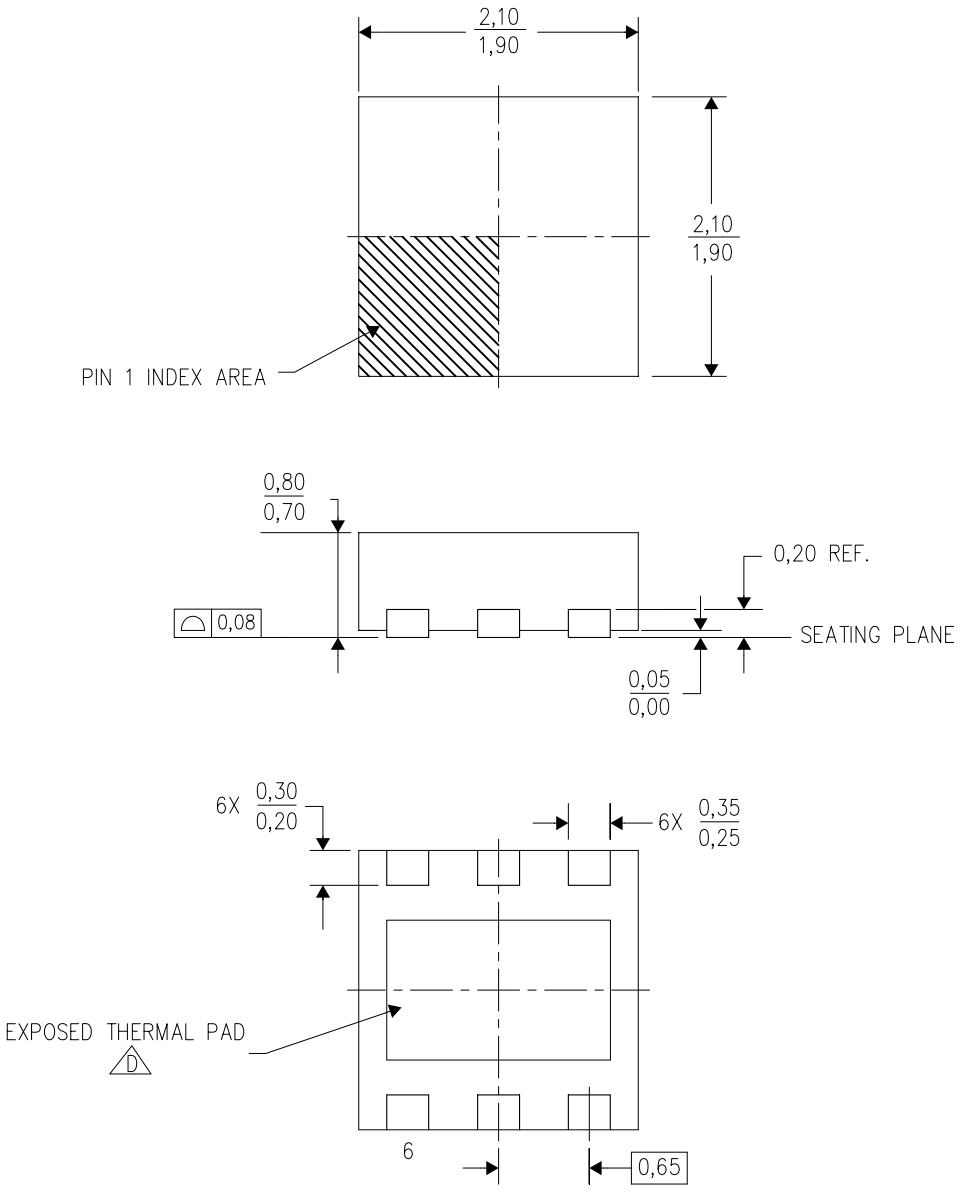



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS71812-33DRVR | WSON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71812-33DRVT | WSON | DRV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71818-33DRVR | WSON | DRV | 6 | 3000 | 205.0 | 200.0 | 33.0 |
| TPS71818-33DRVR | WSON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71818-33DRVT | WSON | DRV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71818-33DRVT | WSON | DRV | 6 | 250 | 205.0 | 200.0 | 33.0 |
| TPS71825-12DRVR | WSON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS71825-12DRVT | WSON | DRV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71828-30DRVR | WSON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71828-30DRVT | WSON | DRV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71913-28DRVR | WSON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71913-28DRVT | WSON | DRV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71918-12DRVR | WSON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71918-12DRVT | WSON | DRV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71918-28DRVR | WSON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71918-28DRVT | WSON | DRV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71921-22DRVR | WSON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71921-22DRVT | WSON | DRV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71926-15DRVR | WSON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71926-15DRVT | WSON | DRV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71928-28DRVR | WSON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71928-28DRVT | WSON | DRV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS719285-285DRVR | WSON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71933-28DRVR | WSON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71933-28DRVT | WSON | DRV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71933-33DRVR | WSON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71933-33DRVT | WSON | DRV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71936-315DRVR | WSON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

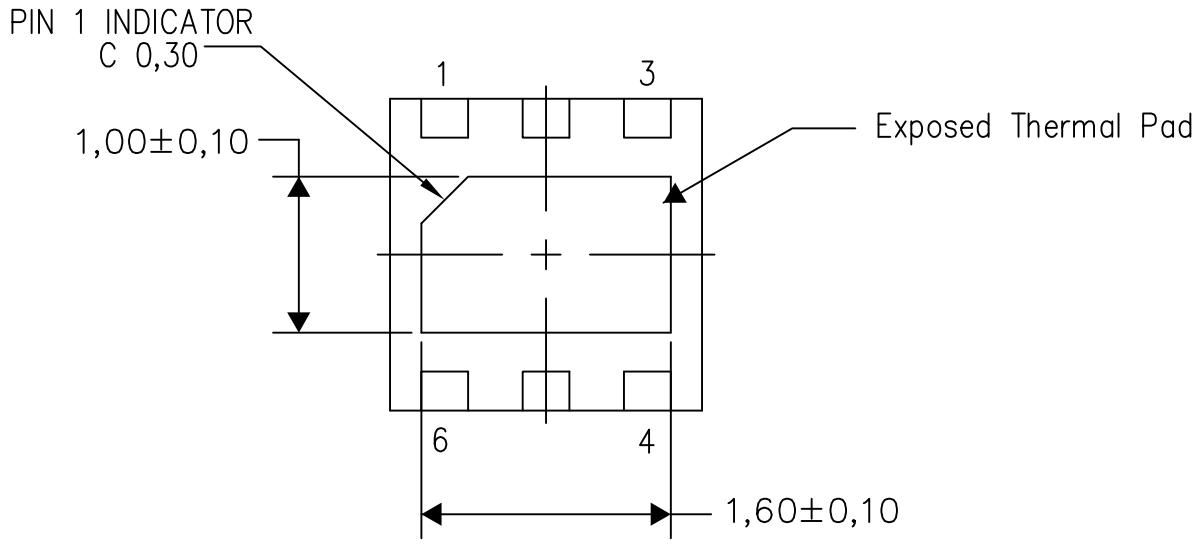
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



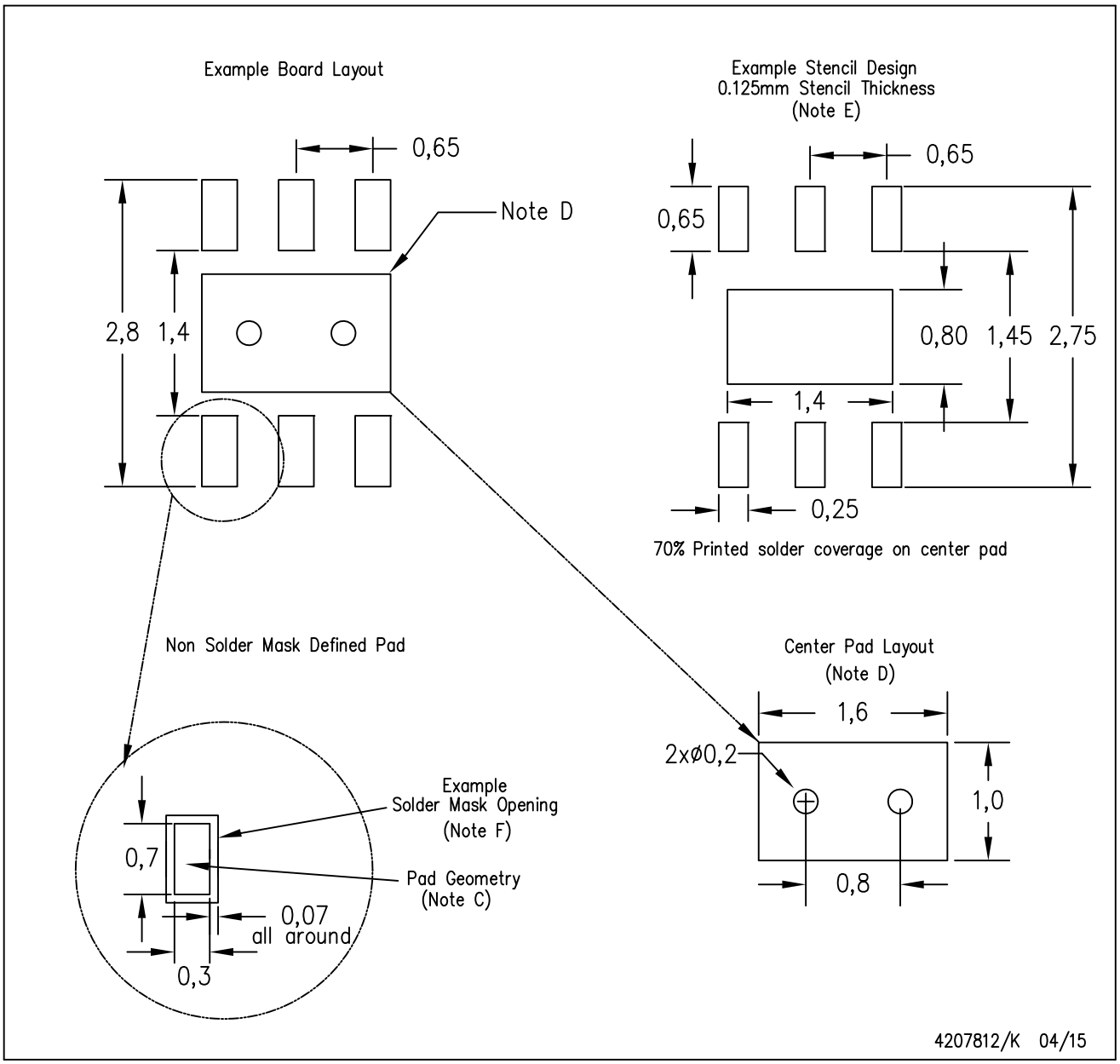

Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



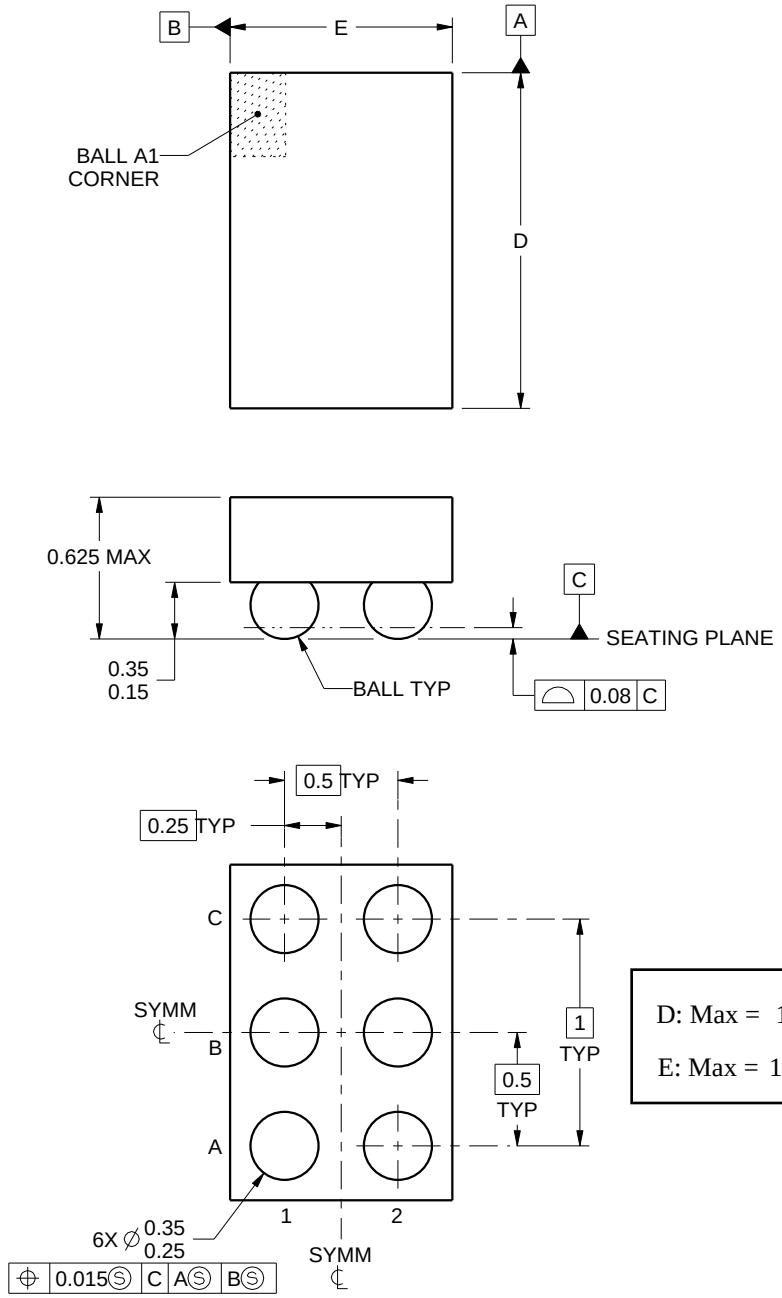

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

# PACKAGE OUTLINE

## YZC0006

## DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY

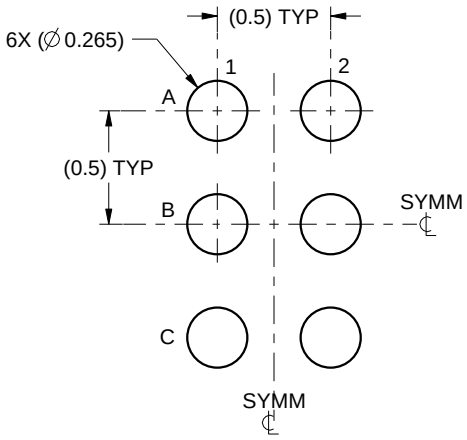



4219522/A 02/2015

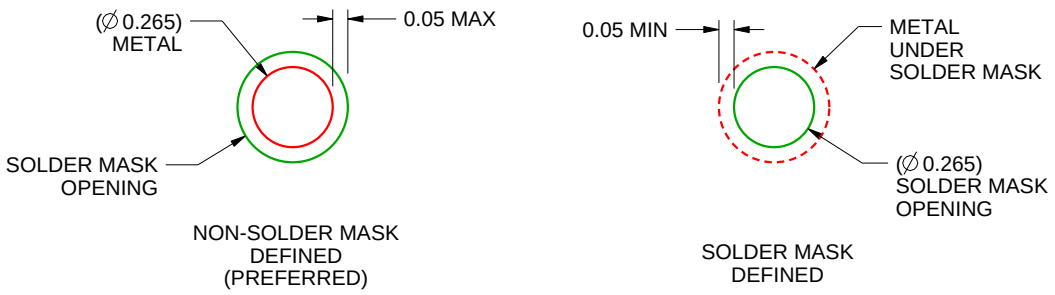
NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.




LAND PATTERN EXAMPLE
SCALE:30X

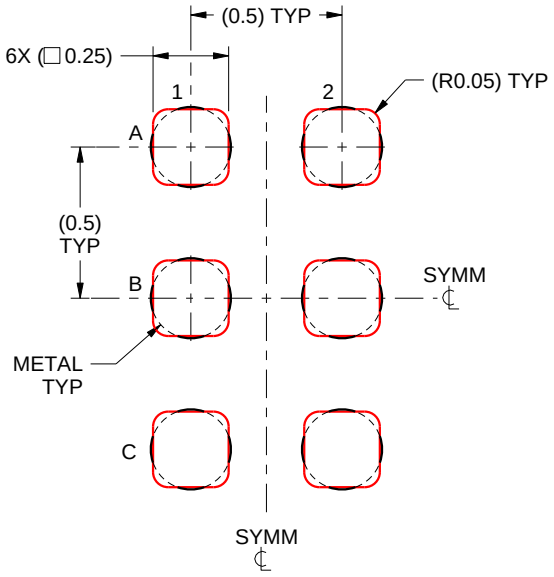



SOLDER MASK DETAILS
NOT TO SCALE

4219522/A 02/2015

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219522/A 02/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265