80mA, 10V, 3.2µA Quiescent Current
LOW-DROPOUT LINEAR REGULATOR in SC70 or SON 2x2

FEATURES

- **Wide Input Voltage Range: 2.5V to 10V**
- **Low Quiescent Current: 3.2µA at 80mA**
- **Stable with any Capacitor > 0.47µF**
- **Output Current: 80mA**
- **Dropout Voltage: 415mV at 50mA Load**
- **Available in Fixed 3.3V or Adjustable (1.2V to 8.8V) Versions**
- **Current Limit**
- **SC70-5 and 2mm x 2mm SON-6 Packages**
- **Specified Junction Temperature Range: −40°C to +125°C**
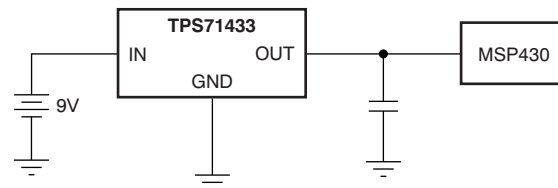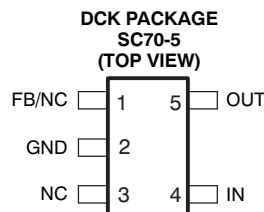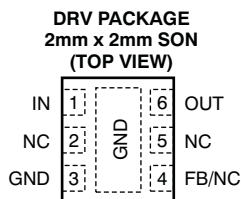- **For MSP430-Specific Output Voltages, see the TPS715xx**

APPLICATIONS

- **Ultralow-Power Microcontrollers**
- **Industrial/Automotive Applications**
- **PDAs**
- **Portable, Battery-Powered Equipment**

DESCRIPTION

The TPS714xx low-dropout (LDO) voltage regulators offer the benefits of wide input voltage range, low-dropout voltage, low-power operation, and miniaturized packaging. These devices, which operate over an input range of 2.5V to 10V, are stable with any capacitor ≥ 0.47µF. The 2.5V to 10V input voltage range, combined with 3.2µA quiescent current, makes this device particularly well-suited for two-cell alkaline, and two-cell lithium, and other low quiescent current sensitive battery applications. The low dropout voltage and low quiescent current allow operation at extremely low power levels. Therefore, the devices are ideal for power battery management ICs. Specifically, because the device is enabled as soon as the applied voltage reaches the minimum input voltage, the output is quickly available to power continuously-operating, battery-charging ICs.

The typical PNP pass transistor has been replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the low dropout voltage (typically 415mV at 50mA of load current) is directly proportional to the load current. The quiescent current (3.2µA, typical) is stable over the entire range of the output load current (0mA to 80mA).

The TPS714xx is available in a 2mm x 2mm SON-6 package ideal for high power dissipation, or an SC70-5 package ideal for handheld and ultra-portable applications.

DRV PACKAGE
2mm x 2mm SON
(TOP VIEW)

IN	1		6	OUT
NC	2	GND	5	NC
GND	3		4	FB/NC

DCK PACKAGE
SC70-5
(TOP VIEW)

FB/NC	1	5	OUT
GND	2		
NC	3	4	IN

TPS714xx

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS[1]

PRODUCT	V_{OUT} [2]
TPS714**xxyyyz**	**XX** is nominal output voltage (for example 33 = 3.3V, 01 = Adjustable) **YYY** is Package Designator **Z** is Package Quantity

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Custom output voltages are available on a quick-turn basis for prototyping. Production quantities are available; minimum package order quantities apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS

Over operating temperature range, unless otherwise noted.[1]

PARAMETER		TPS714xx	UNIT
V_{IN} range		–0.3 to +24	V
V_{OUT} range		- 0.3 to +9.9	V
$V_{FB\ range}$		-0.3 to +4	V
Peak output current		Internally limited	
Continuous total power dissipation		See Power Dissipation Rating table	
Junction temperature range, T_J		–40 to +125	°C
Storage temperature range		–65 to +150	°C
ESD rating	Human body model (HBM)	2	kV
	Charged device model (CDM)	500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATING TABLE

BOARD	PACKAGE	$R_{\theta JA}$°C/W	DERATING FACTOR ABOVE T_A = +25°C	$T_A \leq 25$°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
High-K[1]	DCK	315	3.18mW/°C	320mW	175mW	100mW
High-K[1]	DRV	65	15.4mW/°C	1.54W	850mW	0.62W

(1) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch × 3 inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

Over the operating junction temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 1V, I_{OUT} = 1mA, and C_{OUT} = 1μF, unless otherwise noted. The adjustable version is tested with V_{OUT} = 2.8V. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS	TPS714xx			UNIT
			MIN	TYP	MAX	
Input voltage range[1]	V_{IN}	I_{OUT} = 10mA	2.5		10	V
		I_{OUT} = 80mA	3		10	
Output voltage range (TPS71401)	V_{OUT}		V_{FB}		8.8	V
Internal reference (TPS71401)	V_{FB}		1.12	1.20	1.24	V
Output voltage accuracy[1]	TPS71433 over V_{IN}, I_{OUT}, and Temp	4.3V < V_{IN} < 10V, 1mA ≤ I_{OUT} ≤ 80mA	3.135	3.3	3.465	V
Output voltage line regulation[1]	$\Delta V_{OUT}/\Delta V_{IN}$	V_{OUT} + 1V < V_{IN} ≤ 10V		5		mV
Load regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 1mA to 80mA		30		mV
Feedback pin bias current	$I_{FB\ BIAS}$	I_{OUT} = 0mA, V_{IN} = 3V to 10V, V_{OUT} = 1.2V,		2		nA
Dropout voltage	V_{DO}	I_{OUT} = 80mA, V_{IN} = $V_{OUT(NOM)}$ – 0.1V		670	1300	mV
Output current limit	I_{CL}	V_{OUT} = 0V	100		1100	mA
Ground pin current	I_{GND}	T_J = –40°C to +85°C, 1mA ≤ I_{OUT} ≤ 80mA		3.2	4.2	μA
		1mA ≤ I_{OUT} ≤ 80mA		3.2	5.8	
		V_{IN} = 10V, 1mA ≤ I_{OUT} ≤ 80mA			7.4	
Power-supply ripple rejection	PSRR	f = 100kHz, C_{OUT} = 10μF		60		dB
Output noise voltage	V_{IN}	BW = 200Hz to 100kHz, C_{OUT} = 10μF, I_{OUT} = 50mA		575		μVrms

(1)   Minimum V_{IN} = V_{OUT} + V_{DO}, or the value shown for Input voltage, whichever is greater.

PIN CONFIGURATION
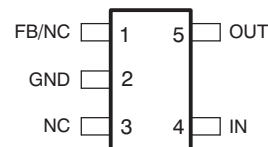
DRV PACKAGE
SON-6
(TOP VIEW)
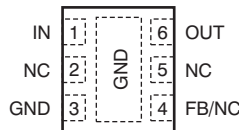
DCK PACKAGE
SC70-5
(TOP VIEW)

Table 1. Pin Descriptions

|	TPS714xx				
	DCK		DRV		
NAME	FIXED	ADJ.	FIXED	ADJ.	DESCRIPTION
FB/NC	-	1	-	4	Adjustable version only. This pin is used to set the output voltage.
GND	2	2	3, Pad	3, Pad	Ground
NC	1,3	3	2, 4, 5	2, 5	No connection. May be left open or tied to ground for improved thermal performance.
IN	4	4	1	1	Unregulated input voltage.
OUT	5	5	6	6	Regulated output voltage. Any output capacitor ≥ 0.47μF can be used for stability.

FUNCTIONAL BLOCK DIAGRAMS
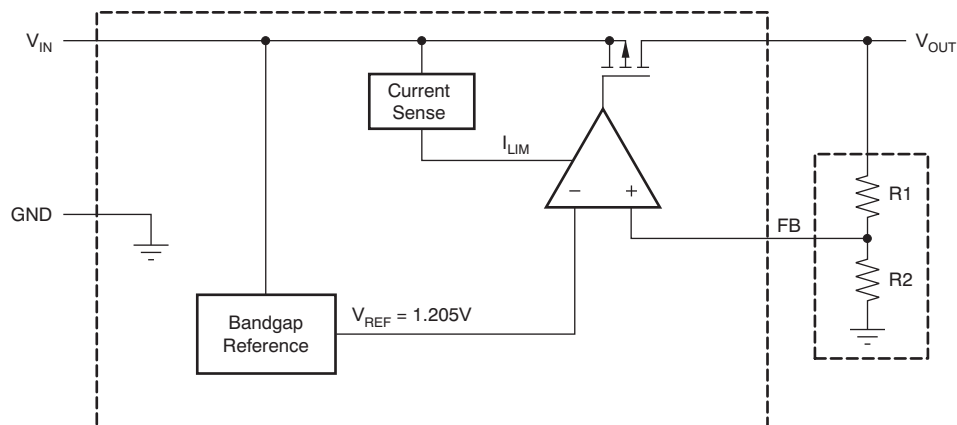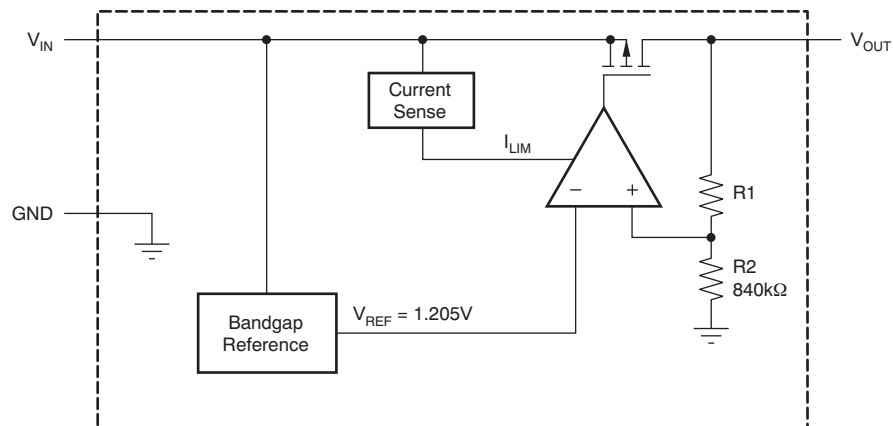
Figure 1. Adjustable Voltage Version

Figure 2. Fixed Voltage Version

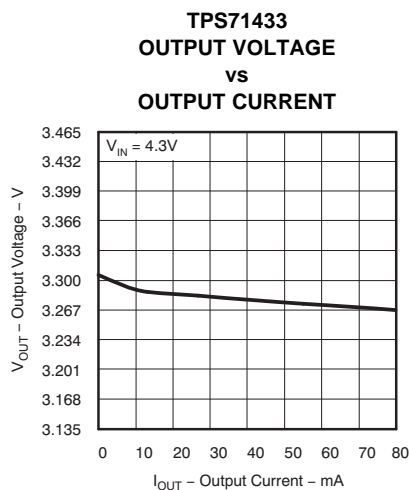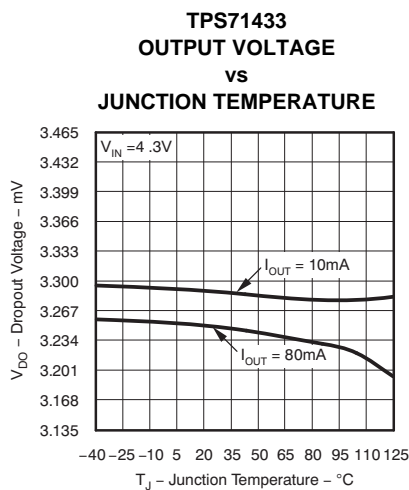# TYPICAL CHARACTERISTICS

At T_A = +25°C, unless otherwise noted.

TPS71433
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

Figure 3.

TPS71433
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

Figure 4.

TPS71433
QUIESCENT CURRENT
vs
JUNCTION TEMPERATURE

Figure 5.

TPS71433
OUTPUT SPECTRAL NOISE
DENSITY
vs
FREQUENCY

Figure 6.

TPS71433
OUTPUT IMPEDANCE
vs
FREQUENCY

Figure 7.

TPS71433
DROPOUT VOLTAGE
vs
OUTPUT CURRENT

Figure 8.

TEXAS
INSTRUMENTS
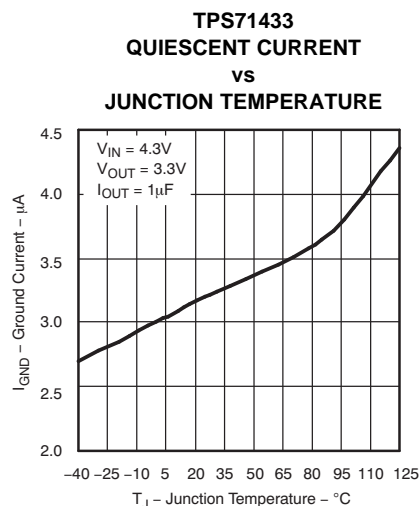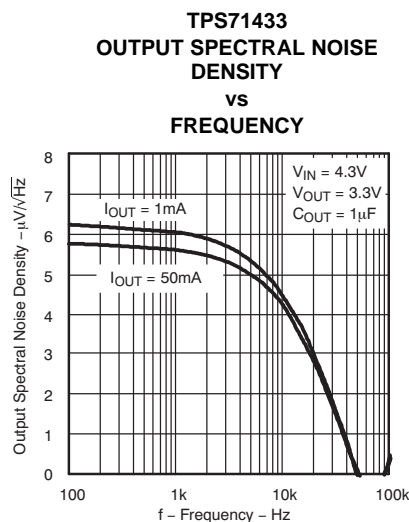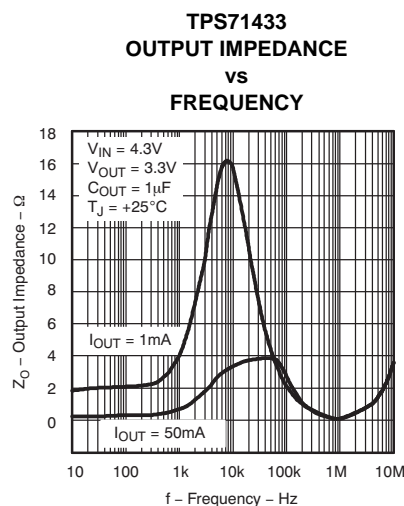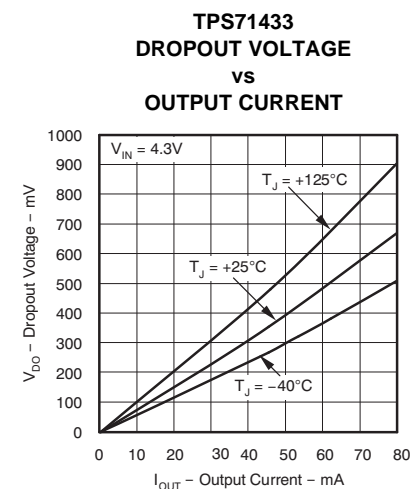
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

TPS71433
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

Figure 9.

TPS71433
V_{OUT}
vs
CURRENT LIMIT

Figure 10.

TPS71433
POWER-SUPPLY RIPPLE
REJECTION
vs
FREQUENCY

Figure 11.

TPS71433
POWER-UP/POWER-DOWN

Figure 12.

TPS71433
LINE TRANSIENT RESPONSE
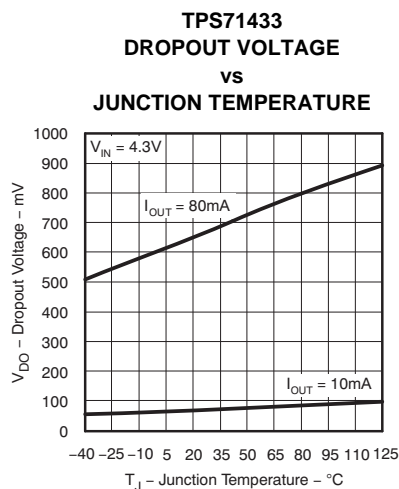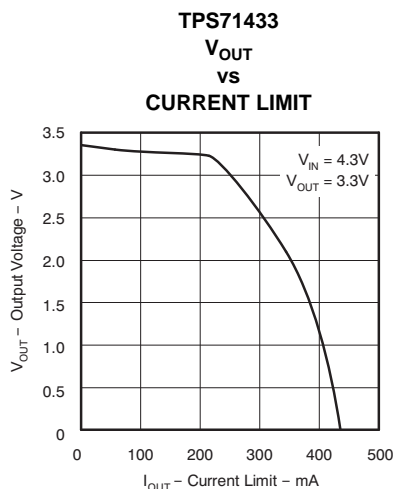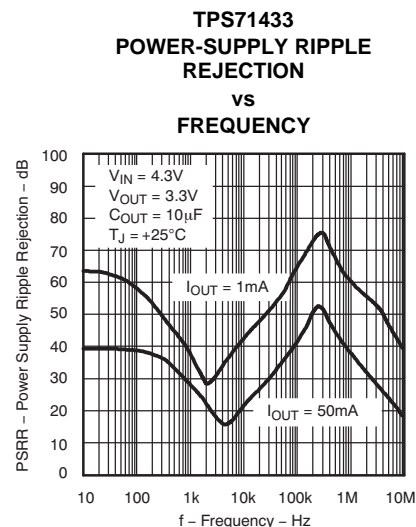
Figure 13.

TPS71433
LOAD TRANSIENT RESPONSE

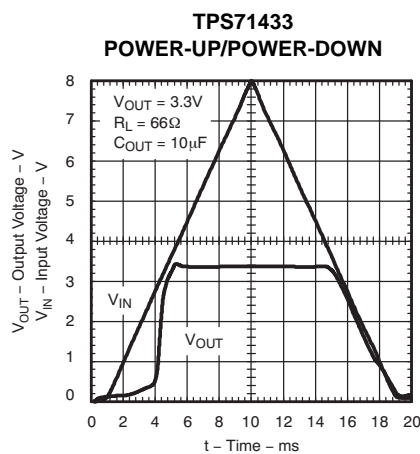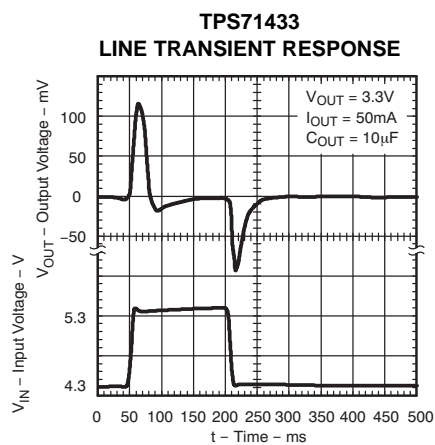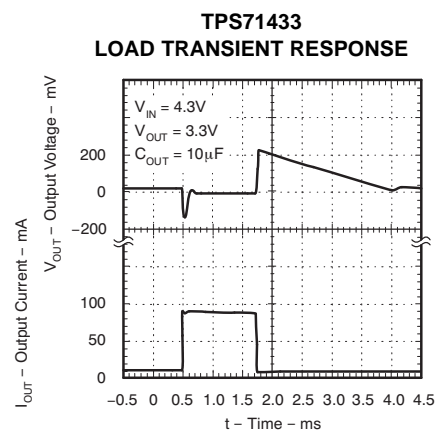**Figure 14.**

APPLICATION INFORMATION

The TPS714xx family of LDO regulators has been optimized for ultralow power applications such as the MSP430 microcontroller. Its ultralow supply current maximizes efficiency at light loads, and its high input voltage range makes it suitable for supplies such as unconditioned solar panels.
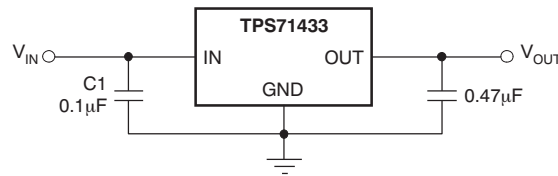

Figure 15. Typical Application Circuit (Fixed Voltage Version)

External Capacitor Requirements

Although not required, a 0.047µF or larger input bypass capacitor, connected between IN and GND and located close to the device, is recommended to improve transient response and noise rejection of the power supply as a whole. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and if the device is located several inches from the power source.

The TPS714xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. Any capacitor (including ceramic and tantalum) that is greater than or equal to 0.47µF properly stabilizes this loop.

Power Dissipation and Junction Temperature

To ensure reliable operation, worst-case junction temperature should not exceed +125°C. This restriction limits the power dissipation that the regulator can manage in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(MAX)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using Equation 1:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

- $T_J max$ is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the Power Dissipation Rating table).
- T_A is the ambient temperature.   (1)

The regulator dissipation is calculated using Equation 2:

$$P_D = \left(V_{IN} - V_{OUT}\right) \times I_{OUT}$$

(2)

Power dissipation resulting from quiescent current is negligible.

Regulator Protection

The TPS714xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS714xx features internal current limiting. During normal operation, the TPS714xx limits output current to approximately 500mA. When current limiting engages, the output voltage scales back linearly until the over-current condition ends. There is no internal thermal shutdown circuit in this device; therefore, care must be taken not to exceed the power dissipation ratings of the package during a fault condition. This device does not have undervoltage lockout; therefore, this constraint should be taken into consideration for specific applications.

Programming the TPS71401 Adjustable LDO Regulator

The output voltage of the TPS71401 adjustable regulator is programmed using an external resistor divider as shown in Figure 16. The output voltage is calculated using Equation 3:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2} \right)$$

(3)

where:

V_{REF} = 1.20V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately a 1.5µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided because leakage current out of the FB pin across R1/R2 creates an offset voltage that artificially increases the feedback voltage and thus erroneously decreases V_{OUT}. The recommended design procedure is to choose R2 = 1MΩ to set the divider current at 1.5µA, and then calculate R1 using Equation 4:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2$$

(4)

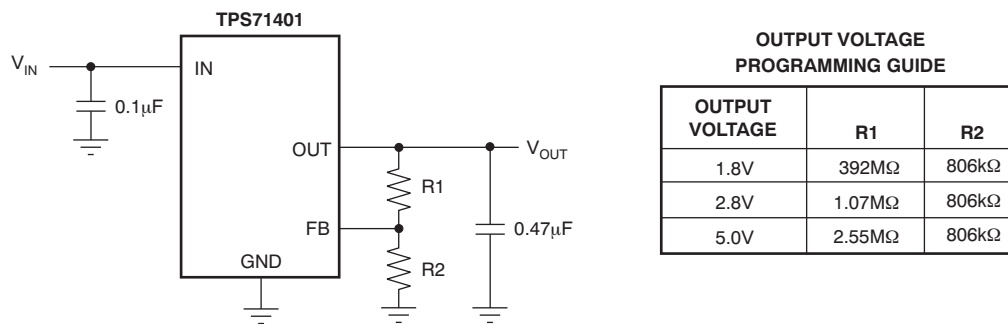| OUTPUT VOLTAGE	R1	R2
1.8V	392MΩ	806kΩ
2.8V	1.07MΩ	806kΩ
5.0V	2.55MΩ	806kΩ

Figure 16. TPS71401 Adjustable LDO Regulator Programming

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December, 2009) to Revision C	Page
• Changed *Ground pin current* maximum specifications	3

Changes from Revision A (April, 2009) to Revision B	Page
• Changed battery type shown in typical circuit illustration	1
• Changed V_{IN} range absolute maximum rating from +11.5V to +24V	2

![Texas Instruments logo]

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS71401DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CVG	Samples
TPS71401DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CVG	Samples
TPS71401DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVG	Samples
TPS71401DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVG	Samples
TPS71433DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CVH	Samples
TPS71433DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CVH	Samples
TPS71433DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVH	Samples
TPS71433DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVH	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS71401DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS71401DCKT	SC70	DCK	5	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS71401DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS71401DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS71433DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS71433DCKT	SC70	DCK	5	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS71433DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS71433DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS71401DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TPS71401DCKT	SC70	DCK	5	250	202.0	201.0	28.0
TPS71401DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS71401DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS71433DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TPS71433DCKT	SC70	DCK	5	250	202.0	201.0	28.0
TPS71433DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS71433DRVT	WSON	DRV	6	250	203.0	203.0	35.0

DCK (R−PDSO−G5)   PLASTIC SMALL−OUTLINE PACKAGE

4093553−3/G   01/2007

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   Falls within JEDEC MO−203 variation AA.

TEXAS
INSTRUMENTS
www.ti.com

DCK (R−PDSO−G5)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35

0,85

2,2

2,2

2x0,65

2x1,30

2x0,65

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356−2/C   07/11

NOTES: A.   All linear dimensions are in millimeters.
           B.   This drawing is subject to change without notice.
           C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
           D.   Publication IPC−7351 is recommended for alternate designs.
           E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

TEXAS INSTRUMENTS
www.ti.com

DRV (S−PWSON−N6) PLASTIC SMALL OUTLINE NO−LEAD

$\frac{2,10}{1,90}$

$\frac{2,10}{1,90}$

PIN 1 INDEX AREA

$\frac{0,80}{0,70}$

0,20 REF.

⌓ | 0,08

SEATING PLANE

$\frac{0,05}{0,00}$

6X $\frac{0,30}{0,20}$

6X $\frac{0,35}{0,25}$

EXPOSED THERMAL PAD
⟨D⟩

6

0,65
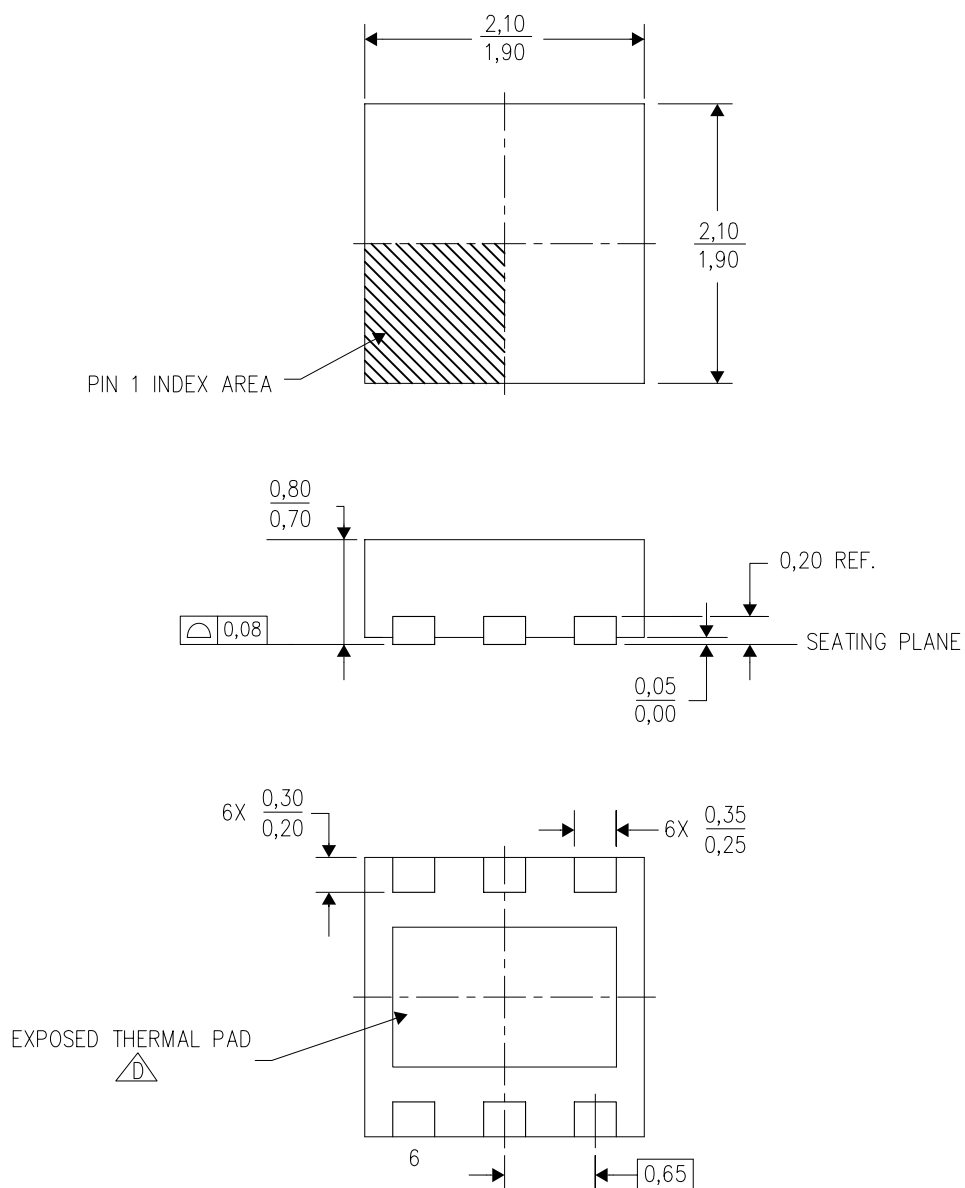
4206925/E 10/10

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. Small Outline No−Lead (SON) package configuration.
    ⟨D⟩ The package thermal pad must be soldered to the board for thermal and mechanical performance.
        See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

DRV (S−PWSON−N6)   PLASTIC SMALL OUTLINE NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR
C 0,30

1,00±0,10

1   3

Exposed Thermal Pad

6   4

1,60±0,10
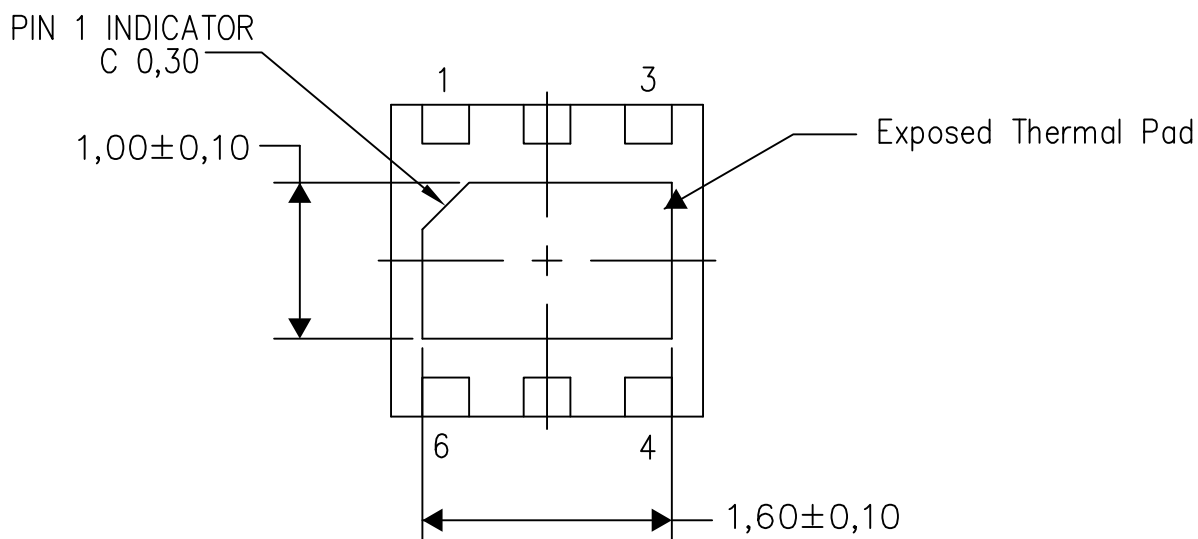
Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S−PWSON−N6)   PLASTIC SMALL OUTLINE NO−LEAD
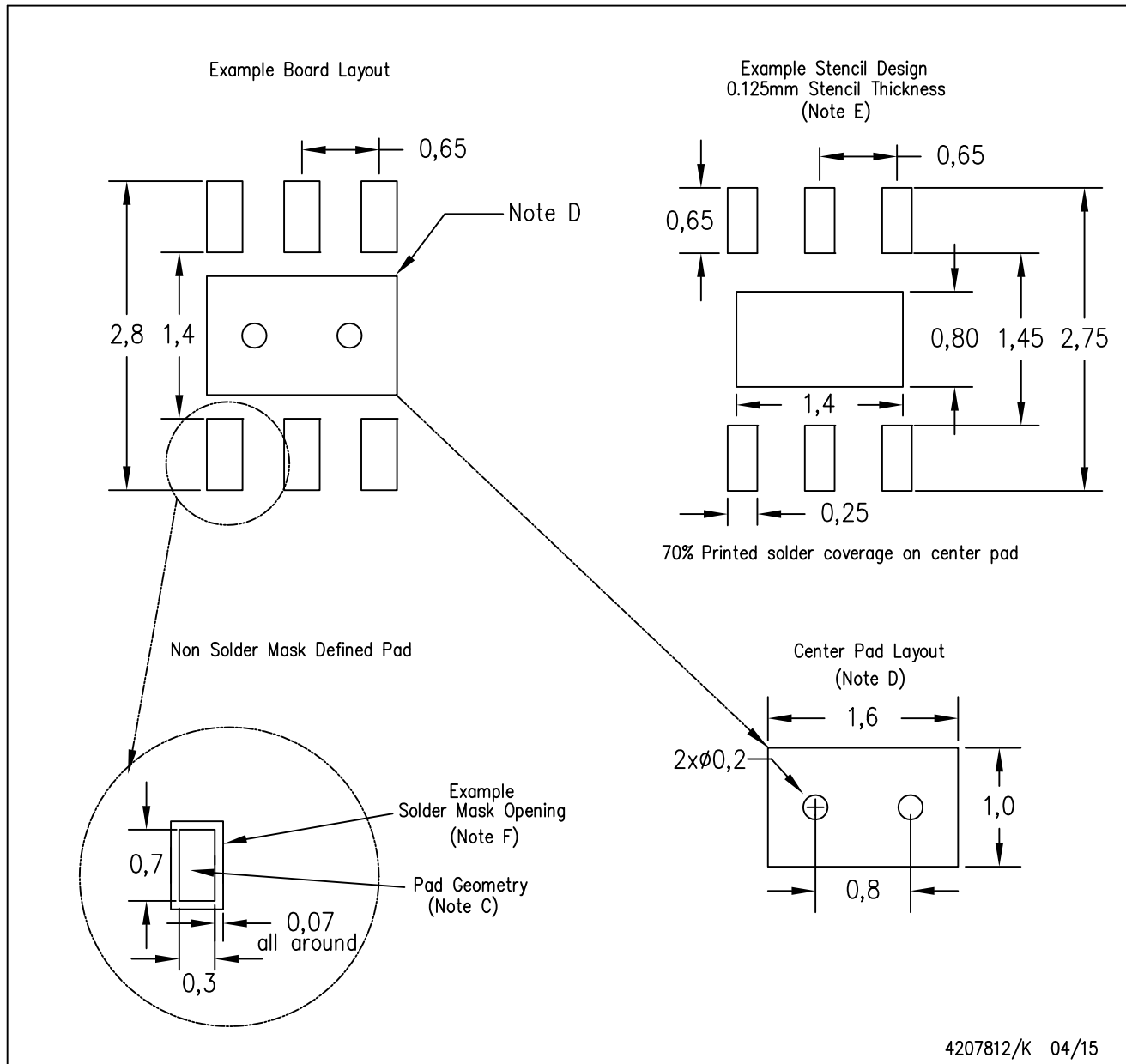
Example Board Layout

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

0,65

Note D

2,8 1,4

0,65

0,65

0,80 1,45 2,75

1,4

0,25

70% Printed solder coverage on center pad

Non Solder Mask Defined Pad

Center Pad Layout
(Note D)

1,6

2xØ0,2

1,0

0,8

Example
Solder Mask Opening
(Note F)

Pad Geometry
(Note C)

0,7

0,07
all around

0,3

4207812/K 04/15

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note,
            QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout.
            These documents are available at www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for solder mask tolerances.

TEXAS
INSTRUMENTS
www.ti.com

IMPORTANT NOTICE

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		