3-MHz Step-Down Regulator and Triple Linear Regulators

Check for Samples: TPS65300-Q1

FEATURES

- **Input VIN Range 5.6 V to 40 V, With Transients up to 45 V**
- **All Outputs Support Ceramic Output Capacitors for Stability**
- **Switch-Mode Regulator With Integrated High-Side Switch**
  - **Recommended Switch-Mode Frequency Range 2 MHz to 3 MHz**
  - **Overcurrent Protection and 1.2-A Peak Switch Current**
- **One Linear Regulators and Two Linear Regulator Controllers With 0.8-V ±1.5% Reference**
- **Status Indicator Output of IGN_EN Input**
- **Soft Start on Ignition (IGN_EN)/Enable Input (EN) Cycle**
- **External Clock Input for Synchronization**
- **Programmable Power-On-Reset Delay, Reset-Function Filter Timer for Fast Negative Transients**
- **Voltage Supervisor for the Following Supplies**
  - **VREG, 3.3 V, 1.2 V**
- **Thermal Shutdown Protection for Excessive Power Dissipation**
- **Operating Junction Temperature Range: –40°C to 150°C**
- **Thermally Enhanced 24-Pin HTSSOP or 24-Pin QFN Package**

APPLICATIONS

- **Power Supply for TMS570 Microcontrollers**
- **Power Supply for C28XXX DSP**
- **General-Purpose Power Supply for Automotive Applications**
  - **Microcontroller and DSP**

DESCRIPTION

The TPS65300-Q1 power supply is a combination of a single switch-mode buck power supply and three linear regulators. This is a monolithic high-voltage switching regulator with an integrated 1.2-A peak current switch, 45-V power MOSFET, and one low-voltage linear regulator and two voltage-regulator controllers.

The device has a voltage supervisor which monitors the output of the switch-mode power supply, the 3.3-V linear regulator, and the 1.2-V linear regulator. An external timing capacitor is used to set the power-on delay and the release of the reset output nRST. This reset output is also used to indicate if the switch-mode supply, the 3.3-V linear regulator supply, or the 1.2-V linear regulator supply is outside the set limits. The 5-V regulator tracks the 3.3-V linear regulator within the specified limits.

The TPS65300-Q1 has a switching frequency range from 2 MHz to 3 MHz, allowing the use of low-profile inductors and low-value input and output ceramic capacitors. External loop compensation gives the user the flexibility to optimize the converter response for the appropriate operating conditions.

This device has built-in protection features such as soft start on IGN_EN ON or enables cycle, pulse-by-pulse current limit, thermal sensing, and shutdown due to excessive power dissipation.

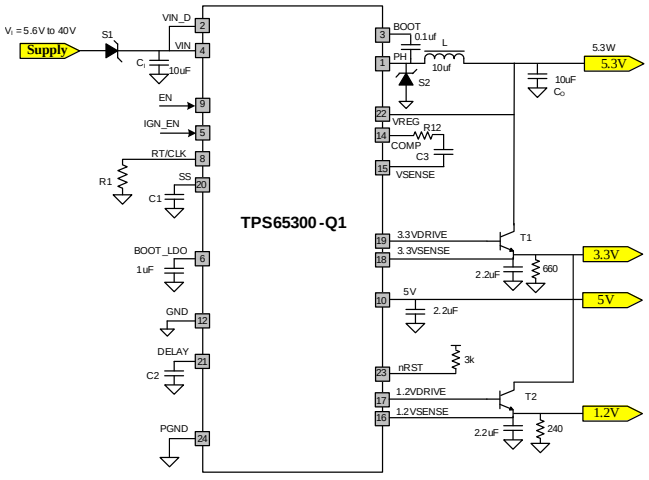


Figure 1. Typical Application Schematic

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_J	Package	Orderable Part Number
–40°C to 125°C	24-pin HTSSOP	TPS65300QPWPRQ1
	24-pin QFN	TPS65300QRHFRQ1

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Buck regulator	VIN, VIN_D	–0.3 to 45	V
	BOOT	–0.3 to 50	V
	PH	–1 to 45 –2 for 30 ns	V
	VSENSE	–0.3 to 5.5	V
Control	IGN_EN	–0.3 to 45	V
	EN(2), 3.3VSENSE, 1.2VSENSE, RT/CLK, VREG	–0.3 to 5.5	V
Output	3.3VDRIVE, 1.2VDRIVE	–0.3 to 8	V
	nRST, IGN_ST	–0.3 to 5.5	V
	DELAY, COMP	–0.3 to 7	V
	BOOT_LDO, 5V	–0.3 to 9	V
Temperature	Operating junction temperature range, T_J	–40 to 150	°C
	Storage temperature range, T_{stg}	–55 to 165	°C
Electrostatic discharge, HBM	ESD(2)	±2	kV

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VIN, VIN_D	5.6		40	V
BOOT	5.6		48	V
PH	–1		40	V
IGN_EN	0		40	V
EN, VSENSE, 3.3VSENSE, 1.2VSENSE, RT/CLK, nRST, IGN_ST	0		5.25	V
VREG, 3.3VDRIVE, 1.2VDRIVE	0		7.5	V
SS, DELAY, COMP	0		6.5	V
BOOT_LDO	0		8.1	V
Operating ambient temperature range, T_A	–40		125	°C

THERMAL INFORMATION

THERMAL METRIC(1)		TPS65300		UNIT
		PWP	RHF	
		24 PINS	24 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	33.6	30.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	16.6	30.8	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	14.5	8.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	0.4	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	14.3	9	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	1.3	1.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

DC CHARACTERISTICS

VIN = 6 V to 27 V, IGN_EN = VIN, T_J = –40°C to 150°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN, VIN_D (Input Power Supply)						
VIN, VIN_D	Supply voltage on VIN, line	Normal mode, after initial start-up	5.6	14	40	V
$I_{q\text{-Normal}}$	Current normal mode	Open-loop test		4.57		mA
$I_{SD\ VIN}$	Shut down	IGN = 0 V, VIN = 12 V, T_A = -40°C to 125°C		2.2	15	µA
$I_{SD\ VIND}$		IGN = 0 V, VIN = 12 V, T_A = -40°C to 125°C		2.2	15	
IGN_EN (Ignition Input)						
V_{IGN_EN}	Input voltage range	Input into IGN_EN pin		14	40	V
V_{IH}	Input high	Enable device to be ON (rising signal)		3.16	4	V
V_{IL}	Input low	Enable device to be OFF (falling signal)	2	3.03		V
I_{IH}	Input high	Enable device to be ON, V_{IGN_EN} = 18 V		23.7	50	µA
EN (Logic Level Enable)						
V_{IH}	Input high	Enable device to be ON (rising signal)		1.7	2.3	V
V_{IL}	Input low	Enable device to be OFF (falling signal)	0.7	1.53		V

DC CHARACTERISTICS (continued)

VIN = 6 V to 27 V, IGN_EN = VIN, T_J = –40°C to 150°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switch-Mode Output 5.3 V						
VREG	Regulator output internal resistor network	Fixed output based on internal resistor network	5.178	5.3	5.542	V
C_O	Output capacitor for 5.3 V	ESR = 0.001 Ω to 100 mΩ; large output capacitance may be required for load transients	10			µF
$r_{ds(on)}$	Internal switch resistance	Measured across VIN_D and PH pins, I_{VREG} = 1 A		0.3		Ω
I_{O-CL}	Switch current limit	VIN = 12 V	1.2	2	3	A
t_{ON-min}	Minimum ON time			40		ns
D_{max}	Maximum duty cycle			97%		
VSENSE (Internal Reference Voltage)						
VREG ref	Internal reference voltage		1.954	2	2.046	V
SS (Soft-Start Timer for Switch-Mode Converter)						
I_{SS}	Soft-start source current	Css = 0.001 µF to 0.01 µF	40	50	60	µA
IGN_ST (Ignition Input Status)						
V_{OL}	Output low	Output asserted low when IGN_EN < 2.2 V, I_{OL} = 1 mA		0.056	0.4	V
I_{IH}	Leakage test	IGN_ST = 5 V		0.05	2	µA
5V (5-V Linear Regulator)						
5Vo	Output voltage	I_O = 1 mA, VREG = 5.3 V	4.9	5	5.1	V
ΔV_{O-Line}	Line regulation	5.15 V < VREG < 5.45 V, I_O = 1 mA, VIN = 12 V		10	20	mV
ΔV_{O-Load}	Load regulation	1 mA < I_O < 200 mA, VREG = 5.3 V, VIN = 12 V		10	30	mV
V_{DO}	Dropout voltage	I_O = 150 mA, measure VREG when V_O(nom) – 0.1 V, then V_{DO} = VREG – (5Vo – 0.1) V, VREG > 5 V		0.15	0.26	V
I_{5V-CL}	Current limit	$5V_O$ = 0.8 x $5V_O$ (nom)	350	1080		mA
C_O	Output capacitor	ESR = 0.001 Ω to 2 Ω. Larger output capacitance may be required for load transients.	1	2.2	10	µF
PSRR	Power-supply rejection ratio	f = 100 Hz, VREG = 5.3 V, I_O = 100 mA, VIN = 12 V	45	60	75	dB
$V_{soft-start}$	Soft start on enable cycle	$5V_O$ = 0 V (initially) with fsw= 2.5MHz		13		ms
3.3V Linear Regulator Controller (3.3VSENSE)						
$3.3V_O$	Output voltage	Io = 5 mA, Vnpn_power input = 5.3 V	3.234	3.3	3.366	V
$\Delta 3.3V_{O-Line}$	Line regulation	3.8 V < Vnpn_power input < 7 V (with nRST not triggered)		1	10	mV
$\Delta 3.3V_{O-Load}$	Load regulation	5 mA < I_O < 550 mA		7.5	30	mV
C_O	Output capacitor for 3.3 V	ESR = 0.001 Ω to 2 Ω. Large output capacitance may be required for load transients.	1	4.7	10	µF
PSRR	Power-supply rejection ratio	f = 100 Hz, VREG = 5.3 V, I_O = 200 mA, VIN = 12 V	45	60	75	dB
t_{ss}	Soft-start time	$3.3V_O$ = 0 V (initially) with fsw= 2.5MHz		12.3		ms

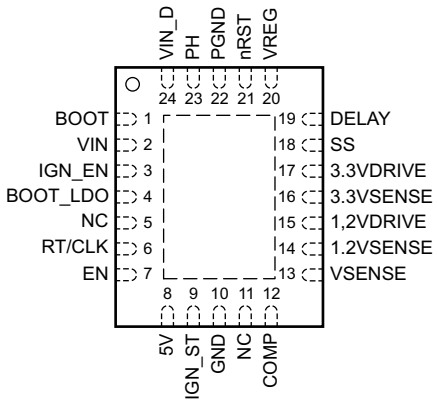
DC CHARACTERISTICS (continued)

VIN = 6 V to 27 V, IGN_EN = VIN, T_J = –40°C to 150°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3.3VDRIVE (Ex. Switch Control Output)						
I_{OH}	Base drive current. NPN turn ON	3.3VDRIVE – 3.3VSENSE = 1 V	10	28	50	mA
I_{OL}	NPN turn off	3.3VDRIVE – 3.3VSENSE at 0.2V	0.1	0.412		mA
1.2V Linear Regulator Controller (1.2VSENSE)						
$1.2V_O$	Output voltage	Io = 5 mA, Vnpn_power input = 5.3 V	1.176	1.2	1.224	V
$\Delta 1.2V_{O\text{-}Line}$	Line regulation	3.25 V < Vnpn_power input < 7 V (with nRST not triggered)		1	10	mV
$\Delta 1.2V_{O\text{-}Load}$	Load regulation	5 mA < I_O < 350 mA		5	15	mV
C_O	Output capacitor for 1.2 V	ESR = 0.001 Ω to 100 mΩ. Large output capacitance may be required for load transients.	8	10	12	µF
PSRR	Power-supply rejection ratio	f = 100 Hz, VREG = 6 V, I_O = 200 mA, VIN = 12 V	45	60	75	dB
t_{ss}	Soft-start time	$1.2V_O$ = 0 V (initially) with fsw= 2.5MHz		8.5		ms
1.2VDRIVE (Ex. Switch Control Output)						
I_{OH}	Base drive current. NPN turn ON	1.2VDRIVE – 1.2VSENSE = 1 V	10	27	50	mA
I_{OL}	NPN turn off	1.2VDRIVE – 1.2VSENSE at 0.2V	0.1	0.47		mA
DELAY (Power-On-Reset Delay)						
$V_{Threshold}$	Threshold voltage	Threshold to release nRST high	1.3	2.05	2.6	V
I_{Charge}	Capacitor charging current		1.4	2	2.6	V
nRST (Reset Indicator)						
V_{OL}	Output low	Reset asserted due to falling VREG or $3.3V_O$ or $1.2V_O$ output voltages, I_{OL} = 1 mA	0	0.16	0.4	V
$t_{nRSTdly}$	Filter time	Delay before nRST is asserted low		11		µs
V_{TH_VREG}	Trigger nRST for VREG output	VREG ramp down	0.87	0.9	0.93	VREG
	Trigger nRST for $3.3V_O$		0.9	0.93	0.96	$3.3\ V_O$
	Trigger nRST for $1.2V_O$		0.9	0.93	0.96	$1.2\ V_O$
I_{IH}	Leakage test	Reset = 5 V		0.07	2	µA
RT/CLK (Oscillator Setting of External Clock Input)						
fsw	Switching freq using RT mode		2		3	MHz
	Switching freq using CLK mode		2		3	
	Minimum clock input pulse duration			40		ns
	Internal oscillator frequency	Switching frequency tolerance for clock	–14%		14%	
	External clock input		–20%		10%	
V_{IH}	Input high				2.3	V
V_{IL}	Input low		0.6			V

DEVICE INFORMATION

RHF Package
(Top View)



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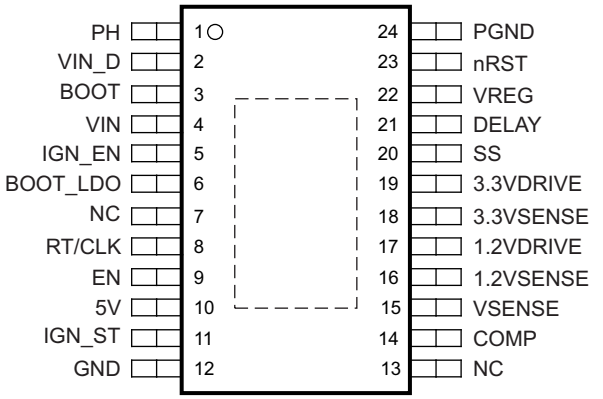
PWP Package
(Top View)



P0110-03

Table 1. Pin Descriptions

PIN			I/O	DESCRIPTION
NAME	NUMBER			
	PWP	RHF		
PH	1	23	O	Source of internal switching FET
VIN_D	2	24	I	Drain input for internal high side MOSFET. Pin 2 and pin 4 must be connected together externally.
BOOT	3	1	O	External bootstrap capacitor connected to PH (pin 1) to drive gate of internal switching FET
VIN	4	2	I	Unregulated input voltage supply. Pin 2 and pin 4 must be connected together externally.
IGN_EN	5	3	I	Ignition input (high-voltage tolerant) internally pulls to ground. Must be externally pulled up to enable
BOOT_LDO	6	4	O	External capacitor connected to ground for stability of internal regulator
NC	7	5	–	Connect to ground
RT/CLK	8	6	I/O	External resistor connected ground to program the internal oscillator. Alternative option is to feed an external clock to provide reference for switching frequency.
EN	9	7	I	A high logic-level input signal to enable and low signal to disable device. Internally pulled down to ground

Table 1. Pin Descriptions (continued)

PIN			I/O	DESCRIPTION
NAME	NUMBER			
	PWP	RHF		
5V	10	8	O	External capacitor to ground for stability of regulated output
IGN_ST	11	9	O	Active-low, open-drain ignition input indicator, output connected to external bias voltage through a resistor. Asserted high after ignition input is high
GND	12	10	O	Ground pin, must be electrically connected to exposed pad on PCB for proper thermal performance
NC	13	11	–	Connect to ground
COMP	14	12	O	Error amplifier output to connect external compensation components
VSENSE	115	13	I	Inverting node of error amplifier for voltage-mode control of preregulated supply
1.2VSENSE	16	14	I	Voltage node of 1.2-V supply
1.2VDRIVE	17	15	O	Output current source to drive the base of an external bipolar transistor to regulate the 1.2V supply
3.3VSENSE	18	16	I	Voltage node of 3.3-V supply
3.3VDRIVE	19	17	O	Output current source to drive the base of an external bipolar transistor to regulate the 3.3V supply
SS	20	18	O	External capacitor to ground to program soft-start time
DELAY	21	19	O	External capacitor to ground to program the power-on-reset delay
VREG	22	20	I	Buck converter output. Integrated internal low-side FET to load output during start-up or limit voltage overshoot
nRST	23	21	O	Active-low, open-drain reset output connected to external bias voltage through a resistor. This output is asserted high after the preregulator, 3.3-V, and 1.2-V regulator outputs are regulating and the delay timer has expired. Also, output is asserted low if any one of these three supplies is out of the set regulation, this threshold is internally set.
PGND	24	22	O	Power ground pin, must be electrically connected to exposed pad on PCB for proper thermal performance
Thermal pad	–	–	–	Electrically connect to ground and solder to ground plane of PCB for thermal efficiency

TYPICAL CHARACTERISTICS

Efficiency vs Output Current on VREG

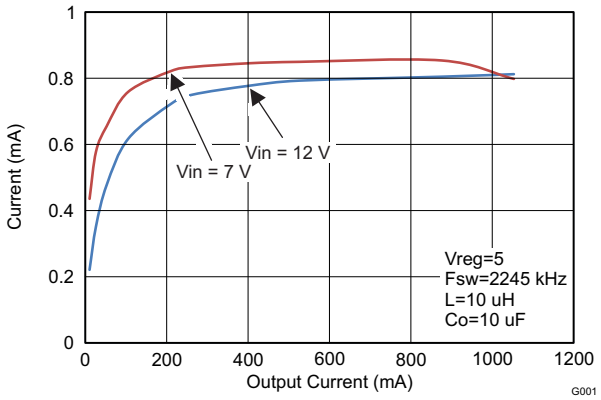


Figure 2.

BUCK CURRENT LIMIT vs TEMPERATURE

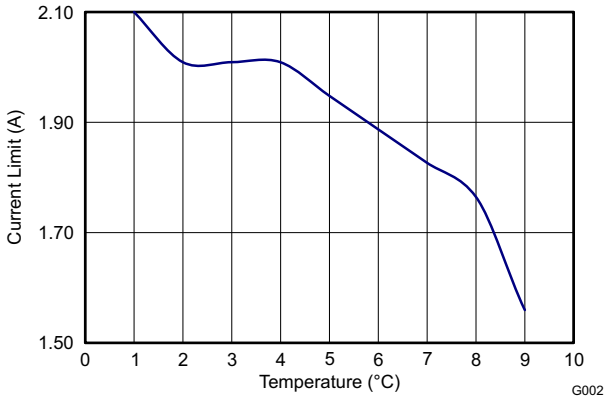


Figure 3.

VSENSE REFERENCE VOLTAGE vs TEMPERATURE

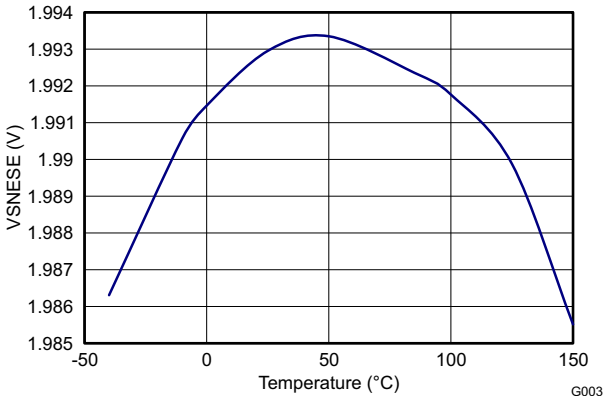


Figure 4.

CURRENT CONSUMPTION I_{IN} vs TEMPERATURE

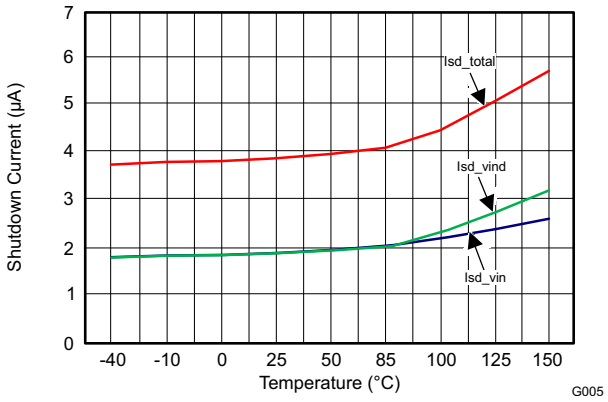


Figure 5.

QUIESCENT CURRENT vs TEMPERATURE

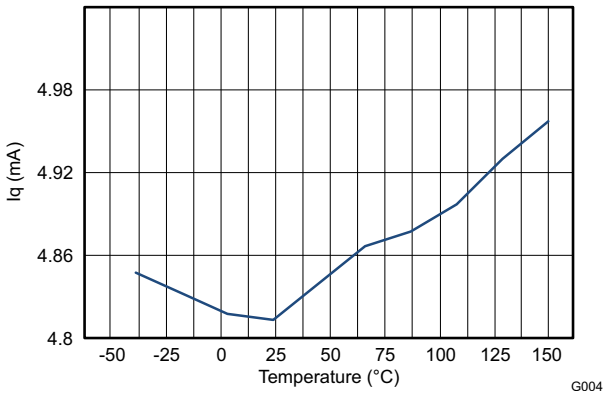


Figure 6.

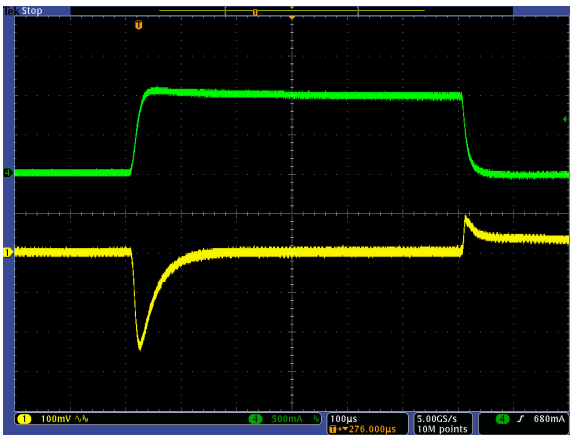


Figure 7. Load Transient Response, 10 mA to 1 A

5-V Linear Regulator ($5V_O$)

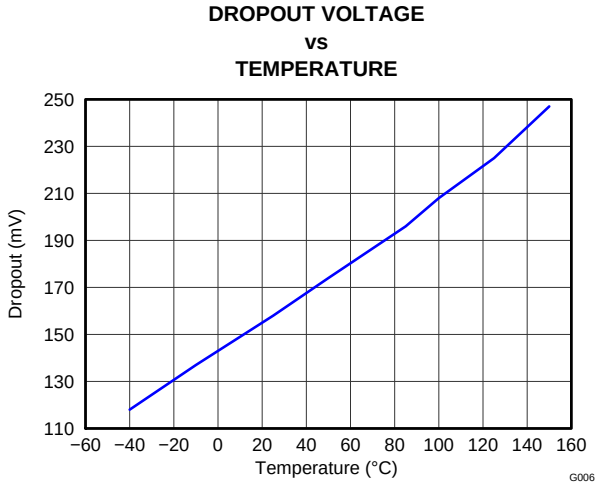


Figure 8.

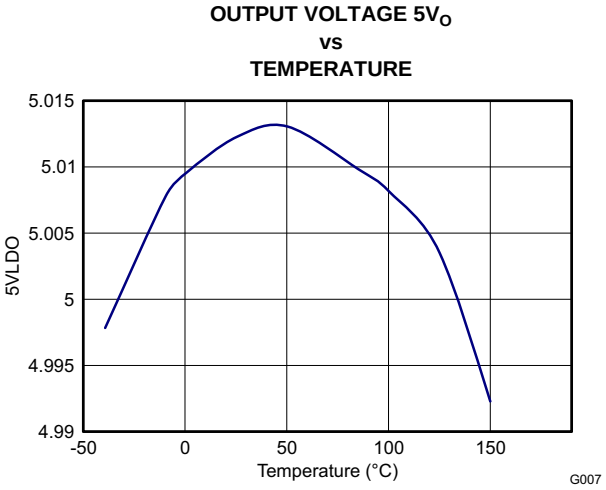


Figure 9.

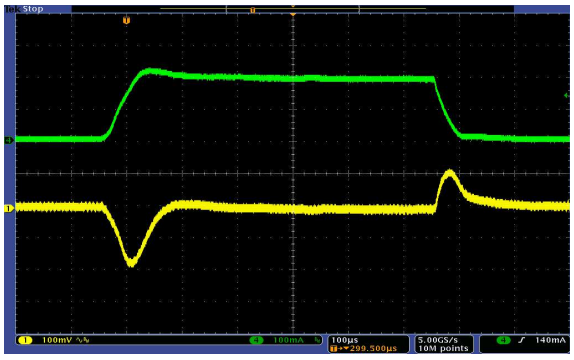


Figure 10. Load Transient Response, 10 mA to 200 mA

3.3-V Linear Regulator Controller ($3.3V_O$)

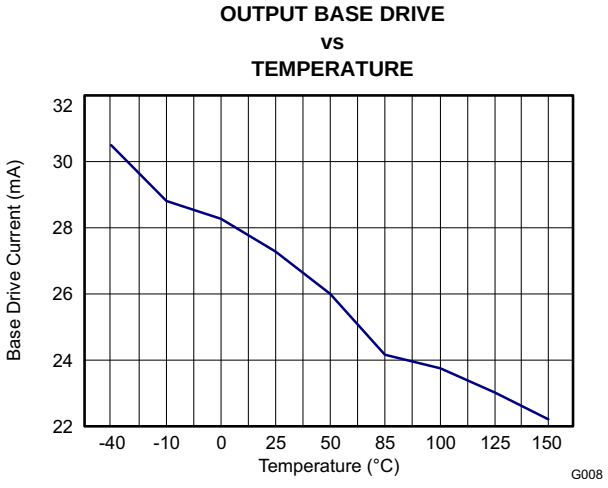


Figure 11.

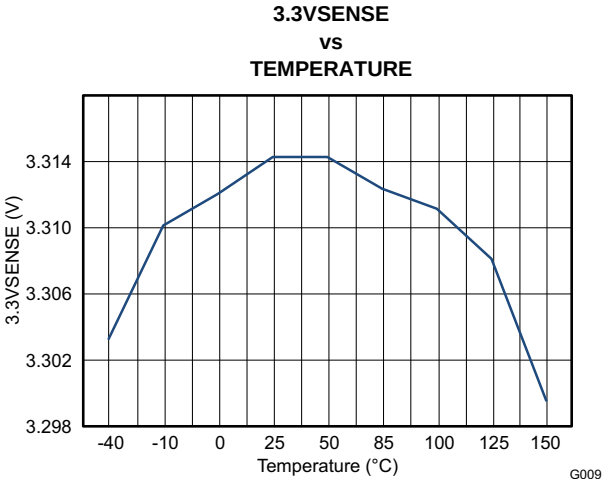


Figure 12.

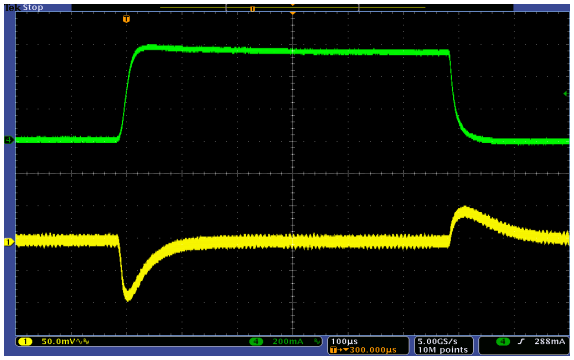


Figure 13. Load Transient Response, 10 mA to 550 mA

1.2V Linear Regulator Controller ($1.2V_O$)

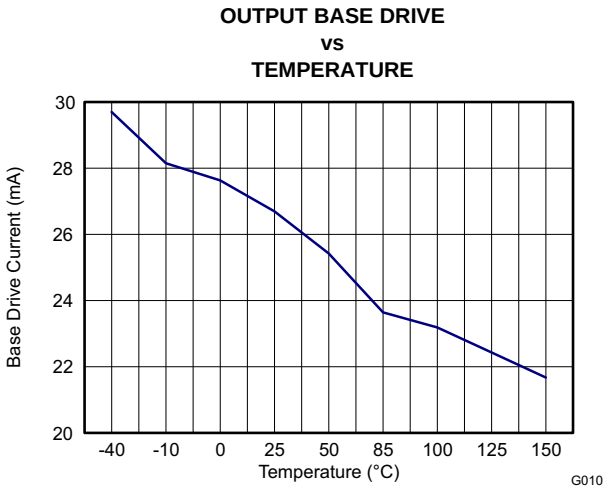


Figure 14.

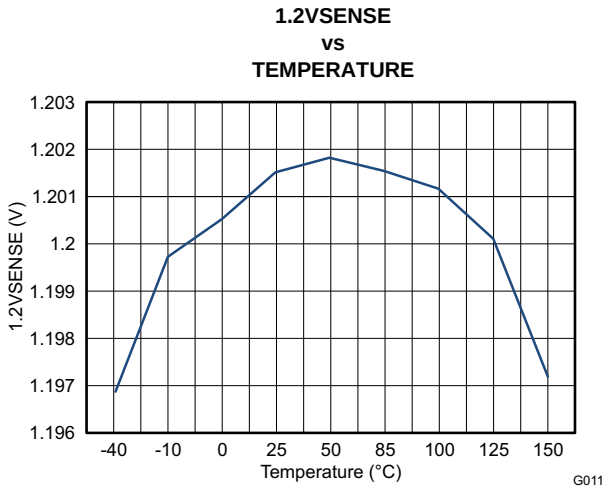


Figure 15.

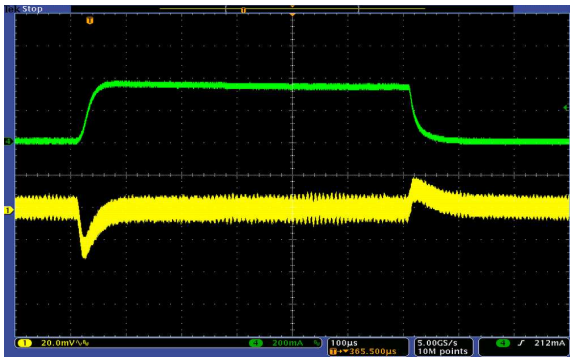


Figure 16. Load Transient Response, 10 mA to 350 mA

INTERNAL FUNCTIONAL BLOCKS

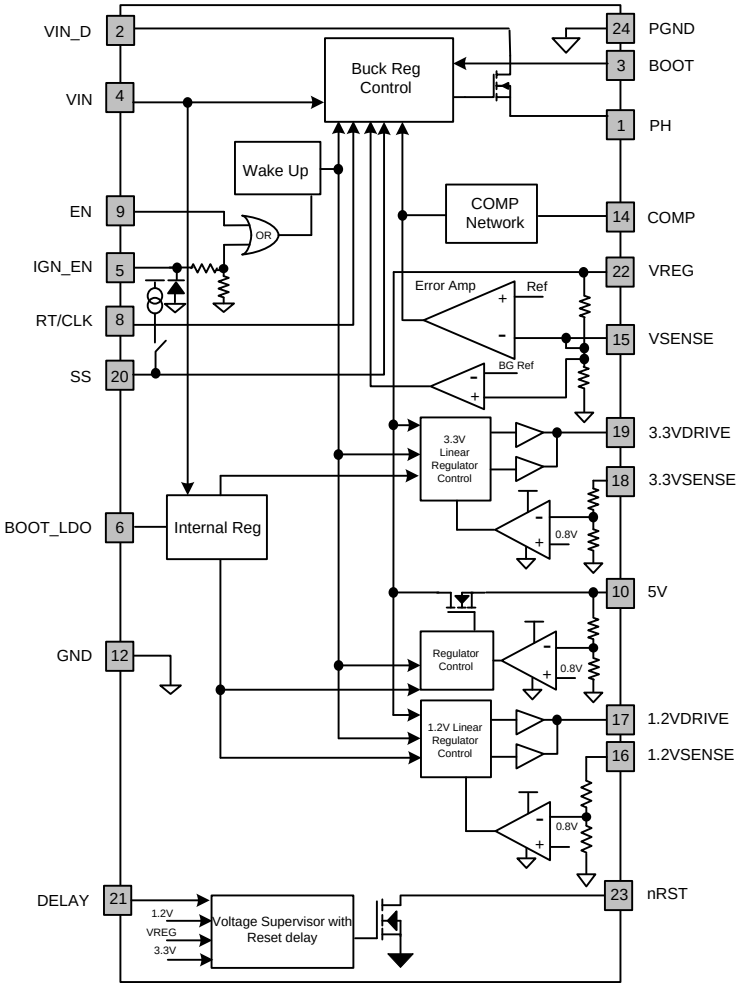


Figure 17. Internal Functional Blocks

PIN FUNCTIONS

Buck Supply, VIN_D

This is an input power source for the internal high-side MOSFET of the switch-mode power supply.

Phase Node for Buck Regulator, PH

This terminal provides the floating voltage reference for the internal drive circuitry.

Bootstrap, BOOT

The ceramic capacitor on this pin acts a as a voltage supply for the internal high-side MOSFET gate-drive circuitry. The capacitor connects between the BOOT and PH terminals. Operating with a duty cycle of 100% automatically reduces the duty cycle to approximately 95% on every fifth cycle to allow this capacitor to recharge.

Voltage-Sense Node, VSENSE

An internal resistor between VREG and this pin and another internal resistor between this pin and ground form the voltage-sense network. This terminal is the inverting input for the error amplifier of the control loop. This input is compared to an internal reference of 2 V for the control circuitry.

Error Amplifier Output, COMP

The error amplifier output forms a compensation network for the voltage mode control topology. The amplifier changes state with increase in voltage output on this pin.

Internal Regulated Boot Supply, BOOT_LDO

The internally regulated supply acts as a refresh power source for the bootstrap capacitor every switching cycle. An external capacitor to ground is needed to stabilize the voltage source.

Clock Pulse, RT/CLK

A resistor to ground on this terminal sets the buck converter switching frequency. Alternatively, an external clock input on this pin overrides the internal free-running clock (default value) by detecting positive edges of consecutive pulses and synchronizing to the external input signal. If the external clock input is removed, the system synchronizes to the internal clock signal of 2.2 MHz.

Output Voltage, VREG

This terminal represents the buck (step-down) output voltage VREG of the converter. The output voltage of the buck-mode regulator is fixed at 5.3V. This output requires a ceramic capacitor (4.7µF to 10µF range).

Ignition Enable Input, IGN_EN

The IGN_EN pin acts as an enable/disable input to activate the step-down power-supply output. The input is high-voltage tolerant up to 45V. An internal resistor limits current flow out of this terminal from the ground terminal during negative inputs.

Logic Level Enable Input, EN

The EN pin is a logic-level disable input to all outputs when IGN_EN is low and all outputs are active.

Regulated Output, 5V

This terminal is the regulated output and requires a low-ESR ceramic capacitor to ground for loop stabilization. This capacitor must be placed close to the pin of the IC. The output requires larger capacitance to compensate for wide load transient steps.

Power-On Delay, DELAY

A capacitor on this pin sets the desired delay time. The output of this pin provides a source current to charge the external capacitor once the VREG, 3.3V and 1.2V supplies have all exceeded the internally set threshold (0.9 × their respective regulated supply values).

3.3-V Drive Output, 3.3VDRIVE

This pin provides an output to drive an external bipolar transistor (BJT) for the 3.3V supply. The output is protected by current limiting of both the source and sink capabilities.

3.3-V Voltage Sense, 3.3VSENSE

This pin is the voltage node of 3.3V supply. Voltage of approximately 1.65V on this terminal initiates a current foldback during shorts on the regulated output.

1.2-V Drive Output, 1.2VDRIVE

This pin provides an output to drive an external bipolar transistor (BJT) for the 1.2V supply. The output is protected by current limiting of both the source and sink capabilities.

1.2-V Voltage Sense, 1.2VSENSE

This pin is the voltage node of 1.2V supply. Voltage of approximately 0.6 V on this terminal initiates a current foldback during shorts on the regulated output.

Soft Start, SS

A ceramic capacitor is connected from this terminal to ground to set a soft-start timer for the buck regulator supply. There is an internal pullup current source of 50 µA typical, which is activated on IGN_EN to charge the external capacitor on the SS pin.

Input Voltage, VIN

The VIN pin is the input power source for the device. This pin must be externally protected against voltage levels greater than 45 V and against a reversed battery. This input line requires a filter capacitor to minimize noise. Additionally, for EMI considerations, an input filter inductor may also be required.

Reset Indicator, nRST

The nRST pin is an open-drain output. The power-on reset output is asserted low until the output voltages on the VREG, 3.3V, and 1.2V supplies exceed their set thresholds and the power-on delay timer has expired. Additionally, whenever the IGN_EN and EN_LIN_REG pins are low or open, nRST is immediately asserted low regardless of the output voltage. If a thermal shutdown occurs due to excessive thermal, conditions this pin is asserted low.

Ignition Input Status, IGN_ST

The IGN_ST pin is an open-drain output. This output indicates whether input signal IGN_EN is present. Additionally, whenever the IGN pin is low or open, IGN_ST is immediately asserted low.

Power Ground, PGND

Power ground terminal, which is internally connected to the exposed thermal pad.

Ground, GND

Signal ground terminal, which is internally connected to the exposed thermal pad.

DEVICE INFORMATION

Buck Converter

PWM Operation

The switch-mode power supply (SMPS) operates in a fixed-frequency adaptive on-time control pulse-width modulation (PWM). The switching frequency is set by an external resistor or synchronized with an external clock input. The internal N-channel MOSFET is turned on (SET) at the beginning of each cycle. This MOSFET is turned off (RESET) when the PWM comparator resets the latch. Once the high external FET is turned OFF, the external Schottky diode recirculates the energy stored in the inductor for the remainder of the switching period.

The external bootstrap capacitor acts as a voltage supply for the internal high side MOSFET. This capacitor is recharged on every recirculation cycle (when the internal high-side MOSFET is turned OFF). In the case of commanding 100% duty cycle for the internal high side MOSFET, the device automatically revert to 87% to allow the bootstrap capacitor to recharge.

Voltage-Mode Control Loop

The voltage-mode control monitors the set output voltage and processes the signal to control the internal MOSFET. A voltage feedback signal is compared to a constant ramp waveform, resulting in a PWM modulation pulse. An input line-voltage feedforward technique is incorporated to compensate for changes in the input voltage and ensures the output voltage is stable by adjusting the ramp waveform for the correct duty cycle. The internal MOSFET is protected from excess power dissipation with a current limit and frequency foldback circuitry during an output-to-ground short-circuit event.

A combination of internal and external components forms a compensation network to ensure error-amplifier gain does not cause instability due to input voltage changes or load perturbations.

Modes of Operation

The converter operates in different modes based on load current, input voltage, and component selection.

Continuous-Conduction Mode (CCM)

This mode of operation is typically when the inductor current is non-zero and the load current is greater than $I_{L\ CCM}$.

$$I_{IND\_CCM} \geq \frac{(1-D)\times VREG}{2\times f_{SW}\times L}$$

where

I_{IND_CCM} = Inductor current in continuous-conduction mode
D = duty cycle
VREG = output voltage
L = Inductor
f_{SW} = switching frequency

In this mode, the duty cycle should always be greater than the minimum t_{ON} or the converter may go into burst mode.

Discontinuous Mode (DCM)

$$I_{IND\_DCM} \geq \frac{(1-D)\times VREG}{2\times f_{SW}\times L}$$

This mode of operation is typically when the inductor current goes to zero and the load current is less than $I_{IND\ DCM}$.

Tracking Mode

When the input voltage is low and the converter approaches approximately 100% duty cycle, the following equation determines the output voltage.

$$VREG = \left(1-\frac{t_{OFF\_MIN}}{T}\right)\times(VIN - I_{Load}\times R_{DS})$$

where

t = Period
R_{DS} = Internal FET resistance
I_{LOAD} = output load current

Output Voltage 5.3V (VREG)

Output voltage VREG is generated by the converter supplied from the battery voltage VIN and the external components (L, C). The output is sensed through an internal resistor divider and compared with an internal reference voltage.

This output requires larger output capacitors (4.7-µF to 10-µF range) to ensure that during load transients the output does not drop below the reset threshold for a period longer than the reset deglitch filter time.

An internal load is enabled for a short period whenever

- a start-up condition occurs, that is, during power up or when IGN_EN or EN is toggled.
- an overvoltage condition exists on this output.

Switching Frequency (RT/CLK)

The oscillator frequency of the buck regulator is selectable by means of a resistor placed at the RT/CLK pin to ground. The switching frequency (f_{SW}) can be set in the range 2 MHz to 3 MHz in this resistor mode. Alternatively, if there is an external clock input signal, the internal oscillator synchronizes to this signal within 10 µs.

The following equation determines the value of resistor (RT) for the required switching frequency f_{SW}.

$$RT = \frac{98.4 \times 10^9}{f_{SW}} \quad \text{(Ohms)}$$

Boost Capacitor (BOOT)

This capacitor provides the gate-drive voltage for the internal MOSFET switch. X7R and X5R grade dielectrics are recommended due to their stable values over temperature. It may be necessary to select a lower value of boost capacitor for low-Vreg and/or high-frequency applications, or to select a higher value for high-Vreg and/or low-frequency applications (for example, 100 nF for 500 kHz/5 V and 220 nF for 500 kHz/8 V.) Usually, a 0.1-µF capacitor is used for the boot capacitor.

Soft Start (SS)

To limit the start-up inrush current for the switch-mode supply, an internal soft-start circuit is used to ramp up the reference voltage from 0 V to its final value of 0.8 V. The regulator uses the internal reference or the SS-pin voltage as the power-supply reference voltage to regulate the output accordingly. The following equation determines the soft-start timing.

$$\text{Time } (t_{SS}) = \frac{C \times 0.8 \text{ V}}{50 \times 10^{-6}}$$

where C = Capacitor on SS pin, usually 0.1 µF or lower

Power-On Delay (DELAY)

The power-on delay function delays the release of the nRST line. The method of operation is to detect when all VREG (5.3 V), 3.3 ,V and 1.2V power-supply outputs are above 90% (typical) of the set value. This then triggers a current source to charge the external capacitor on the DELAY terminal. Once this capacitor is charged to approximately 2 V, the nRST line is asserted high. The delay time is calculated using the following equation:

$$t_{DELAY} = \frac{2 \text{ V} \times C}{2 \text{ µA}}$$

Where C = capacitor on DELAY pin.

Example: For a 20ms delay, C = 20 nf.

Reset (nRST)

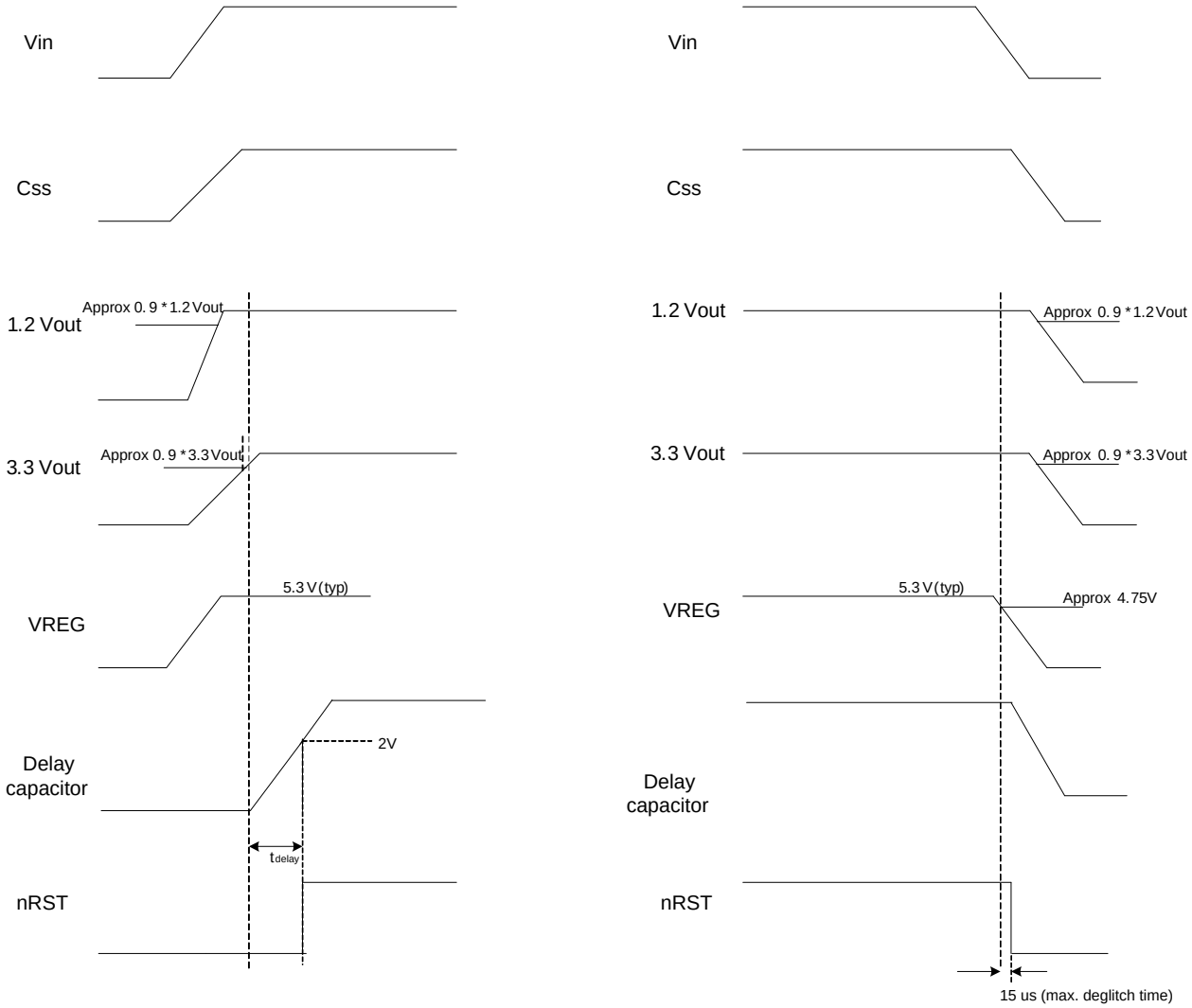
The nRST pin is an open-drain output. The power-on reset signal is a voltage supervisor output to indicate the output voltages on VREG (5.3 V), 3.3V, and 1.2V are within the specified tolerance of their set regulated voltages. Additionally, whenever both the IGN_EN and EN pins are low or open, nRST is immediately asserted low regardless of the output voltage. If a thermal shutdown occurs due to excessive thermal conditions, this pin is asserted low.

Conversely on power down, once the VREG or 3.3V or 1.2V output voltage falls below 90% of its respective set threshold, nRST is pulled low after a de-glitch filter delay of approximately 15 µs (max). This is implemented to prevent nRST from being invoked due to noise on the output supplies.

Thermal Shutdown

This device has independent two thermal sensing circuits for the VREG (5.3 V), 5V regulators; if either one of these circuits detects the power FET junction temperature to be greater than the set threshold, that particular output-power switch is turned OFF. The appropriate FET turns back ON once it is allowed to cool sufficiently. The thermal sensing and shutdown circuitry is only activated when nRST is high.

Reset Function



On power up, ALL three regulated supplies, VREG, 3.3 V, and 1.2 V, must be more than 90% of their respective values before the delay timer capacitor on the DELAY pin can start charging.

On power down, if any one of the three regulated supplies, VREG, 3.3 V, or 1.2 V, drops below 90% of its value, nRST is asserted low after a small deglitch filter time. Once nRST is asserted low, it can only go high again after ALL three supplies are above the 90% value and the DELAY pin voltage is higher than 2 V.

Figure 18. Reset Function

Linear Regulators

Fixed Linear Regulator Output (5.3V)

This is a fixed, regulated output of 5.3 V ±2% over temperature and input supply using a precision voltage-sense resistor network. A low-ESR ceramic capacitor is required for loop stabilization; this capacitor must be placed close to the pin of the IC. This output is protected against shorts to ground by a foldback current limit for safe operating conditions, and a current limit for limiting inrush current due to depleted charge on the output capacitor. Initial IGN_EN or EN initiates power cycle of the soft-start circuit on this regulator. This typically is in the 1ms to 2ms range. This output may require a larger output capacitor to ensure that during load transients the output does not drop below the required regulated specifications.

Fixed Linear Regulator Controller (3.3V)

The linear regulator controller requires an external NPN bipolar pass transistor of sufficient gain stage to support the maximum load current required. The base-drive output current is protected by current limiting both the source and sink drive circuitry. The 3.3VSENSE pin is the remote sense input of the output of the REG3 supply and controls the 3.3VDRIVE output accordingly. This regulator is fixed 3.3V with ±2% tolerance using a precision voltage-sense resistor network. A low-ESR ceramic output capacitor is used for loop compensation of the regulator. A voltage on this pin of less than approximately 50% of the regulated value initiates a current limit on the 3.3VDRIVE output.

This output may require larger output capacitors to support load transients, so the output does not drop below 90% of 3.3 V.

Fixed Linear Regulator Controller (1.2V)

The linear regulator controller requires an external NPN bipolar pass transistor of sufficient gain stage to support the maximum load current required. The 1.2VSENSE pin is the remote sense input of the output of 1.2V supply and controls the 1.2VDRIVE output accordingly. This regulator output is 1.2 V with ±2% tolerance using a precision voltage-sense resistor network. A low-ESR ceramic output capacitor is used for loop compensation of the regulator. A voltage on this pin of less than approximately 50% of the regulated value initiates a current limit on the 1.2VDRIVE output.

This output may require larger output capacitors to support load transients, so the output does not drop below 90% of 1.2V.

Modes of Operation

Operational Mode

The purpose of the EN input is to keep the regulated supplies ON for a period for the microprocessor to log information into the memory locations once the ignition input is disabled. The microprocessor disables the power supplies by pulling EN low after this activity is complete.

APPLICATION INFORMATION

This is a starting point and theoretical representation of the values to be used for the application, further optimization of the components derived may be required to improve the performance of the device.

Buck Converter

Duty Cycle

$$D = \frac{V_O}{V_I}$$

where

V_O = Output voltage

V_I = Input voltage

Output Inductor Selection (L)

The minimum inductor value is calculated using the coefficient K_{IND} that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor, and so the typical range of this ripple current is in the range of K_{IND} = 0.2 to 0.3, depending on the ESR and the ripple-current rating of the output capacitor.

Inductor ripple current

$$I_{Ripple} = K_{IND} \times I_O$$

where

I_O = Output current

Benefits of Low Inductor Value

- Low inductor value gives high di/dt, which allows for fewer output capacitors for good load transient response.
- Gives higher saturation current for the core due to fewer turns
- Fewer turns yields low DCR and therefore less dc inductor losses in the windings.
- High di/dt provides faster response to load steps.

Benefits of High Inductor Value

- Low ripple current leads to lower conduction losses in MOSFETs
- Low ripple; means lower RMS ripple current for capacitors
- Low ripple; yields low ac inductor losses in the core (flux) and windings (skin effect)
- Low ripple; gives continuous inductor current flow over a wide load range

$$L_{Min} = \frac{(V_{I\text{-}Max} - V_O) \times V_O}{f_{SW} \times I_{Ripple} \times V_{I\text{-}Max}}$$

where

f_{SW} is the regulator switching frequency

I_{Ripple} = Allowable ripple current in the inductor, typically ±20% of maximum output load I_O

Inductor Peak Current

$$I_{L\text{-}Peak} = I_O + \frac{I_{Ripple}}{2}$$

Output Capacitor Selection (C_O)

The selection of the output capacitor determines several parameters in the operation of the converter, the modulator pole, the voltage droop on the out capacitor, and the output ripple.

During a load step from no load to full load or changes in the input voltage, the output capacitor must hold up the output voltage above a certain level for a specified time and not issue a reset until the main regulator control loop responds to the change. The capacitance value determines the modulator pole and the rolloff frequency due to the LC output-filter double pole—the output ripple voltage is a product of the output capacitor ESR and ripple current.

The minimum capacitance needed to maintain desired output voltage during a high-to-low load transition and prevent overshoot is

$$C_O = \frac{L\left((I_{O\text{-}max})^2 - (I_{O\text{-}min})^2\right)}{(V_{O\text{-}max})^2 - (V_{O\text{-}min})^2}$$

where

$I_{o\text{-}max}$ is maximum output current.

$I_{o\text{-}min}$ is minimum output current.

The difference between the output current, maximum to minimum, is the worst-case load step in the system.

$V_{o\text{-}max}$ is maximum tolerance of regulated output voltage.

$V_{o\text{-}min}$ is the minimum tolerance of regulated output voltage.

Output capacitor root-mean-square (RMS) ripple current I_{O_RMS}. This is to prevent excess heating or failure due to high ripple currents.

This parameter is sometimes specified by the manufacturer.

$$I_{O\_RMS} = \frac{V_O \times (V_{I\text{-}max} - V_O)}{\sqrt{12} \times V_{I\text{-}max} \times L \times f_{SW}}$$

External Schottky Diode (D)

The TPS65300 requires an external ultrafast Schottky diode with fast reverse-recovery time connected between the PH and power ground terminals. The diode conducts the output current during the off-state of the internal power switch. This diode must have a reverse breakdown higher than the maximum input voltage of the application. A Schottky diode is selected for its lower forward voltage. The Schottky diode is selected based on the appropriate power rating, which factors in the dc conduction losses and the ac losses due to the high switching frequencies. The power dissipation P_D is determined by

$$P_D = I_O \times V_{FD} \times (1 - D) + \frac{(V_I - V_{FD})^2 \times f_{SW} \times C_J}{2}$$

where

V_{FD} = forward conducting voltage of Schottky diode

C_J = junction capacitance of the Schottky diode

Input Capacitor (C_I)

The TPS65300 requires an input ceramic decoupling capacitor type X5R or X7R and bulk capacitance to minimize input ripple voltage. The dc voltage rating of this input capacitance must be greater than the maximum input voltage. The capacitor must have an input ripple-current rating higher than the maximum input ripple current of the converter for the application. The input capacitors for power regulators are chosen to have reasonable capacitance-to-volume ratio and to be fairly stable over temperature. The value of the input capacitance is based on the input voltage desired (ΔV_I).

$$C_I = \frac{I_{O\text{-}max} \times 0.25}{\Delta V_I \times f_{SW}}$$

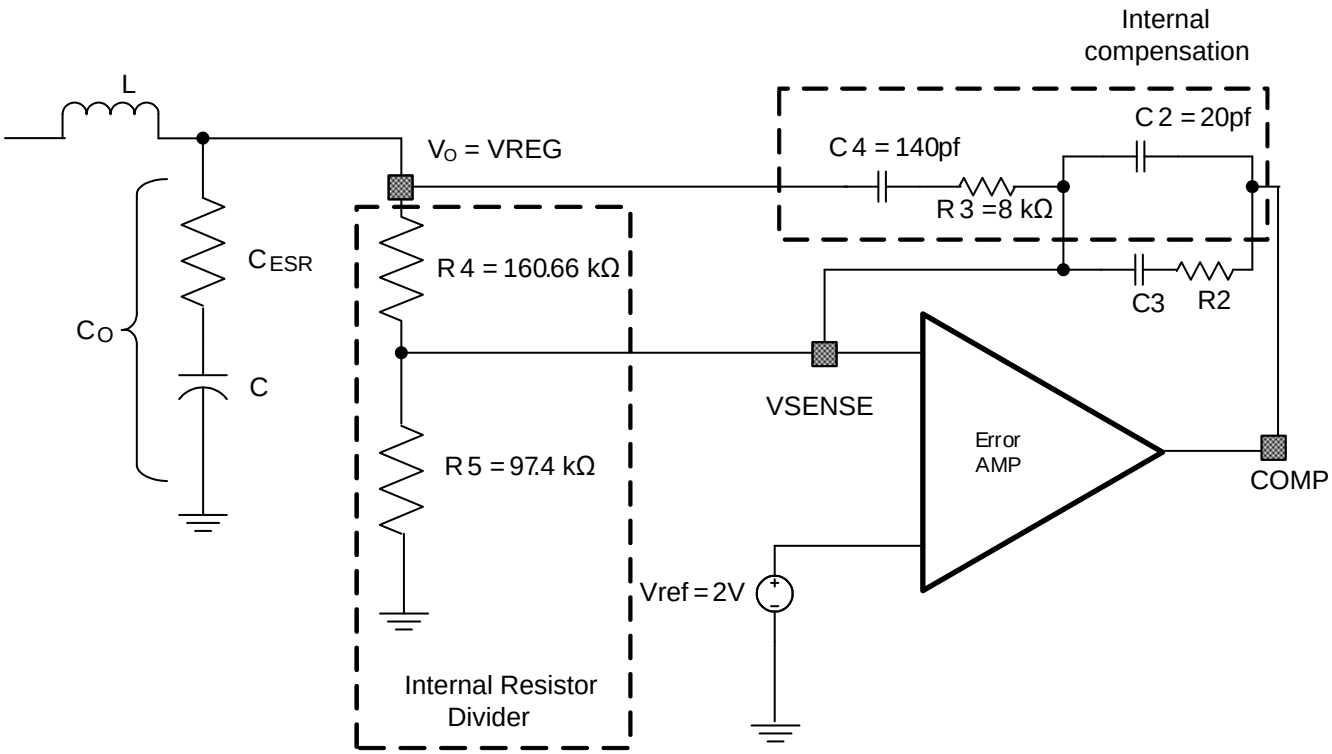
Input capacitor root-mean-square (RMS) ripple current I_{I_RMS} is calculated using the following equation.

$$I_{I\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{I\_min}} \times \left(\frac{V_{I\_min} - V_O}{V_{I\_min}} \right)}$$

Loop Compensation

The double pole is due to the output-filter components inductor and capacitor. The calculations for the following equations use values taken from Figure 19.

Loop-Control Frequency Compensation



Type III Compensation

Figure 19. Loop-Control Frequency Compensation

Type III Compensation

$f_{CO} = f_{SW} \times 0.1$ (the cutoff frequency when the gain is 1 is called the unity-gain frequency).

f_{CO} is typically 1/5 to 1/10 of the switching frequency double-pole frequency response due to the LC output filter. The LC output filter gives a *double pole*, which has a –180° phase shift.

Make the two zeroes close to the double pole (LC), for example, $f_{Z1} \approx f_{Z2} \approx 1/2\pi(LC_{OUT})^{1/2}$.

1. Make the first zero below the filter double pole (approximately 50% to 75% of f_{LC})
2. Make the second zero at the filter double pole (f_{LC})

   Make the two poles above the crossover frequency f_{CO}.
3. Make the first pole at the ESR frequency (f_{ESR})
4. Make the second pole at 0.5 the switching frequency

The following compensation components are integrated in the device with the following typical values. Guidelines for compensation components:

R3 = 8 kΩ, C4 = 140 pF, C2 = 20 pF

The double pole to due to the output filter components LC,

$$f_{LC} = \frac{1}{2\pi\sqrt{LC_O}}$$

The ESR of the output capacitor C gives a zero that has a 90° phase shift. The ESR of the output capacitor should be in the range of 1 mΩ to 100 mΩ.

$$f_{ESR} = \frac{1}{2\pi \times C_O \times ESR}$$

PWM Modulator Gain K

$$K = \frac{V_I}{V_{ramp}}$$

where Vramp = V_I / 10, V_I = Input operating voltage

Resistor Values

Select R5 = 97.4 kΩ

$$R4 = \frac{R5 \times (V_O - V_{ref})}{V_{ref}}, \quad \text{where } V_{ref} = 2\ V$$

$$R2 = \frac{f_{CO} \times V_{ramp} \times R4}{f_{LC} \times V_I}$$

Calculate C3 based on placing a zero at 50% to 75% of the output-filter double-pole frequency (below set at 50%).

$$C3 = \frac{1}{\pi \times R2 \times f_{LC}}$$

Gain of Amplifier

$$A_V = \frac{R2 \times (R4 + R3)}{(R4 \times R3)}$$

Poles and Zero Frequencies

$$f_{P1} = \frac{1}{2\pi \times R2 \times C2}$$

$$f_{P2} = \frac{1}{2\pi \times R3 \times C4}$$

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C3}$$

$$f_{Z2} = \frac{1}{2\pi \times R4 \times C4}$$

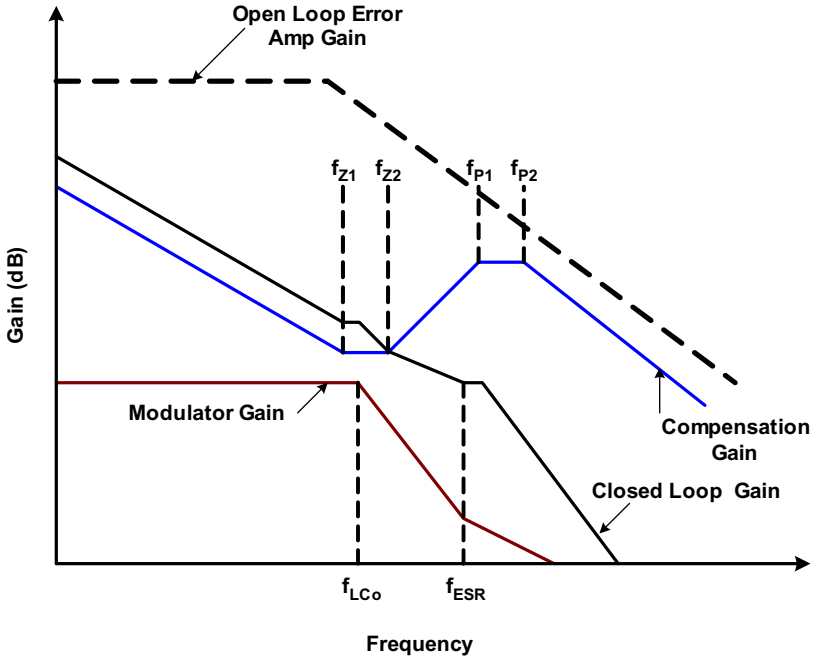


Figure 20. Typical Gain vs Frequency

Power Dissipation

Switch-Mode Power-Supply Losses

The power dissipation losses are applicable for continuous-conduction mode operation (CCM).

$P_{5.3V\_CON} = I_O^2 \times R_{ds(on)} \times (V_O/V_I)$ (Conduction losses)

$P_{5.3V\_SW} = ½ \times V_I \times I_O \times (t_r + t_f) \times f_{SW}$ (Switching losses)

$P_{5.3V\_Gate} = V_{drive} \times Qg \times fsw$ (Gate drive losses)
where typically $Qg = 1 \times 10^{-9}$ (nC)

$P_{IC} = V_I \times$ Iq-normal (Supply losses)

$P_{Total} = P_{CON} + P_{SW} + P_{Gate} + P_{5V\_Lin\ Reg} + P_{IC}$

where

- V_O = VREG = Output voltage
- V_I = Input voltage
- I_O = Output current
- t_r = FET switching rise time (t_r max. = 20 ns)
- t_f = FET switching fall time (t_f max. = 20 ns)
- V_{drive} = FET gate-drive voltage (typically V_{drive} = 6 V and V_{drive} max. = 8 V)
- f_{SW} = Switching frequency

Linear Regulator (5V)

$P_{5V\_Lin\ Reg} = (VREG – 5\ V) \times I_O$

For given operating ambient temperature T_A

$T_J = T_A + R_{th} \times P_{Total}$

For a given max junction temperature $T_{J\text{-}Max}$ = 150°C

$T_{A\text{-}Max} = T_{J\text{-}Max} – R_{th} \times P_{Total}$

where

P_{Total} = Total power dissipation (watts)
T_A = Ambient temperature in °C
T_J = Junction temperature in °C
$T_{A\text{-}Max}$ = Maximum ambient temperature in °C
$T_{J\text{-}Max}$ = Maximum junction temperature in °C
R_{th} = Thermal resistance of package in (°C/W)

Other factors not included in the foregoing information which affect the overall efficiency and power losses are

- Inductor ac and dc losses
- Trace resistance and losses associated with the copper trace routing connection
- Schottky diode

PCB Layout

The following guidelines are recommended for PCB layout of the TPS65300 device.

Inductor L

Use a low-EMI inductor with a ferrite-type shielded core. Other types of inductors may be used; however, they must have low-EMI characteristics and be located away from the low-power traces and components in the circuit.

Input Filter Capacitors C_I

Input ceramic filter capacitors should be located in close proximity to the VIN terminal. Surface-mount capacitors are recommended to minimize lead length and reduce noise coupling.

Feedback

Route the feedback trace such that there is minimum interaction with any noise sources associated with the switching components. Recommended practice is to ensure placing the inductor away from the feedback trace to prevent a source of EMI noise.

Traces and Ground Plane

All power (high-current) traces should be thick and as short as possible. The inductor and output capacitors should be as close to each other as possible. This reduces EMI radiated by the power traces due to high switching currents.

In a two-sided PCB it is recommended to have ground planes on both sides of the PCB to help reduce noise and ground-loop errors. The ground connection for the input and output capacitors and IC ground should be connected to this ground plane.

In a multi-layer PCB, the ground plane is used to separate the power plane (where high switching currents and components are placed) from the signal plane (where the feedback trace and components are) for improved performance.

Also arrange the components such that the switching-current loops curl in the same direction. Place the high-current components such that during conduction the current path is in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles, helping to reduce radiated EMI.

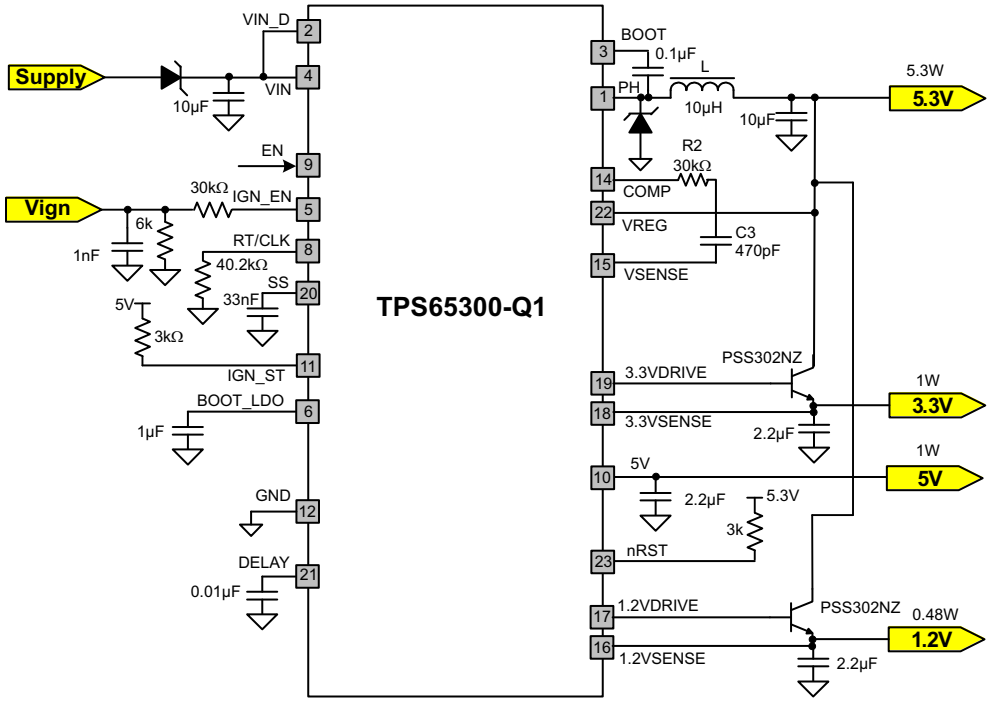
Application Notes

Design Guide – Step-by-Step Design Procedure

Following are the details of a switching regulator design using the requirements of Table 2.

Table 2. Switching Regulator Requirements

Parameter	Requirement
Input voltage, V_I	6.5 V to 27 V, typical 14 V
Output voltage, 5.3 V	5.3 V_O ±2% at 5.3 W
Maximum output current $I_{5.3V\_max}$	1 A
Minimum output current $I_{5.3V\_min}$	0.01 A
Transient response 0.01A to 0.8 A	5%
Reset threshold	90% of output voltage
5V	5V_O at 1 W
3.3V	3.3V_O at 1 W
1.2V	1.2V_O at 0.5 W
Switching frequency f_{SW}	2.5 MHz
Overvoltage threshold	106% of output voltage
Undervoltage threshold	95% of output voltage



L: B82462G4103MOOO (EPCOS) or XFL4020 472MEB (Coilcraft)
S1: MBRS310T3 (ON Semiconductors) or SS3H10 (Vishay)
S2: B240A, SS16 (Vishay)
External BJT: PBSS302NZ (NXP)

Figure 21. Application Schematic

Duty Cycle

$$D = \frac{V_O}{V_I} = \frac{5.3}{14} = 0.378$$

Output Inductor Selection (L)

$$I_{Ripple} = K_{IND} \times I_O = 0.25 \times 1 = 0.25 \text{ A}$$

$$L_{Min} = \frac{(V_{I\text{-}Max} - V_O) \times V_O}{f_{SW} \times I_{RIPPLE} \times V_{I\text{-}Max}} = \frac{(27 - 5.3) \times 5.3}{2.5\,\text{MHz} \times 10^6 \times 0.25 \times 27} = 6.8\ \mu\text{H}$$

Use 10 µH due to variations in temperature and manufacture.

Inductor peak current:

$$I_{L\text{-}Peak} = I_O + \frac{I_{Ripple}}{2} = 1 + \frac{0.25}{2} = 1.125 \text{ A}$$

Output Capacitor Selection (C_O)

$$C_O = \frac{L\left[\left(I_{O\text{-}max}\right)^2 - \left(I_{O\text{-}min}\right)^2\right]}{\left(V_{O\text{-}max}\right)^2 - \left(V_{O\text{-}min}\right)^2}$$

$$C_O = \frac{10 \times 10^{-6}\left[(1)^2 - (0.01)^2\right]}{(5.45)^2 - (5.15)^2} = 3.18\ \mu\text{F}$$

Due to variations in temperature and manufacture, use a 10-µF capacitor with a voltage rating greater than the maximum 10-V output.

$$I_{O\_RMS} = \frac{V_O \times (V_{I\text{-}max} - V_O)}{\sqrt{12} \times V_{I\text{-}max} \times L \times f_{SW}}$$

$$I_{O\_RMS} = \frac{5.3 \times (27 - 5.3)}{\sqrt{12} \times 27 \times 10 \times 10^{-6} \times 2.5 \times 10^6} = 0.049 \text{ A}$$

External Schottky Diode (D) Power Dissipation

$$P_D = I_O \times V_{FD} \times (1 - D) + \frac{(V_I - V_{FD})^2 \times f_{SW} \times C_J}{2}$$

$$P_D = 1 \times 0.55 \times (1 - 0.378) + \frac{(14 - 0.55)^2 \times 2.5\,\text{MHz} \times 30\,\text{pF}}{2} = 0.34 \text{ W}$$

Input Capacitor (C_I)

$$C_I = \frac{I_{O\_max} \times 0.25}{\Delta V_I \times f_{SW}} = \frac{1 \times 0.25}{0.3 \times 2.5\,\text{MHz}} = 0.33\ \mu\text{F}$$

Due to variations in temperature and manufacture, use a 10-µF capacitor with a voltage rating greater than the maximum 45-V transient.

Input-capacitor root-mean-square (RMS) ripple current I_{I_RMS}:

$$I_{I\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{I\_min}} \times \left(\frac{V_{I\_min} - V_O}{V_{I\_min}}\right)} = 1 \times \sqrt{\frac{5.3}{6} \times \left(\frac{6 - 5.3}{6}\right)} = 0.32 \text{ A}$$

Loop Compensation

The double pole is due to the output filter components LC, and the calculations in the formulas refer to Figure 19.

$$f_{LC} = \frac{1}{2\pi\sqrt{LC_O}} = \frac{1}{2\pi\sqrt{10\ \mu H \times 10 \mu F}} = 15.9\ kHz$$

$$f_{ESR} = \frac{1}{2\pi \times C_O \times ESR} = \frac{1}{2\pi \times 10\ \mu F \times 0.005} = 3.2\ MHz$$

$$R4 = \frac{R5 \times (V_O - Vref)}{Vref} = \frac{97.4\ k\Omega \times (5.3 - 2)}{2} = 160.7\ k\Omega$$

$$R2 = \frac{f_{CO} \times V_{ramp} \times R4}{f_{LC} \times V_I} = \frac{250\ kHz \times 1.4 \times 160\ k\Omega}{15.9\ kHz \times 14} = 251.6\ k\Omega$$

Calculate C3 based on placing a zero at 50% to 75% of the output-filter double-pole frequency.

$$C3 = \frac{1}{\pi \times R2 \times f_{LC}} = \frac{1}{\pi \times 251.6\ k\Omega \times 15.9\ kHz} = 80\ pF$$

Poles and Zero Frequencies

$$f_{P1} = \frac{1}{2\pi \times R2 \times C2} = \frac{1}{2\pi \times 251.6\ k\Omega \times 20\ pF} = 31.6\ kHz$$

$$f_{P2} = \frac{1}{2\pi \times R3 \times C4} = \frac{1}{2\pi \times 8\ k\Omega \times 140\ pF} = 142.1\ kHz$$

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C3} = \frac{1}{2\pi \times 251.6\ k\Omega \times 80\ pF} = 7.91\ kHz$$

$$f_{Z2} = \frac{1}{2\pi \times R4 \times C4} = \frac{1}{2\pi \times 160.7\ k\Omega \times 140\ pF} = 7.07\ kHz$$

Power Dissipation

$$P_{5.3V\_CON} = I_O{}^2 \times r_{ds(on)} \times (V_O / V_I) = 1^2 \times 0.5 \times (5.3 / 14) = 0.189\ W$$

$$P_{5.3V\_SW} = 1/2 \times V_I \times I_O \times (t_r + t_f) \times f_{SW}$$
$$= 1/2 \times 14 \times 1 \times (20 \times 10^{-9} + 20 \times 10^{-9}) \times 2.5 \times 10^6 = 0.7\ W$$

$$P_{5.3V\_Gate} = V_{drive} \times Qg \times f_{SW} = 8 \times 1 \times 10^{-9} \times 2.5 \times 10^6 = 0.02\ W$$

$$P_{5V\_LinReg} = (VREG - 5V) \times I_O = (5.3 - 5.0) \times 0.2 = 0.06\ W$$

$$P_{IC} = V_I \times I_{IC} = 14 \times 5\ mA = 0.07\ W$$

$$P_{Total} = P_{5.3V\_CON} + P_{5.3V\_SW} + P_{5.3V\_Gate} + P_{5V\_LinReg} + P_{IC}$$
$$= 0.189 + 0.7 + 0.02 + 0.06 + 0.07 = 1.039\ W$$

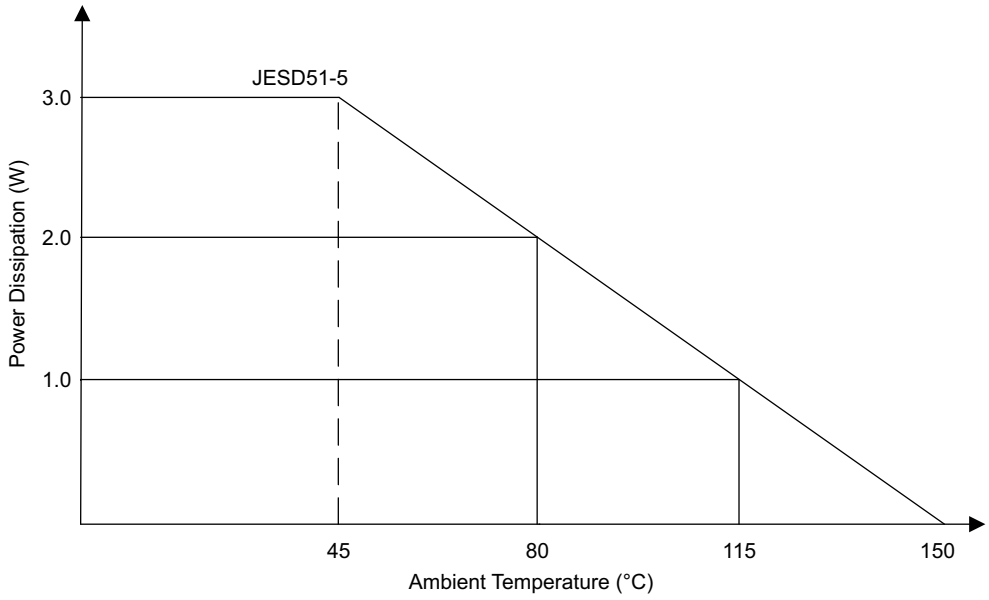


Figure 22. Power Dissipation Derating Profile, 24-Pin PWP Package With Thermal Pad

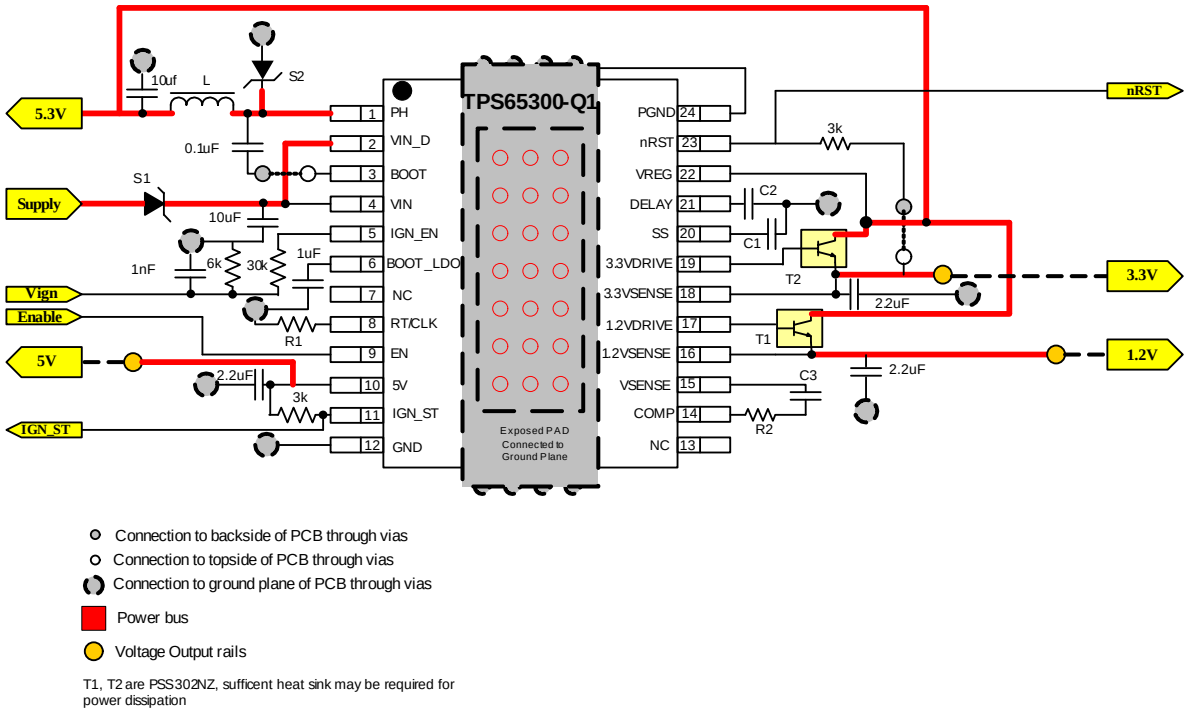


Figure 23. PCB Layout

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS65300QPWPRQ1	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS65300QRHFRQ1	PREVIEW	VQFN	RHF	24	1	TBD	Call TI	Call TI	

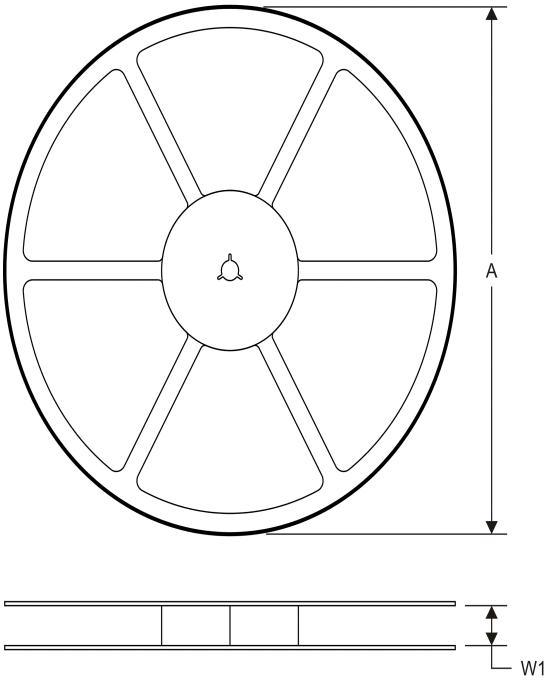
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

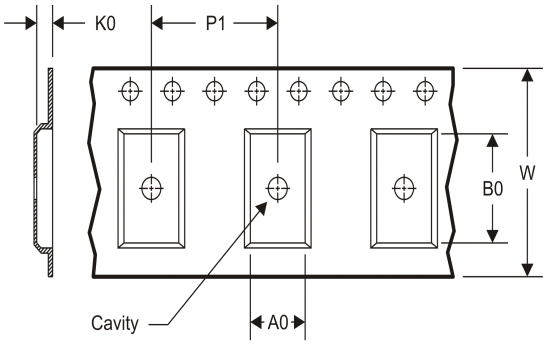
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



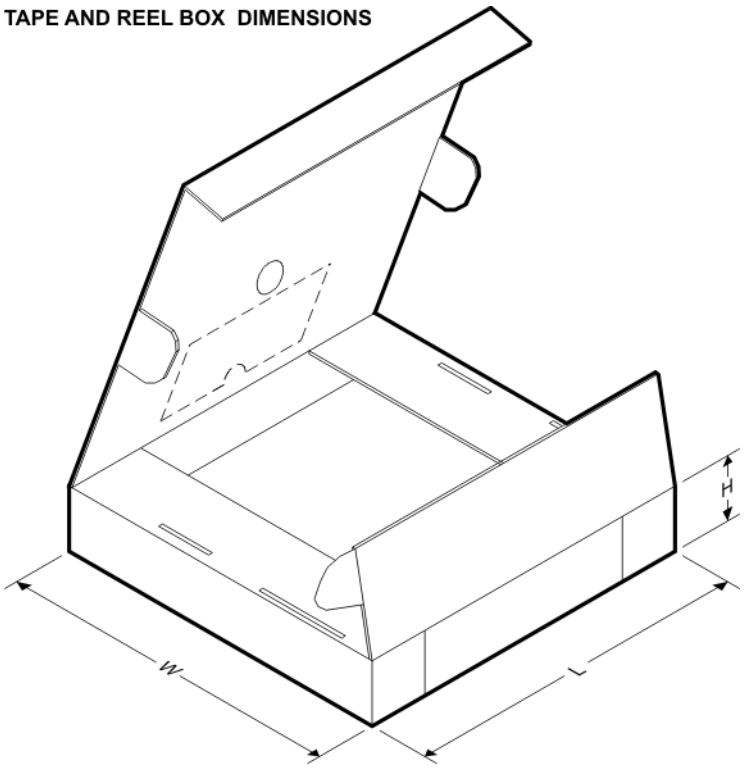
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65300QPWPRQ1	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

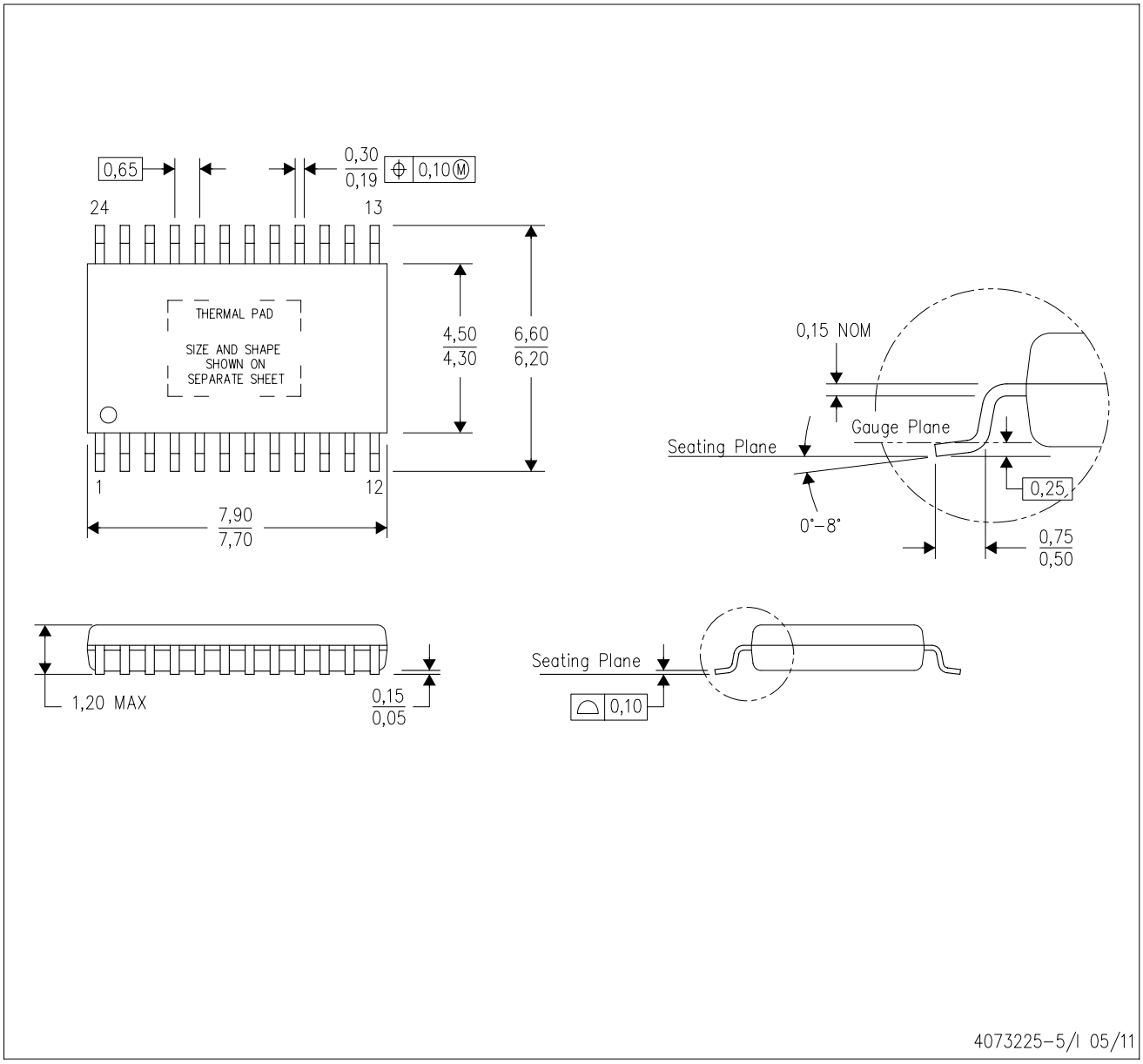
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65300QPWPRQ1	HTSSOP	PWP	24	2000	367.0	367.0	38.0

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

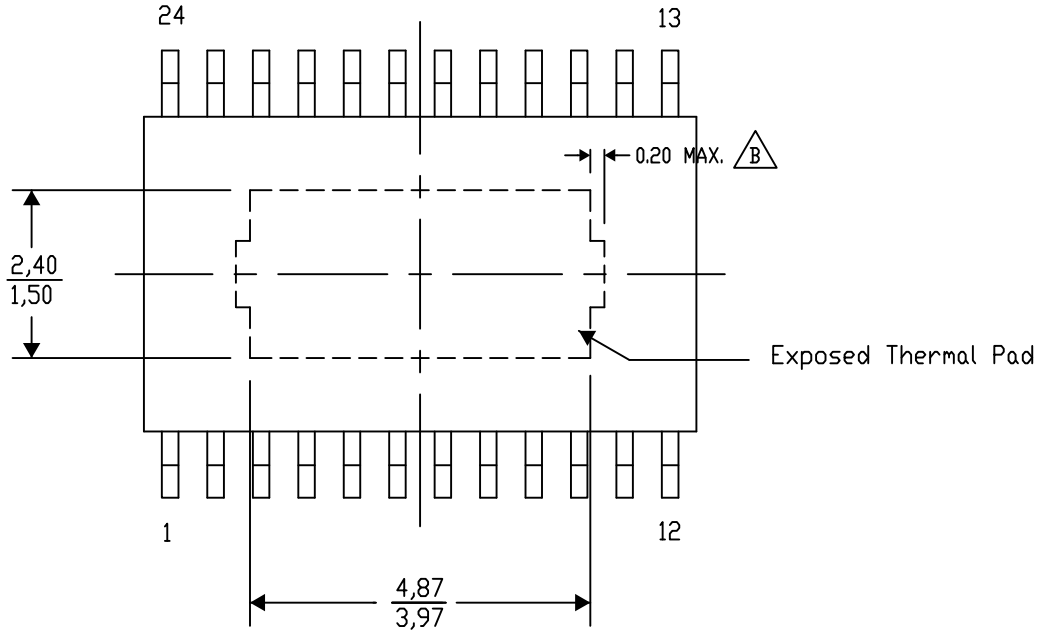
PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–29/AC 07/12

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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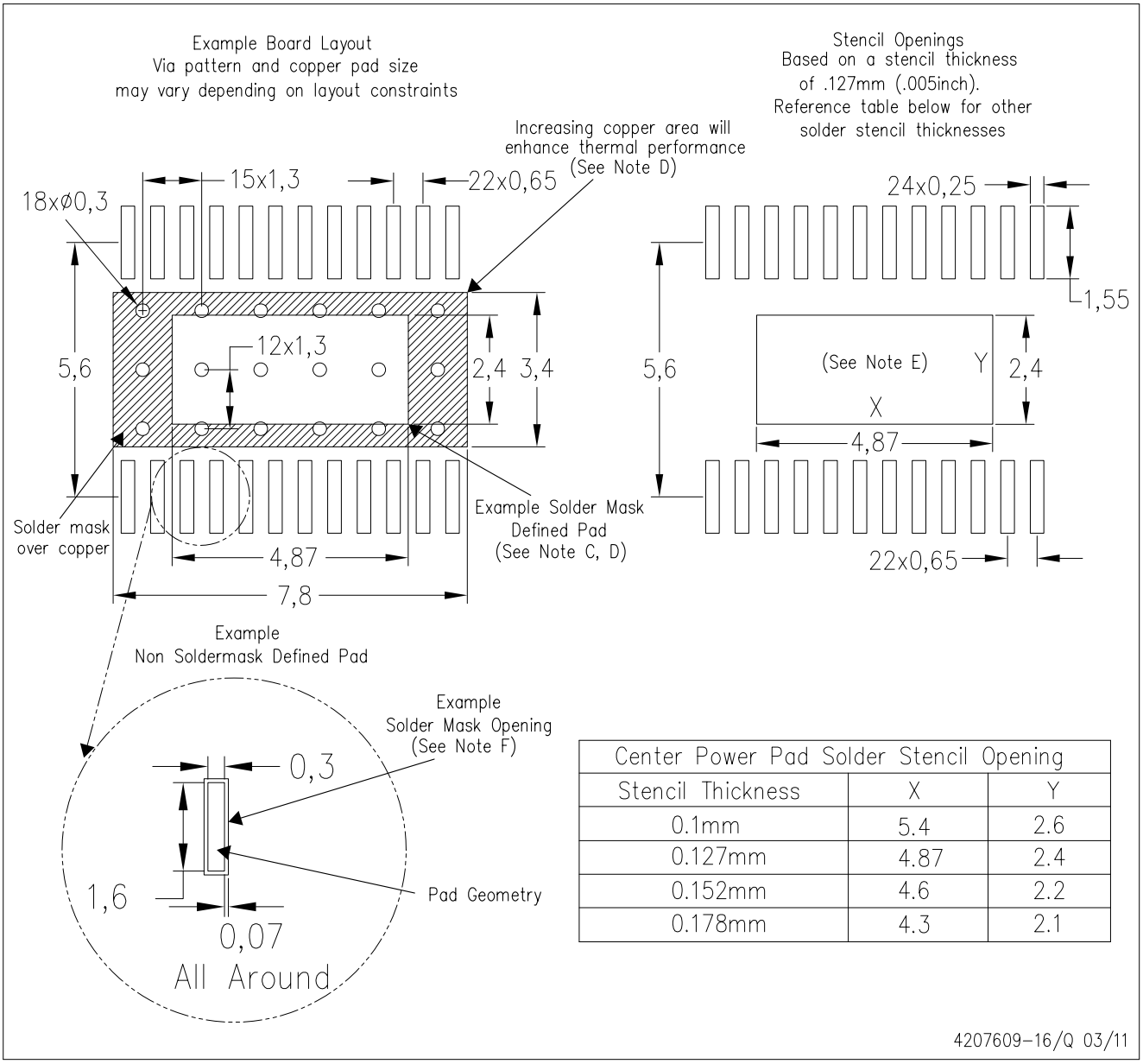
PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.4	2.6
0.127mm	4.87	2.4
0.152mm	4.6	2.2
0.178mm	4.3	2.1

4207609–16/Q 03/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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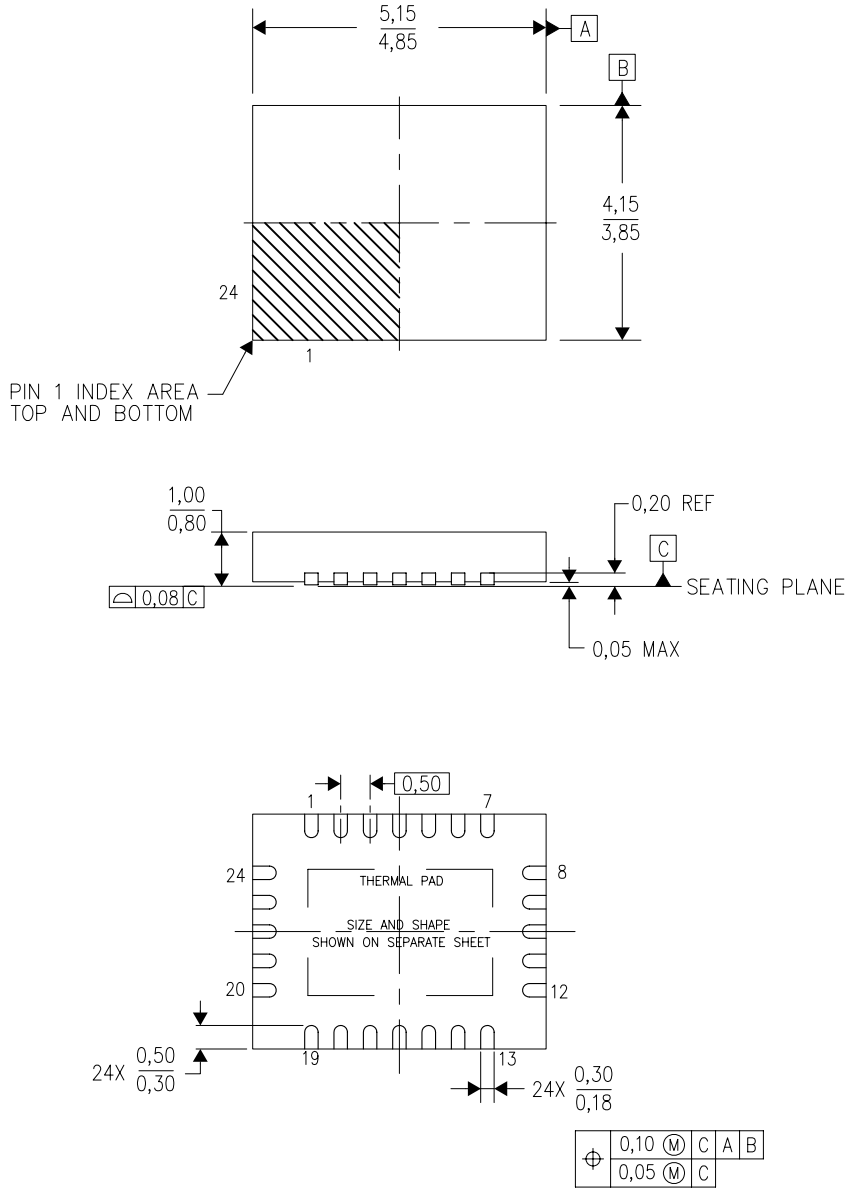
RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



4204845–2/H 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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