TPS65268-Q1 4-V to 8-V, 3-A, 2-A, 2-A Triple Synchronous Step-Down Converter

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Operating Junction Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Operating Input Voltage Range 4- to 8-V Maximum Continuous Output Current 3 A, 2 A, 2 A
- Feedback Reference Voltage 0.6 V ±1%
- Adjustable Clock Frequency from 200 kHz to 2.3 MHz
- Forced Continuous Current Mode (FCCM)
- External Clock Synchronization
- Dedicated Enable and Soft-Start Pins for Each Buck
- Output Voltage Power Good Indicator
- Thermal Overloading Protection

2 Applications

- Automotive
- Car Audio and Video
- Home Gateway and Access Point Networks
- Surveillance

3 Description

The TPS65268-Q1 device incorporates triple-synchronous buck converters with 4- to 8-V wide input voltage. The converter with constant frequency peak current mode is designed to simplify its application while giving designers options to optimize the system according to targeted applications. The switching frequency of the converters is adjustable from 200 kHz to 2.3 MHz with an external resistor. Operation that is 180° out-of-phase between BUCK1 and BUCK2, and BUCK3 (BUCK2 and BUCK3 run in phase) minimizes the input filter requirements.

Each buck converter in the TPS65268-Q1 device operates in forced continuous-current mode (FCCM) at light load condition for reduced output voltage ripple and improved load transient response.

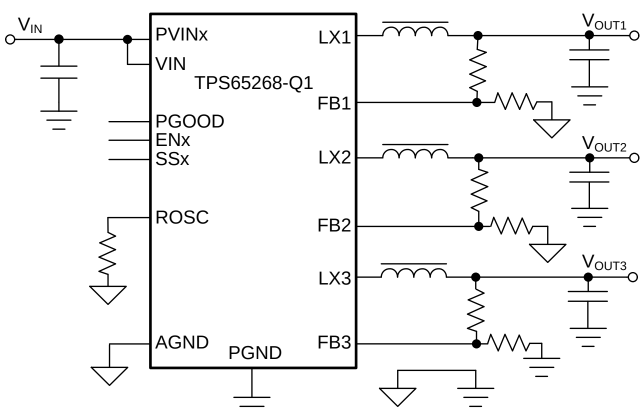
The TPS65268-Q1 device features overvoltage, overcurrent, short-circuit, and overtemperature protection.

Device Information(1)

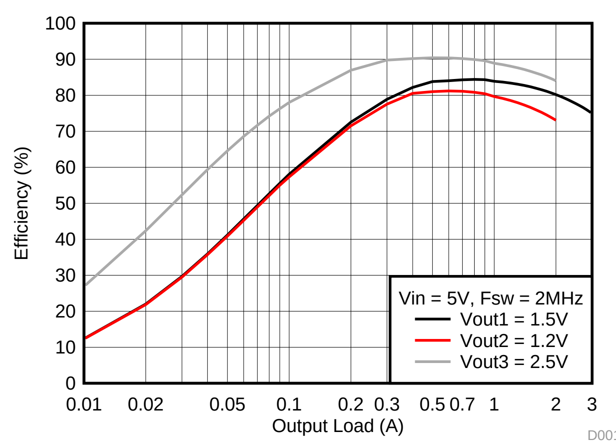
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65268-Q1	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Schematic



Efficiency vs Output Load



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4 Revision History

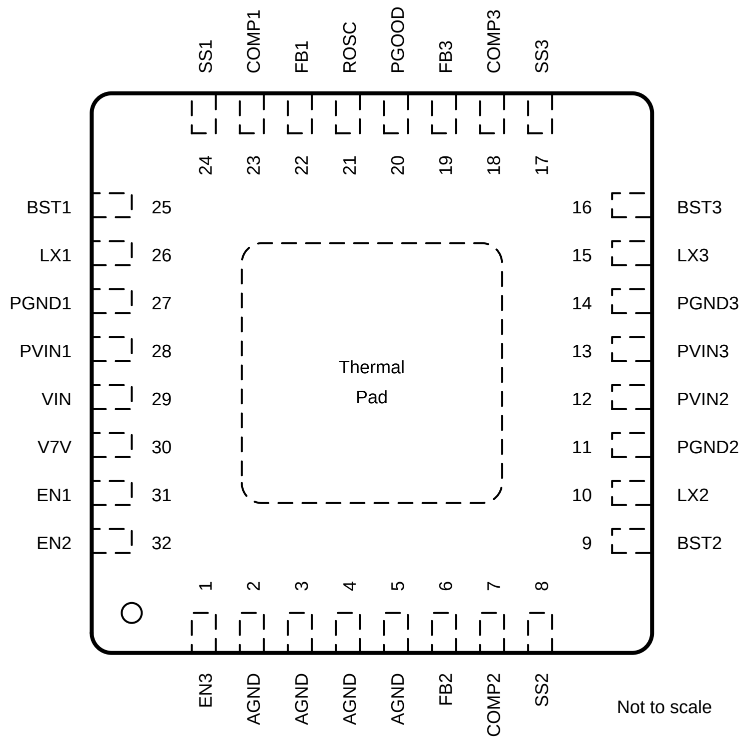
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2018) to Revision A — **Page**

- Changed the maximum value for the BUCK2/BUCK3 peak inductor current limit parameter from 3.9 A to 4 A in the *Electrical Characteristics* table 6
- Changed the unit for soft start current from mA to µA in the *SS Pin Charge Current vs Temperature* graph 9

5 Pin Configuration and Functions

RHB Package
32-Pin VQFN With Exposed Thermal Pad
Top View



No electric signal is down bonded to thermal pad inside the device. Exposed thermal pad must be soldered to PCB for optimal thermal performance.

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	EN3	I	Enable for BUCK3. Float to enable. Use this pin to adjust the UVLO input voltage of BUCK3 with a resistor divider.
2	AGND	G	Analog ground common to buck controllers and other analog circuits. This pin must be routed separately from high-current power grounds to the negative pin of bypass capacitor of input voltage (V_{IN}).
3			
4			
5			
6	FB2	I	Feedback Kelvin sensing pin for BUCK2 output voltage. Connect this pin to the BUCK2 resistor divider.
7	COMP2	O	Error amplifier output and loop compensation pin for BUCK2. Connect a series resistor and capacitor to compensate the control loop of BUCK2 with peak-current PWM mode.
8	SS2	O	Soft-start and tracking input for BUCK2. An internal 5.2-µA pullup current source is connected to this pin. The soft-start time can be programmed by connecting a capacitor between this pin and ground.
9	BST2	O	Boot-strapped supply to the high-side floating gate driver in BUCK2. Connect a capacitor (recommended value of 47 nF) from the BST2 pin to LX2 pin.
10	LX2	O	Switching node connection to the inductor and bootstrap capacitor for BUCK2. The voltage swing at this pin is from a diode voltage below the ground up to the PVIN2 voltage.
11	PGND2	G	Power ground connection of BUCK2. Connect the PGND2 pin as close as possible to the negative pin of VIN2 input ceramic capacitor.
12	PVIN2	P	Input power supply for BUCK2. Connect the PVIN2 pin as close as possible to the positive pin of an input ceramic capacitor (recommended value of 10 µF).

(1) I = Input, O = Output, P = Supply, G = Ground

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
13	PVIN3	P	Input power supply for BUCK3. Connect the PVIN3 pin as close as possible to the positive pin of an input ceramic capacitor (recommended value of 10 µF).
14	PGND3	G	Power ground connection of BUCK3. Connect the PGND3 pin as close as possible to the negative pin of the VIN3 input ceramic capacitor.
15	LX3	O	Switching node connection to the inductor and bootstrap capacitor for BUCK3. The voltage swing at this pin is from a diode voltage below the ground up to the PVIN3 voltage.
16	BST3	O	Boot-strapped supply to the high-side floating gate driver in BUCK3. Connect a capacitor (recommended value of 47 nF) from the BST3 pin to LX3 pin.
17	SS3	O	Soft-start and tracking input for BUCK3. An internal 5.2-µA pullup current source is connected to this pin. The soft-start time can be programmed by connecting a capacitor between this pin and ground.
18	COMP3	O	Error amplifier output and loop compensation pin for BUCK3. Connect a series resistor and capacitor to compensate the control loop of BUCK3 with peak-current PWM mode.
19	FB3	I	Feedback Kelvin sensing pin for BUCK3 output voltage. Connect this pin to the BUCK3 resistor divider.
20	PGOOD	O	Output voltage supervision pin. When all buck converters are in the regulation range of the PGOOD monitor, the PGOOD pin is asserted high.
21	ROSC	O	Clock frequency adjustment pin. Connect a resistor from this pin to ground to adjust the clock frequency. When connected to an external clock, the internal oscillator synchronizes to the external clock.
22	FB1	I	Feedback Kelvin sensing pin for BUCK1 output voltage. Connect this pin to the BUCK1 resistor divider.
23	COMP1	O	Error amplifier output and loop compensation pin for BUCK1. Connect a series resistor and capacitor to compensate the control loop of BUCK1 with peak current PWM mode.
24	SS1	O	Soft-start and tracking input for BUCK1. An internal 5.2-µA pullup current source is connected to this pin. The soft-start time can be programmed by connecting a capacitor between this pin and ground.
25	BST1	O	Boot-strapped supply to the high-side floating gate driver in BUCK1. Connect a capacitor (recommended value of 47 nF) from the BST1 pin to LX1 pin.
26	LX1	O	Switching node connection to the inductor and bootstrap capacitor for BUCK1. The voltage swing at this pin is from a diode voltage below the ground up to the PVIN1 voltage.
27	PGND1	G	Power ground connection of BUCK1. Connect the PGND1 pin as close as possible to the negative pin of PVIN1 input ceramic capacitor.
28	PVIN1	P	Input power supply for BUCK1. Connect the PVIN1 pin as close as possible to the positive pin of an input ceramic capacitor (suggest 10 µF).
29	VIN	P	Buck controller power supply
30	V7V	O	Internal LDO regulator for gate driver and internal controller. Connect a 1-µF capacitor from the pin to power ground.
31	EN1	I	Enable for BUCK1. Float to enable. Use this pin to adjust the UVLO input voltage of BUCK1 with a resistor divider.
32	EN2	I	Enable for BUCK2. Float to enable. Use this pin to adjust the UVLO input voltage of BUCK2 with a resistor divider.
—	PAD	—	No electric signal is down bonded to thermal pad inside the device. Exposed thermal pad must be soldered to PCB for optimal thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)[1]

	MIN	MAX	UNIT
PVIN1, PVIN2, PVIN3,VIN	–0.3	12	V
LX1, LX2, LX3 (Maximum withstand voltage transient < 20 ns)	–1	15	V
BST1, BST2, BST3 referenced to LX1, LX2, LX3 pins respectively	–0.3	7	V
EN1, EN2, EN3, V7V, PGOOD	–0.3	7	V
FB1, FB2, FB3, COMP1 , COMP2, COMP3, ROSC, SS1, SS2, SS3	–0.3	3.6	V
AGND, PGND1, PGND2, PGND3	–0.3	0.3	V
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 8, 9, 16, 17, 24, 25, and 32)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
PVIN1, PVIN2, PVIN3,VIN	4	8	V
LX1, LX2, LX3 (Maximum withstand voltage transient <20 ns)	–0.8	10	V
BST1, BST2, BST3 referenced to LX1, LX2, LX3 pins respectively	–0.1	6.8	V
EN1, EN2, EN3, V7V, PGOOD	–0.1	6.3	V
FB1, FB2, FB3, COMP1 , COMP2, COMP3, ROSC, SS1, SS2, SS3	–0.1	3	V
Operating junction temperature, T_J	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS65268-Q1	UNIT
		RHB (VQFN)	
		32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{IN} = 5 V, f_{SW} = 2 MHz, –40°C ≥ T_J ≥ 125°C, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
V_{IN}	Input voltage range		4		8	V
UVLO	VIN UVLO	VIN rising	3.5	3.8	4	V
		VIN falling	3.1	3.3	3.5	V
$UVLO_{hys}$	VIN UVLO hysteresis			500		mV
IDD_{SDN}	Shutdown supply current	$V_{EN1} = V_{EN2} = V_{EN3}$ = 0 V	2.5	6	15	µA
IDD_{Q_NSW}	Input quiescent current without BUCK1, BUCK2, BUCK3 switching	$V_{EN1} = V_{EN2} = V_{EN3}$ = 3 V, $V_{FB1} = V_{FB2} = V_{FB3}$ = 0.8 V	550	780	1150	µA
IDD_{Q_NSW1}		V_{EN1} = 3 V, $V_{EN2} = V_{EN3}$ = 0 V, V_{FB1} = 0.8 V	180	370	590	
IDD_{Q_NSW2}		V_{EN2} = 3 V, $V_{EN1} = V_{EN3}$ = 0 V, V_{FB2} = 0.8 V	180	370	590	
IDD_{Q_NSW3}		V_{EN3} = 3 V, $V_{EN1} = V_{EN2}$ = 0 V, V_{FB3} = 0.8 V	180	370	590	
V_{V7V}	V7V LDO output voltage	V_{IN} = 5 V, V_{V7V} load current = 0 A		4.96		V
		V_{IN} = 8 V, V_{V7V} load current = 0 A		6.3		V
I_{OCP_V7V}	V7V LDO current limit		78	185	260	mA
FEEDBACK VOLTAGE REFERENCE						
V_{FB}	Feedback voltage	V_{COMP} = 1.2 V	0.594	0.6	0.606	V
BUCK1, BUCK2, BUCK3						
V_{ENxH}	EN1, EN2, EN3 high-level input voltage		1.12	1.2	1.26	V
V_{ENxL}	EN1, EN2, EN3 low-level input voltage		1.05	1.15	1.21	V
I_{ENx1}	EN1, EN2, EN3 pullup current	V_{ENx} = 1 V	2.5	3.9	5.9	µA
I_{ENx2}		V_{ENx} = 1.5 V	5.1	6.9	9.2	
I_{ENhys}	Hysteresis current		2.6	3	3.3	µA
I_{SSX}	Soft-start charging current		3.9	5.2	6.5	µA
t_{ON_MIN}	Minimum on-time		50	75	110	ns
G_{m_EA}	Error amplifier transconductance	–2 µA < I_{COMPx} < 2 µA	140	300	450	µs
$G_{m\_PS1/2/3}$	COMP1/2/3 voltage to inductor current G_m (1)	I_{LX} = 0.5 A		7.4		A/V
I_{LIMIT1}	BUCK1 peak inductor current limit		4.8	5.9	7	A
$I_{LIMITSINK1}$	BUCK1 low-side sink current limit		0.7	1.3	1.8	A
$I_{LIMIT2/3}$	BUCK2/BUCK3 peak inductor current limit		2.55	3.3	4	A
$I_{LIMITSINK2/3}$	BUCK2/BUCK3 low-side sink current limit		0.5	1	1.4	A
Rdson_HS1	BUCK1 high-side switch resistance	V_{IN} = 5 V		110		mΩ
Rdson_LS1	BUCK1 low-side switch resistance	V_{IN} = 5 V		67		mΩ
Rdson_HS2	BUCK2 high-side switch resistance	V_{IN} = 5 V		149		mΩ
Rdson_LS2	BUCK2 low-side switch resistance	V_{IN} = 5 V		94		mΩ
Rdson_HS3	BUCK3 high-side switch resistance	V_{IN} = 5 V		149		mΩ
Rdson_LS3	BUCK3 low-side switch resistance	V_{IN} = 5 V		94		mΩ
POWER GOOD						
V_{th_PG}	Feedback voltage threshold	FBx undervoltage falling		92.5		$\%V_{ref}$
		FBx undervoltage rising		95		
		FBx overvoltage rising		107.5		
		FBx overvoltage falling		105		
$t_{DEGLITCH(PG)\_F}$	PGOOD falling edge deglitch time			112		cycles
$t_{RDEGLITCH(PG)\_R}$	PGOOD rising edge deglitch time			616		cycles
I_{PG}	PGOOD pin leakage				0.1	µA
V_{LOW_PG}	PGOOD pin low voltage	I_{SINK} = 1 mA			0.4	V
OSCILLATOR						
f_{SW}	Switching frequency	R_{OSC} = 88.7 kΩ	430	500	560	kHz
f_{SW_range}	Switching frequency		200		2300	kHz
f_{SYNC_w}	Clock sync minimum pulse width		80			ns

(1) Lab validation result

Electrical Characteristics (continued)

V_{IN} = 5 V, f_{SW} = 2 MHz, –40°C ≥ T_J ≥ 125°C, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYNC_HI}	Clock sync high threshold				2	V
f_{SYNC_LO}	Clock sync low threshold		0.4			V
f_{SYNC}	Clock sync frequency range		200		2300	kHz
THERMAL PROTECTION						
T_{TRIP_OTP}	Thermal protection trip point[1]	Temperature rising		160		°C
T_{HYST_OTP}	Thermal protection trip point hysteresis[1]			20		°C

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
HICCUP TIMING					
t_{Hiccup_wait}	Overcurrent wait time[1]		256		cycles
t_{Hiccup_re}	Hiccup time before restart[1]		8192		cycles

(1) Lab validation result

6.7 Typical Characteristics

T_A = 25°C, V_{IN} = 5 V, V_{OUT1} = 1.5 V, V_{OUT2} = 1.2 V, V_{OUT3} = 2.5 V, f_{SW} = 2 MHz (unless otherwise noted)

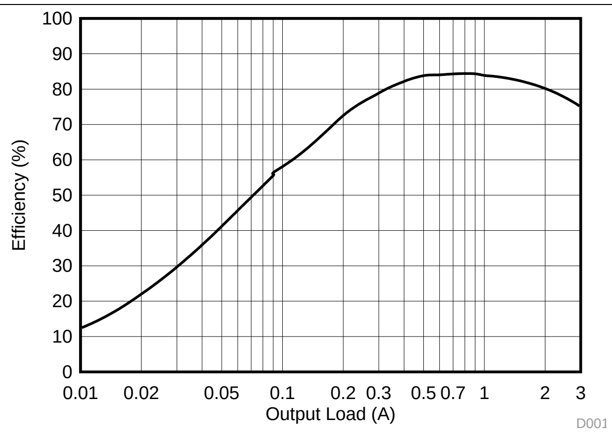


Figure 1. BUCK1 Efficiency

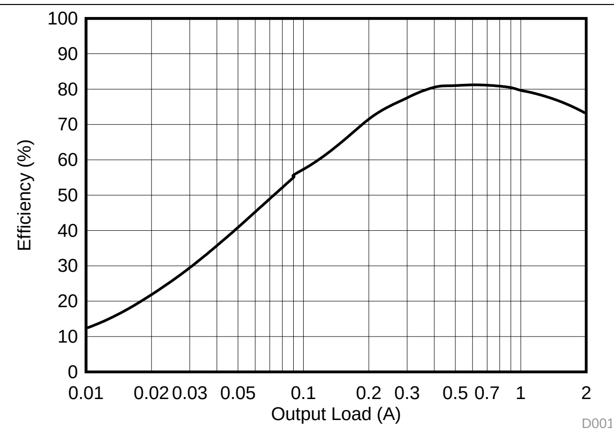


Figure 2. BUCK2 Efficiency

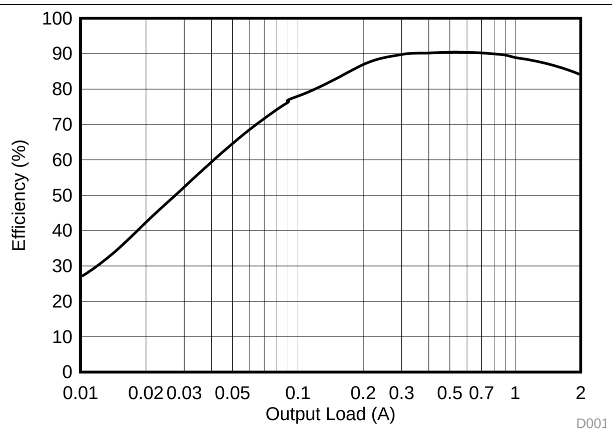


Figure 3. BUCK3 Efficiency

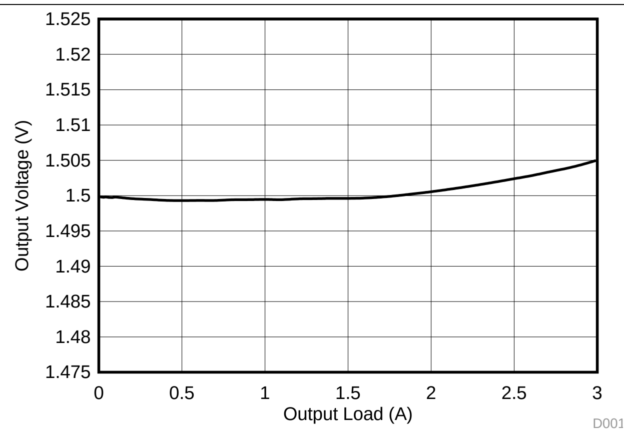


Figure 4. BUCK1, Load Regulation

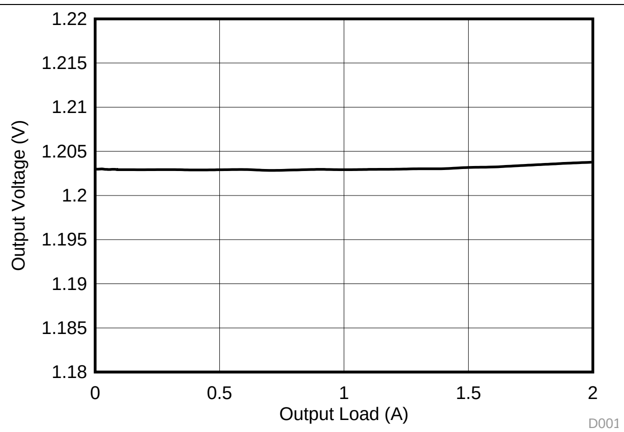


Figure 5. BUCK2, Load Regulation

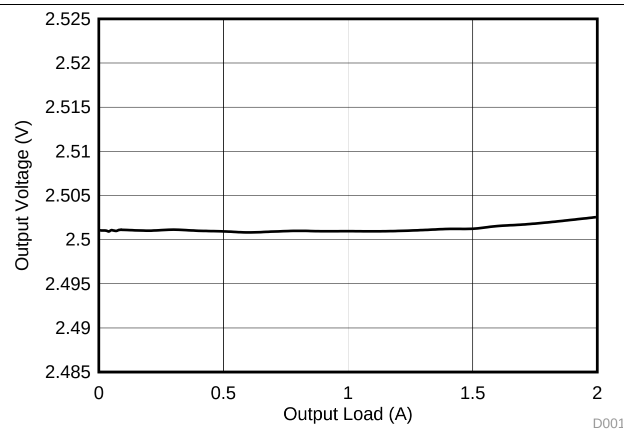


Figure 6. BUCK3, Load Regulation

Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 5 V, V_{OUT1} = 1.5 V, V_{OUT2} = 1.2 V, V_{OUT3} = 2.5 V, f_{SW} = 2 MHz (unless otherwise noted)

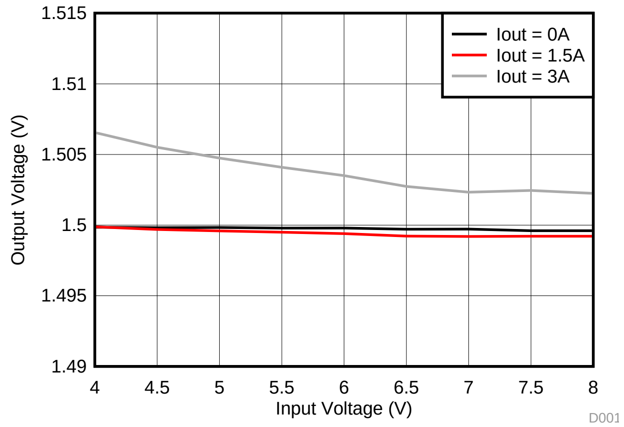


Figure 7. BUCK1, Line Regulation

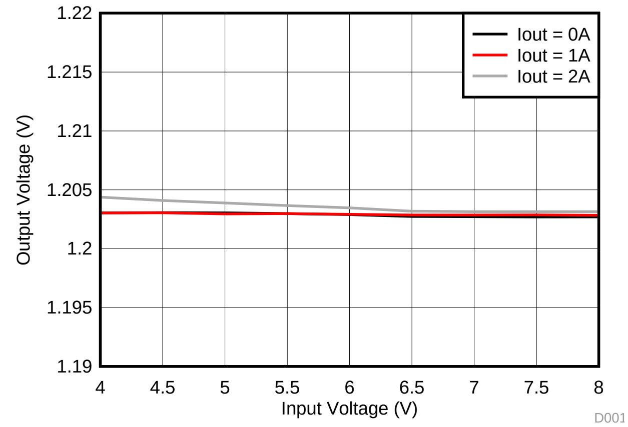


Figure 8. BUCK2, Line Regulation

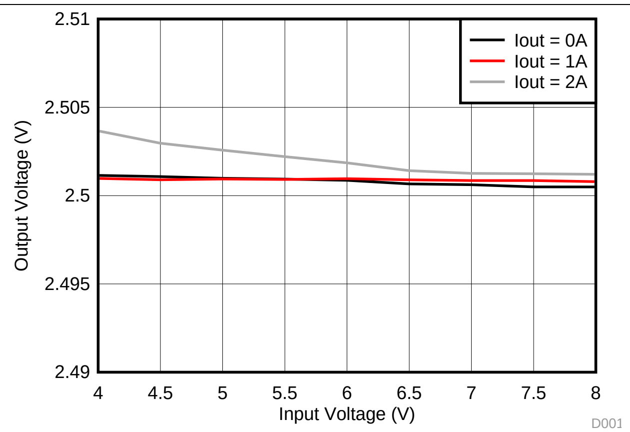


Figure 9. BUCK3, Line Regulation

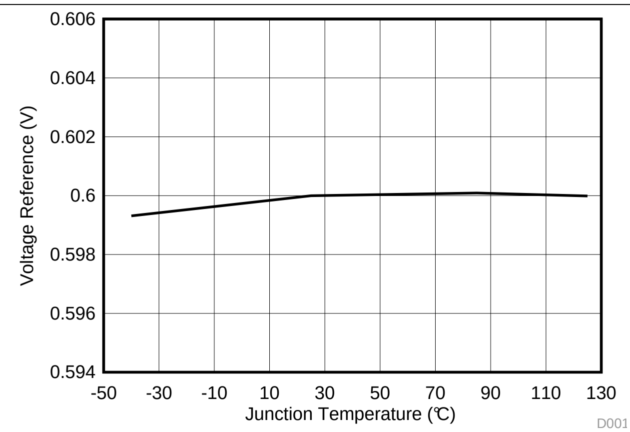
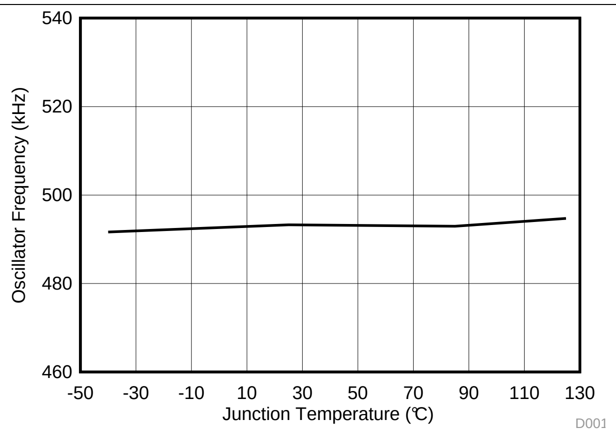
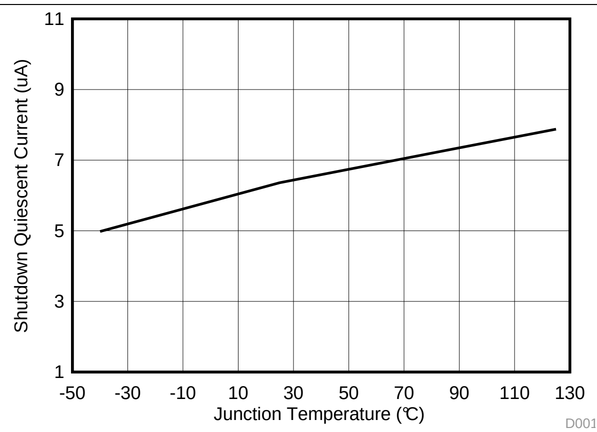


Figure 10. Voltage Reference vs Temperature



ROSC = 88.7 kΩ

Figure 11. Oscillator Frequency vs Temperature

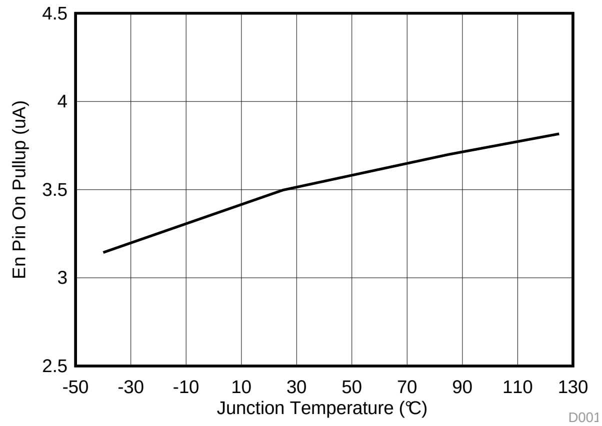


V_{IN} = 5 V

Figure 12. Shutdown Quiescent Current vs Temperature

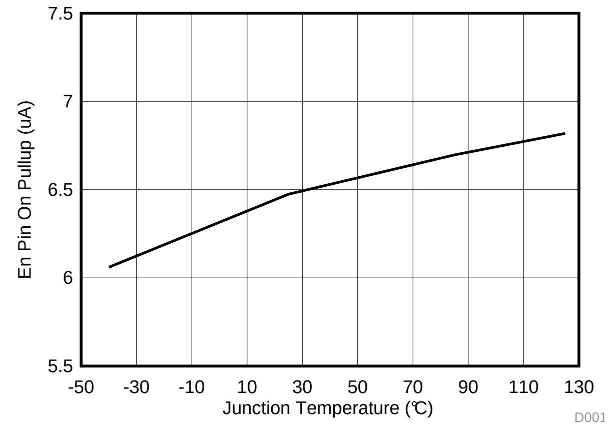
Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 5 V, V_{OUT1} = 1.5 V, V_{OUT2} = 1.2 V, V_{OUT3} = 2.5 V, f_{SW} = 2 MHz (unless otherwise noted)



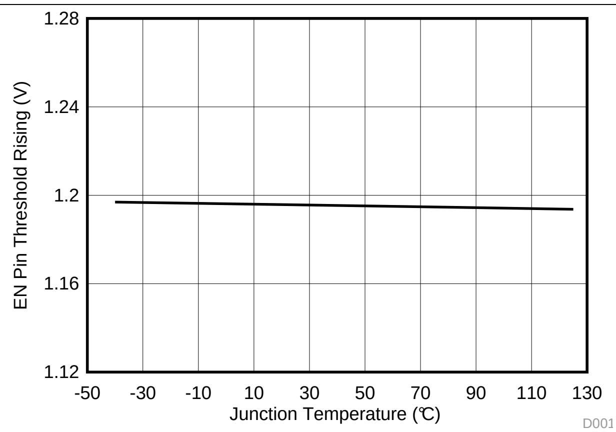
V_{EN} = 1 V V_{IN} = 5 V

Figure 13. EN Pin Pullup Current vs Temperature



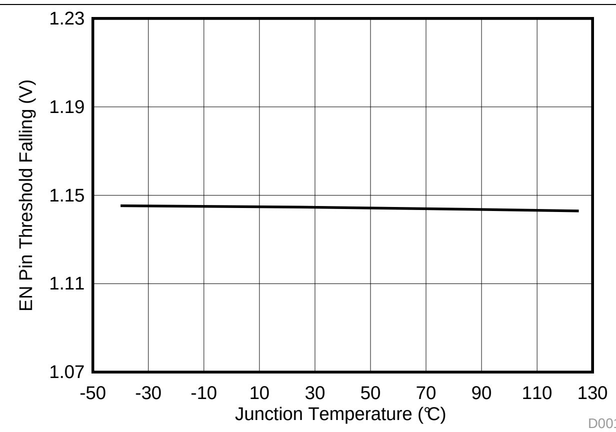
V_{EN} = 1.5 V V_{IN} = 5 V

Figure 14. EN Pin Pullup Current vs Temperature



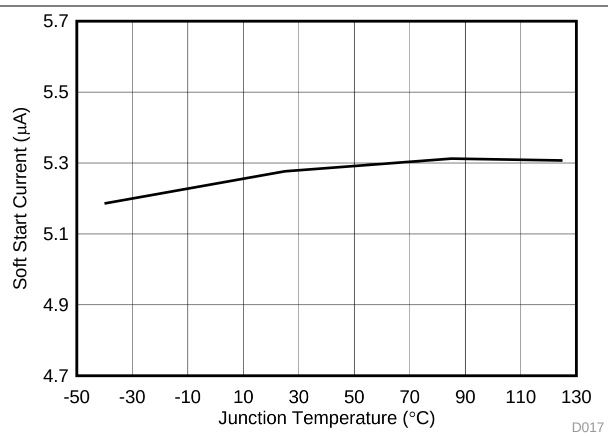
V_{IN} = 5 V

Figure 15. EN Pin Threshold Rising vs Temperature



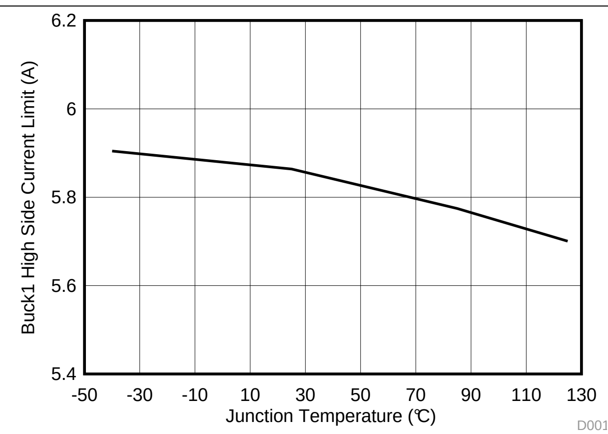
V_{IN} = 5 V

Figure 16. EN Pin Threshold Falling vs Temperature



V_{IN} = 5 V

Figure 17. SS Pin Charge Current vs Temperature

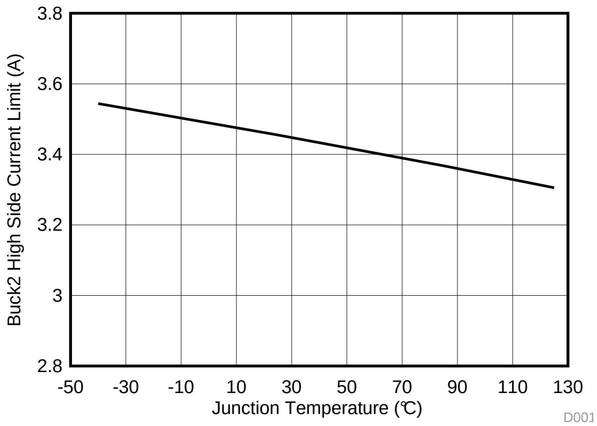


V_{IN} = 5 V

Figure 18. Buck1 High-Side Current Limit vs Temperature

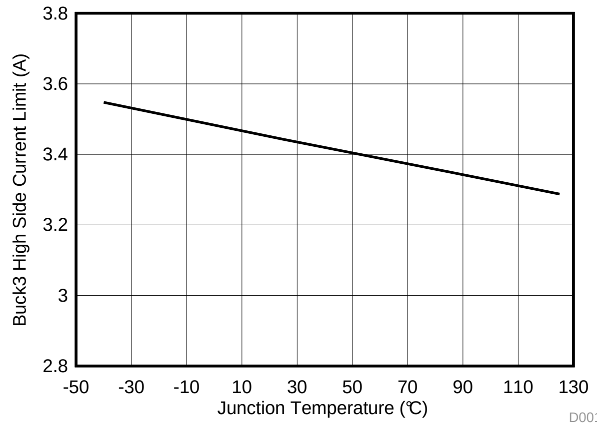
Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 5 V, V_{OUT1} = 1.5 V, V_{OUT2} = 1.2 V, V_{OUT3} = 2.5 V, f_{SW} = 2 MHz (unless otherwise noted)



V_{IN} = 5 V

Figure 19. Buck2 High-Side Current Limit vs Temperature



V_{IN} = 5 V

Figure 20. Buck3 High-Side Current Limit vs Temperature

7 Detailed Description

7.1 Overview

The TPS65268-Q1 device is a monolithic triple synchronous step-down (buck) converter with 3-A, 2-A, 2-A output currents. The feedback voltage reference for each buck converter is 0.6 V. Each buck converter is independent with dedicated enable, soft-start, and loop compensation pins.

In the light load condition, the converter operates at continuous current mode (CCM) with a fixed frequency for optimized output ripple.

The TPS65268-Q1 device implements a constant-frequency, peak current-mode control that simplifies external loop compensation. The wide switching frequency of 200 kHz to 2.3 MHz allows for optimizing system efficiency, filtering size, and bandwidth. The switching frequency can be adjusted with an external resistor connecting between the ROSC pin and ground. The TPS65268-Q1 device also has an internal phase-locked loop (PLL) controlled by the ROSC pin that can be used to synchronize the switching cycle to the falling edge of an external system clock. The switching clock of BUCK1 is 180° out-of-phase operation from the clocks of BUCK2 and BUCK3 channels to reduce input current ripple, input capacitor size, and power-supply-induced noise.

The TPS65268-Q1 device is designed for safe monotonic startup into prebiased loads. The default startup is when the input voltage (V_{IN}) is typically 3.8 V. The ENx pin can also be used to adjust the undervoltage lockout (UVLO) of the input voltage with an external resistor divider. In addition, the ENx pin has an internal 3.9-µA current source, so the ENx pin can be left floating to automatically power up the converters.

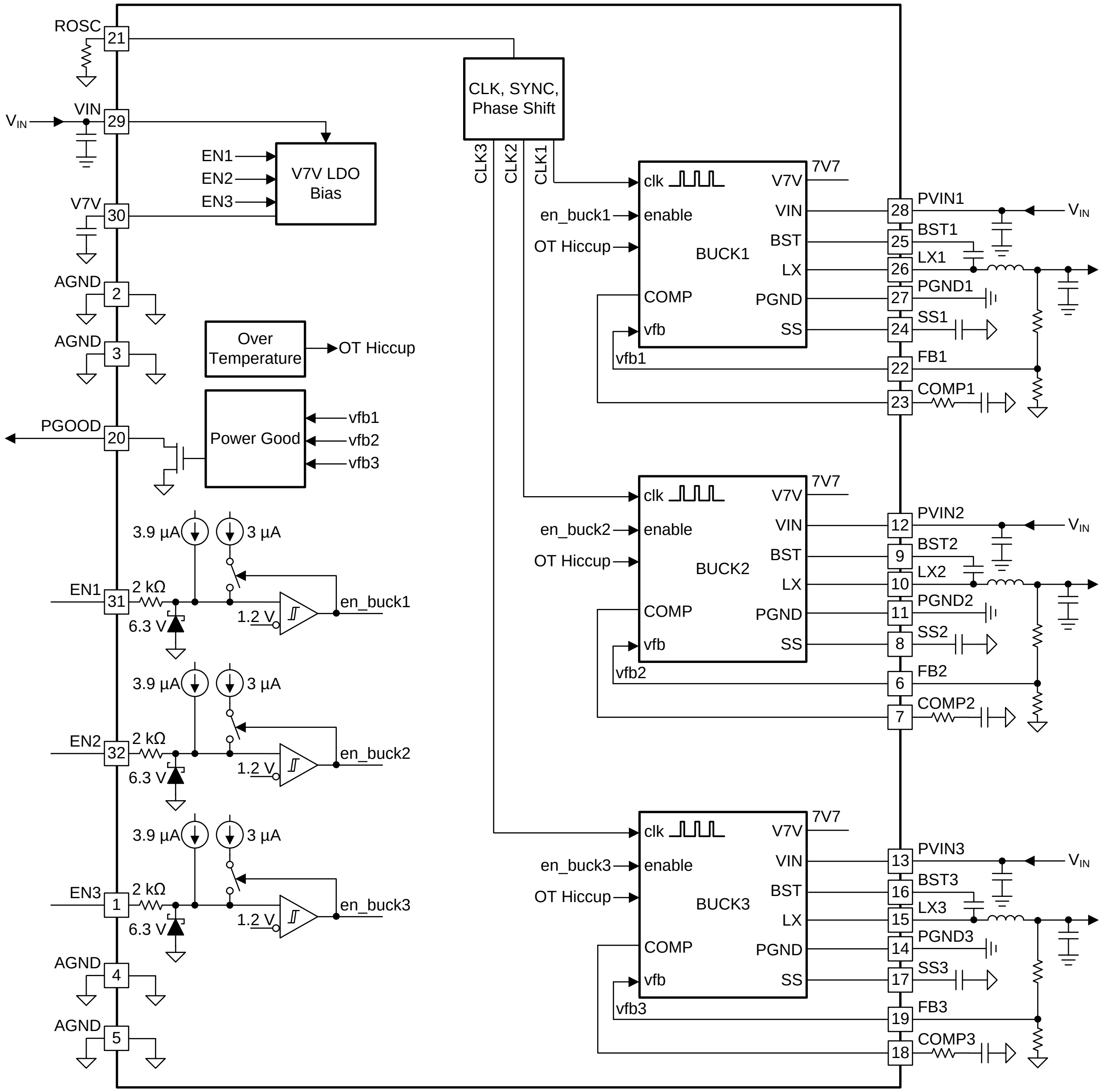
The TPS65268-Q1 device reduces the external component count by integrating the bootstrap circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BST and LXx pins. A UVLO circuit monitors the bootstrap capacitor voltage (V_{BST}-V_{LX}) in each buck converter. When the V_{BST}-V_{LX} voltage drops to the threshold, the LXx pin is pulled low to recharge the bootstrap capacitor. The TPS65268-Q1 device can operate at 100% duty cycle as long as the bootstrap capacitor voltage is higher than the BOOT-LX UVLO threshold, which is typically 2.1 V.

The TPS65268-Q1 device has power-good comparators with hysteresis, which monitor the output voltages through internal feedback voltages. The device also features the PGOOD pin to supervise output voltages of the buck converter. When all buck converters are in the regulation range and power sequence is complete, the PGOOD pin is asserted high.

The soft-start and tracking pin (SSx) is used to minimize inrush currents or provide power-supply sequencing during power up. A small value capacitor or resistor divider is connected to the pin for soft-start or voltage tracking.

The TPS65268-Q1 device is protected from overload and overtemperature fault conditions. The converter minimizes excessive output overvoltage transients by taking advantage of the power-good comparator. During an output overvoltage condition, the high-side MOSFET is turned off until the internal feedback voltage is lower than 105% of the 0.6-V reference voltage. The TPS65268-Q1 device implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections to avoid inductor current runaway. If the overcurrent (OC) condition has lasted for more than the OC wait time (256 clock cycle), the converter shuts down and restarts after the hiccup time (8192 clock cycles). The TPS65268-Q1 device shuts down if the junction temperature is higher than thermal shutdown trip point. When the junction temperature drops 20°C typically below the thermal shutdown trip point, the TPS65268-Q1 device is restarted under control of the soft-start circuit automatically.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adjusting the Output Voltage

The output voltage of each buck converter is set with a resistor divider from the output of the buck converter to the FB pin as shown in Figure 21. TI recommends using1% tolerance or better resistors. Use Equation 1 to calculate the value of R2.

Feature Description (continued)

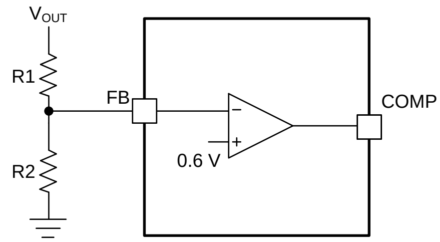


Figure 21. Voltage Divider Circuit

$$R2 = R1 \times \frac{0.6}{V_{OUT} - 0.6} \tag{1}$$

To improve efficiency at light loads, consider using larger value resistors. If the values are too high, the regulator is more sensitive to noise. Table 1 lists the recommended resistor values.

Table 1. Output Resistor Divider Selection

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)
1	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	31.6	10
3.3	45.3	10
3.3	22.6	4.99
5	73.2	10
5	36.5	4.99

7.3.2 Enable and Adjusting UVLO

The ENx pin provides electrical on and off control of the device. After the ENx pin voltage exceeds the threshold voltage, the device starts operation. If each ENx pin voltage is pulled below the threshold voltage, the regulator stops switching and enters a low quiescent-current (I_Q) state.

The ENx pin has an internal pullup current source, allowing the user to float the ENx pin to enable the device. If an application requires controlling the ENx pin, use open-drain or open-collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal UVLO threshold of the input voltage. The internal UVLO threshold of the input voltage has a hysteresis of 500 mV. If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVINx in split-rail applications, then the user can configure the ENx pin as shown in Figure 22, Figure 23, and Figure 24. When using the external UVLO function, TI recommends setting the hysteresis higher than 500 mV.

The ENx pin has a small pullup current, I_p, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h after the ENx pin crosses the enable threshold. Use Equation 2 and Equation 3 to calculate the UVLO thresholds.

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \tag{2}$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1\left(I_h + I_p\right)}$$

where

- I_h = 3 µA
- I_p = 3.9 µA
- $V_{ENRISING}$ = 1.2 V
- $V_{ENFALLING}$ = 1.15 V (3)

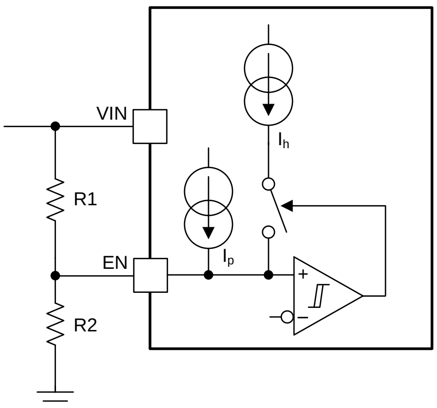


Figure 22. Adjustable V_{IN} UVLO

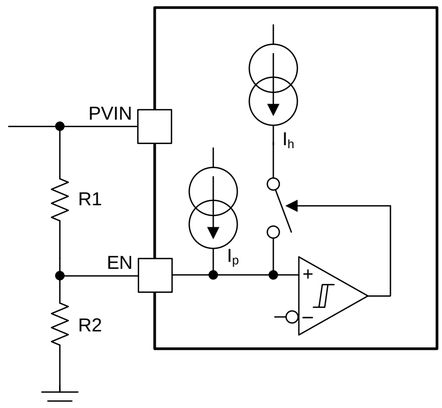


Figure 23. Adjustable PVIN UVLO, V_{IN} > 4 V

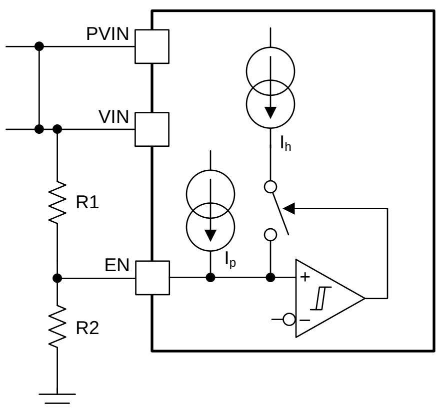


Figure 24. Adjustable V_{IN} and PVIN UVLO

7.3.3 Soft-Start Time

The voltage on the respective SSx pin controls the startup of buck output. When the voltage on the SSx pin is less than the internal 0.6-V reference, the TPS65268-Q1 device regulates the internal feedback voltage to the voltage on the SSx pin instead of 0.6 V. The SSx pin can be used to program an external soft-start function or to allow the output of buck converter to track another supply during start-up. The device has an internal pullup current source of 5.2 µA (typical) that charges an external soft-start capacitor to provide a linear ramping voltage at the SSx pin. The TPS65268-Q1 device regulates the internal feedback voltage to the voltage on the SSx pin, allowing the output voltage to rise smoothly from 0 V to the regulated voltage of the pin without inrush current. Use Equation 4 to calculate the approximate soft-start time.

$$t_{SS}\ (ms) = \frac{C_{SS}\ (nF) \times V_{ref}\ (V)}{I_{SS}\ (\mu A)}$$

where

- t_{SS} is the soft-start time

- C_{SS} is the soft-start capacitance
- I_{SS} is the soft-start current
- V_{ref} is the reference voltage (4)

Many of the common power-supply sequencing methods can be implemented using the SSx and ENx pins. Figure 25 shows the method implementing ratiometric sequencing by connecting the SSx pins of the three buck channels. The regulator outputs ramp up and reach regulation at the same time. When calculating the soft-start time, the pullup current source must be tripled in Equation 4.

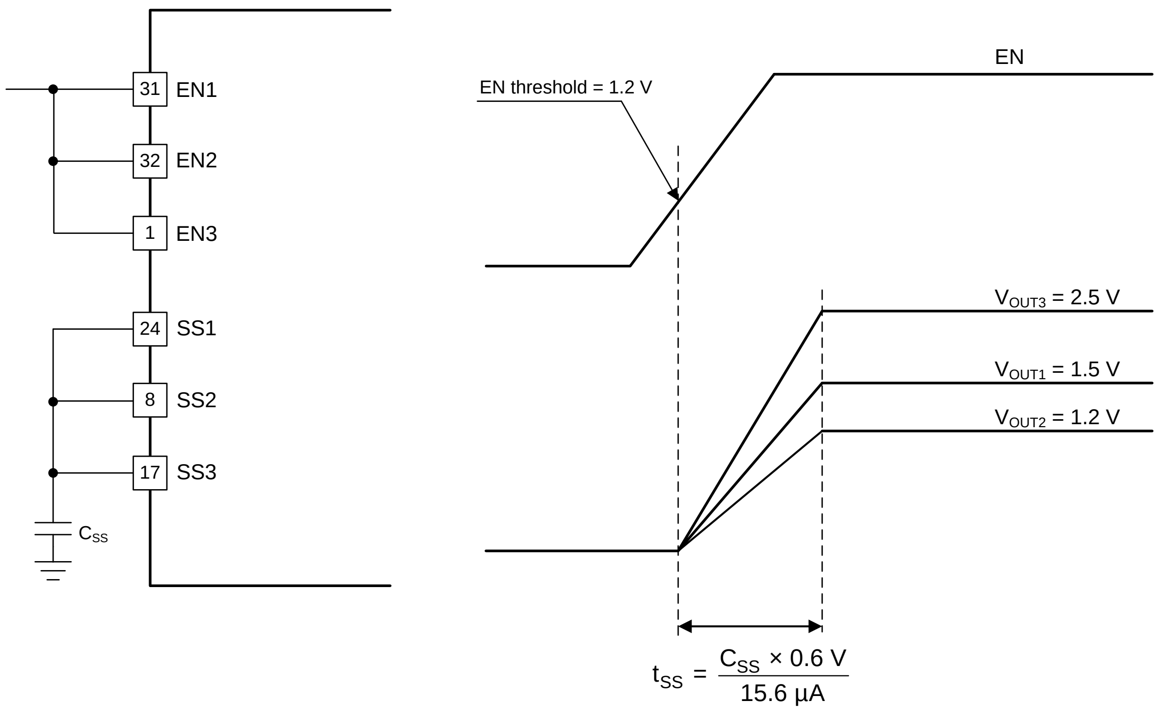
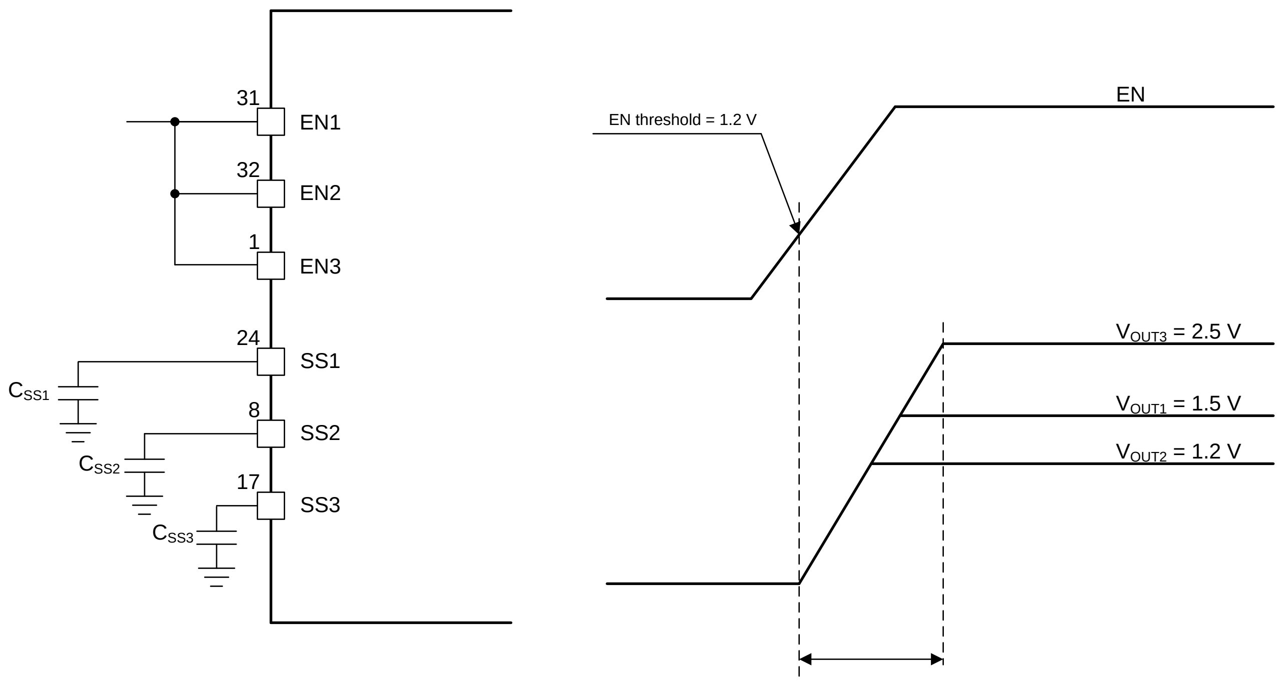


Figure 25. Ratiometric Power-Up Using SSx Pins

The user can implement simultaneous power-supply sequencing by connecting the capacitor to the SSx pin, shown in Figure 26. Use Equation 4 and Equation 5 to calculate the value of the capacitors.

$$\frac{C_{SS1}}{V_{OUT1}} = \frac{C_{SS2}}{V_{OUT2}} = \frac{C_{SS3}}{V_{OUT3}} \quad (5)$$



$$t_{SS} = \frac{C_{SS}\ 3 \times 0.6\ \text{V}}{5.2\ \mu\text{A}}$$

Figure 26. Simultaneous Startup Sequence Using SSx Pins

7.3.4 Power-Up Sequencing

The TPS65268-Q1 device has a dedicated enable pin and soft-start pin for each converter. The converter enable pins are biased by a current source that allows for easy sequencing by the addition of an external capacitor. Disabling the converter with an active pulldown transistor on the ENx pin allows for predictable power-down timing operation. Figure 27 shows the timing diagram of a typical buck power-up sequence with connecting a capacitor at the ENx pin.

A typical 1.4-µA current is charging the ENx pin from the input supply. When the ENx pin voltage rises to typical 0.4 V, the internal V7V LDO regulator turns on. A 3.9-µA pullup current sources the ENx pin. After the ENx pin voltage reaches the ENx enabling threshold, a 3-µA hysteresis current sources to the pin to improve noise sensitivity. The internal soft-start comparator compares the SSx pin voltage to 1.2 V. When the SSx pin voltage ramps up to 1.2 V, PGOOD monitor is enabled. After PGOOD deglitch time, PGOOD is deasserted. The SSx pin voltage is eventually clamped around 2.1 V.

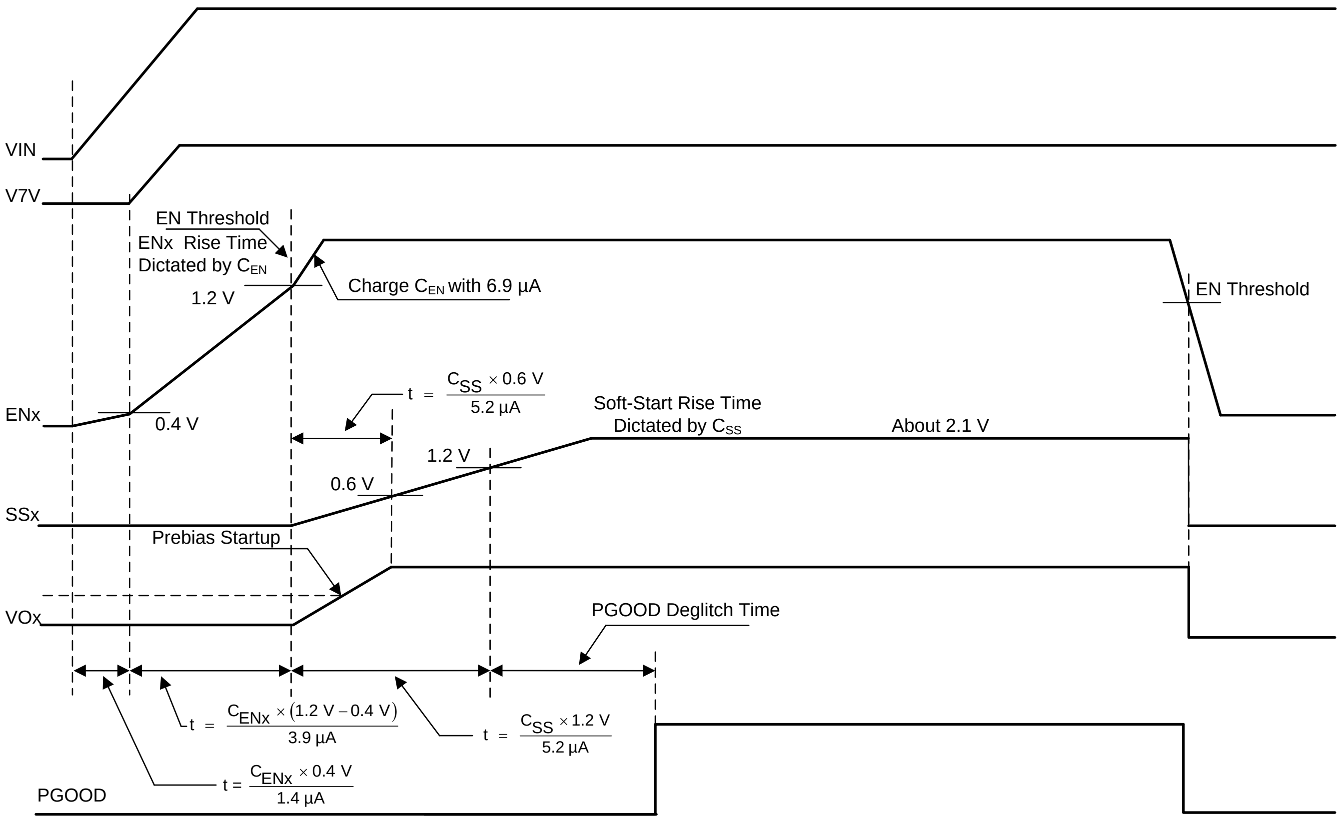


Figure 27. Startup Power Sequence

7.3.5 V7V Low-Dropout Regulator and Bootstrap

Power for the high-side and low-side MOSFET drivers and most other internal circuitry is derived from the V7V pin. The internal built-in low-dropout (LDO) linear regulator supplies 4.96 V (typical) from 5 V V_{IN} to the V7V voltage. The user should connect a 1-µF ceramic capacitor from the V7V pin to power ground.

If the input voltage decreases to the UVLO threshold voltage, the UVLO comparator detects the V7V pin voltage and forces the converter off.

Each high-side MOSFET driver is biased from the floating bootstrap capacitor, C_B, shown in Figure 28, which is normally recharged during each cycle through an internal low-side MOSFET or the body diode of a low-side MOSFET when the high-side MOSFET turns off. The boot capacitor is charged when the BST pin voltage is less than the input voltage and the BST-LX voltage is below regulation. TI recommends using a 47-nF ceramic capacitor. TI recommends using a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage. Each low-side MOSFET driver is powered from the V7V pin directly.

To improve dropout, the device is designed to operate at 100% duty cycle as long as the BST to LXx pin voltage is greater than the BST-LX UVLO threshold, which is typically 2.1 V. When the voltage between the BST and LXx pins drops below the BST-LX UVLO threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged.

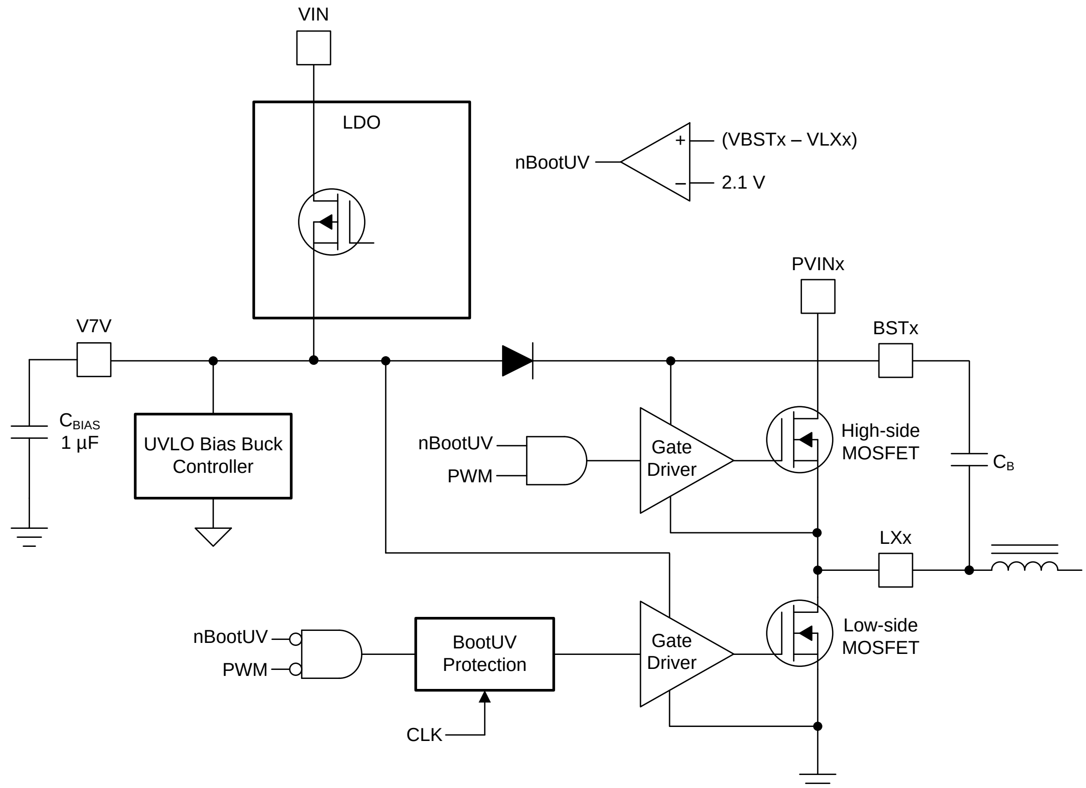


Figure 28. V7V Linear Dropout Regulator and Bootstrap Voltage Diagram

7.3.6 Out-of-Phase Operation

To reduce the input ripple current, the switch clock of BUCK1 is 180° out-of-phase from the clock of BUCK2 and BUCK3. This operation enables the system to have less input current ripple to reduce the size, cost, and EMI of the input capacitors.

7.3.7 Output Overvoltage Protection (OVP)

The device incorporates an OVP circuit to minimize output voltage overshoot. When the output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. After the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state voltage. In some applications with small output capacitance, the load can respond faster than the error amplifier which leads to the possibility of an output overshoot. Each buck converter compares the FB pin voltage to the OVP threshold. If the FB pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVP threshold, the high-side MOSFET turns on at the next clock cycle.

7.3.8 Slope Compensation

To prevent the subharmonic oscillations when the device operates at duty cycles greater than 50%, the TPS65268-Q1 devices adds built-in slope compensation, which is a compensating ramp to the switch current signal.

7.3.9 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and low-side MOSFET.

7.3.9.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control that uses the COMP pin voltage to control the turnoff of the high-side MOSFET and the turnon of the low-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the COMP pin voltage are compared and, when the peak switch current intersects the current reference, the high-side switch is turned off.

7.3.9.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on, its conduction current is monitored by the internal circuitry. During normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET can also sink current from the load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) has lasted for more than the hiccup wait time which is programmed for 256 switching cycles shown in Figure 29, the device shuts down and restarts after the hiccup time of 8192 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent condition.

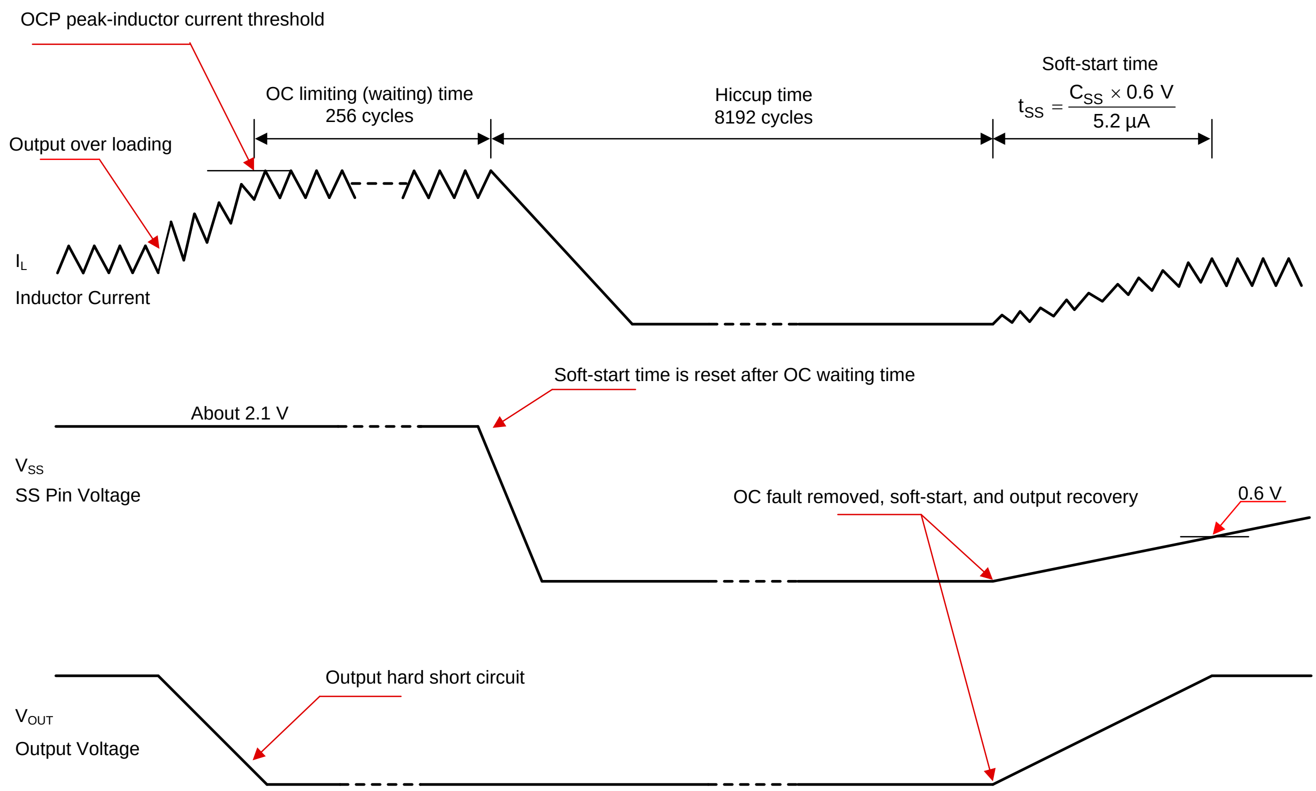


Figure 29. Overcurrent Protection

7.3.10 Power Good

The PGOOD pin is an open-drain output. When the feedback voltage of each buck converter is between 95% (rising) and 105% (falling) of the internal voltage reference, the PGOOD pin pulldown is deasserted and the pin floats. TI recommends using a pullup resistor with a value of 10 kΩ to 100 kΩ connected to a voltage source that is 5.5 V or less. The PGOOD pin is in a defined state when the VIN input voltage is greater than 1 V, but with reduced current sinking capability. The PGOOD pin achieves full current sinking capability after the VIN input voltage is above UVLO threshold, which is 3.8 V.

The PGOOD pin is pulled low when any feedback voltage of buck converter is lower than 92.5% (falling) or greater than 107.5% (rising) of the nominal internal reference voltage. Also, when the PGOOD pin is pulled low and during an UVLO condition on the input voltage, thermal shutdown is asserted, the ENx pin is pulled low, or the converter is in soft-start period.

7.3.10.1 Adjustable Switching Frequency

The ROSC pin can be used to set the switching frequency by connecting a resistor to ground. The switching frequency of the device is adjustable from 200 kHz to 2.3 MHz.

To determine the ROSC resistance for a given switching frequency, use Equation 6 or the curve in Figure 30. To reduce the solution size, the user should set the switching frequency as high as possible, but consider tradeoffs of the supply efficiency and minimum controllable on-time.

$$f_{OSC}\ (\text{kHz}) = 37254 \times R^{-0.966}\ (\text{k}\Omega) \tag{6}$$

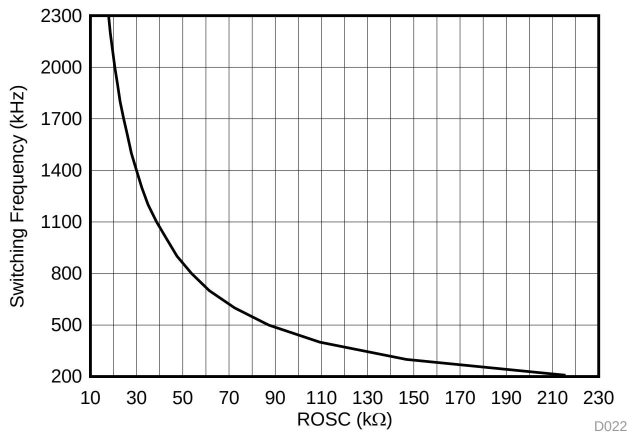


Figure 30. ROSC vs Switching Frequency

When an external clock applies to ROSC pin, the internal PLL has been implemented to allow internal clock synchronizing to an external clock from 200 kHz to 2300 kHz. To implement the clock synchronization feature, connect a square-wave clock signal to the ROSC pin with a duty cycle from 20% to 80%. The clock signal amplitude must transition lower than 0.4 V and higher than 2.0 V. The start of the switching cycle is synchronized to the falling edge of ROSC pin.

In applications where both resistor mode and synchronization mode are needed, the user can configure the device as shown in Figure 31. Before an external clock is present, the device works in resistor mode and the ROSC resistor sets the switching frequency. When an external clock is present, the synchronization mode overrides the resistor mode. The first time the ROSC pin is pulled above the ROSC high threshold (2 V), the device switches from the resistor mode to the synchronization mode and the ROSC pin is in the high impedance state as the PLL starts to lock onto the frequency of the external clock. TI does not recommend switching from the synchronization mode back to the resistor mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by ROSC resistor.

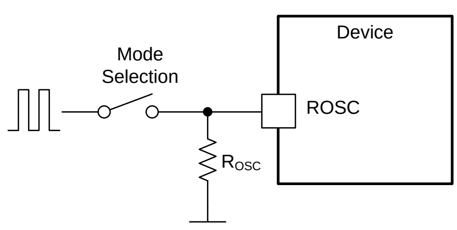


Figure 31. Works With Resistor Mode and Synchronization Mode

7.3.11 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C (typical). The device reinitiates the power-up sequence when the junction temperature drops below 140°C (typical).

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the ENx voltage is above the enable threshold, the TPS65268-Q1 device operates at continuous current mode (CCM) with a fixed frequency for optimized output ripple.

7.4.2 Standby Operation

When the TPS65268-Q1 device operates in normal CCM, the device can be placed in standby by pulling the ENx pin low.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is a triple-synchronous step-down DC-DC converter. The device is typically used to convert a higher DC voltage to lower DC voltages with continuous available output current of 3 A, 2 A, 2 A.

8.2 Typical Application

The following design procedure can be used to select component values for the TPS65268-Q1. This section presents a simplified discussion of the design process.

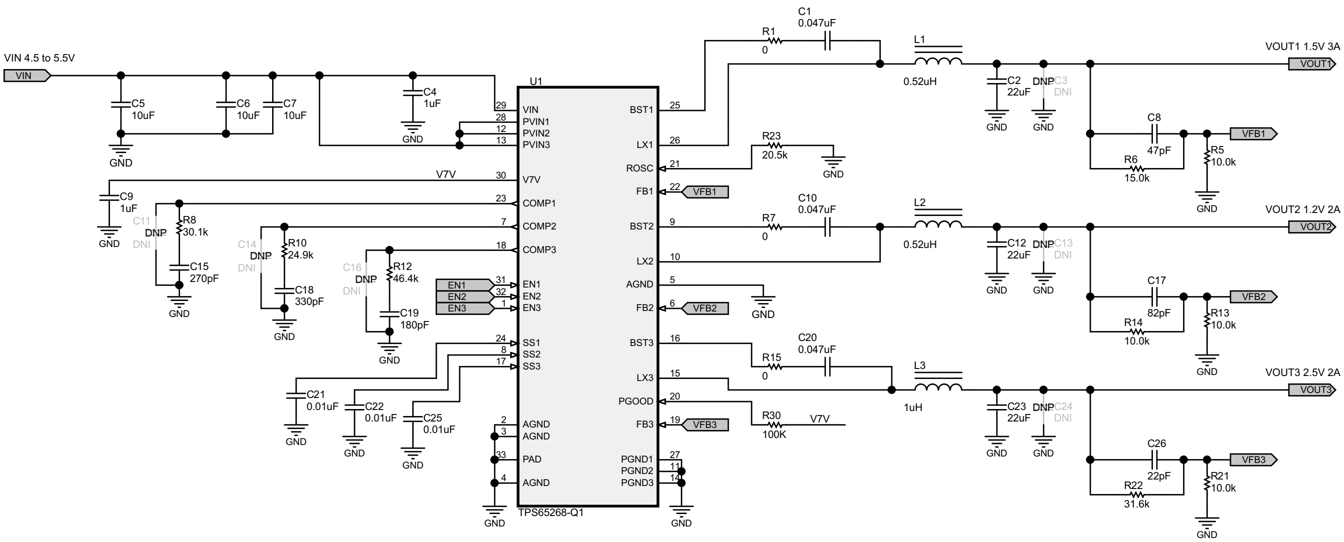


Figure 32. Typical Application Schematic

8.2.1 Design Requirements

This example details the design of triple-synchronous step-down converter. A few parameters must be known to start the design process. These parameters are typically determined at the system level. For this example, start with the known parameters listed in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
V_{OUT1}	1.5 V
I_{OUT1}	3 A
V_{OUT2}	1.2 V
I_{OUT2}	2 A
V_{OUT3}	2.5 V
I_{OUT3}	2 A
Transient response 1-A load step	±5%
Input voltage	5 V normal, 4.5 to 5.5V
Output voltage ripple	±1%

Table 2. Design Parameters (continued)

PARAMETER	VALUE
Switching frequency	2 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Output Inductor Selection

Use Equation 7 to calculate the value of the output inductor. LIR is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor-ripple currents impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, LIR is normally from 0.1 to 0.3 for the majority of applications. Use Equation 7 to calculate the value of the inductor.

$$L = \frac{V_{INmax} - V_{OUT}}{I_{OUT} \times LIR} \times \frac{V_{OUT}}{V_{INmax} \times f_{SW}} \tag{7}$$

For the output filter inductor, the RMS current and saturation current ratings must not be exceeded. Use Equation 8 and to calculate RMS inductor current (I_{Lrms}) and peak inductor current (I_{Lpeak}).

$$I_{Lrms} = \sqrt{I_{OUT}^2 + \frac{\left(\frac{V_{OUT} \times (V_{INmax} - V_{OUT})}{V_{INmax} \times L \times f_{SW}}\right)^2}{12}} \tag{8}$$

$$I_{Lpeak} = I_{OUT} + \frac{I_{ripple}}{2}$$

where

$$I_{ripple} = \frac{V_{INmax} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{INmax} \times f_{SW}}$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the peak inductor current level calculated in Equation 9. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

8.2.2.2 Output Capacitor Selection

The three primary considerations for selecting the value of the output capacitor are:

- Output capacitor which determines the modulator pole
- Output voltage ripple
- How the regulator responds to a large change in load current

The output capacitance must be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation would occur if the desired hold-up times for the regulator occur where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if the current requirements of the load experience a large, fast increase, such as a transition from no load to full load. The regulator typically requires two or more clock cycles for the control loop to experience a change in load current and output voltage, and to adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. Use Equation 10 to calculate the minimum output capacitance (C_O) required to accomplish this.

$$C_{OUT} = \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}}$$

where

- ΔI_{OUT} is the change in output current
- f_{sw} is the regulators switching frequency
- ΔV_{OUT} is the allowable change in the output voltage (10)

Equation 11 calculates the minimum output capacitance required to meet the output voltage ripple specification.

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{OUTripple}}{I_{OUTripple}}}$$

where

- f_{SW} is the switching frequency
- $V_{OUTripple}$ is the maximum allowable output voltage ripple
- $I_{OUTripple}$ is the inductor ripple current (11)

Use Equation 12 to calculate the maximum ESR an output capacitor can have to meet the output voltage ripple specification.

$$R_{esr} < \frac{V_{OUTripple}}{I_{OUTripple}} \tag{12}$$

Additional capacitance deratings for aging, temperature, and DC bias should be factored in, which increase this minimum value. Capacitors generally have limits to the amount of ripple current they can support without failing or producing excess heat. The user must specify an output capacitor that can support the inductor ripple current. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. Use Equation 13 to calculate the RMS ripple current that the output capacitor must support ($I_{COUTrms}$).

$$I_{COUTrms} = \frac{V_{OUT} \times \left(V_{INmax} - V_{OUT}\right)}{\sqrt{12} \times V_{INmax} \times L \times f_{SW}} \tag{13}$$

8.2.2.3 Input Capacitor Selection

The TPS65268-Q1 device requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor with at least 10 µF of effective capacitance on the PVIN input voltage pins. In some applications, additional bulk capacitance may also be required for the PVIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS65268-Q1. Use Equation 14 to calculate the input ripple current (I_{INrms}).

$$I_{INrms} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{INmin}} \times \frac{\left(V_{INmin} - V_{OUT}\right)}{V_{INmin}}} \tag{14}$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations because of temperature can be minimized by selecting a dielectric material that is stable over temperature. Ceramic dielectric capacitors with type X5R and X7R are usually selected for power regulator capacitors because they have a high capacitance-to-volume ratio and are fairly stable over temperature. The DC bias must also be considered when selecting an output capacitor. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. The input capacitance value determines the input ripple voltage of the regulator. Use Equation 15 to calculate the input voltage ripple (ΔV_{IN}).

$$\Delta V_{IN} = \frac{I_{OUTmax} \times 0.25}{C_{IN} \times f_{SW}} \tag{15}$$

8.2.2.4 Loop Compensation

The TPS65268-Q1 device incorporates a peak current-mode control scheme. The error amplifier is a transconductance amplifier with a gain of 300 µS. A typical type II compensation circuit adequately delivers a phase margin from 40° to 90°. The C_b capacitor adds a high-frequency pole to attenuate high-frequency noise when needed. To calculate the external compensation components, follow these steps:

1. Select a switching frequency, f_{SW}, that is appropriate for the application depending on the inductor size,

capacitor size, output ripple, EMI, and so forth. Selecting the switching frequency is a trade-off between performance and cost. To achieve a smaller size and lower cost, a higher switching frequency is desired. To optimize efficiency, a lower switching frequency is desired.

2. Set up the crossover frequency, f_C, which is typically from 1/5 to 1/20 of f_{SW}.
3. Use Equation 16 to calculate the value of R_C.

$$R_C = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUT}}{G_{m\_EA} \times V_{ref} \times G_{M\_PS}}$$

where
- G_{m_EA} is the error amplifier gain (300 µS).
- G_{m_PS} is the power stage voltage to current conversion gain (7.4 A/V). (16)

4. Use Equation 17 to calculate the value C_c by placing a compensation zero at or before the dominant pole ($f_p = \frac{1}{C_{OUT} \times R_L \times 2\pi}$).

$$C_c = \frac{R_L \times C_{OUT}}{R_C} \tag{17}$$

5. Optional: Use Equation 18 to calculate the value of C_B capacitor to cancel the zero from the ESR associated with C_O.

$$C_b = \frac{R_{esr} \times C_{OUT}}{R_C} \tag{18}$$

6. Optional: Implement type III compensation with the addition of one capacitor, C1. This implementation allows for slightly higher loop bandwidths and higher phase margins. If used, used Equation 19 to calculate the value of C1.

$$C1 = \frac{1}{2\pi \times R1 \times f_C} \tag{19}$$

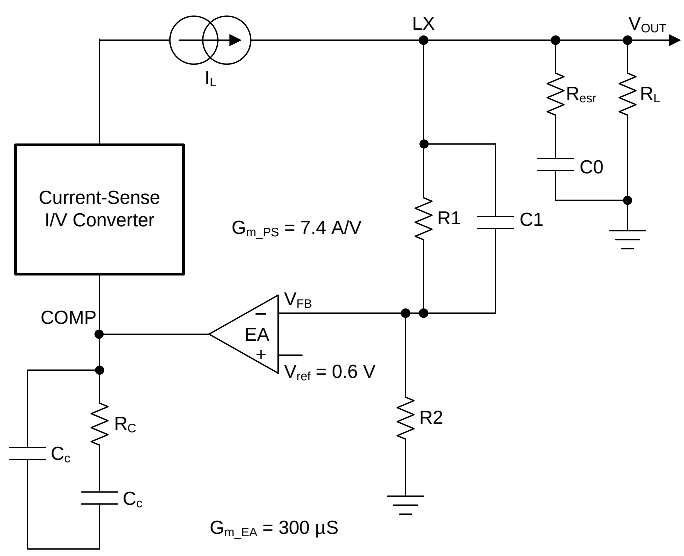
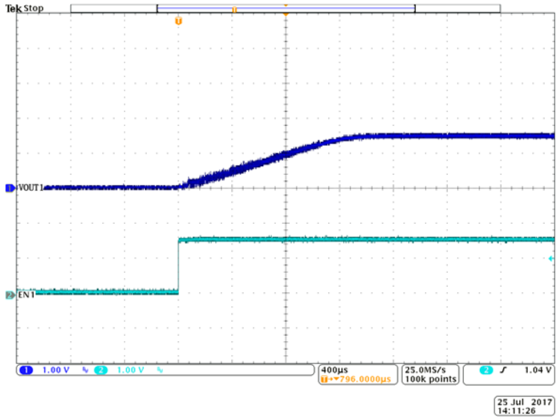


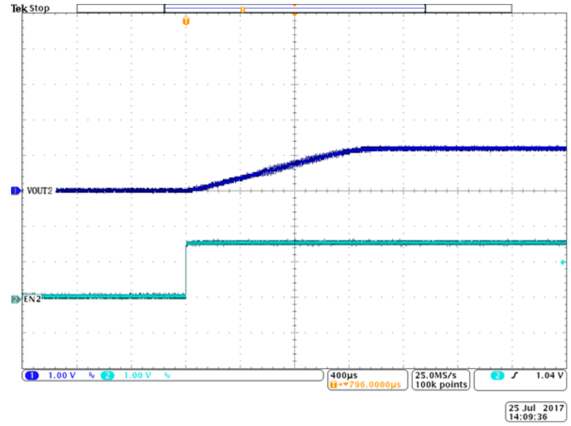
Figure 33. DC-DC Loop Compensation

8.2.3 Application Curves



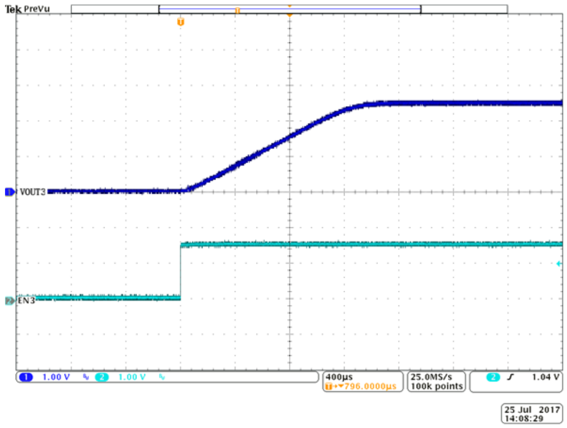
I_{OUT} = 3 A

Figure 34. BUCK1 Soft-Start



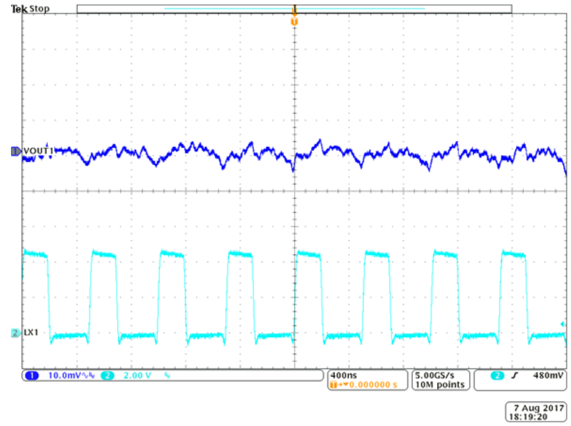
I_{OUT} = 2 A

Figure 35. BUCK2 Soft-Start



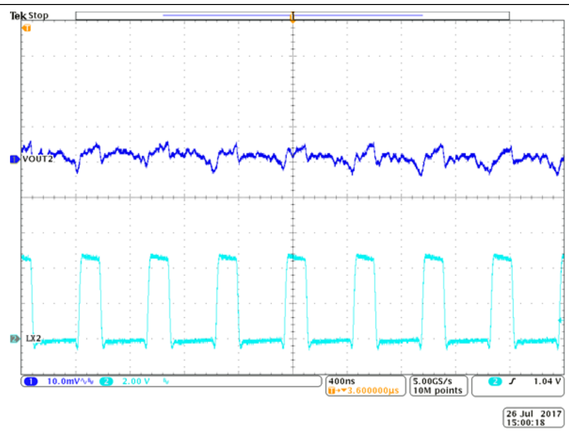
I_{OUT} = 2 A

Figure 36. BUCK3 Soft-Start



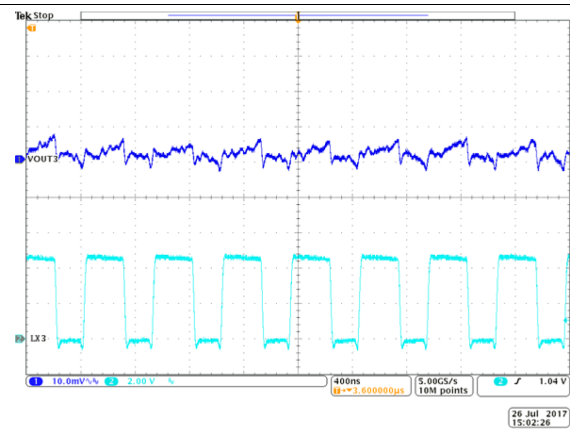
I_{OUT} = 3 A

Figure 37. BUCK1 Output Voltage Ripple



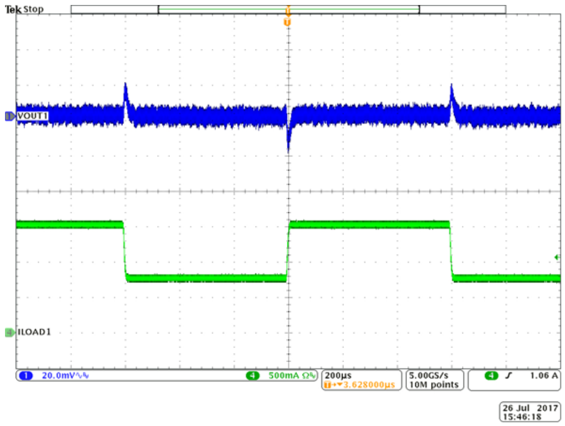
I_{OUT} = 2 A

Figure 38. BUCK2 Output Voltage Ripple



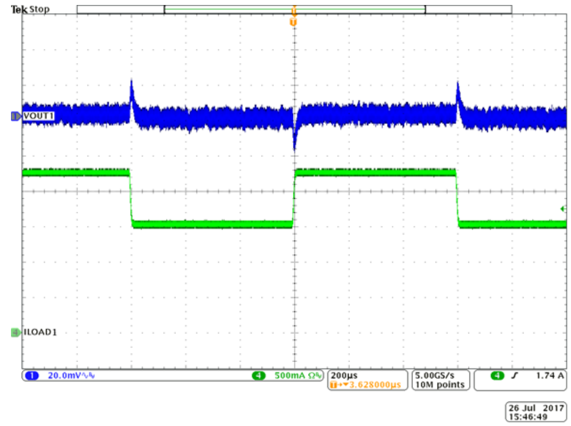
I_{OUT} = 2 A

Figure 39. BUCK3 Output Voltage Ripple



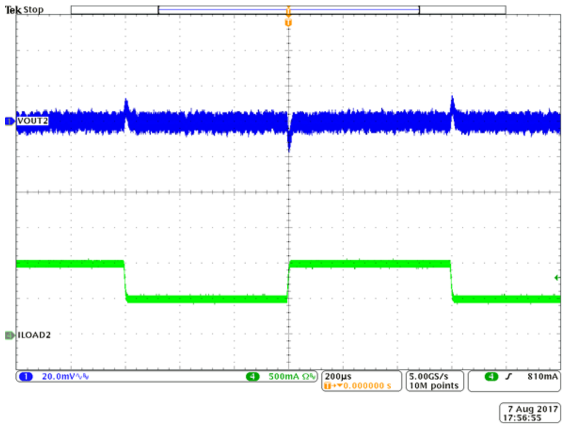
I_{OUT} = 0.75 to 1.5 A SR = 0.25 A/µs

Figure 40. BUCK1 Load Transient



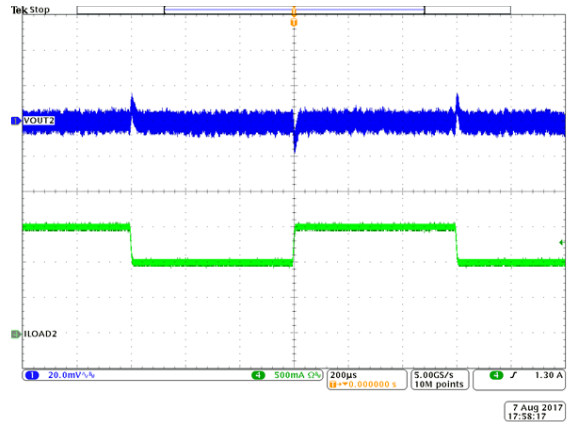
I_{OUT} = 1.5 to 2.25 A SR = 0.25 A/µs

Figure 41. BUCK1 Load Transient



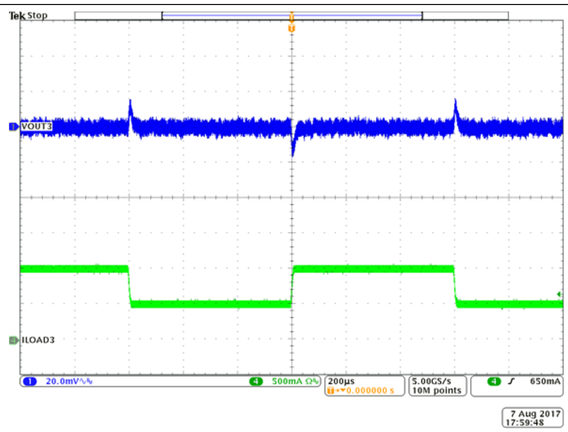
I_{OUT} = 0.5 to 1 A SR = 0.25 A/µs

Figure 42. BUCK2 Load Transient



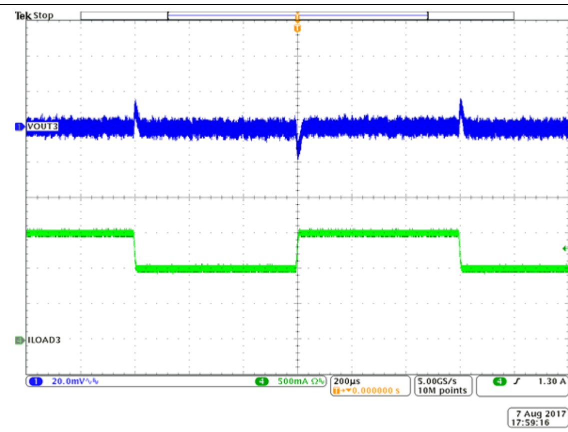
I_{OUT} = 1 to 1.5 A SR = 0.25 A/µs

Figure 43. BUCK2 Load Transient



I_{OUT} = 0.5 to 1 A SR = 0.25 A/µs

Figure 44. BUCK3 Load Transient



I_{OUT} = 1 to 1.5 A SR = 0.25 A/µs

Figure 45. BUCK3 Load Transient

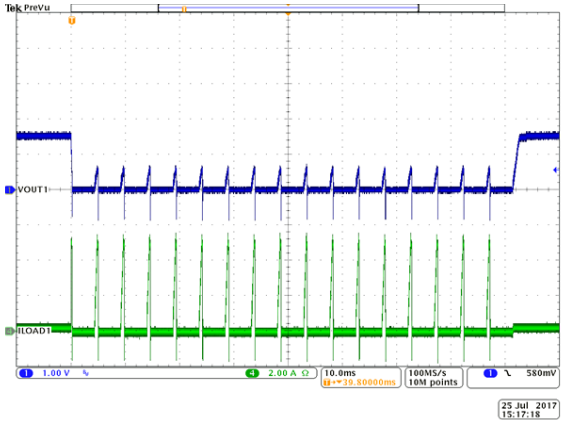


Figure 46. BUCK1 Hiccup and Recovery

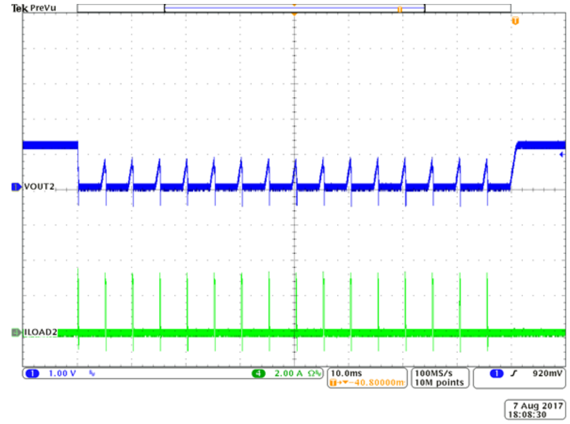


Figure 47. BUCK2 Hiccup and Recovery

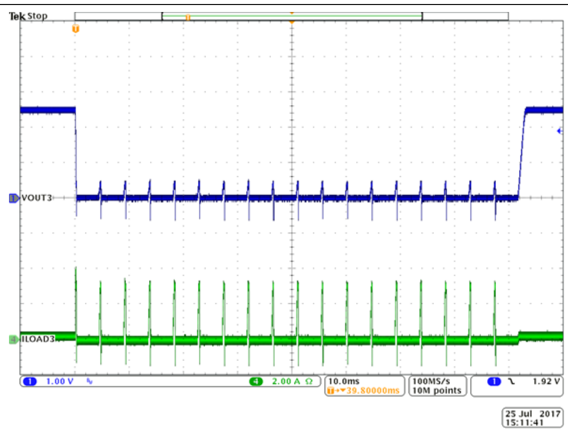


Figure 48. BUCK3 Hiccup and Recovery

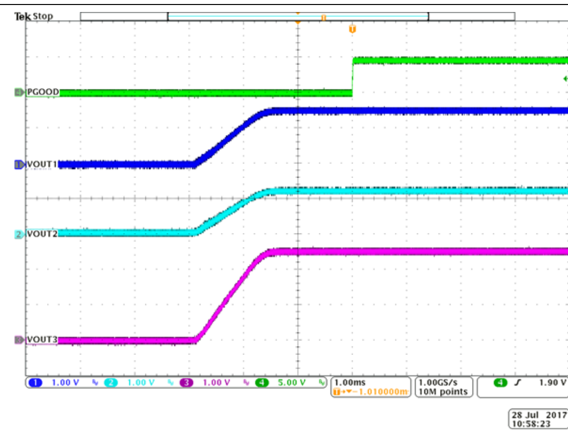


Figure 49. PGOOD

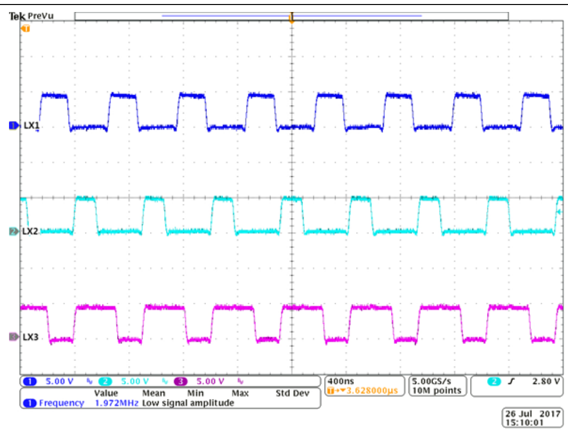


Figure 50. 180° Out-of-Phase

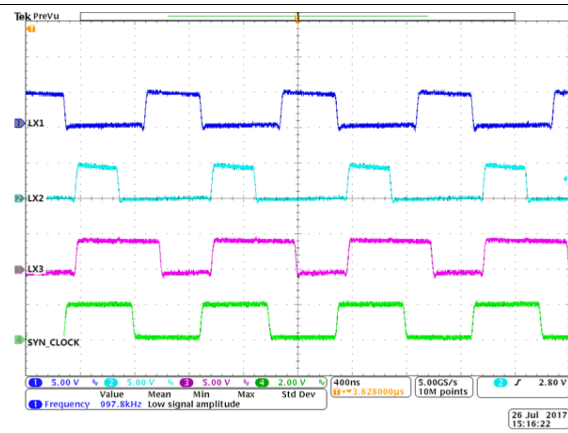
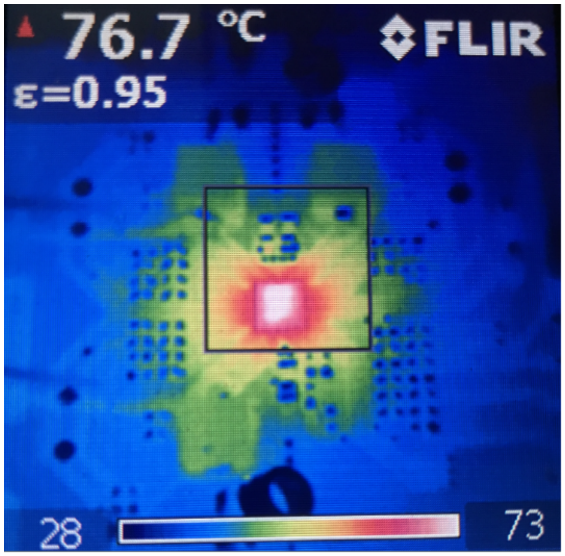


Figure 51. Synchronization With External Clock



V_{IN} = 12 V, V_{OUT1} = 1.5 V/2 A, V_{OUT2} = 1.2 V/1.5 A,
V_{OUT3} = 2.5 V/1.5 A,
T_A = 28°C EVM condition 4 layers, 75 mm × 75 mm

Figure 52. Thermal Signature of TPS65268-Q1EVM Operating

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 4 V to 8 V. This input power supply should be well regulated. If the input supply is located more than a few inches from the TPS65268-Q1 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

Figure 53 shows the TPS65268-Q1 layout example on a 2-layer printed circuit board (PCB).

Layout is a critical portion of good power-supply design. The top layer contains the main power traces for PVIN, VOx, and LX. The top layer also has connections for the remaining pins of the TPS65268-Q1 device and a large top-side area filled with ground. The top-layer ground area should be connected to the bottom-layer ground using vias at the input bypass capacitor, the output filter capacitor, and directly under the TPS65268-Q1 device to provide a thermal path from the exposed thermal pad land to ground. The bottom layer acts as ground plane connecting analog ground and power ground.

For operation at full rated load, the top-side ground area together with the bottom-side ground plane must provide adequate heat dissipating area. Several signals paths conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the performance of the power supplies. To help eliminate these problems, bypass the PVIN pin to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric. Take care to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections. The VIN pin must also be bypassed to ground using a low-ESR ceramic capacitor with X5R or X7R dielectric.

Because the LX connection is the switching node, the output inductor should be located close to the LXx pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output filter capacitor ground should use the same power ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The small signal components should be grounded to the analog ground path.

The FB and COMP pins are sensitive to noise so the resistors and capacitors should be located as close as possible to the device and routed with minimal lengths of trace. The additional external components can be placed approximately as shown in Figure 53.

10.2 Layout Example

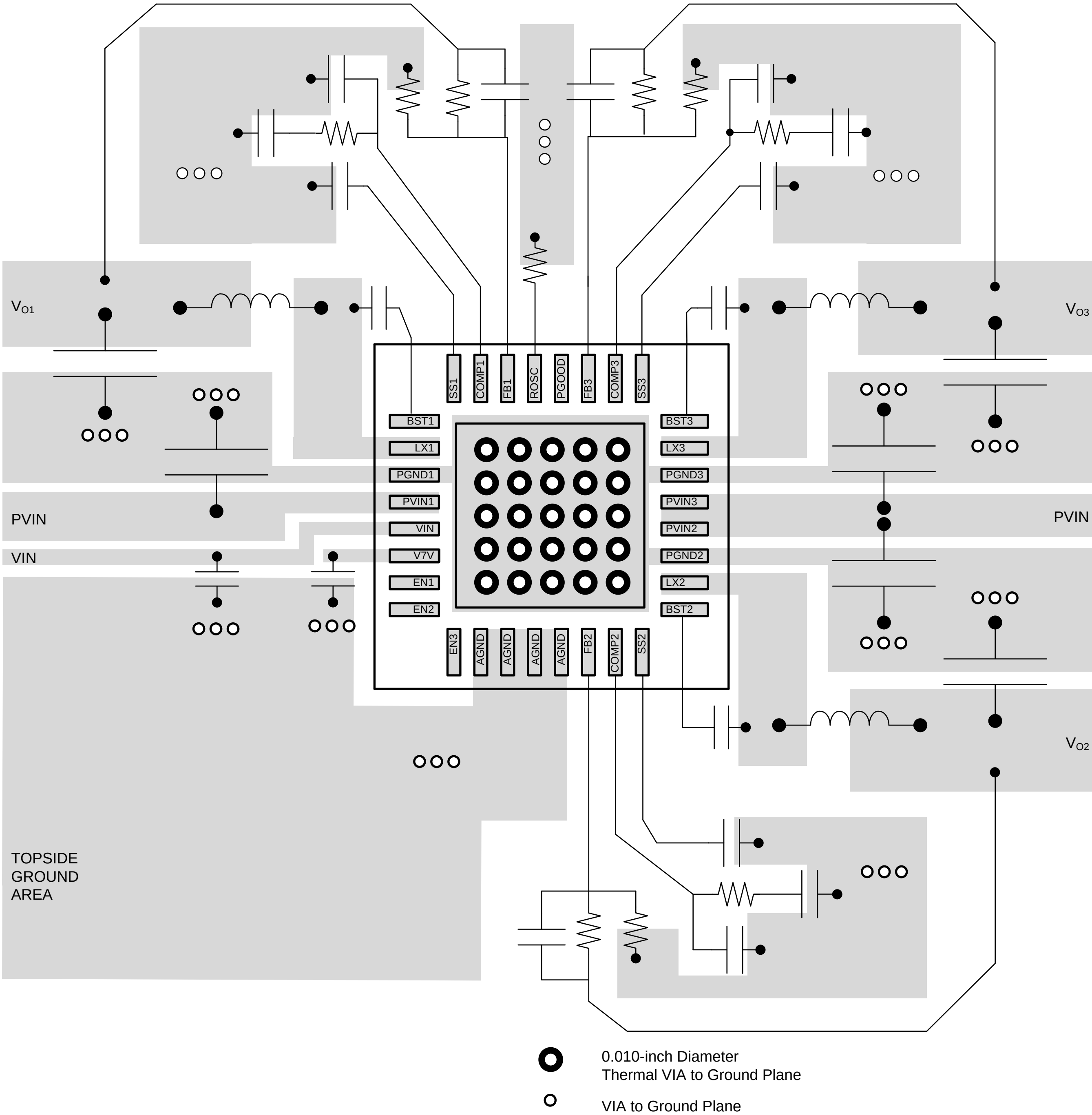


Figure 53. PCB Layout

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65268QRHBRQ1	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 268-1Q	Samples
TPS65268QRHBTQ1	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 268-1Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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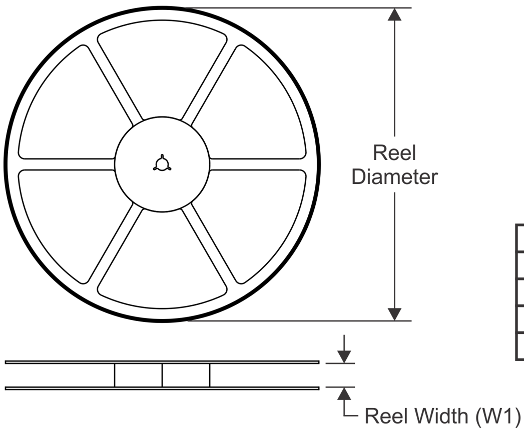
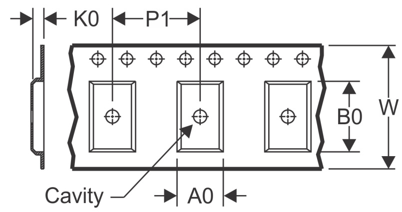
TAPE AND REEL INFORMATION

REEL DIMENSIONS

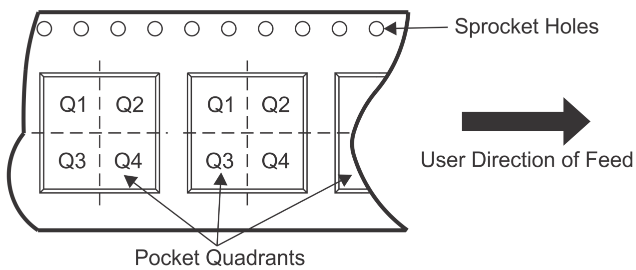


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

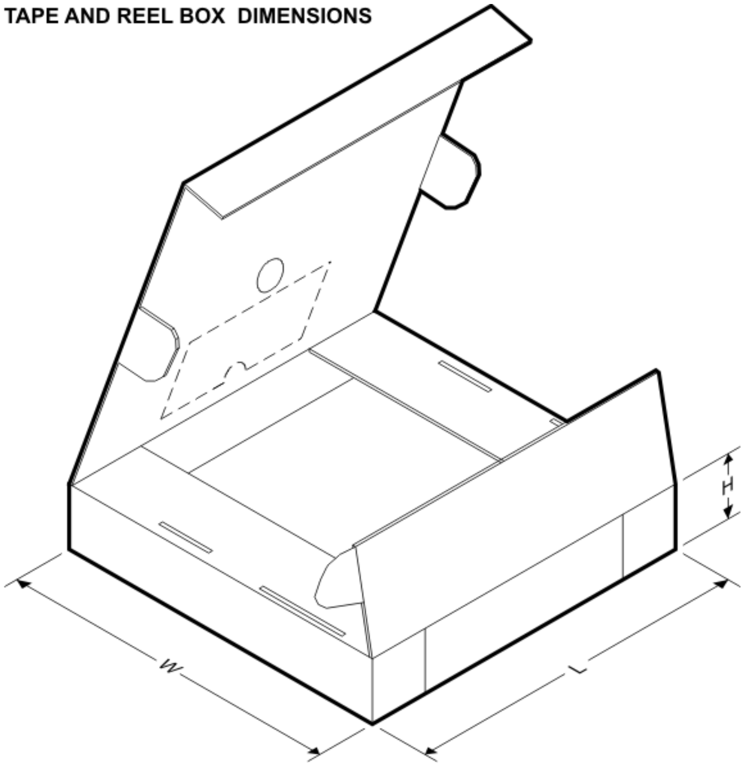
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65268QRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65268QRHBTQ1	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

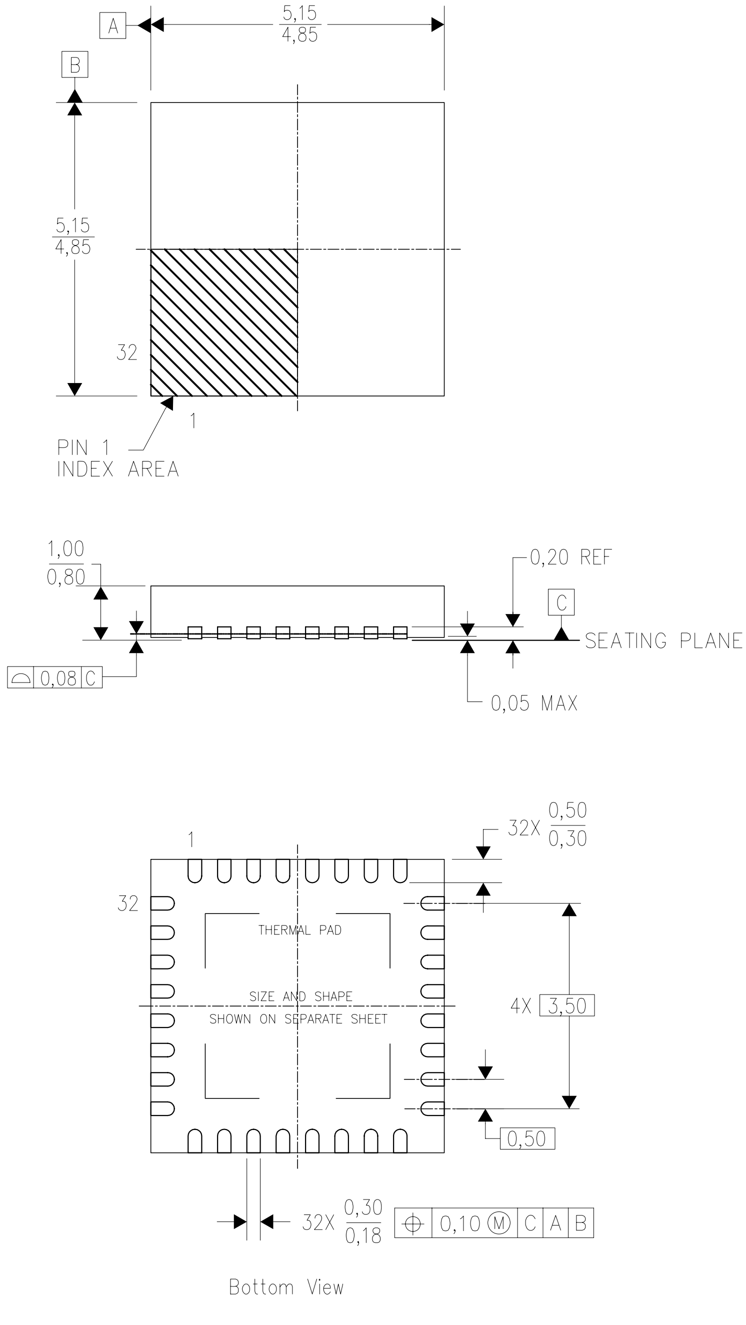
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65268QRHBRQ1	VQFN	RHB	32	3000	367.0	367.0	35.0
TPS65268QRHBTQ1	VQFN	RHB	32	250	210.0	185.0	35.0

RHB (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.

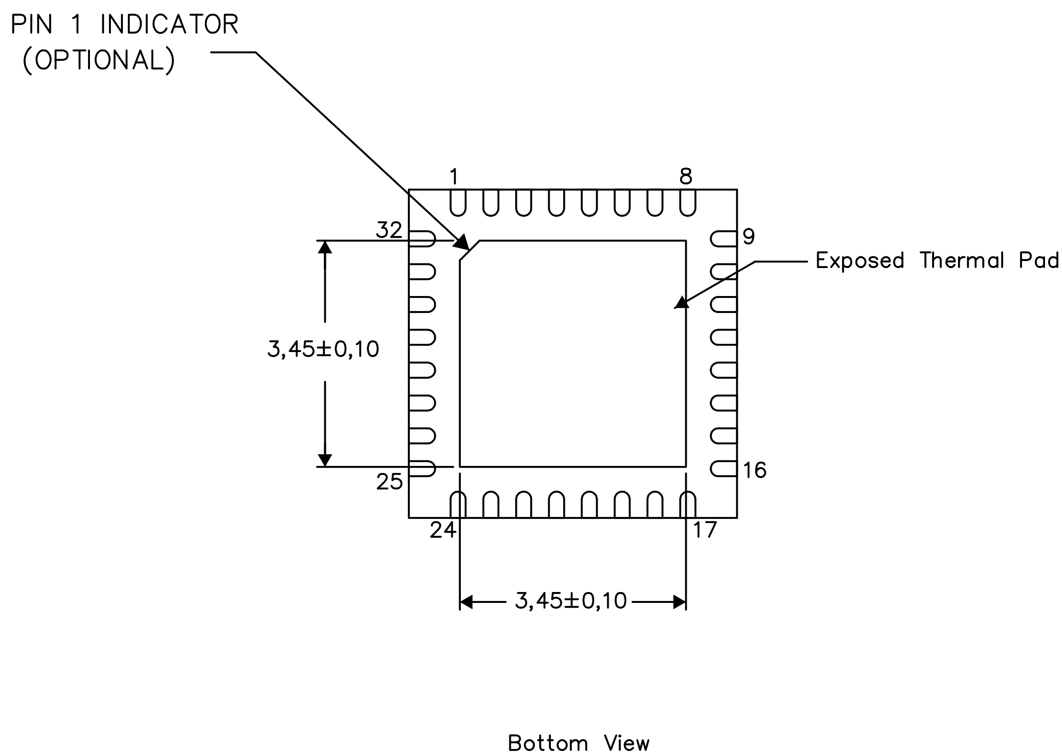
RHB (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

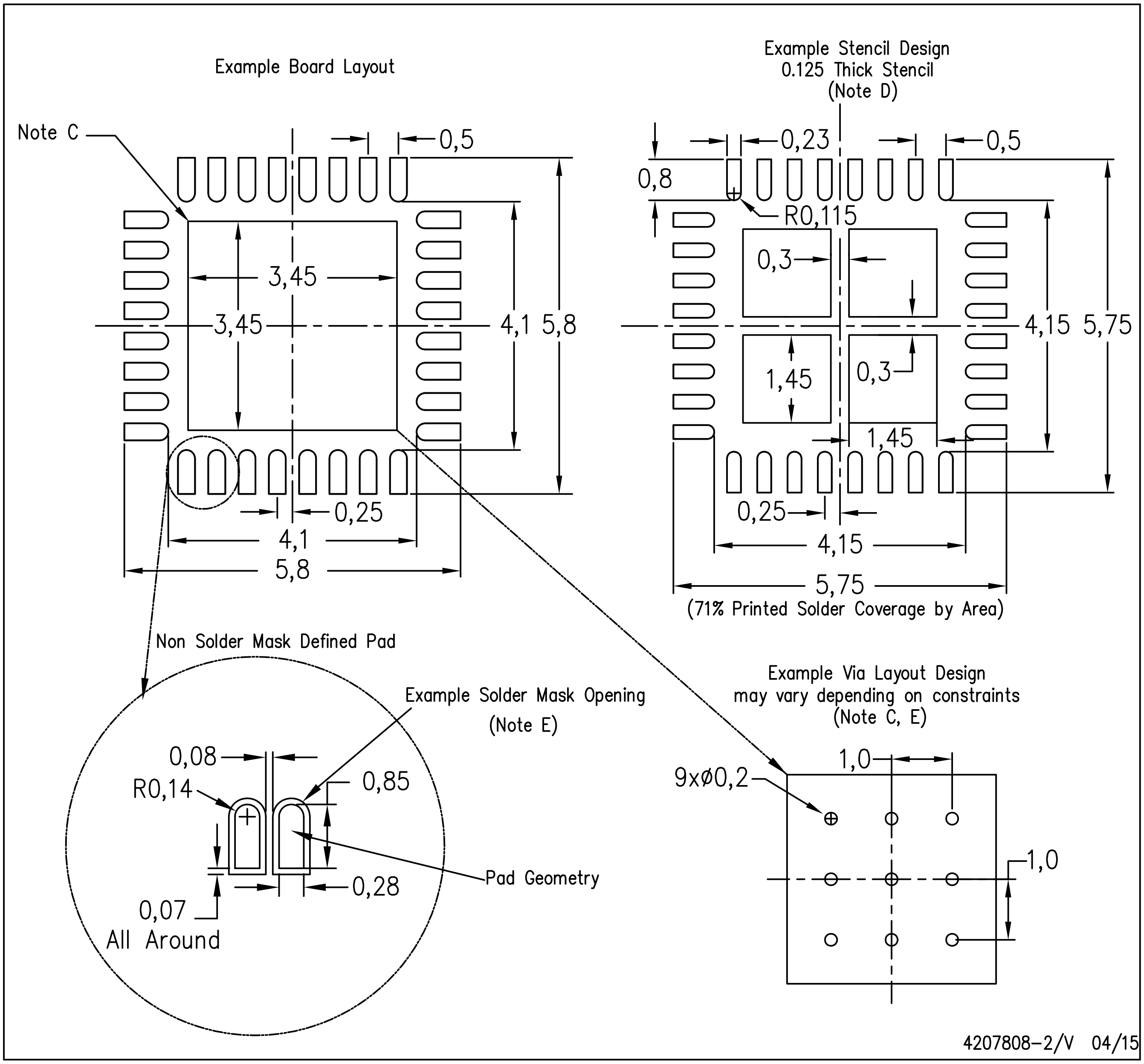


Exposed Thermal Pad Dimensions

4206356-2/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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