

TPS546D24 2.95-V to 16-V, 40-A, up to 4x Stackable, PMBus® Buck Converter

1 Features

- Split Rail Support: 2.95-V to 16-V PVIN; 2.95-V to 16-V AVIN (4-V_{IN} VDD5 for Switching)
- Integrated 4.5-mΩ/0.9-mΩ MOSFETs
- Average Current Mode Control With Selectable Internal Compensation
- 2x, 3x, 4x Stackable With Current Sharing up to 160 A, Supporting a Single Address per Output
- Selectable 0.6-V to 5.5-V Output via Pin Strap or 0.25-V to 5.5-V via PMBus VOUT_COMMAND
- Extensive PMBus Command Set With Telemetry for V_{OUT}, I_{OUT} and Internal Die Temperature
- Differential Remote Sensing With Internal FB Divider for < 1% V_{OUT} Error –40°C to +150°C T_J
- AVS and Margining Capabilities Through PMBus
- MSEL Pins Pin Programming PMBus Defaults
- 12 Selectable Switching Frequencies from 225 kHz to 1.5 MHz (8 Pin-Strap Options)
- Frequency Sync In/Sync Out
- Supports Prebiased Output
- Supports Strongly Coupled Inductor
- 7 mm × 5 mm × 1.5 mm, 40-pin QFN, Pitch = 0.5 mm
- Create a Custom Design Using the TPS546D24 With [WEBENCH® Power Designer](#)

2 Applications

- Data Center Switches, Rack Servers
- Active Antenna System, Remote Radio and Baseband Unit
- Automated Test Equipment, CT, PET, and MRI
- ASIC, SoC, FPGA, DSP Core, and I/O Voltage

3 Description

The TPS546D24 is a highly integrated, non-isolated DC/DC converter capable of high frequency operation and 40-A current output from a 7-mm × 5-mm package. Two, three, and four TPS546D24 devices can be interconnected to provide up to 160 A on a single output. The device has an option to overdrive the internal 5-V LDO with an external 5-V supply via the VDD5 pin to improve efficiency and reduce power dissipation of the converter.

The TPS546D24 uses a proprietary fixed-frequency current-mode control with input feedforward and selectable internal compensation components for minimal size and stability over a wide range of output capacitances

The PMBus interface with 1-MHz clock support gives a convenient, standardized digital interface for converter configuration as well as monitoring of key parameters including output voltage, output current, and internal die temperature. Response to fault conditions can be set to restart, latch off, or ignore, depending on system requirements. Back-channel communication between stacked devices enables all TPS546D24 converters powering a single output rail to share a single address to simplify system software/firmware design. Key parameters including output voltage, switching frequency, soft-start time, and overcurrent fault limits can also be configured through BOM selection program without PMBus communication to support program free power-up.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|----------------|-------------------|
| TPS546D24 | LQFN-CLIP (40) | 7.00 mm × 5.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application

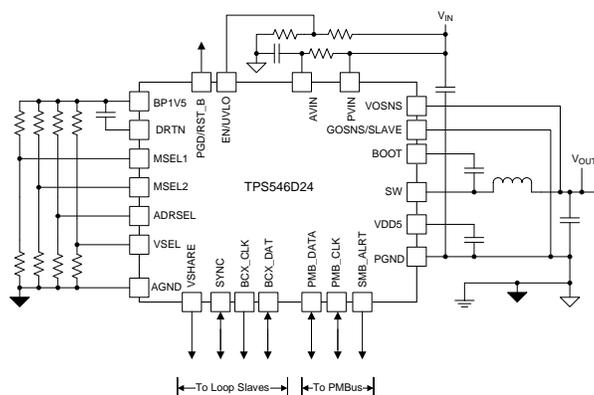


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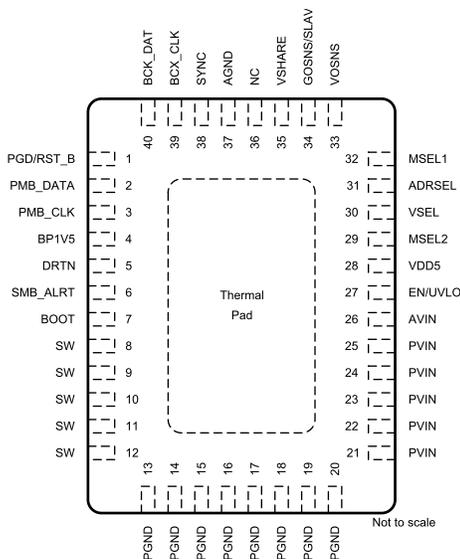
4 Revision History

| DATE | REVISION | NOTES |
|---------------|----------|-----------------|
| November 2018 | * | Initial release |

ADVANCE INFORMATION

5 Pin Configuration and Functions

RVF Package
40-Pin LQFN-CLIP With Exposed Thermal Pad
Top View



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|-----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NO. | NAME | | |
| 1 | PGD/RST_B | I/O | Open-drain power good or VOUT_COMMAND reset#, As determined by user accessible bit (See MFR_SPECIFIC_29 (MISC_OPTIONS, (EDh) in PMBus Command detailed descriptions) . The default pin function is an open drain power-good indicator. |
| 2 | PMB_DATA | I/O | PMBus DATA pin. See PMBus specification. |
| 3 | PMB_CLK | I | PMBus CLK pin. See PMBus specification. |
| 4 | BP1V5 | O | Output of the 1.5-V internal regulator. This regulator powers the digital circuitry and should be bypassed with a minimum of 1 μ F to DRTN. Connect a pullup resistor of 5.1 k Ω from VDD5 to BP1V5. BP1V5 is not designed to power external circuit. |
| 5 | DRTN | — | Digital bypass return for bypass capacitor for BP1V5. Internally Connected to AGND. Do not Connect to PGND or AGND. |
| 6 | SMB_ALERT | O | SMBus alert pin. See SMBus specification. |
| 7 | BOOT | I | Bootstrap pin for the internal flying high side driver. Connect a typical 100 nF from this pin to SW. To reduce the voltage spike at SW, an optional BOOT resistor of up to 8 Ω may be placed in series with the BOOT capacitor to slow down turn-on of the high-side FET. |
| 8 | SW | I/O | Switched power output of the device. Connect the output averaging filter and bootstrap to this group of pins. |
| 9 | | | |
| 10 | | | |
| 11 | | | |
| 12 | | | |

ADVANCE INFORMATION

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|-----|-------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NO. | NAME | | |
| 13 | PGND | — | Power stage ground return. These pins are internally connected to the thermal pad. |
| 14 | | | |
| 15 | | | |
| 16 | | | |
| 17 | | | |
| 18 | | | |
| 19 | | | |
| 20 | PVIN | I | Input power to the power stage. Low-impedance bypassing of these pins to PGND is critical. |
| 21 | | | |
| 22 | | | |
| 23 | | | |
| 24 | | | |
| 25 | | | |
| 26 | AVIN | I | Input power to the controller. Bypass with a minimum 1- μ F ceramic capacitor PGND. |
| 27 | EN/UVLO | I | Enable switching as the PMBus CONTROL pin. EN/UVLO can also be connected to a resistor divider to program input voltage UVLO. |
| 28 | VDD5 | O | Output of the 5-V internal regulator. This regulator powers the driver stage of the controller and should be bypassed with a minimum of 4.7 μ F to PGND at the thermal pad. Connect a pullup resistor of 5.1 k Ω from VDD5 to BP1V5. Low impedance bypassing of this pin to PGND is critical. |
| 29 | MSEL2 | I | Connect this pin to a resistor divider between BP1V5 and AGND for different options of soft-start time, overcurrent fault limit, and multiphase information. |
| 30 | VSEL | I | Connect this pin to a resistor divider between BP1V5 and AGND for different options of internal voltage feedback divider and default output voltage. See <i>Set Output Voltage</i> section. |
| 31 | ADRSEL | I | Connect this pin to a resistor divider between BP1V5 and AGND for different options of PMBus addresses and frequency sync (including determination of SYNC pin as SYNC IN or SYNC OUT function). |
| 32 | MSEL1 | I | Connect this pin to a resistor divider between BP1V5 and AGND for different options of switching frequency and internal compensation parameters. See section. |
| 33 | VOSNS | I | The positive input of the remote sense amplifier. For a standalone device or the loop master device in a multiphase configuration, connect VOSNS pin to the output voltage at the load. For the loop slave device in a multiphase configuration, the remote sense amplifier is not required for output voltage sensing or regulation, this pin can be left floating. |
| 34 | GOSNS/SLAVE | I | The negative input of the remote sense amplifier for loop master device or should be pulled up high to indicate loop slave. For standalone device or the loop master device in a multiphase configuration, connect GOSNS pin to the ground at the load. For the loop slave device in a multiphase configuration, the GOSNS pin must be pulled up to BP1V5 to indicate the device a loop slave. |
| 35 | VSHARE | I/O | Voltage sharing signal for multiphase operation. For stand-alone device, the VSHARE pin must be left floating. |
| 36 | NC | - | Not internally connected. Pin can be left floating or connected to PGND at the thermal pad. |
| 37 | AGND | - | Analog ground return for controller. Connect the AGND pin directly to the thermal pad on the PCB board. |
| 38 | SYNC | I/O | For frequency synchronization, can be programmed as SYNC IN or SYNC OUT pin by ADRSEL pin or the SYNC_CONFIG PMBus Command. The SYNC pin can be left floating when not used. |
| 39 | BCX_CLK | I | Clock for back-channel communications between stacked devices. |
| 40 | BCK_DAT | I/O | Data for back-channel communications between stacked devices. |
| — | Thermal pad | — | Package thermal pad, internally connected to PGND. The thermal pad must have adequate solder coverage for proper operation. |

ADVANCE INFORMATION

6 Device and Documentation Support

6.1 Device Support

6.1.1 Third-Party Products Disclaimer

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6.1.2 Development Support

6.1.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TPS546D24 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

6.1.2.2 Texas Instruments Fusion Digital Power Designer

The TPS546D24 devices are supported by Texas Instruments Digital Power Designer. Fusion Digital Power Designer is a graphical user interface (GUI) which can be used to configure and monitor the devices via PMBus using a Texas Instruments USB-to-GPIO adapter.

Click this link to download the Texas Instruments [Fusion Digital Power Designer](#) software package.

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.4 Trademarks

E2E is a trademark of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

PMBus is a registered trademark of System Management Interface Forum, Inc..

6.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. These data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|-------------------------|----------------------|--------------|-------------------------|---------|
| TPS546D24RVFR | PREVIEW | LQFN-CLIP | RVF | 40 | 2500 | TBD | Call TI | Call TI | -40 to 125 | | |
| TPS546D24RVFT | PREVIEW | LQFN-CLIP | RVF | 40 | 250 | TBD | Call TI | Call TI | -40 to 125 | | |
| XPS546D24RVFT | ACTIVE | LQFN-CLIP | RVF | 40 | 250 | TBD | Call TI | Call TI | -40 to 125 | | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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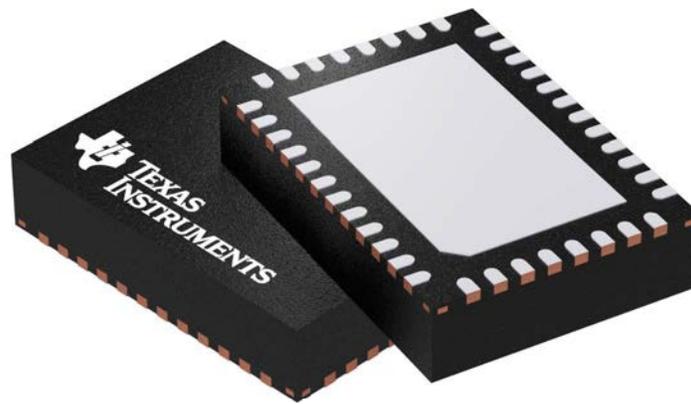
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GENERIC PACKAGE VIEW

RVF 40

LQFN-CLIP - 1.52 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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