TEXAS INSTRUMENTS

TPS54335-2A

SLUSCK3 – JULY 2016

TPS54335-2A 4.5-V to 28-V Input, 3-A Output, Synchronous Step-Down DC-DC Converter

1 Features

- Synchronous 128-mΩ and 84-mΩ MOSFETs for 3-A Continuous Output Current
- Internal 2-ms Soft-Start, 50-kHz to 1.5-MHz Adjustable Frequency
- Low 2-µA Shutdown, Quiescent Current
- 0.8-V Voltage Reference with ±0.8% Accuracy
- Current Mode Control
- Monotonic Startup into Pre-Biased Outputs
- Pulse Skipping for Light-Load Efficiency
- Hiccup Mode Overcurrent Protection
- Thermal Shutdown (TSD) and Overvoltage Transition Protection
- 10-Pin VSON Package

2 Applications

- Consumer Applications such as a Digital TV (DTV), Set Top Box (STB, DVD/Blu-ray Player), LCD Display, CPE (Cable Modem, WiFi Router), DLP Projectors, Smart Meters
- Battery Chargers
- Industrial and Car Audio Power Supplies
- 5-V, 12-V, and 24-V Distributed Power Bus Supply

3 Description

The TPS54335-2A synchronous converter with an input-voltage range of 4.5 V to 28 V. This device has an integrated low-side switching FET that eliminates the need for an external diode which reduces component count.

Efficiency is maximized through the integrated 128-mΩ and 84-mΩ MOSFETs, low I_Q and pulse skipping at light loads. Using the enable pin, the shutdown supply current is reduced to 2 µA. This step-down (buck) converter provides accurate regulation for a variety of loads with a well-regulated voltage reference that is 1.5% over temperature.

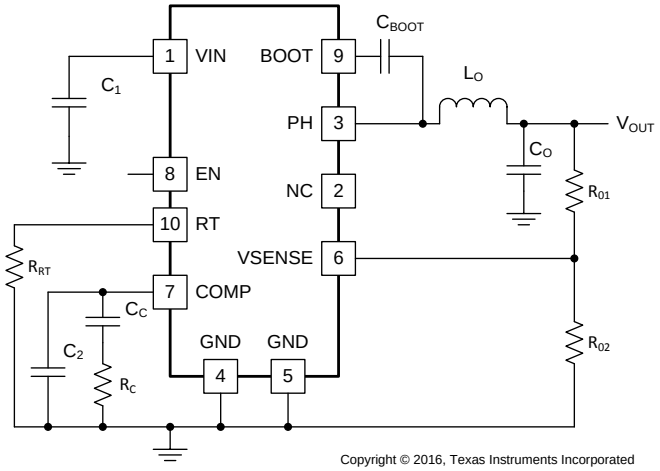
Cycle-by-cycle current limiting on the high-side MOSFET protects the TPS54335-2A in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. A low-side sinking current-limit turns off the low-side MOSFET to prevent excessive reverse current. Hiccup protection is triggered if the overcurrent condition continues for longer than the preset time. Thermal shutdown disables the device when the die temperature exceeds the threshold and enables the device again after the built-in thermal hiccup time.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54335-2A	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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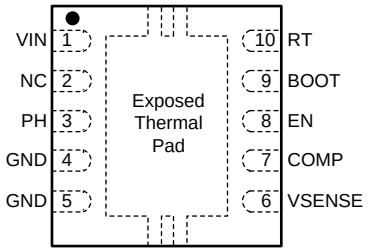
4 Revision History

DATE	REVISION	NOTES
July, 2016	*	Initial Release

5 Pin Configuration and Functions

DRC Package
10-Pin VSON With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	VSON		
BOOT	9	O	A bootstrap capacitor is required between the BOOT and PH pins. If the voltage on this capacitor is below the minimum required by the output device, the output is forced to switch off until the capacitor is refreshed.
COMP	7	O	This pin is the error-amplifier output and the input to the output switch-current comparator. Connect frequency compensation components to this pin.
EN	8	I	This pin is the enable pin. Float the EN pin to enable.
NC	2	—	No Connect
GND	4	—	Ground
GND	5	—	Ground
PH	3	O	The PH pin is the source of the internal high-side power MOSFET.
RT	10	O	Connect the RT pin to an external timing resistor to adjust the switching frequency of the device.
VIN	1	—	This pin is the 4.5-V to 28-V input supply voltage.
VSENSE	6	I	This pin is the inverting node of the transconductance (gm) error amplifier.
Thermal pad		—	For proper operation, connect the GND pin to the exposed thermal pad. This thermal pad should be connected to any internal PCB ground plane using multiple vias for good thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	30	V
	EN	–0.3	6	V
	BOOT	–0.3	(V_{PH} + 7.5)	V
	VSENSE	–0.3	3	V
	COMP	–0.3	3	V
	RT	–0.3	3	V
Output voltage	BOOT-PH	0	7.5	V
	PH	–1	30	V
	PH, 10-ns transient	–3.5	30	V
V_{DIFF} (GND to exposed thermal pad)		–0.2	0.2	V
Source current	EN	100	100	µA
	RT	100	100	µA
	PH		Current-limit	A
Sink current	PH		Current-limit	A
	COMP	200	200	µA
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under the *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS–001, all pins(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{SS}	Supply input voltage	4.5	28	V
V_{OUT}	Output voltage	0.8	24	V
I_{OUT}	Output current	0	3	A
T_J	Operating junction temperature(1)	–40	150	°C

(1) The device must operate within 150°C to ensure continuous function and operation of the device.

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC		TPS54335-2A DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	°C/W

6.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document unless otherwise noted. These specifications are interpreted as conditions that will not degrade the parametric or functional specifications of the device for the life of the product containing it. T_J = –40°C to 150°C, V = 4.5 to 28 V, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND UVLO (VIN PIN)					
Operating input voltage		4.5		28	V
Input UVLO threshold	Rising V		4	4.5	V
Input UVLO hysteresis			180	400	mV
VIN-shutdown supply current	= 0 V		2	10	µA
VIN-operating non-switching supply current	= 810 mV		310	800	µA
ENABLE (EN PIN)					
Enable threshold	Rising		1.21	1.28	V
Enable threshold	Falling	1.1	1.17		V
Input current	= 1.1 V		1.15		µA
Hysteresis current	= 1.3 V		3.3		µA
VOLTAGE REFERENCE					
Reference	T_J =25°C	0.7936	0.8	0.8064	V
		0.788	0.8	0.812	
MOSFET					
High-side switch resistance(1)	= 3 V		160	280	mΩ
	= 6 V		128	230	mΩ
Low-side switch resistance(1)	V = 12 V		84	170	mΩ
ERROR AMPLIFIER					
Error-amplifier transconductance (gm)	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		1300		µmhos
Error-amplifier source and sink	V_{COMP} = 1 V, 100-mV overdrive		100		µA
Start switching peak current threshold(2)			0.5		A
COMP to I_{SWITCH} gm			8		A/V
CURRENT-LIMIT					
High-side switch current-limit threshold		4	4.9	6.5	A
Low-side switch sourcing current-limit		3.5	4.7	6.1	A
Low-side switch sinking current-limit			0		A

(1) Measured at pins
(2) Not production tested.

Electrical Characteristics (continued)

The electrical ratings specified in this section apply to all specifications in this document unless otherwise noted. These specifications are interpreted as conditions that will not degrade the parametric or functional specifications of the device for the life of the product containing it. T_J = –40°C to 150°C, V = 4.5 to 28 V, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN					
Thermal shutdown(2)		160	175		°C
Thermal shutdown hysteresis(2)			10		°C
BOOT PIN					
BOOT-PH UVLO			2.1	3	V

6.6 Timing Requirements

	MIN	TYP	MAX	UNIT
CURRENT-LIMIT				
Hiccup wait time		512		Cycles
Hiccup time before restart		16384		Cycles
THERMAL SHUTDOWN				
Thermal shutdown hiccup time		32768		Cycles
SOFT START				
Internal soft-start time, TPS54335-2A		2		ms

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PH PIN					
Minimum on time	Measured at 90% to 90% of VIN, I_{PH} = 2 A		94	145	ns
Minimum off time	≥ 3 V		0%		
SWITCHING FREQUENCY					
Switching frequency range, TPS54335-2A		50		1500	kHz
	R = 100 kΩ	384	480	576	kHz
	R = 1000 kΩ, –40°C to 105°C	40	50	60	kHz
	R = 30 kΩ	1200	1500	1800	kHz

6.8 Typical Characteristics

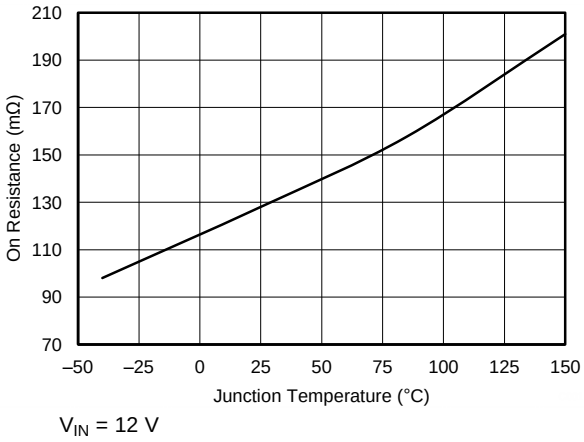


Figure 1. High-Side MOSFET on Resistance vs Junction Temperature

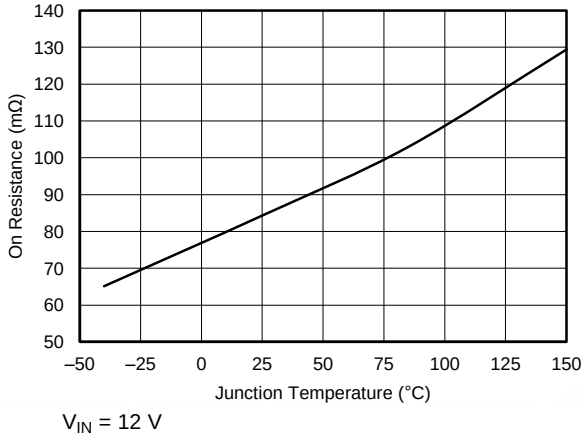


Figure 2. Low-Side MOSFET on Resistance vs Junction Temperature

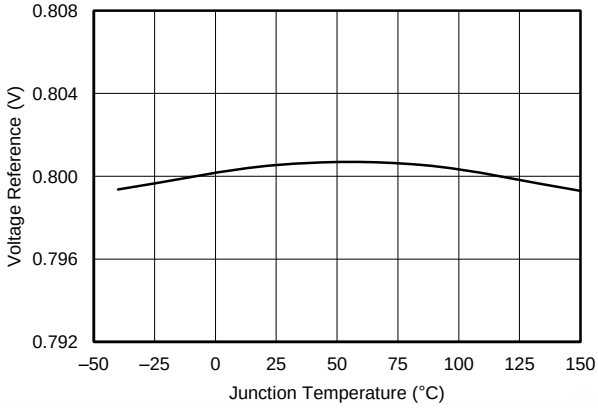


Figure 3. Voltage Reference vs Junction Temperature

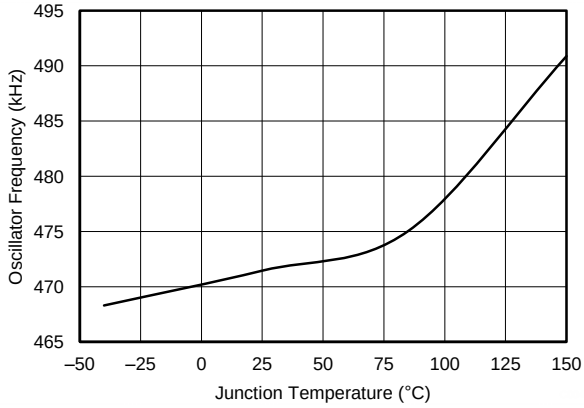


Figure 4. Oscillator Frequency vs Junction Temperature

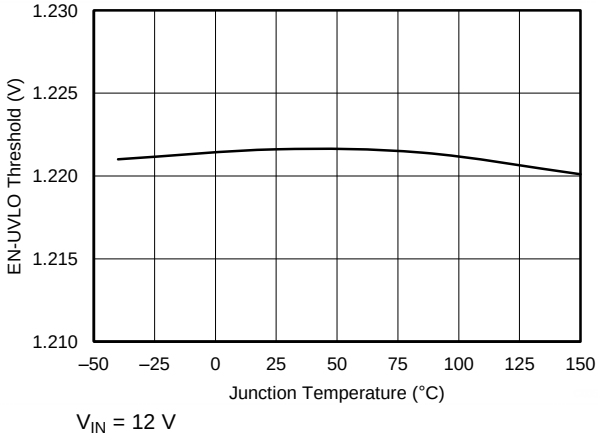


Figure 5. UVLO Threshold vs Junction Temperature

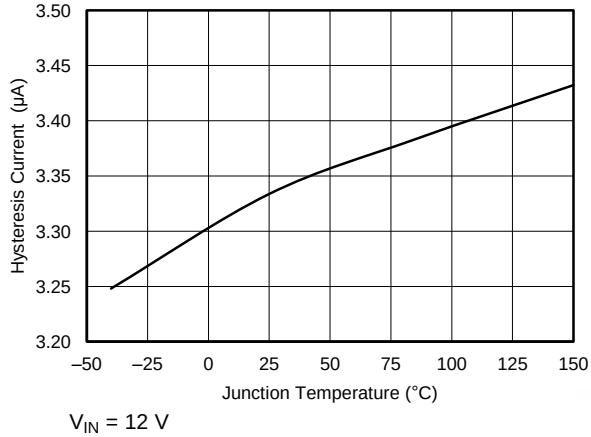


Figure 6. Hysteresis Current vs Junction Temperature

Typical Characteristics (continued)

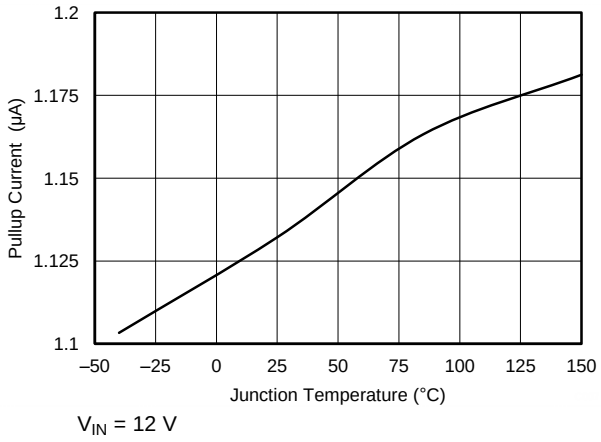


Figure 7. Pullup Current vs Junction Temperature

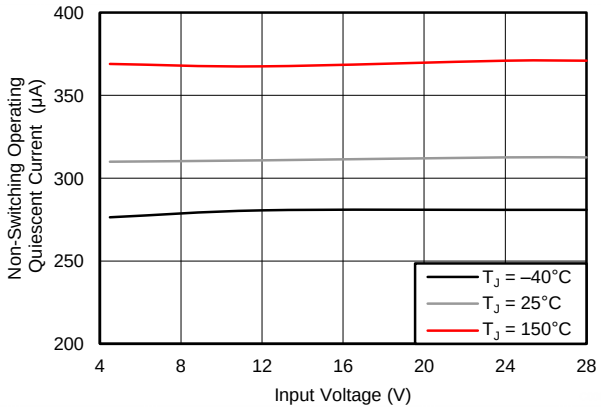


Figure 8. Non-Switching Operating Quiescent Current vs Input Voltage

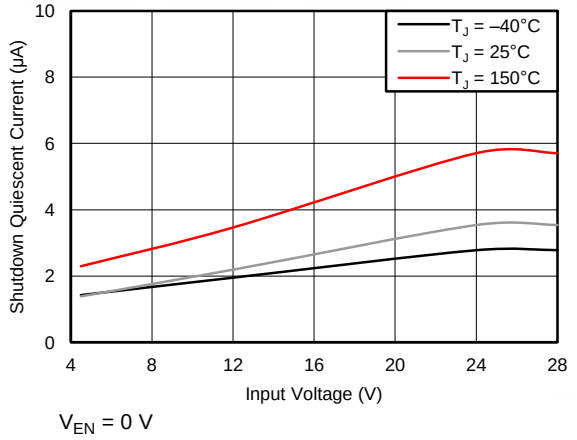


Figure 9. Shutdown Quiescent Current vs Input Voltage

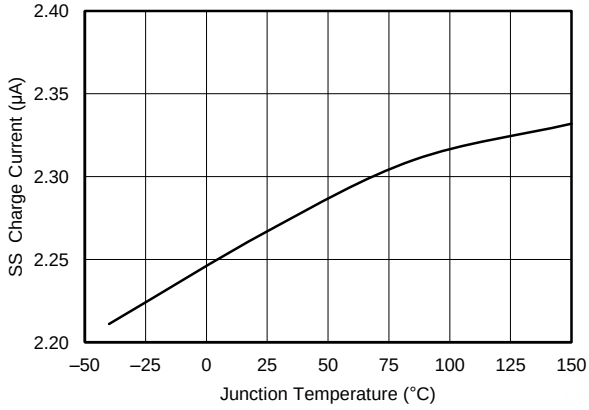


Figure 10. SS Charge Current vs Junction Temperature

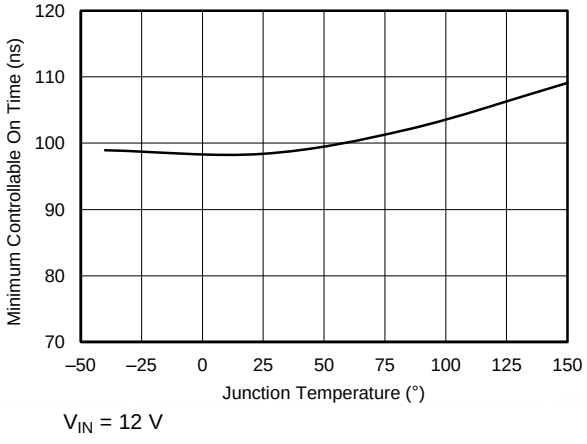


Figure 11. Minimum Controllable On Time vs Junction Temperature

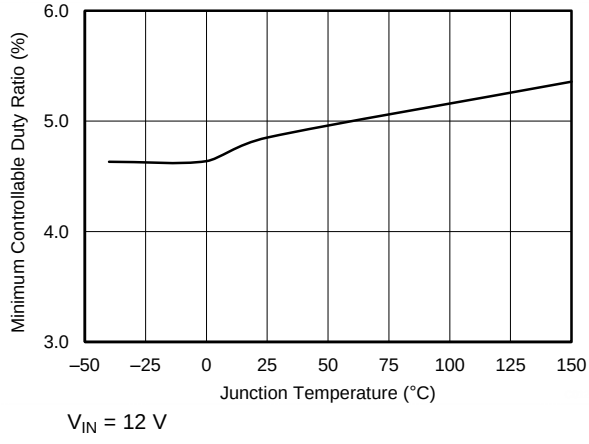


Figure 12. Minimum Controllable Duty Ratio vs Junction Temperature

Typical Characteristics (continued)

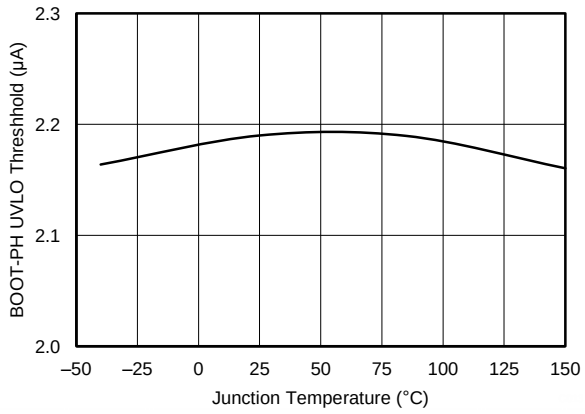


Figure 13. BOOT-PH UVLO Threshold vs Junction Temperature

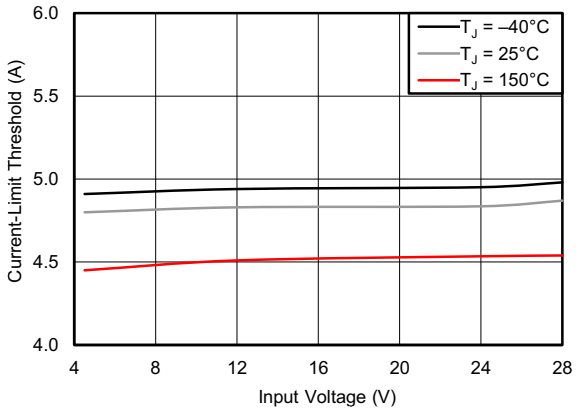


Figure 14. Current Limit Threshold vs Input Voltage

7 Detailed Description

7.1 Overview

The device is a 28-V, 3-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients the device implements a constant-frequency, peak current-mode control which reduces output capacitance and simplifies external frequency-compensation design.

The device has been designed for safe monotonic startup into pre-biased loads. The device has a typical default startup voltage of 4 V. The EN pin has an internal pullup-current source that can provide a default condition when the EN pin is floating for the device to operate. The total operating current for the device is 310 μA (typical) when not switching and under no load. When the device is disabled, the supply current is less than 5 μA.

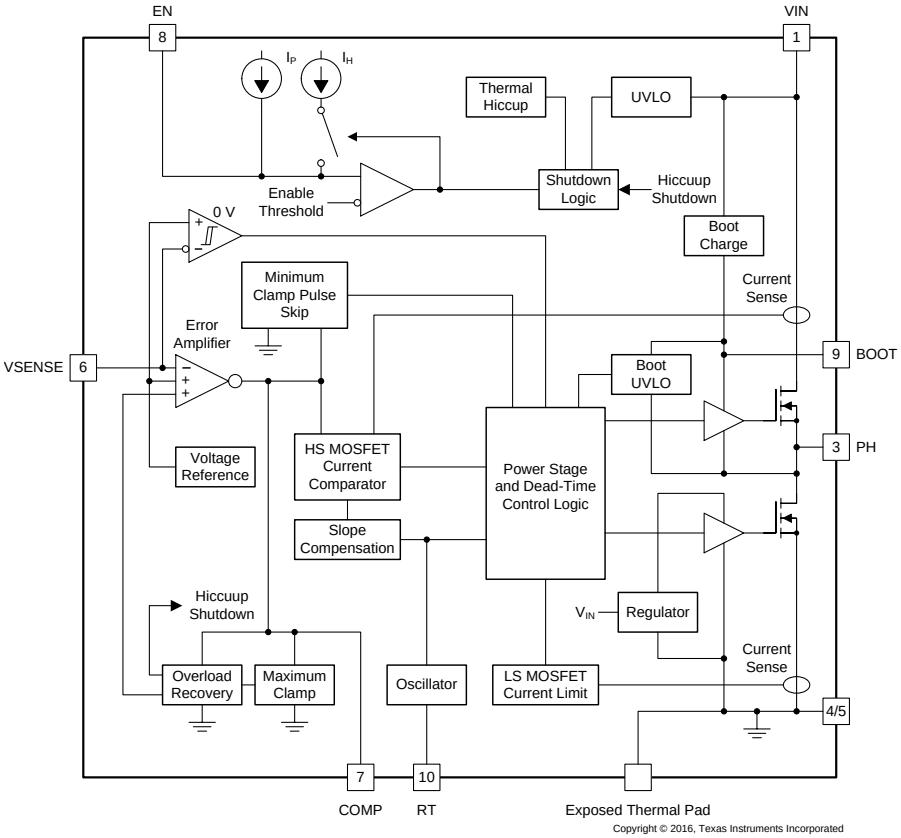
The integrated 128-mΩ and 84-mΩ MOSFETs allow for high-efficiency power-supply designs with continuous output currents up to 3 A.

The device reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and PH pins. The boot capacitor voltage is monitored by an UVLO circuit and turns off the high-side MOSFET when the voltage falls below a preset threshold. The output voltage can be stepped down to as low as the 0.8-V reference voltage.

The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage power-good comparator. When the regulated output voltage is greater than 106% of the nominal voltage, the overvoltage comparator is activated, and the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 104%.

The TPS54335–2A device has a wide switching frequency of 50 kHz to 1500 kHz which allows for efficiency and size optimization when selecting the output filter components. The internal 2-ms soft-start time is implemented to minimize inrush currents.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed-Frequency PWM Control

The device uses a fixed-frequency, peak current-mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is compared to the current of the high-side power switch. When the power-switch current reaches the COMP voltage level the high-side power switch is turned off and the low-side power switch is turned on. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current-limit by clamping the COMP pin voltage to a maximum level and also implements a minimum clamp for improved transient-response performance.

7.3.2 Light-Load Operation

The device monitors the peak switch current of the high-side MOSFET. When the peak switch current is lower than 0.5 A (typical), the device stops switching to boost the efficiency until the peak switch current again rises higher than 0.5 A (typical).

7.3.3 Voltage Reference

The voltage-reference system produces a precise ±1.5% voltage-reference over temperature by scaling the output of a temperature-stable bandgap circuit.

7.3.4 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the VSENSE pin. Using divider resistors with 1% tolerance or better is recommended. Begin with a value of 10 kΩ for the upper resistor divider, R1, and use Equation 1 to calculate the value of R2. Consider using larger value resistors to improve efficiency at light loads. If the values are too high then the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R2 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R1 \quad (1)$$

Feature Description (continued)

7.3.5 Enabling and Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the threshold voltage, the device begins operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters the low-quiescent (I_Q) state.

The EN pin has an internal pullup-current source which allows the user to float the EN pin to enable the device. If an application requires control of the EN pin, use open-drain or open-collector output logic to interface with the pin.

The device implements internal undervoltage-lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 180 mV.

If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown in Figure 15. When using the external UVLO function, setting the hysteresis at a value greater than 500 mV is recommended.

The EN pin has a small pullup-current, I_p, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h when the EN pin crosses the enable threshold. Use Equation 2, and Equation 3 to calculate the values of R1 and R2 for a specified UVLO threshold.

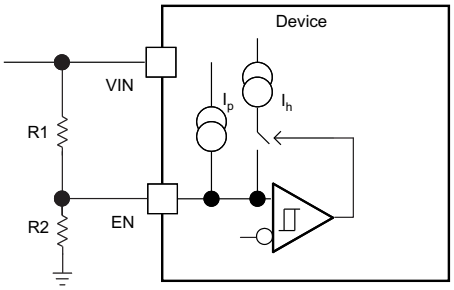


Figure 15. Adjustable VIN Undervoltage Lockout

$$R1 = \frac{V_{START}\left(\frac{V_{ENfalling}}{V_{ENrising}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENfalling}}{V_{ENrising}}\right) + I_h}$$

where

- I_P = 1.15 µA
- I_H = 3.3 µA
- $V_{ENfalling}$ = 1.17 V
- $V_{ENrising}$ = 1.21 V

(2)

$$R2 = \frac{R1 \times V_{ENfalling}}{V_{STOP} - V_{ENfalling} + R1(I_p + I_h)}$$

where

- I_P = 1.15 µA
- I_H = 3.3 µA
- $V_{ENfalling}$ = 1.17 V
- $V_{ENrising}$ = 1.21 V

(3)

Feature Description (continued)

7.3.6 Error Amplifier

The device has a transconductance amplifier as the error amplifier. The error amplifier compares the VSENSE voltage to the lower of the internal soft-start voltage or the internal 0.8-V voltage reference. The transconductance of the error amplifier is 1300 μA/V (typical). The frequency compensation components are placed between the COMP pin and ground.

7.3.7 Slope Compensation and Output Current

The device adds a compensating ramp to the signal of the switch current. This slope compensation prevents subharmonic oscillations as the duty cycle increases. The available peak inductor current remains constant over the full duty-cycle range.

7.3.8 Safe Startup into Pre-Biased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased startup, both high-side and low-side MOSFETs are not allowed to be turned on until the internal soft-start voltage is higher than VSENSE pin voltage.

7.3.9 Bootstrap Voltage (BOOT)

The device has an integrated boot regulator. The boot regulator requires a small ceramic capacitor between the BOOT and PH pins to provide the gate-drive voltage for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than the VIN voltage and when the BOOT-PH voltage is below regulation. The value of this ceramic capacitor should be 0.1 μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage. When the voltage between BOOT and PH pins drops below the BOOT-PH UVLO threshold, which is 2.1 V (typical), the high-side MOSFET turns off and the low-side MOSFET turns on, allowing the boot capacitor to recharge.

7.3.10 Output Overvoltage Protection (OVP)

The device incorporates an output overvoltage-protection (OVP) circuit to minimize output voltage overshoot. For example, when the power-supply output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. When the condition is removed, the regulator output rises and the error-amplifier output transitions to the steady-state voltage. In some applications with small output capacitance, the power-supply output voltage can respond faster than the error amplifier which leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the VSENSE pin voltage to the OVP threshold. If the VSENSE pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off which prevents current from flowing to the output and minimizes output overshoot. When the VSENSE voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

7.3.11 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

Feature Description (continued)

7.3.11.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the COMP pin voltage are compared. When the peak switch current intersects the current reference the high-side switch turns off.

7.3.11.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on, the conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current-limit. If the low-side sourcing current-limit is exceeded, the high-side MOSFET does not turn on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET turns on again when the low-side current is below the low-side sourcing current-limit at the start of a cycle.

The low-side MOSFET can also sink current from the load. If the low-side sinking current-limit is exceeded the low-side MOSFET turns off immediately for the remainder of that clock cycle. In this scenario, both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) occurs for more than the hiccup wait time, which is programmed for 512 switching cycles, the device shuts down and restarts after the hiccup time of 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

7.3.12 Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C typically. When the junction temperature drops below 165°C typically, the internal thermal-hiccup timer begins to count. The device reinitiates the power-up sequence after the built-in thermal-shutdown hiccup time (32768 cycles) is over.

7.3.13 Small-Signal Model for Loop Response

Figure 16 shows an equivalent model for the device control loop which can be modeled in a circuit-simulation program to check frequency and transient responses. The error amplifier is a transconductance amplifier with a gm of 1300 µA/V. The error amplifier can be modeled using an ideal voltage-controlled current source. The resistor, R_{oea} (3.07 MΩ), and capacitor, C_{oea} (20.7 pF), model the open-loop gain and frequency response of the error amplifier. The 1-mV AC-voltage source between the nodes ***a*** and ***b*** effectively breaks the control loop for the frequency response measurements. Plotting ***ac***-***c*** and ***c***-***b*** show the small-signal responses of the power stage and frequency compensation respectively. Plotting ***a***-***b*** shows the small-signal response of the overall loop. The dynamic loop response can be checked by replacing the load resistance, R_L, with a current source with the appropriate load-step amplitude and step rate in a time-domain analysis.

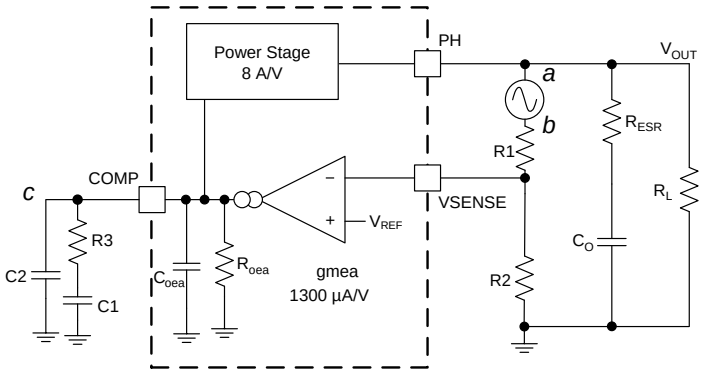


Figure 16. Small-Signal Model For Loop Response

Feature Description (continued)

7.3.14 Simple Small-Signal Model for Peak Current-Mode Control

Figure 17 is a simple small-signal model that can be used to understand how to design the frequency compensation. The device power stage can be approximated to a voltage-controlled current-source (duty-cycle modulator) supplying current to the output capacitor and load resistor. The control-to-output transfer function is shown in Equation 4 and consists of a DC gain, one dominant pole and one ESR zero. The quotient of the change in switch current and the change in the COMP pin voltage (node ***c*** in Figure 16) is the power-stage transconductance (gm_{ps}) which is 8 A/V for the device. The DC gain of the power stage is the product of gm_{ps} and the load resistance, R_L, with resistive loads as shown in Equation 5. As the load current increases, the DC gain decreases. This variation with load may seem problematic at first glance, but fortunately the dominant pole moves with the load current (see Equation 6). The combined effect is highlighted by the dashed line in Figure 18. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes designing the frequency compensation easier.

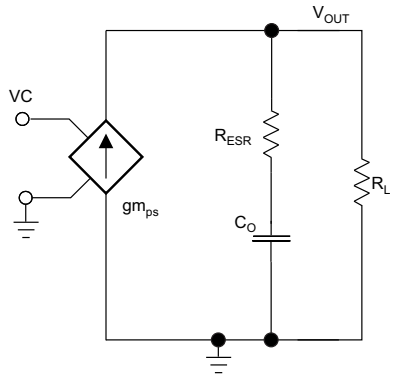


Figure 17. Simplified Small-Signal Model for Peak Current-Mode Control

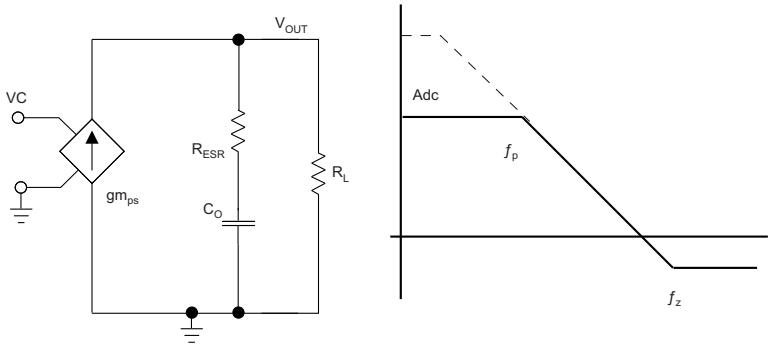


Figure 18. Simplified Frequency Response for Peak Current-Mode Control

Feature Description (continued)

$$\frac{V_{OUT}}{VC} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times f_z}\right)}{\left(1 + \frac{s}{2\pi \times f_p}\right)} \quad (4)$$

$$Adc = gm_{ps} \times R_L$$

where

- gm_{ps} is the power stage gain (8 A/V)
- R_L is the load resistance (5)

$$f_p = \frac{1}{C_O \times R_L \times 2\pi}$$

where

- C_O is the output capacitance (6)

$$f_z = \frac{1}{C_O \times R_{ESR} \times 2\pi}$$

where

- R_{ESR} is the equivalent series resistance of the output capacitor (7)

7.3.15 Small-Signal Model for Frequency Compensation

The device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used Type II compensation circuits and a Type III frequency compensation circuit, as shown in Figure 19. In Type 2A, one additional high frequency pole, C6, is added to attenuate high frequency noise. In Type III, one additional capacitor, C11, is added to provide a phase boost at the crossover frequency. See *Designing Type III Compensation for Current Mode Step-Down Converters* (SLVA352) for a complete explanation of Type III compensation.

The following design guidelines are provided for advanced users who prefer to compensate using the general method. The following equations only apply to designs whose ESR zero is above the bandwidth of the control loop which is usually true with ceramic output capacitors.

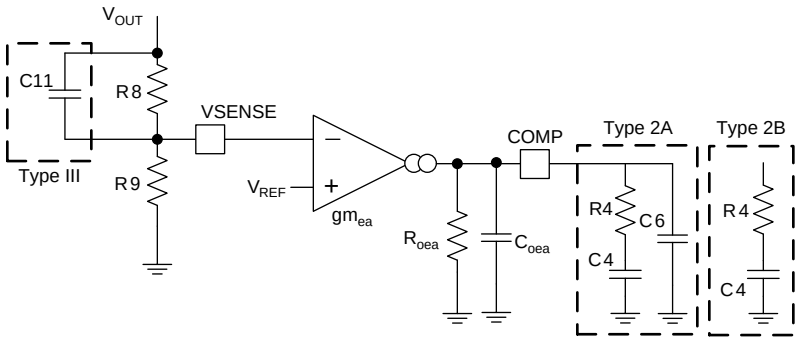


Figure 19. Types of Frequency Compensation

Feature Description (continued)

The general design guidelines for device loop compensation are as follows:

1. Determine the crossover frequency, f_c. A good starting value for f_c is 1/10th of the switching frequency, f_{SW}.
2. Use Equation 8 to calculate the value of R4.

$$R4 = \frac{2\pi \times f_c \times V_{OUT} \times C_O}{gm_{ea} \times V_{REF} \times gm_{ps}} \quad (8)$$

where

- gm_{ea} is the GM amplifier gain (1300 μA/V)
- gm_{ps} is the power stage gain (8 A/V)
- V_{REF} is the reference voltage (0.8 V)

3. Place a compensation zero at the dominant pole and use Equation 9 to calculate the value of f_p.

$$\left(f_p = \frac{1}{C_O \times R_L \times 2\pi} \right) \quad (9)$$

4. Use Equation 10 to calculate the value of C4.

$$C4 = \frac{R_L \times C_O}{R4} \quad (10)$$

5. The use of C6 is optional. C6 can be used to cancel the zero from the ESR (equivalent series resistance) of the output capacitor C_O. If used, use Equation 11 to calculate the value of C6.

$$C6 = \frac{R_{ESR} \times C_O}{R4} \quad (11)$$

6. Type III compensation can be implemented with the addition of one capacitor, C11. The use of C11 allows for slightly higher loop bandwidths and higher phase margins. If used, use Equation 12 to calculate the value of C11.

$$C11 = \frac{1}{(2 \times \pi \times R8 \times f_C)} \quad (12)$$

7.4 Device Functional Modes

7.4.1 Operation With V_I < 4.5 V (minimum V_I)

The device is designed to operate with input voltages above 4.5 V. The typical VIN UVLO threshold is 4V and if VIN falls below this threshold the device stops switching. If the EN pin voltage is above EN threshold the device becomes active when the VIN pin passes the UVLO threshold. .

7.4.2 Operation With EN Control

The enable threshold is 1.2-V typical. If the EN pin voltage is below this threshold the device does not switch even though the Vin is above the UVLO threshold. The IC quiescent current is reduced in this state. Once the EN is above the threshold with VIN above UVLO threshold the device is active again and the soft-start sequence is initiated.

7.4.3 Operation With EN Control

The enable threshold is 1.2-V typical. If the EN pin voltage is below this threshold the device does not switch even though the V_{IN} is above the UVLO threshold. The device's quiescent current is reduced in this state. Once the EN is above the threshold with VIN above UVLO threshold the device is active again and the soft-start sequence is initiated.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS54335-2A family of devices are step-down DC-DC converters. The devices are typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 3 A. Use the following design procedure to select component values for each device. Alternately, use the WEBENCH software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.1.1 Supplementary Guidance

The device must operate within 150°C to ensure continuous function and operation of the device.

8.1.2 The DRC Package

The TPS54335-2A device is packaged in the a 3-mm × 3-mm SON package which is designated as DRC (see the *Mechanical, Packaging, and Orderable Information* section for all package options).

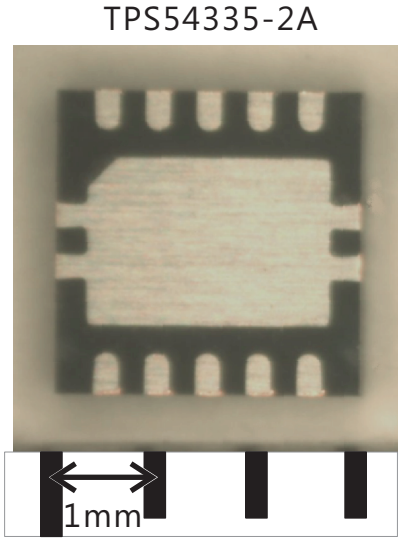


Figure 20. TPS54335-2A DRC Package

8.2 Typical Applications

TPS54335-2A typical application.

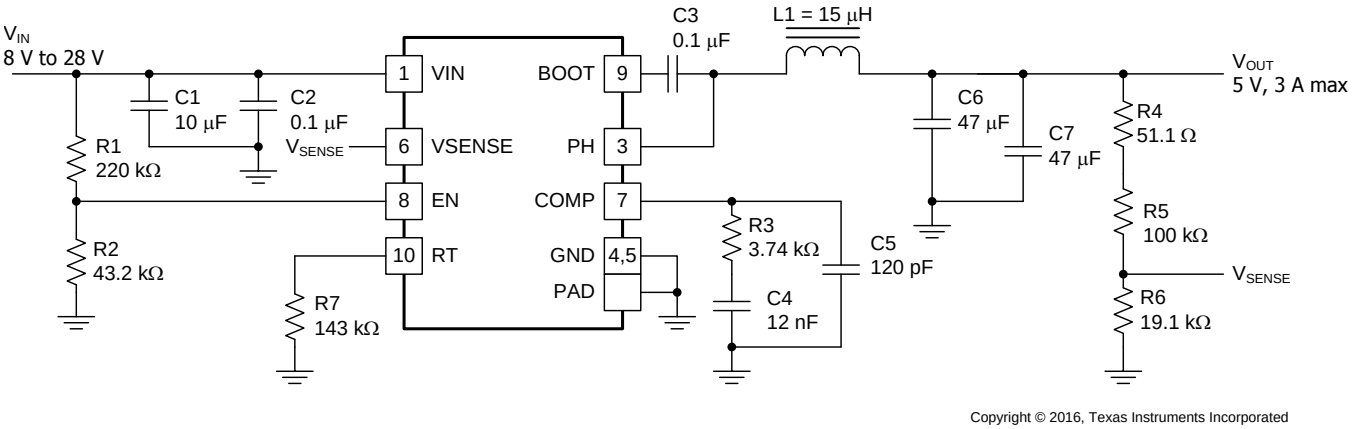


Figure 21. Typical Application Schematic, TPS54335-2A

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8 to 28 V
Output voltage	5 V
Transient response, 1.5-A load step	ΔV_O = ±5 %
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	3 A
Operating Frequency	340 kHz

8.2.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS54335-2A device. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process using the TPS54335-2A device.

For this design example, use the input parameters listed in Table 1.

8.2.2.1 Switching Frequency

Use to calculate the required value for R7. The calculated value is 140.6 kΩ. Use the next higher standard value of 143 kΩ for R7.

8.2.2.2 Output Voltage Set Point

The output voltage of the TPS54335-2A device is externally adjustable using a resistor divider network. In the application circuit of , this divider network is comprised of R5 and R6. Use Equation 13 and Equation 14 to calculate the relationship of the output voltage to the resistor divider.

$$R6 = \frac{R5 \times V_{ref}}{V_{OUT} - V_{ref}} \tag{13}$$

$$V_{OUT} = V_{ref} \times \left[\frac{R5}{R6} + 1\right] \tag{14}$$

Select a value of R5 to be approximately 100 kΩ. Slightly increasing or decreasing R5 can result in closer output-voltage matching when using standard value resistors. In this design, R5 = 100 kΩ and R6 = 19.1 kΩ which results in a 4.988-V output voltage. The 51.1-Ω resistor, R4, is provided as a convenient location to break the control loop for stability testing.

8.2.2.3 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) set point can be adjusted using the external-voltage divider network of R1 and R2. R1 is connected between the VIN and EN pins of the TPS54335-2A device. R2 is connected between the EN and GND pins. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the minimum input voltage is 8 V, so the start-voltage threshold is set to 7.15 V with 1-V hysteresis. Use Equation 2 and Equation 3 to calculate the values for the upper and lower resistor values of R1 and R2.

8.2.2.4 Input Capacitors

The TPS54335-2A device requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The typical recommended value for the decoupling capacitor is 10 μF. A high-quality ceramic type X5R or X7R is recommended. The voltage rating should be greater than the maximum input voltage. A smaller value can be used as long as all other requirements are met; however a 10-μF capacitor has been shown to work well in a wide variety of circuits. Additionally, some bulk capacitance may be needed, especially if the TPS54335-2A circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but should be rated to handle the maximum input voltage including ripple voltage, and should filter the output so that input ripple voltage is acceptable. For this design, a 10-μF, X7R dielectric capacitor rated for 35 V is used for the input decoupling capacitor. The ESR is approximately 2 mΩ, and the current rating is 3 A. Additionally, a small 0.1-μF capacitor is included for high frequency filtering.

Use Equation 15 to calculate the input ripple voltage (ΔV_{IN}).

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{SW}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \quad (15)$$

where

- C_{BULK} is the bulk capacitor value
- f_{SW} is the switching frequency
- $I_{OUT(MAX)}$ is the maximum load current
- ESR_{MAX} is the maximum series resistance of the bulk capacitor

The maximum RMS (root mean square) ripple current must also be checked. For worst case conditions, use Equation 16 to calculate $I_{CIN(RMS)}$.

$$I_{CIN(RMS)} = \frac{I_{O(MAX)}}{2} \quad (16)$$

In this case, the input ripple voltage is 227 mV and the RMS ripple current is 1.5 A.

NOTE

The actual input-voltage ripple is greatly affected by parasitics associated with the layout and the output impedance of the voltage source.

The *Design Requirements* section shows the actual input voltage ripple for this circuit which is larger than the calculated value. This measured value is still below the specified input limit of 400 mV. The maximum voltage across the input capacitors is $V_{IN(MAX)} + \Delta V_{IN} / 2$. The selected bypass capacitor is rated for 35 V and the ripple current capacity is greater than 3 A. Both values provide ample margin. The maximum ratings for voltage and current must not be exceeded under any circumstance.

8.2.2.5 Output Filter Components

Two components must be selected for the output filter, the output inductor (L_O) and C_O. Because the TPS54335-2A device is an externally compensated device, a wide range of filter component types and values can be supported.

8.2.2.5.1 Inductor Selection

Use Equation 17 to calculate the minimum value of the output inductor (L_{MIN}).

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (17)$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current

In general, the value of K_{IND} is at the discretion of the designer; however, the following guidelines may be used. For designs using low-ESR output capacitors, such as ceramics, a value as high as K_{IND} = 0.3 can be used. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results.

For this design example, use K_{IND} = 0.3. The minimum inductor value is calculated as 13.4 µH. For this design, a close standard value of 15 µH was selected for L_{MIN}.

For the output filter inductor, the RMS current and saturation current ratings must not be exceeded. Use Equation 18 to calculate the RMS inductor current ($I_{L(RMS)}$).

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times f_{SW} \times 0.8} \right)^2} \quad (18)$$

Use Equation 19 to calculate the peak inductor current ($I_{L(PK)}$).

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times f_{SW}} \quad (19)$$

For this design, the RMS inductor current is 3.002 A and the peak inductor current is 3.503 A. The selected inductor is a Coilcraft 15 µH, XAL6060-153MEB. This inductor has a saturation current rating of 5.8 A and an RMS current rating of 6 A which meets the requirements. Smaller or larger inductor values can be used depending on the amount of ripple current the designer wants to allow so long as the other design requirements are met. Larger value inductors have lower AC current and result in lower output voltage ripple. Smaller inductor values increase AC current and output voltage ripple. In general, for the TPS54335-2A device, use inductors with values in the range of 0.68 µH to 100 µH.

8.2.2.5.2 Capacitor Selection

Consider three primary factors when selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation occurs if the desired hold-up times are present for the regulator. In this case, the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily unable to supply sufficient output current if a large, fast increase occurs affecting the current requirements of the load, such as a transition from no load to full load. The regulator usually requires two or more clock cycles for the control loop to notice the change in load current and output voltage and to adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of drop in the output voltage. Use Equation 20 to calculate the minimum required output capacitance.

$$C_O > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}}$$

where

- ΔI_{OUT} is the change in output current
- f_{SW} is the switching frequency of the regulator
- ΔV_{OUT} is the allowable change in the output voltage

(20)

For this example, the transient load response is specified as a 5% change in the output voltage, V_{OUT}, for a load step of 1.5 A. For this example, ΔI_{OUT} = 1.5 A and ΔV_{OUT} = 0.05 × 5 = 0.25 V. Using these values results in a minimum capacitance of 35.3 µF. This value does not consider the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 21 calculates the minimum output capacitance required to meet the output voltage ripple specification. In this case, the maximum output voltage ripple is 30 mV. Under this requirement, Equation 21 yields 12.3 µF.

$$C_O > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{OUTripple}}{I_{ripple}}}$$

where

- f_{SW} is the switching frequency
- $V_{OUTripple}$ is the maximum allowable output voltage ripple
- I_{ripple} is the inductor ripple current

(21)

Use Equation 22 to calculate the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. Equation 22 indicates the ESR should be less than 29.8 mΩ. In this case, the ESR of the ceramic capacitor is much smaller than 29.8 mΩ.

$$R_{ESR} < \frac{V_{OUTripple}}{I_{ripple}}$$

(22)

Additional capacitance deratings for aging, temperature, and DC bias should be considered which increases this minimum value. For this example, two 47-µF 10-V X5R ceramic capacitors with 3 mΩ of ESR are used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS value of the maximum ripple current. Use Equation 23 to calculate the RMS ripple current that the output capacitor must support. For this application, Equation 23 yields 116.2 mA for each capacitor.

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT} \right)}{V_{IN(MAX)} \times L_{OUT} \times f_{SW} \times N_C} \right)$$

(23)

8.2.2.6 Compensation Components

Several possible methods exist to design closed loop compensation for DC-DC converters. For the ideal current-mode control, the design equations can be easily simplified. The power stage gain is constant at low frequencies, and rolls off at –20 dB/decade above the modulator pole frequency. The power stage phase is 0 degrees at low frequencies and begins to fall one decade below the modulator pole frequency reaching a minimum of –90 degrees which is one decade above the modulator pole frequency. Use Equation 24 to calculate the simple modulator pole (f_{p_mod}).

$$f_{p\_mod} = \frac{I_{OUT}\,max}{2\pi \times V_{OUT} \times C_{OUT}} \tag{24}$$

For the TPS54335-2A device, most circuits have relatively high amounts of slope compensation. As more slope compensation is applied, the power stage characteristics deviate from the ideal approximations. The phase loss of the power stage will now approach –180 degrees, making compensation more difficult. The power stage transfer function can be solved but it requires a tedious calculation. Use the PSpice model to accurately model the power-stage gain and phase so that a reliable compensation circuit can be designed. Alternately, a direct measurement of the power stage characteristics can be used which is the technique used in this design procedure. For this design, the calculated values are as follows:

L1 = 15 µH

C6 and C7 = 47 µF

ESR = 3 mΩ

Figure 22 shows the power stage characteristics.

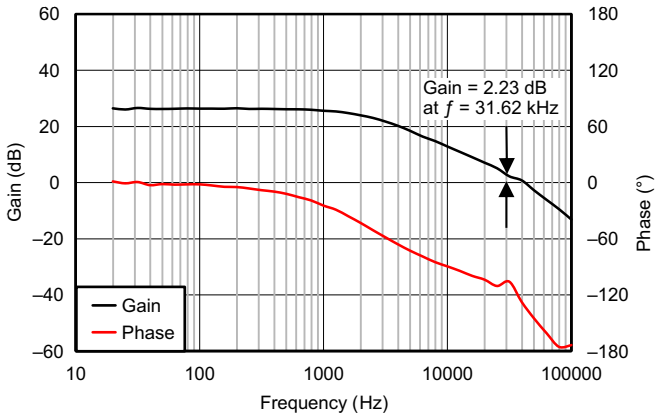


Figure 22. Power Stage Gain and Phase Characteristics

For this design, the intended crossover frequency is 31.62 kHz (an actual measured data point exists for that frequency). From the power stage gain and phase plots, the gain at 31.62 kHz is 2.23 dB and the phase is about -106 degrees. For 60 degrees of phase margin, additional phase boost from a feed-forward capacitor in parallel with the upper resistor of the voltage set point divider is not needed. R3 sets the gain of the compensated error amplifier to be equal and opposite the power stage gain at crossover. Use Equation 25 to calculate the required value of R3.

$$R3 = \frac{10^{\frac{-G_{PWRSTG}}{20}}}{gm_{ea}} \times \frac{V_{OUT}}{V_{REF}} \quad (25)$$

To maximize phase gain, the compensator zero is placed one decade below the crossover frequency of 31.62 kHz. Use Equation 26 to calculate the required value for C4.

$$C4 = \frac{1}{2 \times \pi \times R3 \times \frac{f_{CO}}{10}} \quad (26)$$

To maximize phase gain the high frequency pole is placed one decade above the crossover frequency of 31.62 kHz. The pole can also be useful to offset the ESR of aluminum electrolytic output capacitors. Use Equation 27 to calculate the value of C5.

$$C5 = \frac{1}{2 \times \pi \times R3 \times 10 \times f_{CO}} \quad (27)$$

For this design the calculated values for the compensation components are as follows:

R3 = 3.74 kΩ
C4 = 0.012 µF
C5 = 120 pF

8.2.2.7 Bootstrap Capacitor

Every TPS54335-2A design requires a bootstrap capacitor, C3. The bootstrap capacitor value must 0.1 μF. The bootstrap capacitor is located between the PH and BOOT pins. The bootstrap capacitor should be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

8.2.2.8 Power Dissipation Estimate

The following formulas show how to estimate the device power dissipation under continuous-conduction mode operations. These formulas should not be used if the device is working in the discontinuous conduction mode (DCM) or pulse-skipping Eco-mode™.

The device power dissipation includes:

1. Conduction loss:

$$P_{CON} = I_{OUT}^2 \times r_{DS(on)} \times V_{OUT} / V_{IN}$$

where

- I_{OUT} is the output current (A)
- $r_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω)
- V_{OUT} is the output voltage (V)
- V_{IN} is the input voltage (V)

(28)

2. Switching loss:

$$E = 0.5 \times 10^{-9} \times V_{IN}^2 \times I_{OUT} \times f_{SW}$$

where

- f_{SW} is the switching frequency (Hz)

(29)

3. Gate charge loss:

$$P_G = 22.8 \times 10^{-9} \times f_{SW} \quad (30)$$

4. Quiescent current loss:

$$P_Q = 0.11 \times 10^{-3} \times V_{IN} \quad (31)$$

Therefore:

$$P_{tot} = P_{CON} + E + P_G + P_Q$$

where

- P_{tot} is the total device power dissipation (W)

(32)

For given T_A :

$$T_J = T_A + R_{th} \times P_{tot}$$

where

- T_A is the ambient temperature (°C)
- T_J is the junction temperature (°C)
- R_{th} is the thermal resistance of the package (°C/W)

(33)

For given T_J = 150°C:

$$T_A max = T_J max - R_{th} \times P_{tot}$$

where

- $T_A max$ is the maximum ambient temperature (°C)
- $T_J max$ is the maximum junction temperature (°C)

(34)

8.2.3 Application Curves

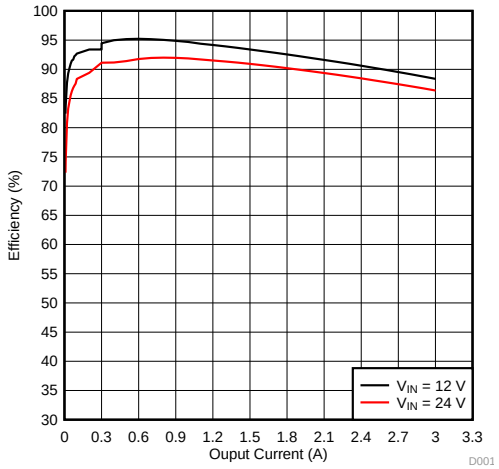


Figure 23. TPS54335-2A Efficiency

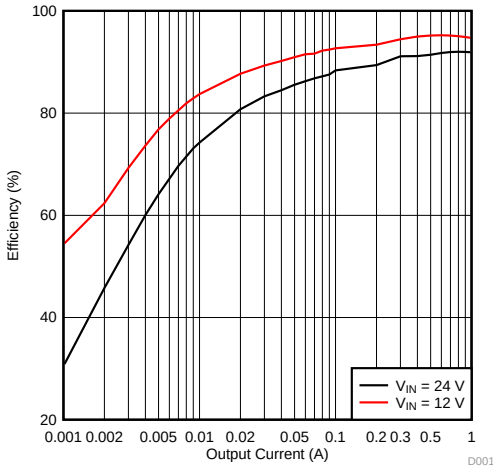


Figure 24. TPS54335-2A Low-Current Efficiency

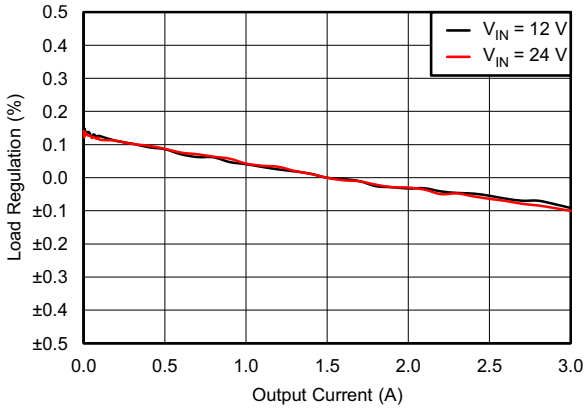


Figure 25. TPS54335-2A Load Regulation

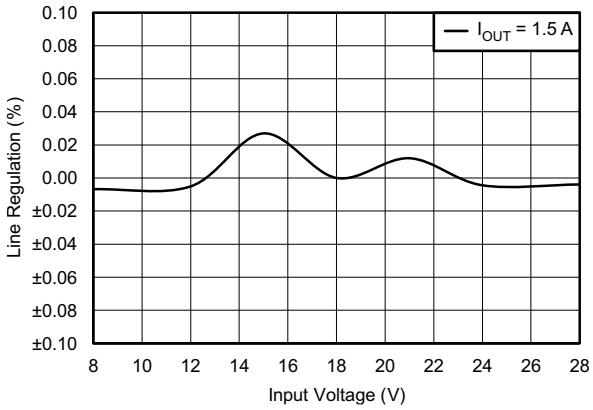


Figure 26. TPS54335-2A Line Regulation

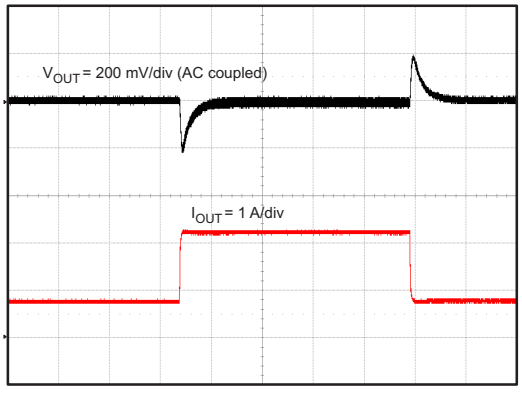


Figure 27. TPS54335-2A Transient Response

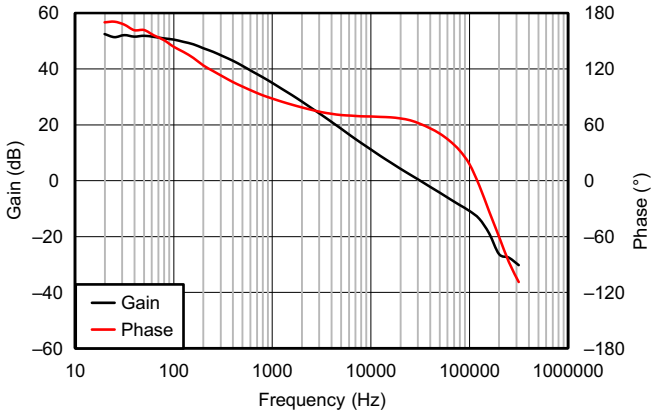


Figure 28. TPS54335-2A Loop Response

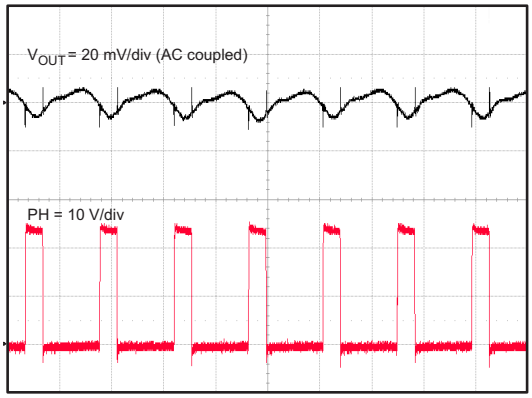


Figure 29. TPS54335-2A Full-Load Output Ripple

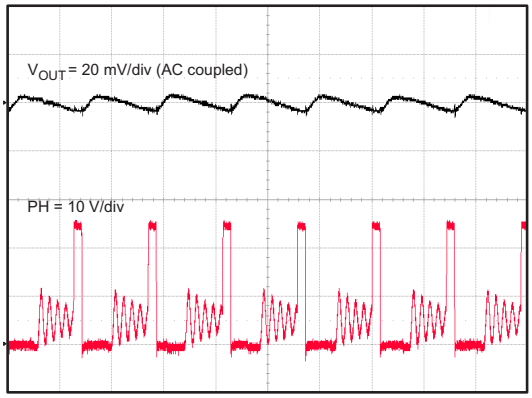


Figure 30. TPS54335-2A 100-mA Output Ripple

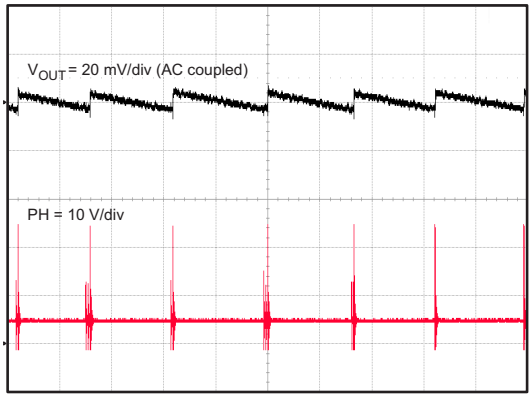


Figure 31. TPS54335-2A No-Load Output Ripple

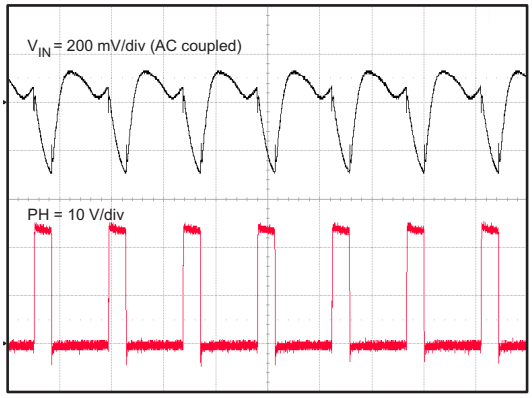


Figure 32. TPS54335-2A Full-Load Input Ripple

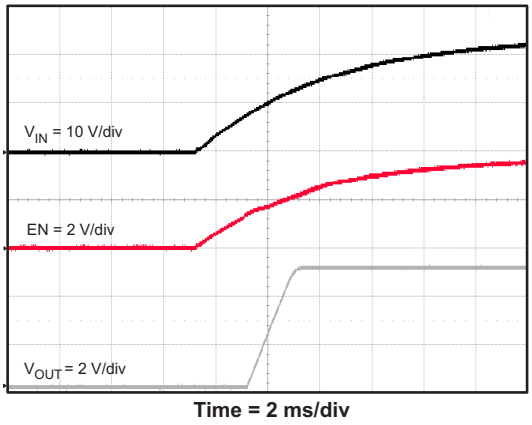


Figure 33. TPS54335-2A Startup Relative To VIN

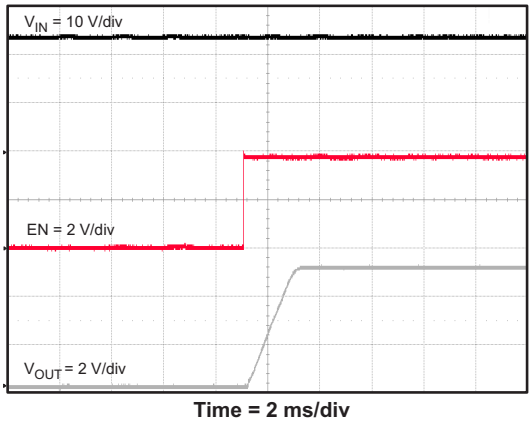


Figure 34. TPS54335-2A Startup Relative To Enable

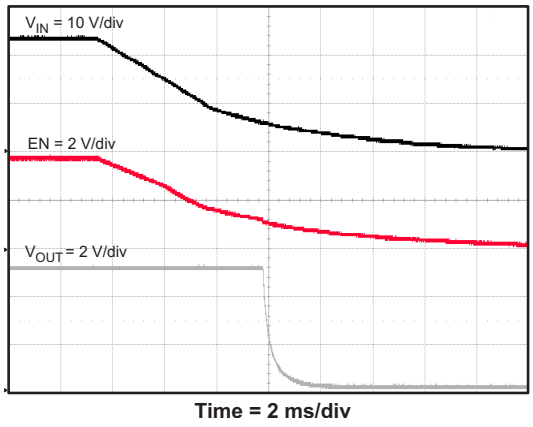


Figure 35. TPS54335-2A Shutdown Relative To VIN

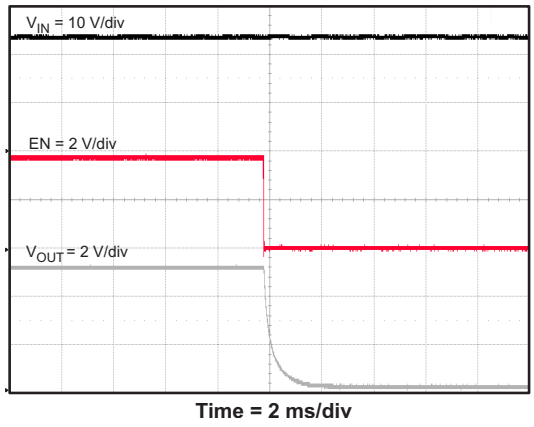


Figure 36. TPS54335-2A Shutdown Relative To EN

9 Power Supply Recommendations

The devices are designed to operate from an input supply ranging from 4.5 V to 28 V. The input supply should be well regulated. If the input supply is located more than a few inches from the converter an additional bulk capacitance typically 100 µF may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

The VIN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connection, the VIN pin, and the GND pin of the IC. The typical recommended bypass capacitance is 10-μF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN and GND pins of the device. See Figure 37 for a PCB layout example. The GND pin should be tied to the PCB ground plane at the pin of the IC. To facilitate close placement of the input bypass capacitors, the PH pin should be routed to a small copper area directly adjacent to the pin. Use vias to route the PH signal to the bottom side or an inner layer. If necessary, allow the top-side copper area to extend slightly under the body of the closest input bypass capacitor. Make the copper trace on the bottom or internal layer short and wide as practical to reduce EMI issues. Connect the trace with vias back to the top side to connect with the output inductor as shown after the GND pin. In the same way use a bottom or internal layer trace to route the PH signal across the VIN pin to connect to the boot capacitor as shown. Make the circulating loop from the PH pin to the output inductor and output capacitors and then back to GND as tight as possible while preserving adequate etch width to reduce conduction losses in the copper . For operation at a full rated load, the ground area near the IC must provide adequate heat dissipating area. Connect the exposed thermal pad to the bottom or internal layer ground plane using vias as shown. Additional vias may be used adjacent to the IC to tie top-side copper to the internal or bottom layer copper. The additional external components can be placed approximately as shown. Use a separate ground trace to connect the feedback, compensation, UVLO, and RT returns. Connect this ground trace to the main power ground at a single point to minimize circulating currents. Obtaining acceptable performance with alternate layout schemes is possible; however this layout has been shown to produce good results and is intended as a guideline.

10.2 Layout Example

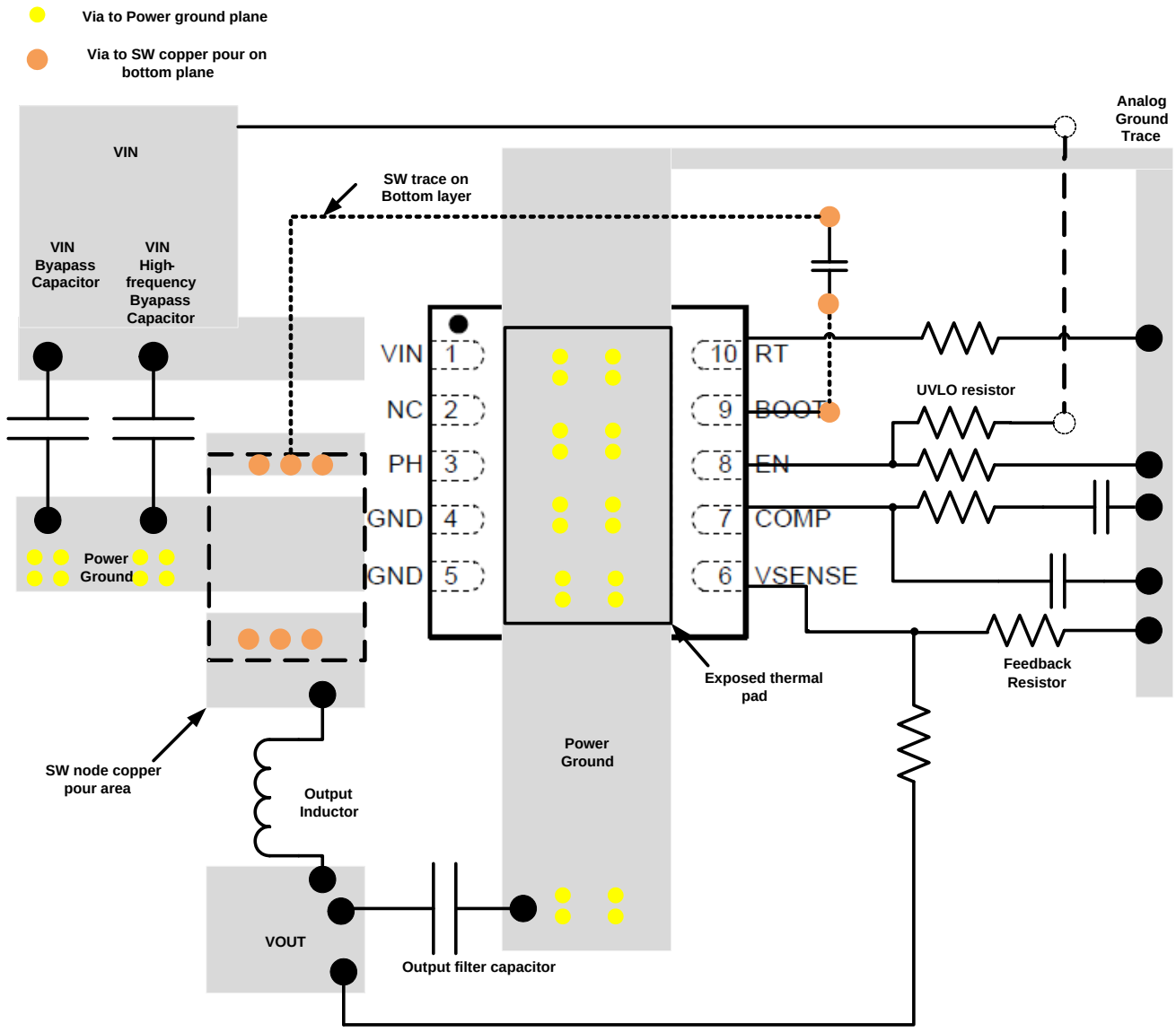


Figure 37. TPS54335-2ADRC Board Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For the WEBENCH circuit design and selection simulation services, go to www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Designing Type III Compensation for Current Mode Step-Down Converters (SLVA352)

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

Eco-mode, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54335-2ADRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	543352	Samples
TPS54335-2ADRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	543352	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

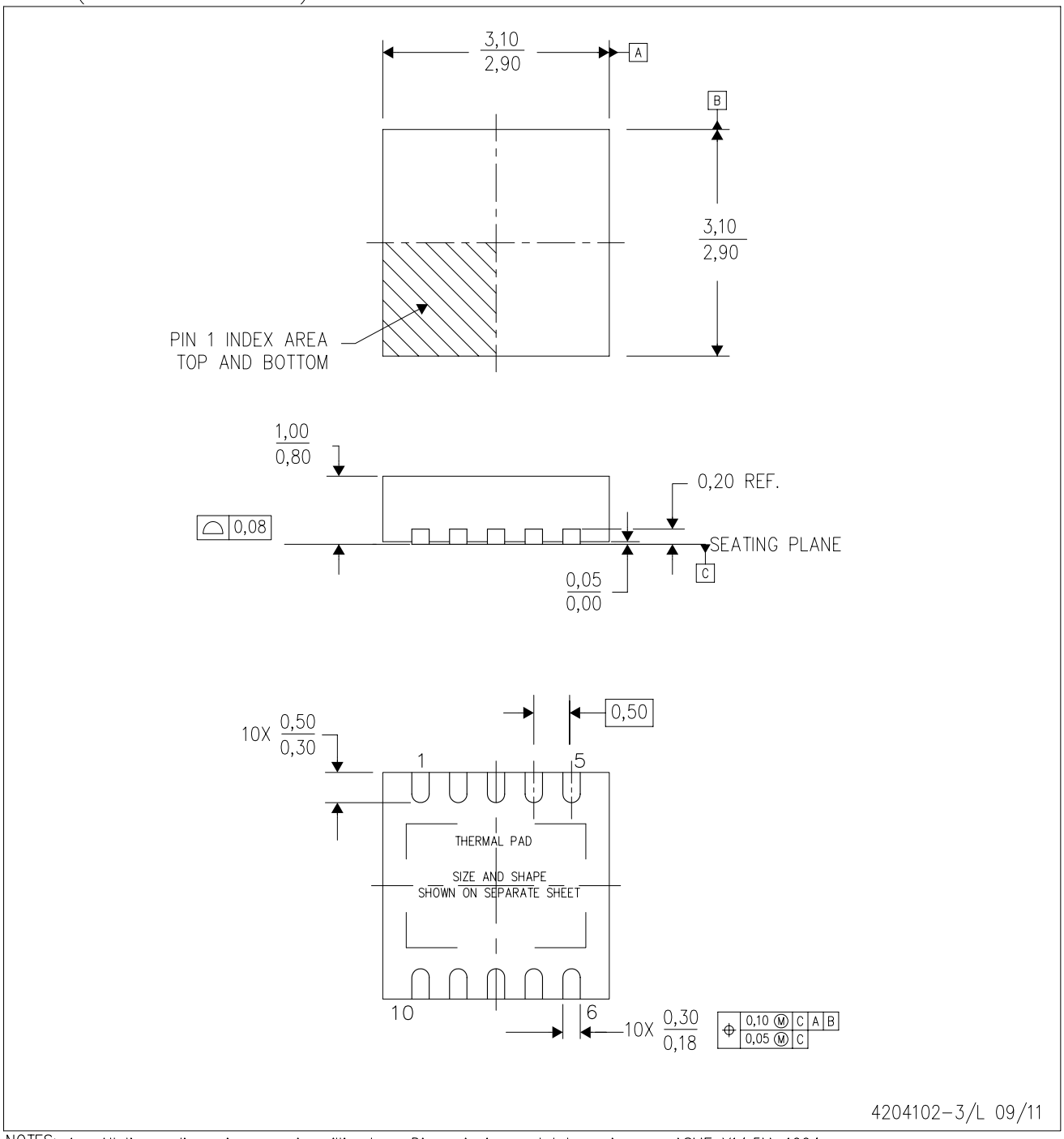
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

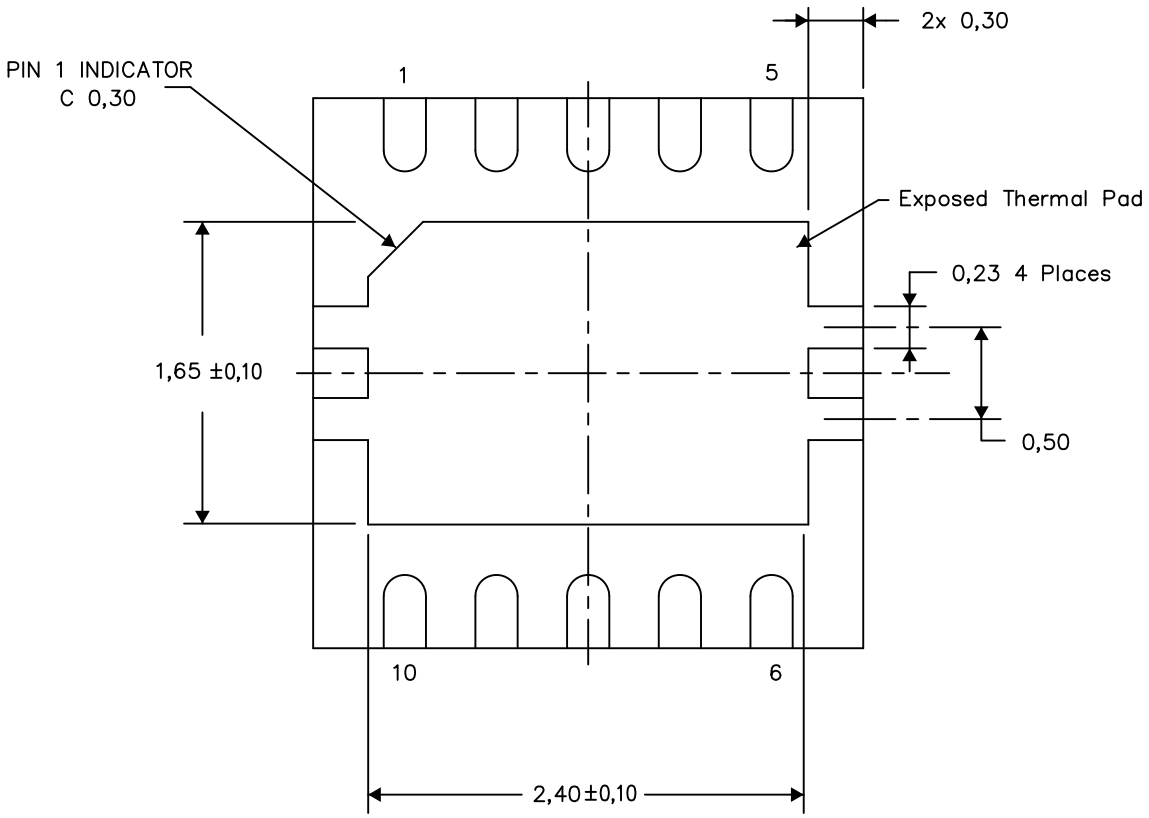
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



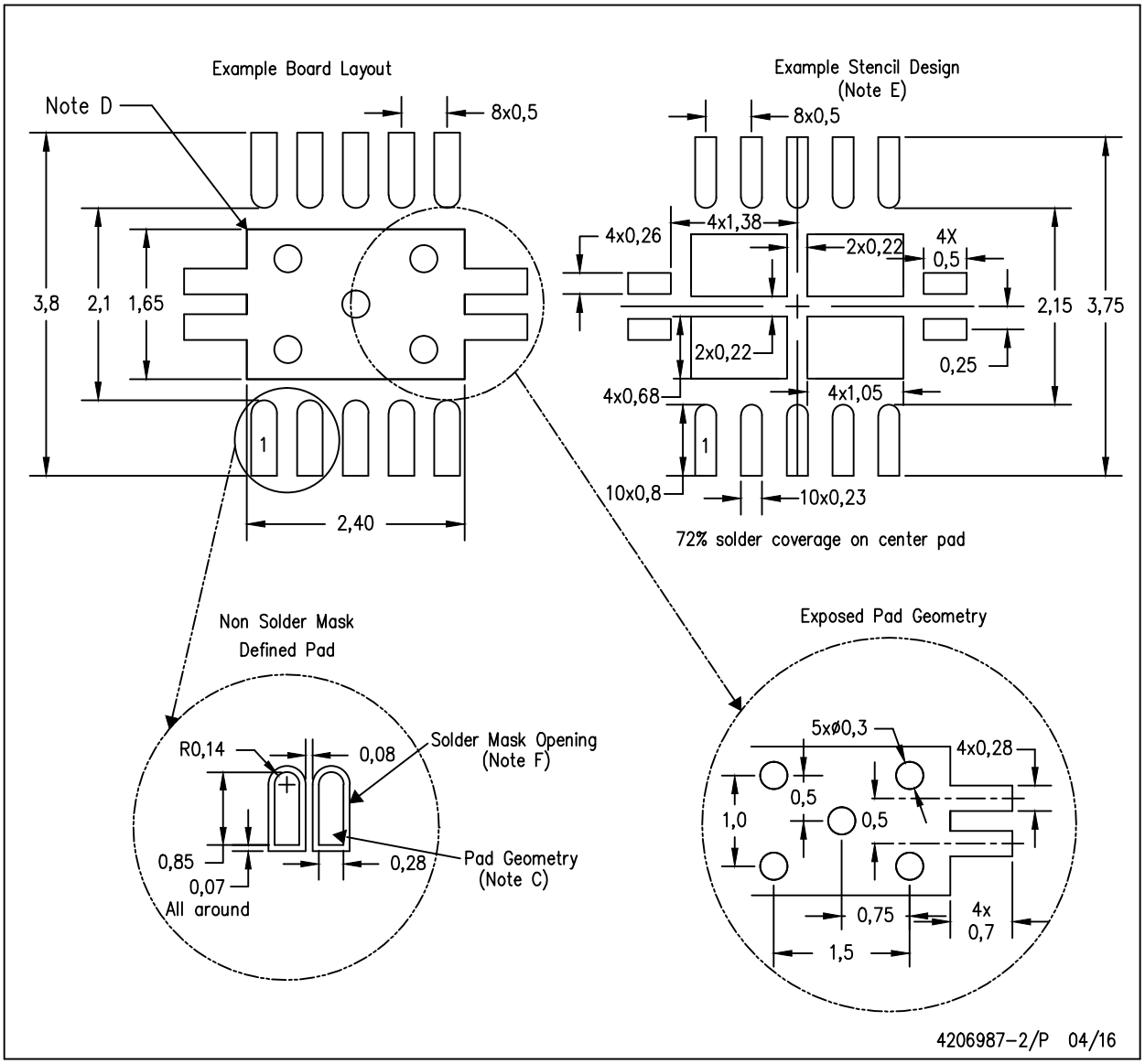
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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