

DUAL SYNCHRONOUS STEP-DOWN CONTROLLER FOR LOW VOLTAGE POWER RAILS

Check for Samples: [TPS53129](#)

FEATURES

- **D-CAP2™ Mode Control**
 - Fast Transient Response
 - No External Parts Required for Loop Compensation
 - Compatible With Ceramic Output Capacitors
- High Initial Reference Accuracy ($\pm 1\%$)
- Low Output Ripple
- Wide Input Voltage Range: 4.5 V to 24 V
- Output Voltage Range: 0.76 V to 5.5 V
- Low-Side $R_{DS(ON)}$ Loss-Less Current Sensing
- Adaptive Gate Drivers with Integrated Boost Diode
- Adjustable Soft Start
- Non-Sinking Pre-Biased Soft Start

- 700-kHz Switching Frequency
- Cycle-by-Cycle Over-Current Limiting Control
- 30-mV to 300-mV OCP Threshold Voltage
- Thermally Compensated OCP by 4000 ppm/°C at I_{TRIP}

APPLICATIONS

- Point-of-Load Regulation in Low Power Systems for Wide Range of Applications
 - Digital TV Power Supply
 - Networking Home Terminal
 - Digital Set-Top Box (STB)
 - DVD Player/Recorder
 - Gaming Consoles

DESCRIPTION

The TPS53129 is a dual, adaptive on-time D-CAP2™ mode synchronous buck controller. The TPS53129 enables system designers to complete the suite of various end equipment's power bus regulators with cost effective, low component count, and low standby current solution. The main control loop for the TPS53129 uses the D-CAP2™ mode control which provides a very fast transient response with no external components. The TPS53129 also has a circuit that enables the device to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR, ceramic capacitors. The fixed frequency emulated adaptive on-time control supports seamless operation between PWM mode at heavy load condition and reduced frequency operation at light load for high efficiency down to milliampere range. The device provides convenient and efficient operation with input voltages from 4.5 V to 24 V and output voltages from 0.76 V to 5.5 V.

The TPS53129 is available in 4-mm x 4-mm 24-pin QFN (RGE) or 24-pin TSSOP (PW) packages, and is specified from -40°C to 85°C ambient temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

D-CAP2 is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2009–2010, Texas Instruments Incorporated

TYPICAL APPLICATION CIRCUITS

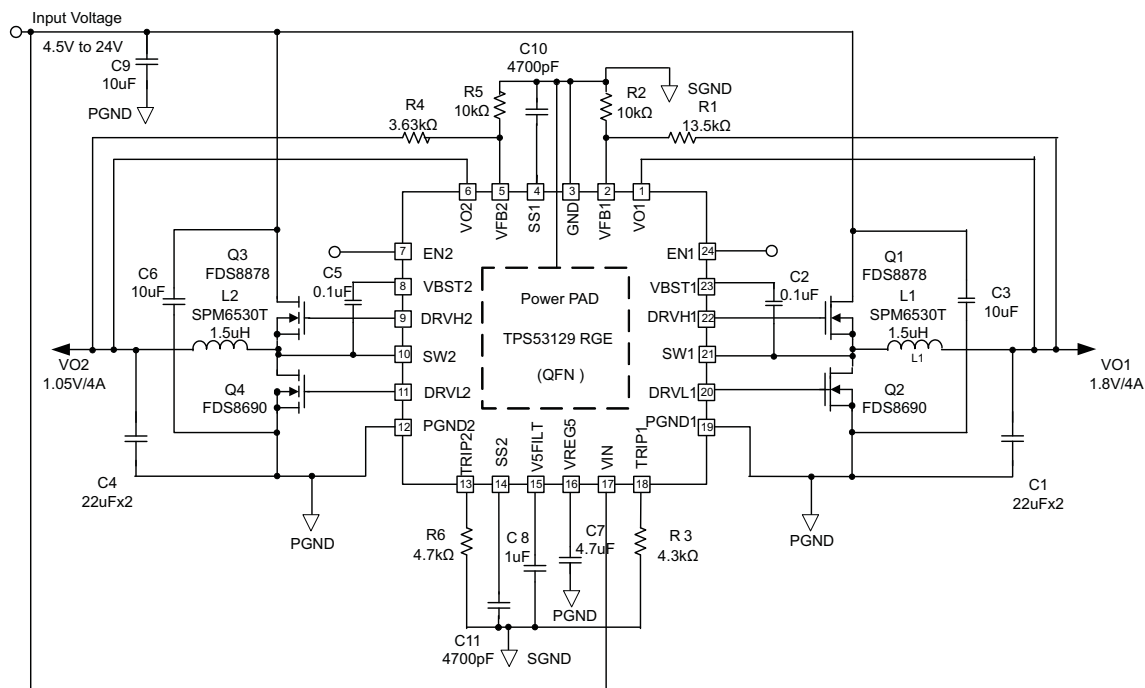


Figure 1. QFN

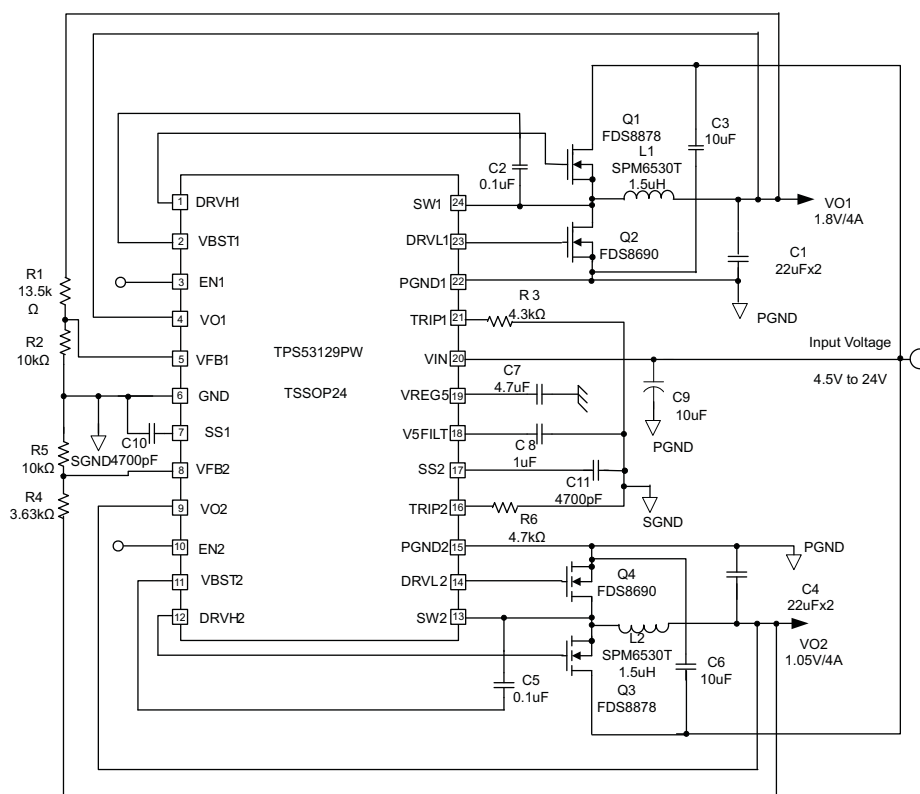


Figure 2. TSSOP

ORDERING INFORMATION⁽¹⁾

| T _A | PACKAGE ^{(2) (3)} | ORDERING PART NUMBER | PINS | OUTPUT SUPPLY | ECO PLAN |
|----------------|------------------------------|----------------------|------|---------------|------------------------------|
| –40°C to 85°C | Plastic Quad Flat Pack (QFN) | TPS53129RGET | 24 | Tape-and-Reel | Green (RoHS and no Sb/Br) |
| | | TPS53129RGER | | Tape-and-Reel | |
| | TSSOP | TPS53129PWR | | Tape-and-Reel | |
| | | TPS53129PW | | Tube | |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) All packaging options have Cu NIPDAU lead/ball finish.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | VALUE | UNIT |
|------------------|-------------------------------------|--|-------------|
| V _I | Input voltage range | VIN, EN1, EN2 | –0.3 to 26 |
| | | VBST1, VBST2 | –0.3 to 32 |
| | | VBST1 - SW1, VBST2 - SW2 | –0.3 to 6 |
| | | V5FILT, VFB1, VFB2, TRIP1, TRIP2, VO1, VO2 | –0.3 to 6 |
| | | SW1, SW2 | –2 to 26 |
| V _O | Output voltage range | DRVH1, DRVH2 | –1 to 32 |
| | | DRVH1 - SW1, DRVH2 - SW2 | –0.3 to 6 |
| | | DRVL1, DRVL2, VREG5, SS1, SS2 | –0.3 to 6 |
| | | PGND1, PGND2 | –0.3 to 0.3 |
| T _A | Operating ambient temperature range | –40 to 85 | °C |
| T _{STG} | Storage temperature range | –55 to 150 | °C |
| T _J | Junction temperature range | –40 to 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

2-oz. trace and copper pad with solder

| PACKAGE | T _A < 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 85°C POWER RATING |
|--------------|---------------------------------------|--|---------------------------------------|
| 24-pin QFN | 2.33 W | 23.3 mW/°C | 0.93 W |
| 24-pin TSSOP | 0.778 W | 7.8 mW/°C | 0.31 W |

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|-----------------|----------------------|--------------------------|------|-----|------|
| V _{IN} | Supply input voltage | VIN | 4.5 | 24 | V |
| | | V5FILT | 4.5 | 5.5 | |
| V _I | Input voltage | VBST1, VBST2 | –0.1 | 30 | V |
| | | VBST1 - SW1, VBST2 - SW2 | –0.1 | 5.5 | |
| | | VFB1, VFB2, VO1, VO2 | –0.1 | 5.5 | |
| | | TRIP1, TRIP2 | –0.1 | 0.3 | |
| | | EN1, EN2 | –0.1 | 24 | |
| | | SW1, SW2 | –1.8 | 24 | |

RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|----------------|--------------------------------|-------------------------------|------|-----|------|
| V _O | Output voltage | DRVH1, DRVH2 | −0.1 | 30 | V |
| | | VBST1 - SW1, VBST2 - SW2 | −0.1 | 5.5 | |
| | | DRVL1, DRVL2, VREG5, SS1, SS2 | −0.1 | 5.5 | |
| | | PGND1, PGND2 | −0.1 | 0.1 | |
| T _A | Operating free-air temperature | | −40 | 85 | °C |
| T _J | Operating junction temperature | | −40 | 125 | °C |

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|-------------------------------------|---|-------|-----|-------|------|
| SUPPLY CURRENT | | | | | | |
| I _{IN} | VIN supply current | VIN current, T _A = 25°C, VREG5 tied to V5FILT, EN1 = EN2 = 5 V, VFB1 = VFB2 = 0.8 V, SW1 = SW2 = 0.5 V | | 450 | 800 | μA |
| I _{VINSDN} | VIN shutdown current | VIN current, T _A = 25°C, no load , EN1 = EN2 = 0 V, VREG5 = ON | | 30 | 60 | μA |
| VFB VOLTAGE AND DISCHARGE RESISTANCE | | | | | | |
| V _{BG} | Bandgap initial regulation accuracy | T _A = 25°C | −1 | | 1 | % |
| V _{VFBTHx} | VFBx threshold voltage | T _A = 25°C, SW _{inj} = OFF | 748 | 758 | 768 | mV |
| | | T _A = 0°C to 70°C, SW _{inj} = OFF ⁽¹⁾ | 746.6 | | 769.4 | |
| | | T _A = -40°C to 85°C, SW _{inj} = OFF ⁽¹⁾ | 745 | | 771 | |
| I _{VFB} | VFB input current | VFBx = 0.8 V, T _A = 25°C | −100 | −10 | 100 | nA |
| R _{Dischg} | VO discharge resistance | ENx = 0 V, VOx = 0.5 V, T _A = 25°C | | 40 | 80 | Ω |
| VREG5 OUTPUT | | | | | | |
| V _{VREG5} | VREG5 output voltage | T _A = 25°C, 5.5 V < VIN < 24 V, 0 < I _{VREG5} < 10 mA | 4.8 | 5.0 | 5.2 | V |
| V _{LN5} | Line regulation | 5.5 V < VIN < 24 V, I _{VREG5} = 10 mA | | | 20 | mV |
| V _{LD5} | Load regulation | 1 mA < I _{VREG5} < 10 mA | | | 40 | mV |
| I _{VREG5} | Output current | VIN = 5.5 V, V _{REG5} = 4.0 V, T _A = 25°C | | 170 | | mA |
| OUTPUT: N-CHANNEL MOSFET GATE DRIVERS | | | | | | |
| R _{DRVH} | DRVH resistance | Source, I _{DRVHx} = −100 mA | | 5.5 | 11 | Ω |
| | | Sink, I _{DRVHx} = 100 mA | | 2.5 | 5 | |
| R _{DRVL} | DRVL resistance | Source, I _{DRVLx} = −100 mA | | 4 | 8 | Ω |
| | | Sink, I _{DRVLx} = 100 mA | | 2 | 4 | |
| T _D | Dead time | DRVHx-low to DRVLx-on | 20 | 50 | 80 | ns |
| | | DRVLx-low to DRVHx-on | 20 | 40 | 80 | |
| INTERNAL BOOST DIODE | | | | | | |
| V _{FBST} | Forward voltage | V _{VREG5-VBSTx} , I _F = 10 mA, T _A = 25°C | 0.7 | 0.8 | 0.9 | V |
| I _{VBSTLK} | VBST leakage current | VBSTx = 29 V, SWx = 24 V, T _A = 25°C | | 0.1 | 1 | μA |
| ON-TIME TIMER CONTROL | | | | | | |
| T _{ON1L} | CH1 on time | SW1 = 12 V, VO1 = 1.8 V | | 165 | | ns |
| T _{ON2L} | CH2 on time | SW2 = 12 V, VO2 = 1.8 V | | 140 | | ns |

(1) Not production tested - ensured by design.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|--|-------|------|-------|--------|
| T _{OFF1L} | CH1 min off time | SW1 = 0.7 V, T _A = 25°C, VFB1 = 0.7 V | | 216 | | ns |
| T _{OFF2L} | CH2 min off time | SW2 = 0.7 V, T _A = 25°C, VFB2 = 0.7 V | | 216 | | ns |
| SOFT START | | | | | | |
| I _{SSC} | SS1/SS2 charge current | V _{SS1} /V _{SS2} = 0 V, T _A = 25°C | –1.44 | –2 | –2.56 | μA |
| TC _{ISSC} | I _{SSC} temperature coefficient | On the basis of 25°C ⁽¹⁾ | –3.3 | | 3.3 | nA/°C |
| I _{SSD} | SS1/SS2 discharge current | V _{SS1} /V _{SS2} = 0.5 V | 100 | 150 | | μA |
| UVLO | | | | | | |
| V _{UV5VFILT} | V5FILT UVLO threshold | V5FILT rising | 3.7 | 4.0 | 4.3 | V |
| | | Hysteresis | 0.2 | 0.3 | 0.4 | |
| LOGIC THRESHOLD | | | | | | |
| V _{ENH} | ENx high-level input voltage | EN 1/2 | 2.0 | | | V |
| V _{ENL} | ENx low-level input voltage | EN 1/2 | | | 0.3 | V |
| CURRENT SENSE | | | | | | |
| I _{TRIP} | TRIP source current | V _{TRIPx} = 0.1 V, T _A = 25°C | 8.5 | 10 | 11.5 | μA |
| TC _{I_{TRIP}} | I _{TRIP} temperature coefficient | On the basis of 25°C | | 4000 | | ppm/°C |
| V _{OCLoff} | OCP compensation offset | (V _{TRIPx-GND} –V _{PGNDx-SWx}) voltage, V _{TRIPx-GND} = 60 mV, T _A = 25°C | –15 | 0 | 15 | mV |
| | | (V _{TRIPx-GND} –V _{PGNDx-SWx}) voltage, V _{TRIPx-GND} = 60 mV | –20 | | 20 | |
| V _{ZC} | Zero cross detection comparator offset | V _{PGNDx-LLx} voltage | | 0.5 | | mV |
| V _{Rtrip} | Current limit threshold setting range | V _{TRIPx-GND} voltage | 30 | | 300 | mV |
| OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION | | | | | | |
| V _{OVP} | Output OVP trip threshold | OVP detect | 110 | 115 | 120 | % |
| T _{OVPDEL} | Output OVP prop delay | | | 1.5 | | μs |
| V _{UVP} | Output UVP trip threshold | UVP detect | 65 | 70 | 75 | % |
| | | Hysteresis (recover < 20 μs) | | 10 | | |
| T _{UVPDEL} | Output UVP delay | | 17 | 30 | 40 | μs |
| T _{UVPEN} | Output UVP enable delay | UVP enable delay / soft-start time | x1.4 | x1.7 | x2.0 | ms |
| THERMAL SHUTDOWN | | | | | | |
| T _{SDN} | Thermal shutdown threshold | Shutdown temperature ⁽²⁾ | | 150 | | °C |
| | | Hysteresis ⁽²⁾ | | 20 | | |

(2) Not production tested - ensured by design.

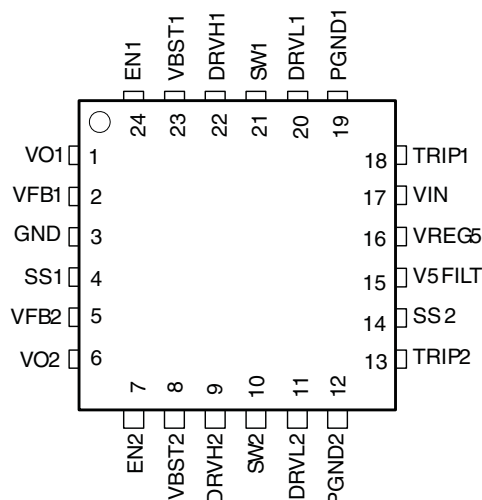
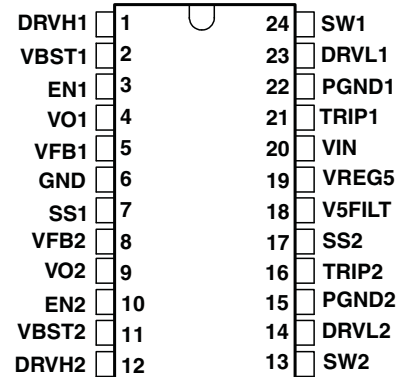
TERMINAL FUNCTIONS

PIN Fuction Table

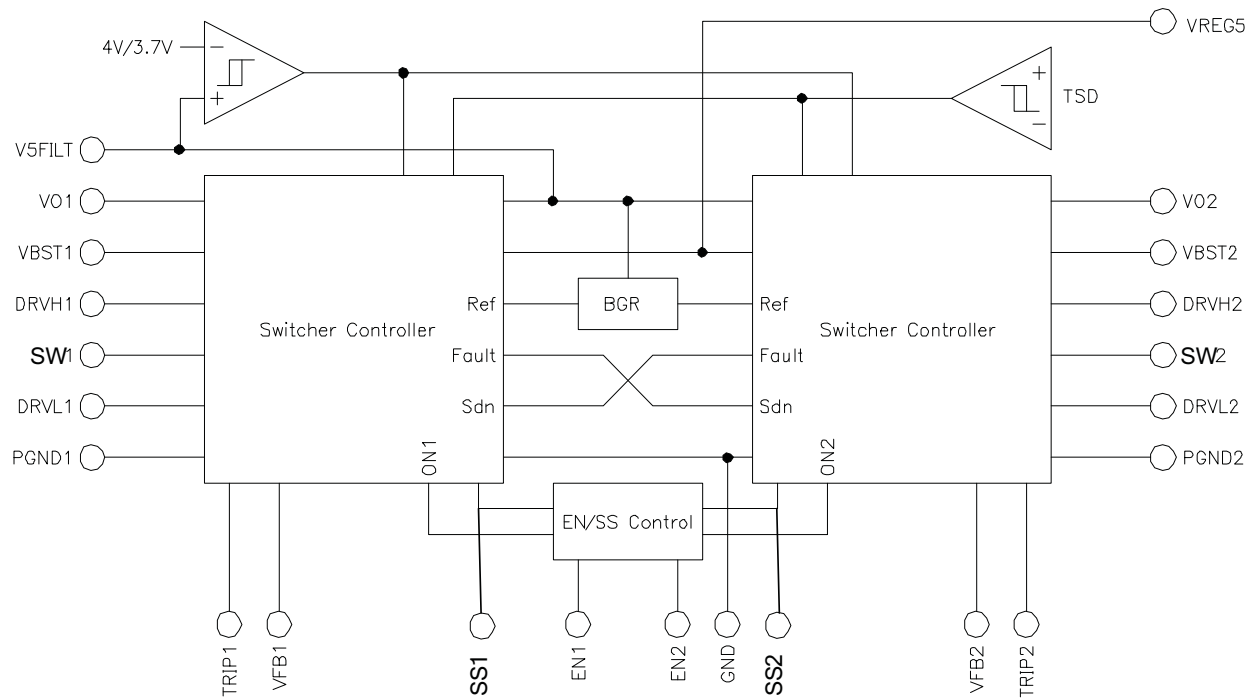
| TERMINAL | | | I/O | DESCRIPTION |
|--------------|--------|----------|-----|--|
| NAME | QFN 24 | TSSOP 24 | | |
| VBST1, VBST2 | 23, 8 | 2, 11 | I | Supply input for high-side NFET driver. Bypass to SWx with a high-quality 0.1-μF ceramic capacitor. An external schottky diode can be added from VREG5 if forward drop is critical to drive the high-side FET. |
| EN1, EN2 | 24, 7 | 3, 10 | I | Enable. Pull High to enable SMPS. |
| VO1, VO2 | 1, 6 | 4, 9 | I | Output voltage inputs for on-time adjustment and output discharge. Connect directly to the output voltage. |

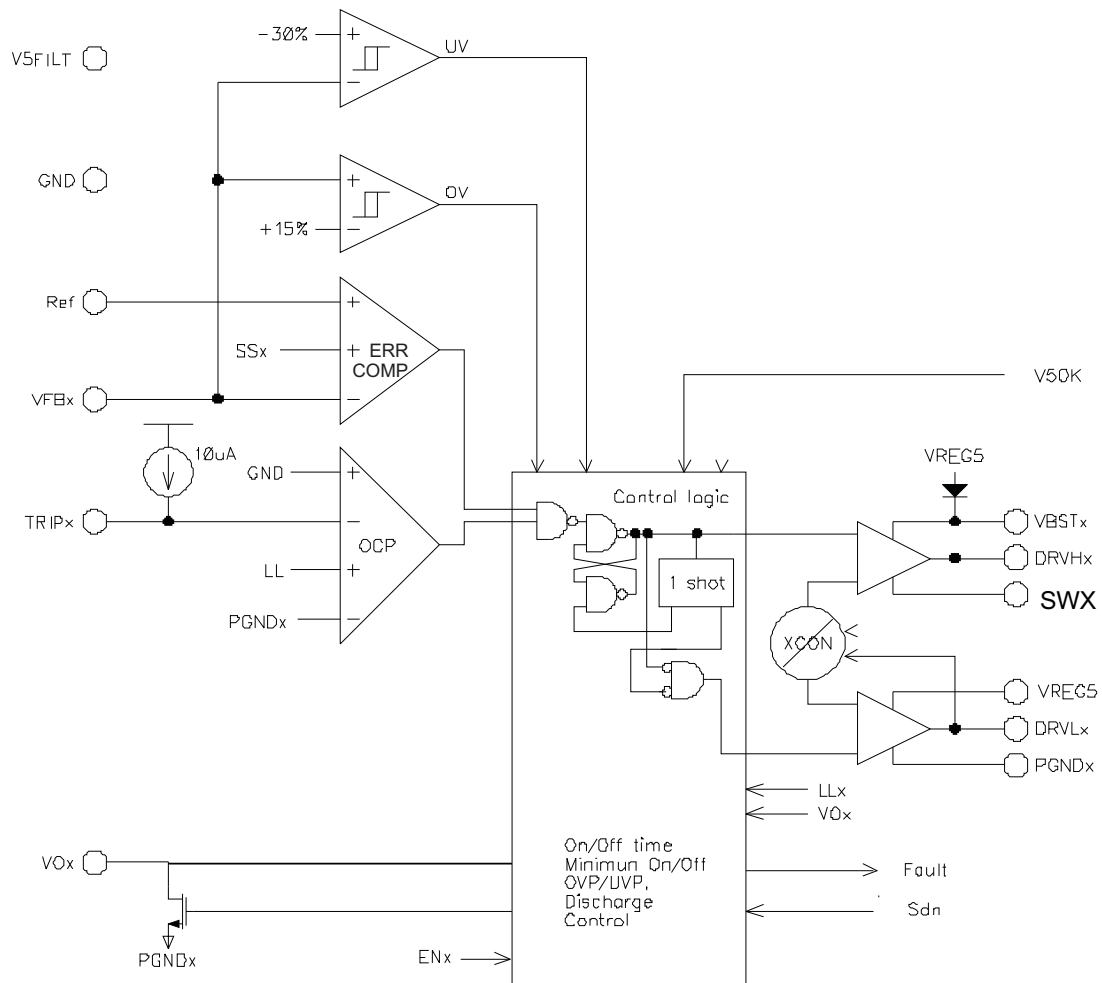
PIN Function Table (continued)

| TERMINAL | | | I/O | DESCRIPTION |
|-----------------|-----------|-------------|-----|--|
| NAME | QFN 24 | TSSOP 24 | | |
| VFB1, VFB2 | 2, 5 | 5, 8 | I | D-CAP2 feedback inputs. Connect to output voltage with resistor divider. |
| GND | 3 | 6 | I | Signal ground pin. Connect to PGND1, PGND2 and system ground at a single point. |
| DRVH1, DRVH2 | 22, 9 | 1, 12 | O | High-side N-Channel MOSFET gate driver outputs. SWx referenced drivers switch between SWx (OFF) and VBSTx (ON). |
| SW1, SW2 | 21, 10 | 24, 13 | I/O | Switch node connections for both the high-side drivers and the over current comparators. |
| DRVL1, DRVL2 | 20, 11 | 23, 14 | O | Low-side N-Channel MOSFET gate driver outputs. PGND referenced drivers switch between PGNDx (OFF) and VREG5 (ON). |
| PGND1, PGND2 | 19, 12 | 22, 15 | I/O | Power ground connections for both the low-side drivers and the over current comparators. Connect PGND1, PGND2 and GND strongly together near the IC. |
| TRIP1, TRIP2 | 18, 13 | 21, 16 | I | Over current threshold programming pin. Connect to GND with a resistor to GND to set threshold for low-side $R_{DS(ON)}$ current limit. |
| VIN | 17 | 20 | I | Supply Input for 5-V linear regulator. Bypass to GND with a minimum high-quality 0.1- μ F ceramic capacitor. |
| V5FILT | 15 | 18 | I | 5-V supply input for the entire control circuitry except the MOSFET drivers. Bypass to GND with a minimum high-quality 1.0- μ F ceramic capacitor. V5FILT is connected to VREG5 via an internal 10- Ω resistor. |
| VREG5 | 16 | 19 | O | Output of 5-V linear regulator and supply for MOSFET drivers. Bypass to GND with a minimum high-quality 4.7- μ F ceramic capacitor. VREG5 is connected to V5FILT via an internal 10- Ω resistor. |
| SS1, SS2 | 4, 14 | 7, 17 | I | Soft-start programming pin. Connect capacitor from SSx pin to GND to program soft-start time. |

**QFN PACKAGE
(TOP VIEW)****TSSOP PACKAGE
(TOP VIEW)**

FUNCTIONAL BLOCK DIAGRAM





DETAILED DESCRIPTION

PWM Operation

The main control loop of the TPS53129 is an adaptive on-time pulse width modulation (PWM) controller using a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the synchronous high-side MOSFET is turned on. After an internal one-shot timer expires, this MOSFET is turned off. When the feedback voltage falls below the reference voltage, the one-shot timer is reset and the high-side MOSFET is turned back on. The one shot is set by the converter input voltage VIN, and the output voltage VO, to maintain a pseudo-fixed frequency over the input voltage range. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP mode control. The low-side MOSFET is turned off when the inductor current information detects zero level. This enables seamless transition to the reduced frequency operation at light-load conditions so that high efficiency is kept over a broad range of load current.

Light-Load Condition

TPS53129 automatically reduces switching frequency at light-load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly and without increase of Vout ripple or load regulation. Detail operation is described as follows. As the output current decreases from heavy-load condition, the inductor current is also reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous condition modes. The low-side MOSFET is turned off when this zero inductor current is detected. As the load current is further decreased, the converter runs in discontinuous conduction mode and it takes longer and longer to discharge the output capacitor to the level that requires the next ON cycle. The ON time is kept the same as that in the heavy-load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction. The transition load point to the light load operation, IOUT(LL) (i.e., threshold between continuous and discontinuous condition mode) can be calculated as follows.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \frac{V_{IN} - V_{OX}}{V_{IN}} \times V_{OX} \quad (1)$$

Where fSW is the PWM switching frequency.

Switching frequency versus output current in the light-load condition is a function of L, fSW, VIN and VOUT, but it decreases almost proportional to the output current from the IOUT(LL) given in [Equation 1](#).

Drivers

Each channel of the TPS53129 contains two high-current resistive MOSFET gate drivers. The low-side driver is a PGND referenced, VREG5 powered driver designed to drive the gate of a high-current, low RDS(ON) N-channel MOSFET whose source is connected to PGND. The high-side driver is a floating SWx referenced VBST powered driver designed to drive the gate of a high-current, low RDS(ON) N-channel MOSFET. To maintain the VBST voltage during the high-side driver ON time, a capacitor is placed from SWx to VBSTx. Each driver draws average current equal to gate charge (Qg at Vgs = 5 V) times switching frequency (fSW).

To prevent cross-conduction, there is a narrow dead-time when both high-side and low-side drivers are OFF between each driver transition. During this time the inductor current is carried by one of the MOSFETs body diodes.

PWM Frequency and Adaptive On-Time Control

TPS53129 employs adaptive on-time control scheme and does not have a dedicated on board oscillator.

TPS53129 runs with pseudo-constant frequency by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage. Therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

5-Volt Regulator

The TPS53129 has an internal 5-V low-dropout (LDO) regulator to provide a regulated voltage for all both drivers and the IC's internal logic. A high-quality 4.7-μF or greater ceramic capacitor from VREG5 to GND is required to stabilize the internal regulator. An internal 10-Ω resistor from VREG5 filters the regulator output to the IC's analog and logic input voltage, V5FILT. An additional high-quality 1.0-μF ceramic capacitor is required from V5FILT to GND to filter switching noise from VREG5.

Soft Start

The TPS53129 has a programmable soft-start. When the ENx pin becomes high, 2.0-μA current begins charging the capacitor connected from the SS pin to GND. The internal reference for the D-CAP2™ mode control comparator is overridden by the soft-start voltage until the soft-start voltage is greater than the internal reference for smooth control of the output voltage during start up.

Pre-Bias Support

The TPS53129 supports pre-bias start-up without sinking current from the output capacitor. When enabled, the low-side driver is held off until the soft-start commands a voltage higher than the pre-bias level (internal soft-start becomes greater than feedback voltage (VFB)), then the TPS53129 slowly activates synchronous rectification by limiting the first DRV1 pulses with a narrow on-time. This limited on-time is then incremented on a cycle-by-cycle basis until it coincides with the full 1-D off-time. This scheme prevents the initial sinking of current from the pre-bias output, and ensure that the output voltage (VOUT) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

Output Discharge Control

TPS53129 discharges the outputs when ENx is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO, and thermal shutdown). The device discharges output using an internal 40-Ω MOSFET which is connected to VOx and PGNDx. The external low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output. This discharge ensures that on start the regulated voltage always initializes from 0 V.

Over Current Limit

TPS53129 has cycle-by-cycle over current limit feature. The over current limits the inductor valley current by monitoring the voltage drop across the low-side MOSFET $R_{DS(ON)}$ during the low-side driver on-time. If the inductor current is larger than the over current limit (OCL), the TPS53129 delays the start of the next switching cycle until the sensed inductor current falls below the OCL current. MOSFET $R_{DS(ON)}$ current sensing is used to provide an accuracy and cost effective solution without external devices. To program the OCL, the TRIP pin should be connected to GND through a trip voltage setting resistor, according to the following equations.

$$V_{TRIP} = \left(I_{OCL} - \frac{(V_{IN} - V_O)}{2 \cdot L1 \cdot f_{SW}} \cdot \frac{V_O}{V_{IN}} \right) \cdot R_{DS(ON)} \quad (2)$$

$$R_{TRIP} (k\Omega) = \frac{V_{TRIP} (mV)}{I_{TRIP} (\mu A)} \quad (3)$$

The trip voltage should be between 30 mV to 300 mV over all operational temperature, including the 4000-ppm/°C temperature slope compensation for the temperature dependency of the $R_{DS(ON)}$.

If the load current exceeds the over current limit, the voltage will begin to drop. If the over current conditions continues the output voltage will fall below the under voltage protection threshold and the TPS53129 will shut down.

In an over current condition, the current to the load exceeds the current to the output capacitor; thus the output voltage tends to fall off. Eventually, it will end up with crossing the under voltage protection threshold and shutdown.

Over/Under Voltage Protection

TPS53129 monitors a resistor divided feedback voltage to detect over and under voltage. If the feedback voltage is higher than 115% of the reference voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver OFF and the low-side MOSFET driver ON.

When the feedback voltage is lower than 70% of the reference voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 30 μ s, TPS53129 latches OFF both top and bottom MOSFET drivers. This function is enabled approximately $1.7 \times T_{SS}$ after power-on. The OVP and UVP latch off is reset when EN goes low level.

UVLO Protection

TPS53129 has V5FILT under voltage lock out protection (UVLO) that monitors the voltage of V5FILT pin.

When the V5FILT voltage is lower than UVLO threshold voltage, the device is shut off. All output drivers are OFF and output discharge is ON. The UVLO is non-latch protection.

Thermal Shutdown

The TPS53129 includes an over temperature protection shut-down feature. If the TPS53129 die temperature exceeds the OTP threshold (typically 150°C), both the high-side and low-side drivers are shut off, the output voltage discharge function is enabled and then the device is shut off until the die temperature drops. Thermal shutdown is a non-latch protection.

TYPICAL CHARACTERISTICS

VIN SUPPLY CURRENT
vs
JUNCTION TEMPERATURE

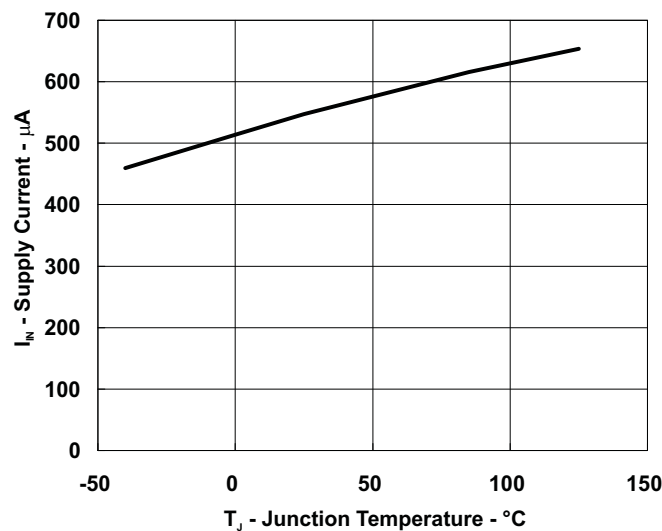


Figure 3.

VIN SHUTDOWN CURRENT
vs
JUNCTION TEMPERATURE

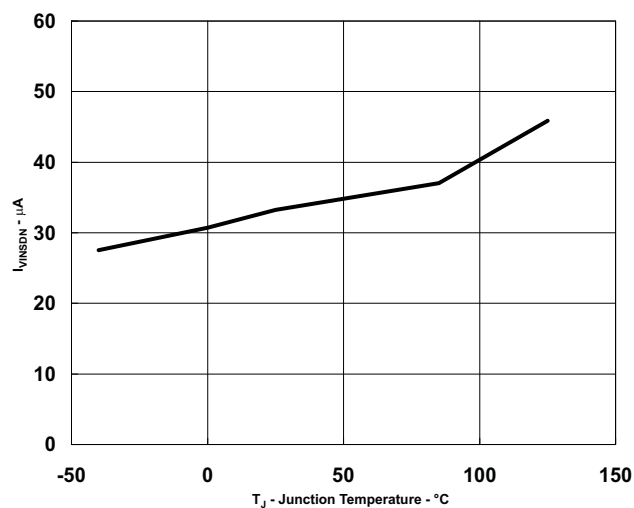


Figure 4.

TRIP SOURCE CURRENT
vs
JUNCTION TEMPERATURE

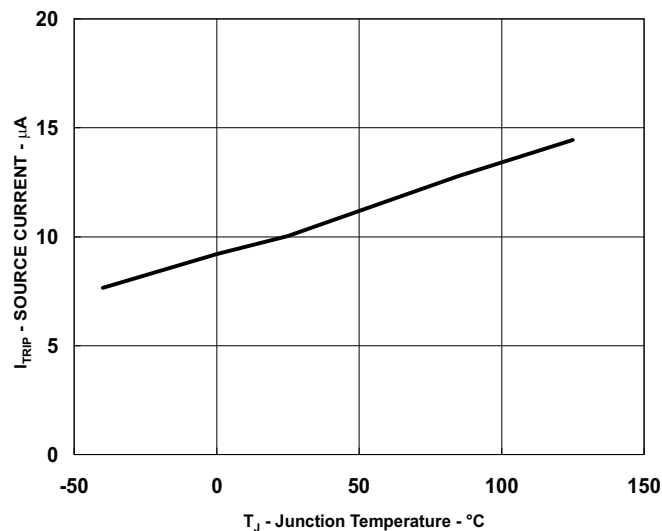


Figure 5.

VREG5 VOLTAGE
vs
JUNCTION TEMPERATURE

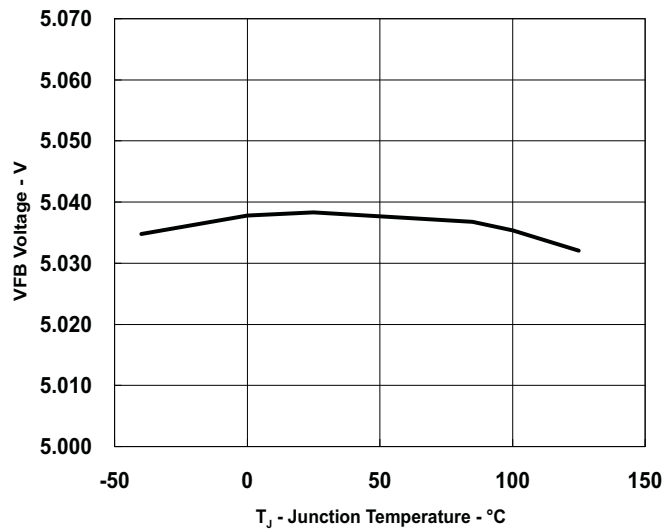


Figure .

TYPICAL CHARACTERISTICS (continued)

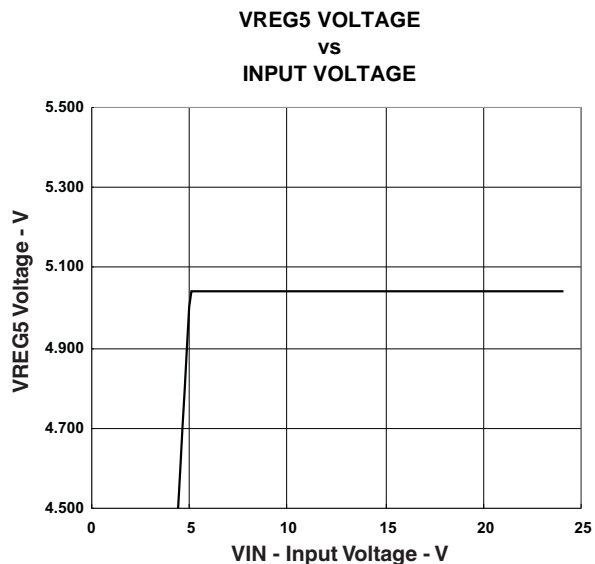


Figure 6.

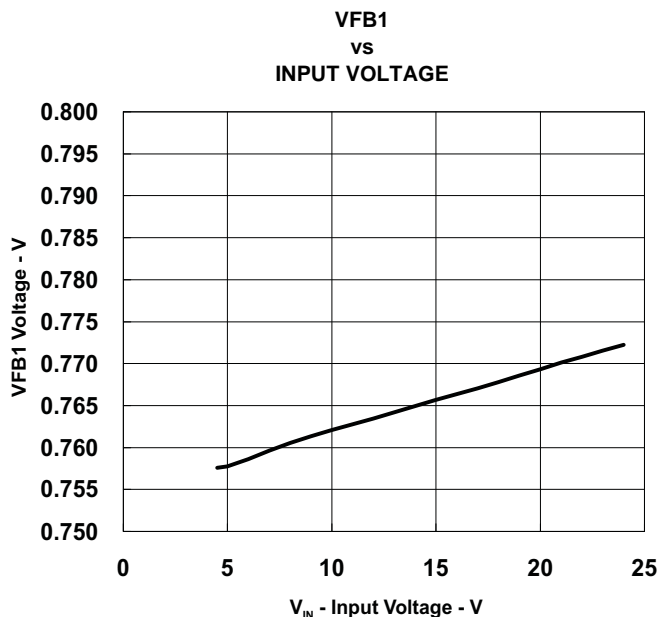


Figure 7.

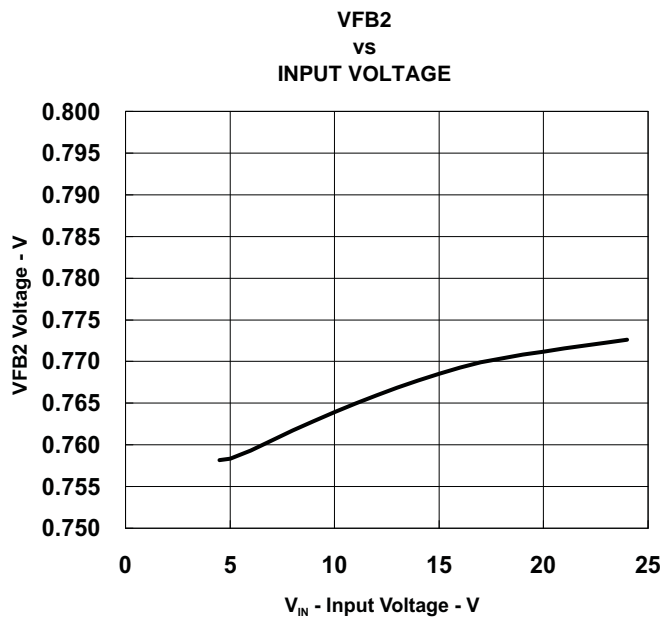


Figure 8.

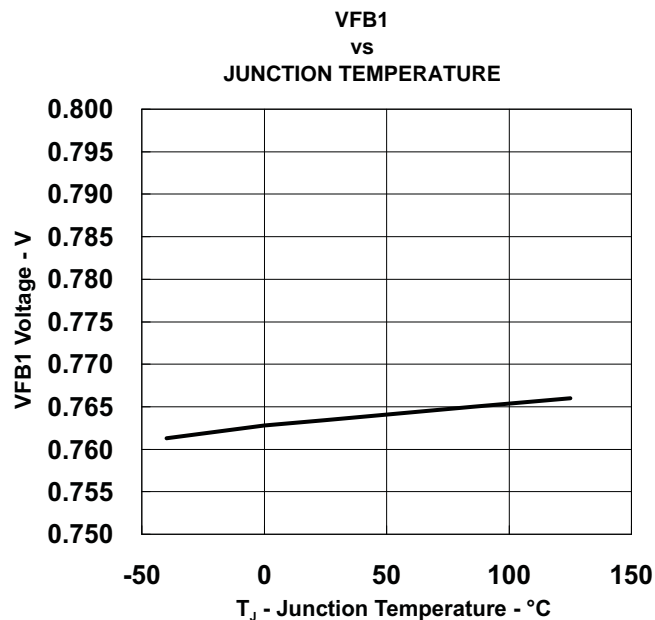


Figure 9.

TYPICAL CHARACTERISTICS (continued)

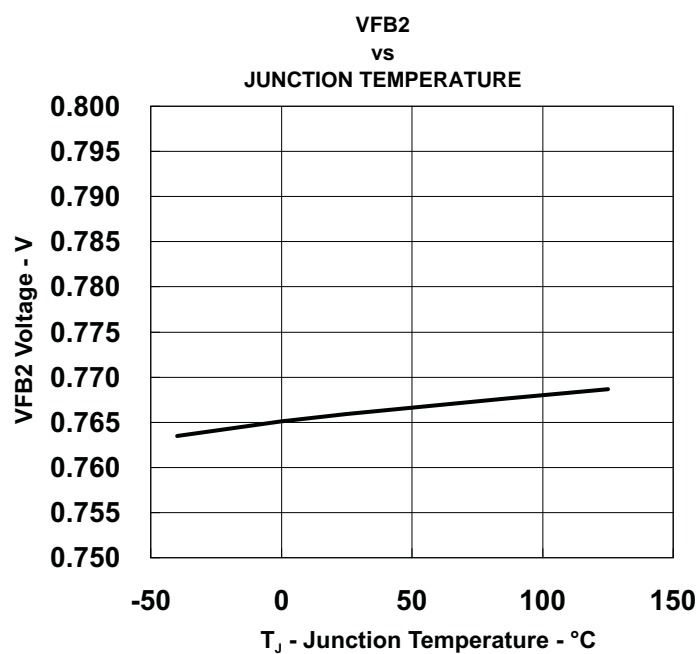


Figure 10.

TYPICAL APPLICATION PERFORMANCE

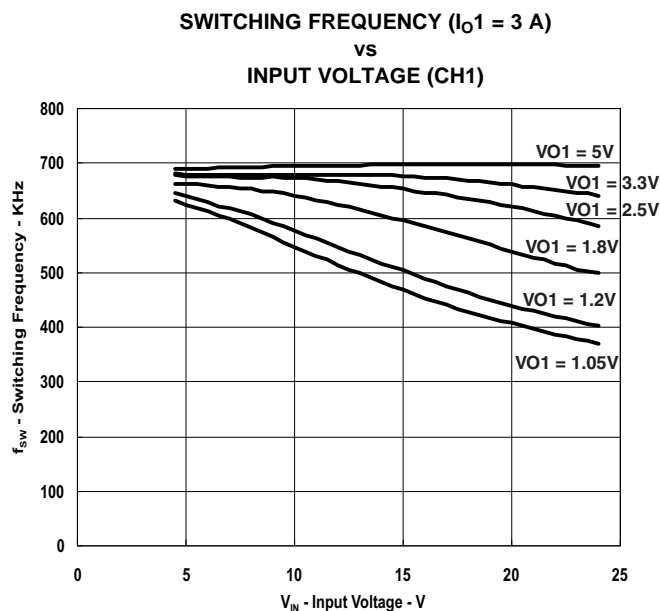


Figure 11.

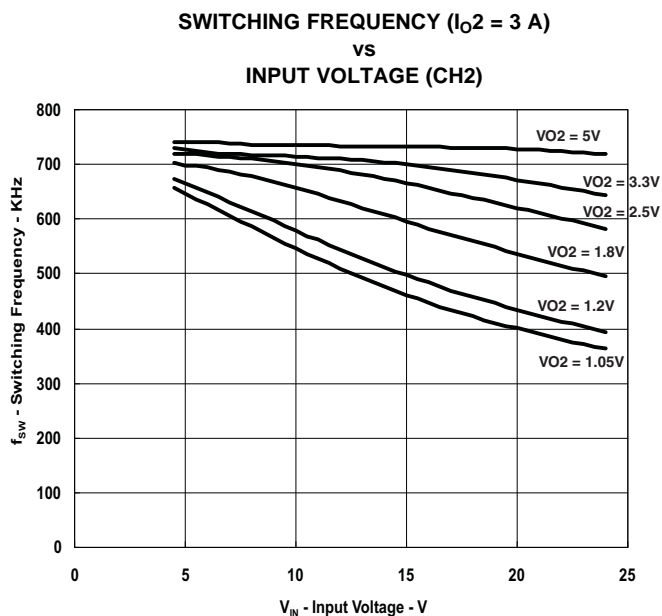


Figure 12.

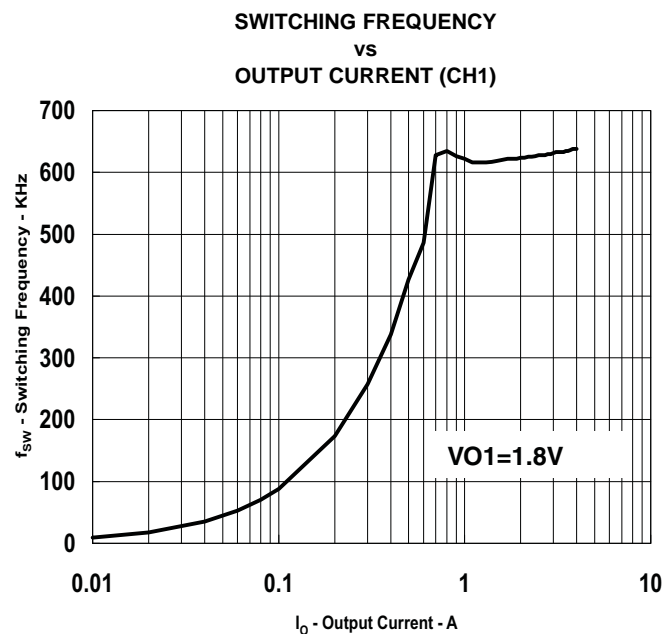


Figure 13.

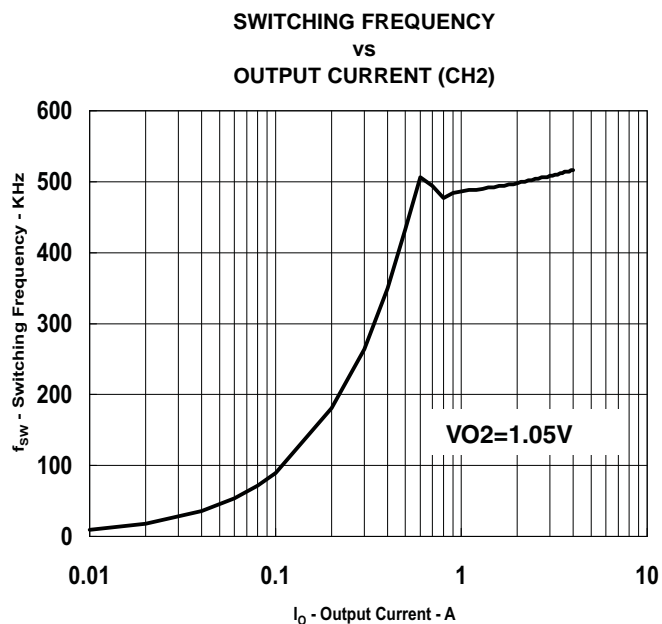


Figure 14.

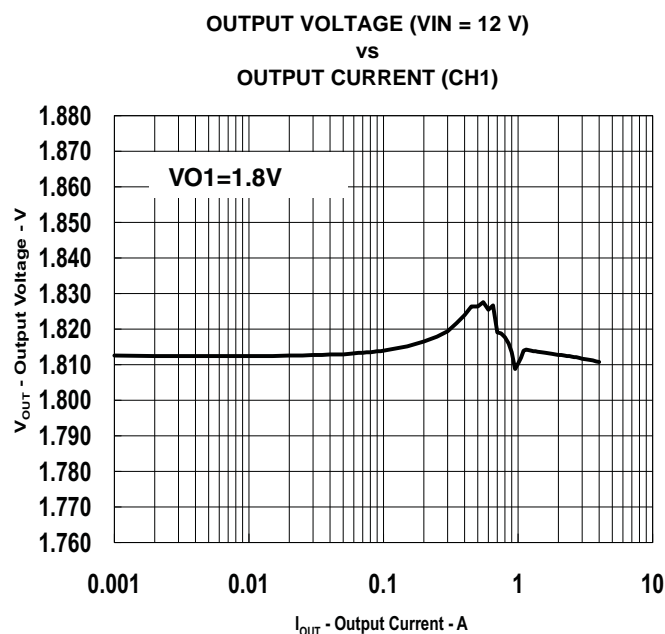


Figure 15.

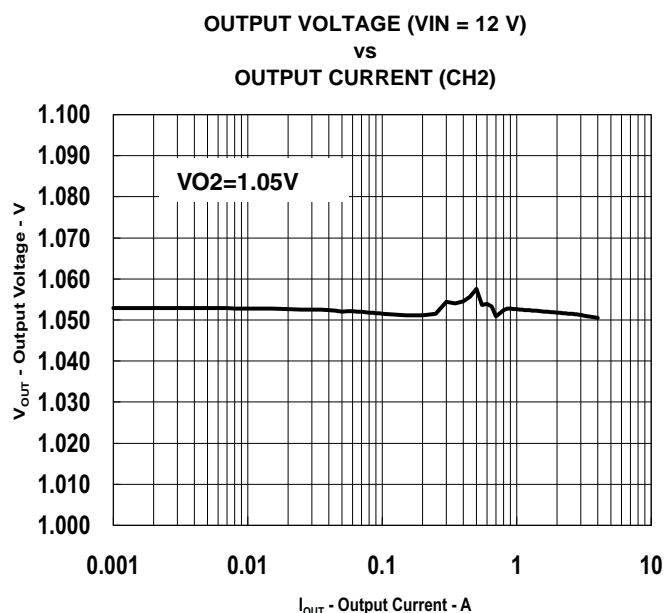


Figure 16.

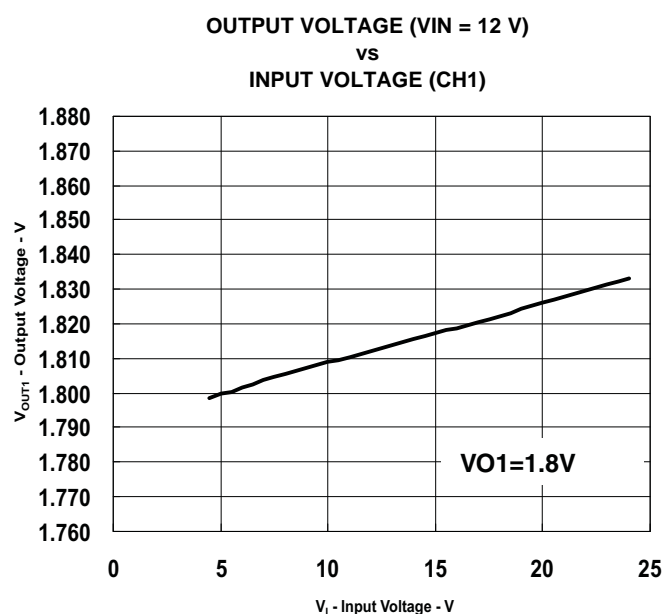


Figure 17.

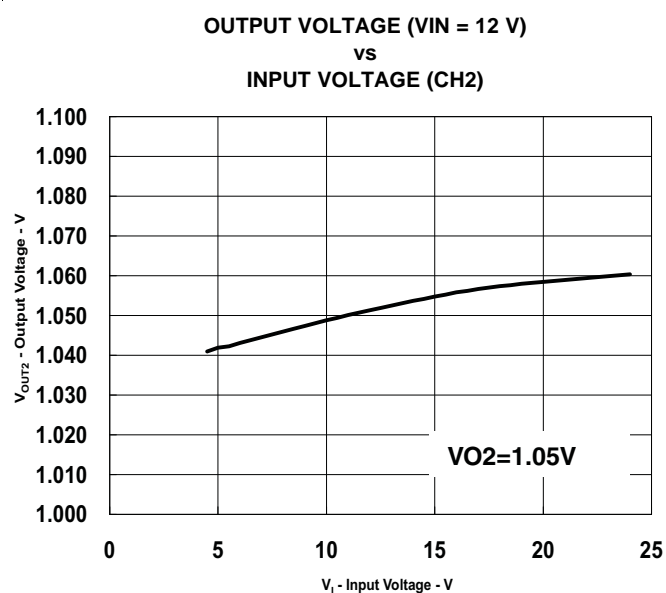


Figure 18.

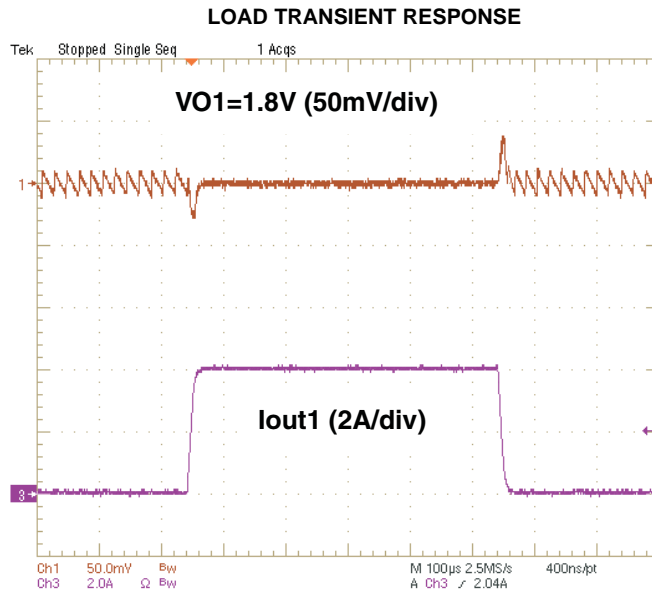


Figure 19.

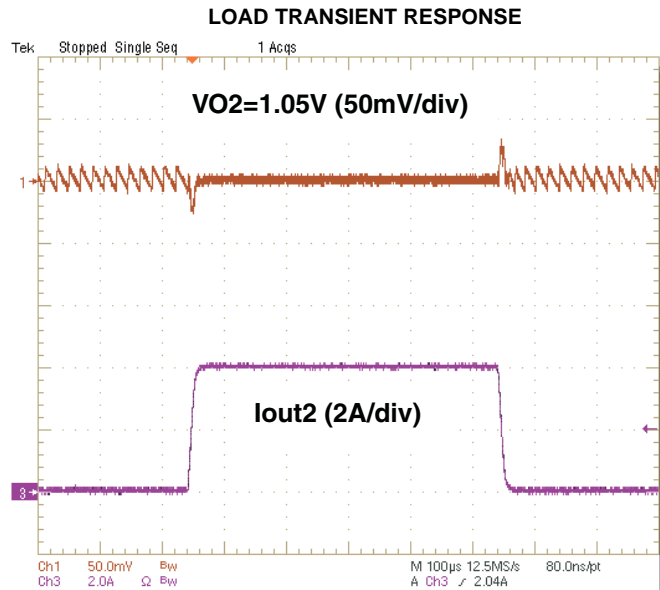


Figure 20.

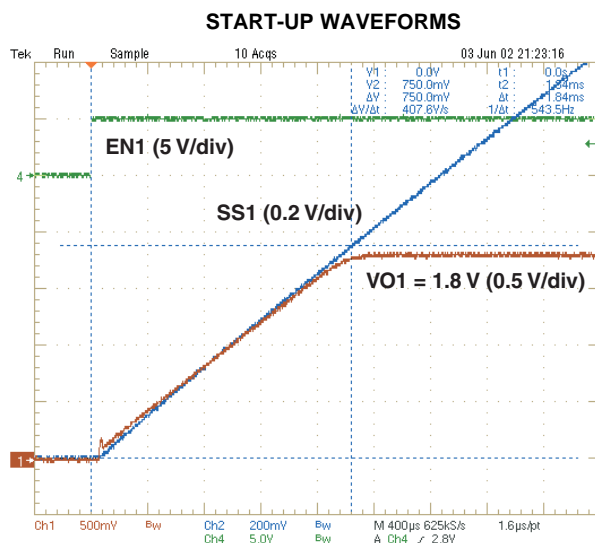


Figure 21.

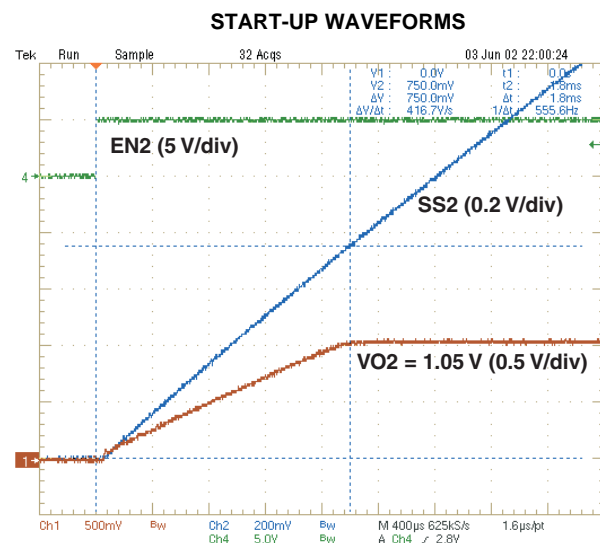


Figure 22.

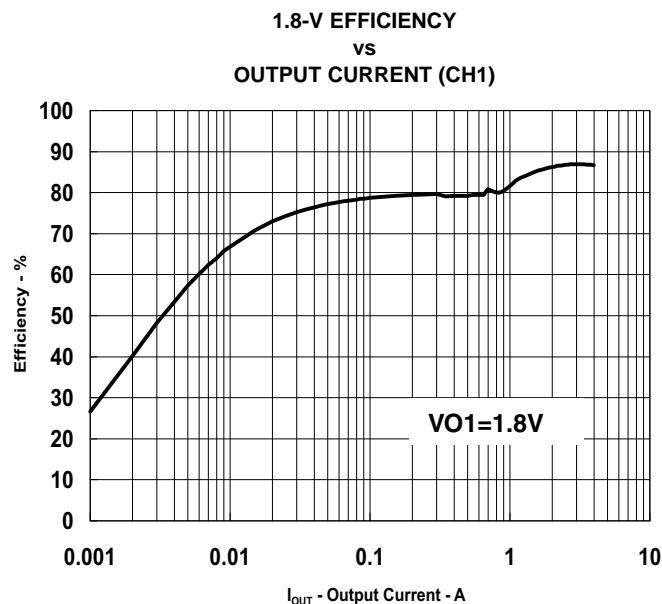


Figure 23.

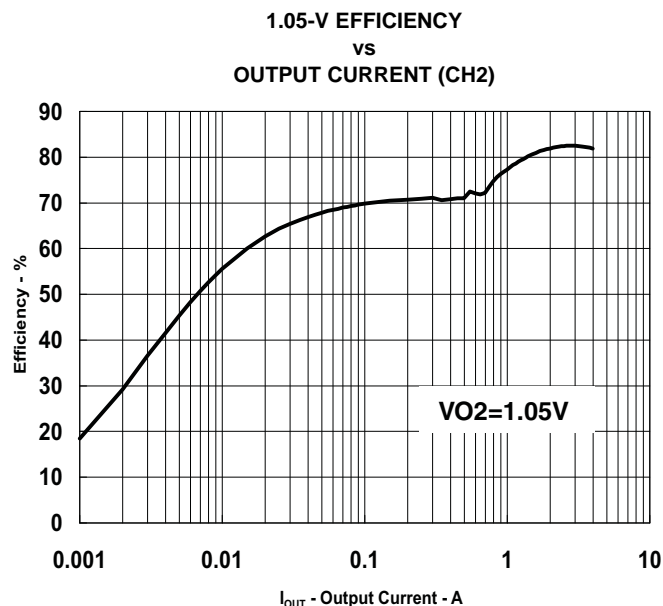


Figure 24.

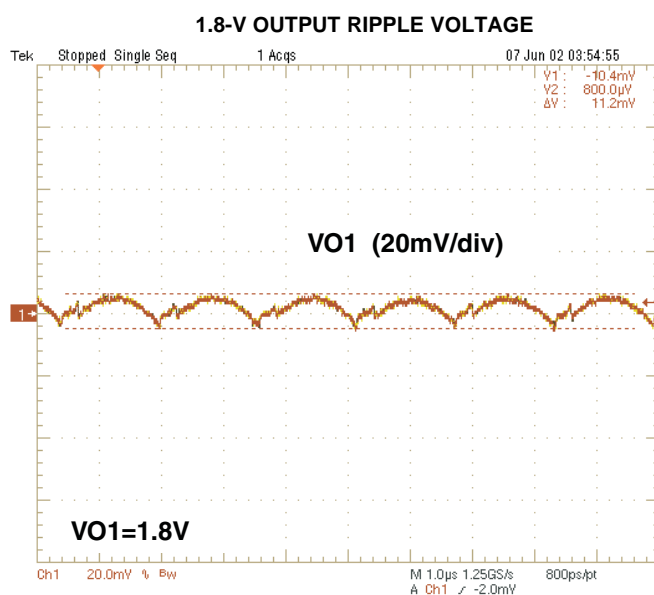


Figure 25.

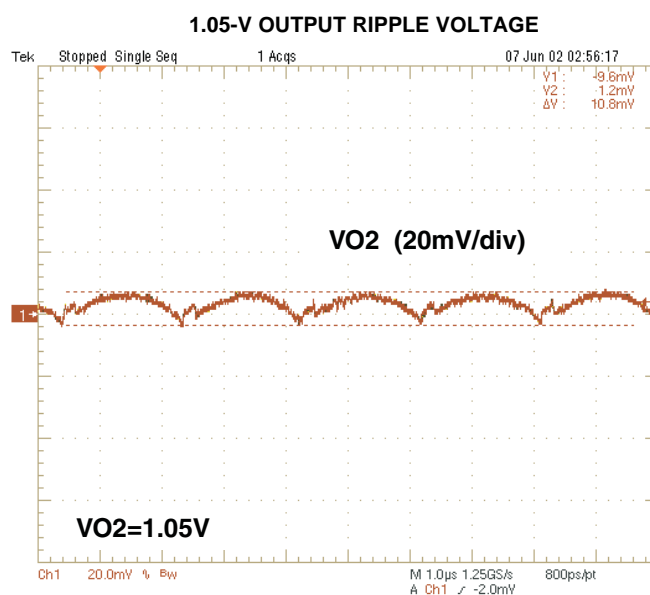


Figure 26.

APPLICATION INFORMATION

1. Choose inductor.

The inductance value is selected to provide approximately 30% peak to peak ripple current at maximum load. Larger ripple current increases output ripple voltage, improve S/N ratio and contribute to stable operation.

Equation 4 can be used to calculate L1.

$$L1 = \frac{(V_{IN(max)} - V_{O1})}{I_{L1(ripple)} \times f_{SW}} \times \frac{V_{O1}}{V_{IN(max)}} = \frac{3 \times (V_{IN(max)} - V_{O1})}{I_{O1} \times f_{SW}} \times \frac{V_{O1}}{V_{IN(max)}} \quad (4)$$

The inductors current ratings needs to support both the RMS (thermal) current and the Peak (saturation) current. The RMS and peak inductor current can be estimated as follows.

$$I_{L1(RIPPLE)} = \frac{V_{IN(MAX)} - V_{O1}}{L1 \cdot f_{SW}} \cdot \frac{V_{O1}}{V_{IN(MAX)}} \quad (5)$$

$$I_{L1(PEAK)} = \frac{V_{TRIP}}{R_{DS(ON)}} + I_{L1(RIPPLE)} \quad (6)$$

$$I_{L1(RMS)} = \sqrt{I_{O1}^2 + \frac{1}{12} (I_{L1(RIPPLE)})^2} \quad (7)$$

Note: The calculation above shall serve as a general reference. To further improve transient response, the output inductance could be reduced further. This needs to be considered along with the selection of the output capacitor.

2. Choose output capacitor.

The capacitor value and ESR determines the amount of output voltage ripple and load transient response. it is recommended to use a ceramic output capacitor.

$$C1 = \frac{I_{L1(RIPPLE)}}{8 \cdot V_{O1(RIPPLE)}} \cdot \frac{1}{f_{SW}} \quad (8)$$

$$C1 = \frac{\Delta I_{load}^2 \cdot L1}{2 \cdot V_{O1} \cdot \Delta V_{OS}} \quad (9)$$

$$C1 = \frac{\Delta I_{load}^2 \cdot L1}{2 \cdot K \cdot \Delta V_{US}} \quad (10)$$

Where

$$K = (V_{IN} - V_{O1}) \cdot \frac{T_{on}}{T_{on} + T_{min(off)}} \quad (11)$$

Select the capacitance value greater than the largest value calculated from Equation 8, Equation 9 and Equation 10. The capacitance for C1 should be greater than 66 μF.

Where

ΔV_{OS} = The allowable amount of overshoot voltage in load transition

ΔV_{US} = The allowable amount of undershoot voltage in load transition

T_{min(off)} = Minimum off time

3. Choose input capacitor.

The TPS53129 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A minimum 10-μF high-quality ceramic capacitor is recommended for the input capacitor. The capacitor voltage rating needs to be greater than the maximum input voltage.

4. Choose bootstrap capacitor.

The TPS53129 requires a bootstrap capacitor from SW to VBST to provide the floating supply for the high-side drivers. A minimum 0.1-μF high-quality ceramic capacitor is recommended. The voltage rating should be greater than 10 V.

5. Choose VREG5 and V5FILT capacitor.

The TPS53129 requires both the VREG5 regulator and V5FILT input are bypassed. A minimum 4.7-μF high-quality ceramic capacitor must be connected between the VREG5 and GND for proper operation. A minimum 1-μF high-quality ceramic capacitor must be connected between the V5FILT and GND for proper operation. Both of these capacitors' voltage ratings should be greater than 10 V.

6. Choose output voltage divider resistors.

The output voltage is set with a resistor divider from the output voltage node to the VFBx pin. It is recommended to use 1% tolerance or better resistors. Select R2 between 10 kΩ and 100 kΩ and use [Equation 12](#) or [Equation 13](#) to calculate R1.

$$V_{swinj} = (V_{IN} - V_O \cdot 0.5875) \cdot \left(\frac{1}{f_{SW}}\right) \cdot \left(\frac{V_O}{V_{IN}}\right) \cdot 4975 \quad (12)$$

$$R1 = \left(\frac{V_O}{V_{FB} + \frac{V_{FB(RIPPLE)} + V_{swinj}}{2}} - 1 \right) \cdot R2 \quad (13)$$

Where

$V_{FB(RIPPLE)}$ = Ripple voltage at VFB

V_{swinj} = Ripple voltage at error comparator

7. Choose register setting for over current limit.

$$V_{TRIP} = \left(I_{OCL} - \frac{(V_{IN} - V_O)}{2 \cdot L1 \cdot f_{SW}} \cdot \frac{V_O}{V_{IN}} \right) \cdot R_{DS(ON)} \quad (14)$$

$$R_{TRIP} (k\Omega) = \frac{V_{TRIP} (mV) - V_{OCLoff}}{I_{TRIP(min)} (\mu A)} \quad (15)$$

Where

$R_{DS(ON)}$ = Low side FET on-resistance

$I_{TRIP(min)}$ = TRIP pin source current (8.5 μA)

V_{OCLoff} = Minimum over current limit offset voltage (–20 mV)

I_{OCL} = Over current limit

8. Choose soft start capacitor.

Soft start time equation is as follows.

$$C_{SS} = \frac{T_{SS} \cdot I_{SSC}}{V_{FB}} \quad (16)$$

LAYOUT SUGGESTIONS

- Keep the input switching current loop as small as possible.
- Place the input capacitor (C3,C6) close to the top switching FET. The output current loop should also be kept as small as possible.
- Keep the SW node as physically small and short as possible as to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin (FBx) of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|--------------------------------------|
| TPS53129PW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS53129PWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS53129RGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Request Free Samples |
| TPS53129RGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Purchase Samples |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

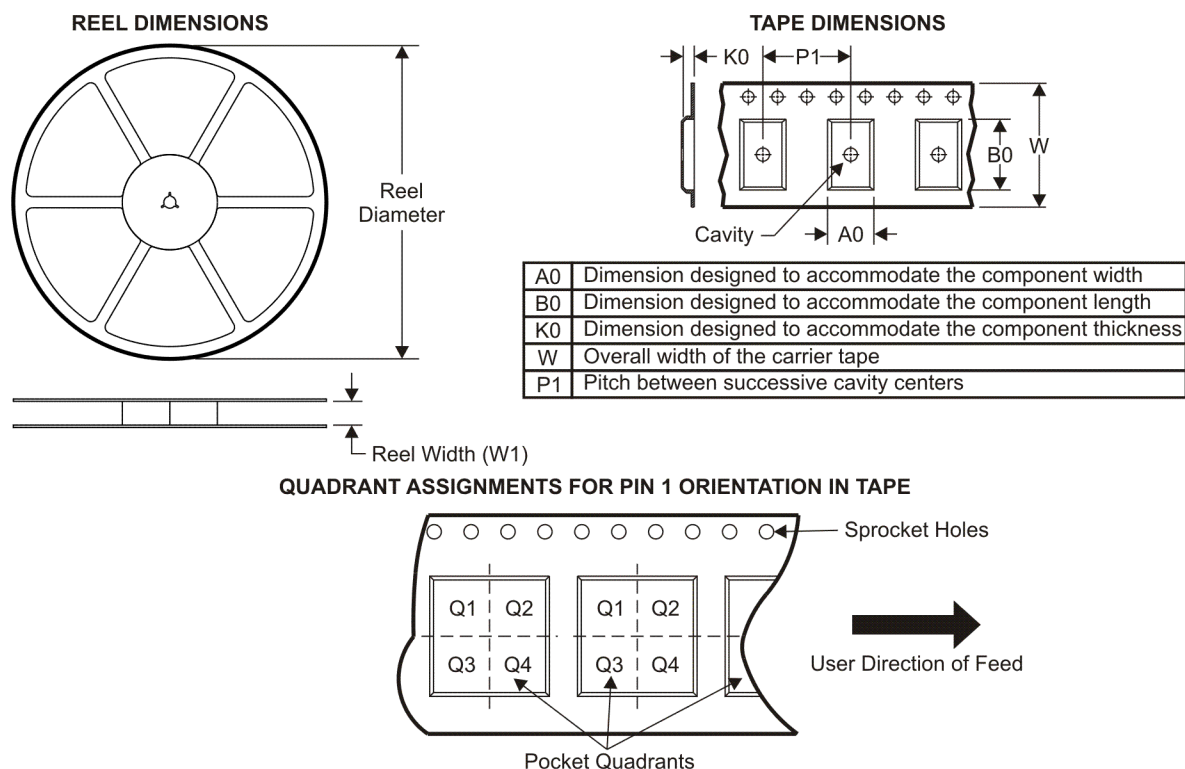
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS53129PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| TPS53129RGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS53129RGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

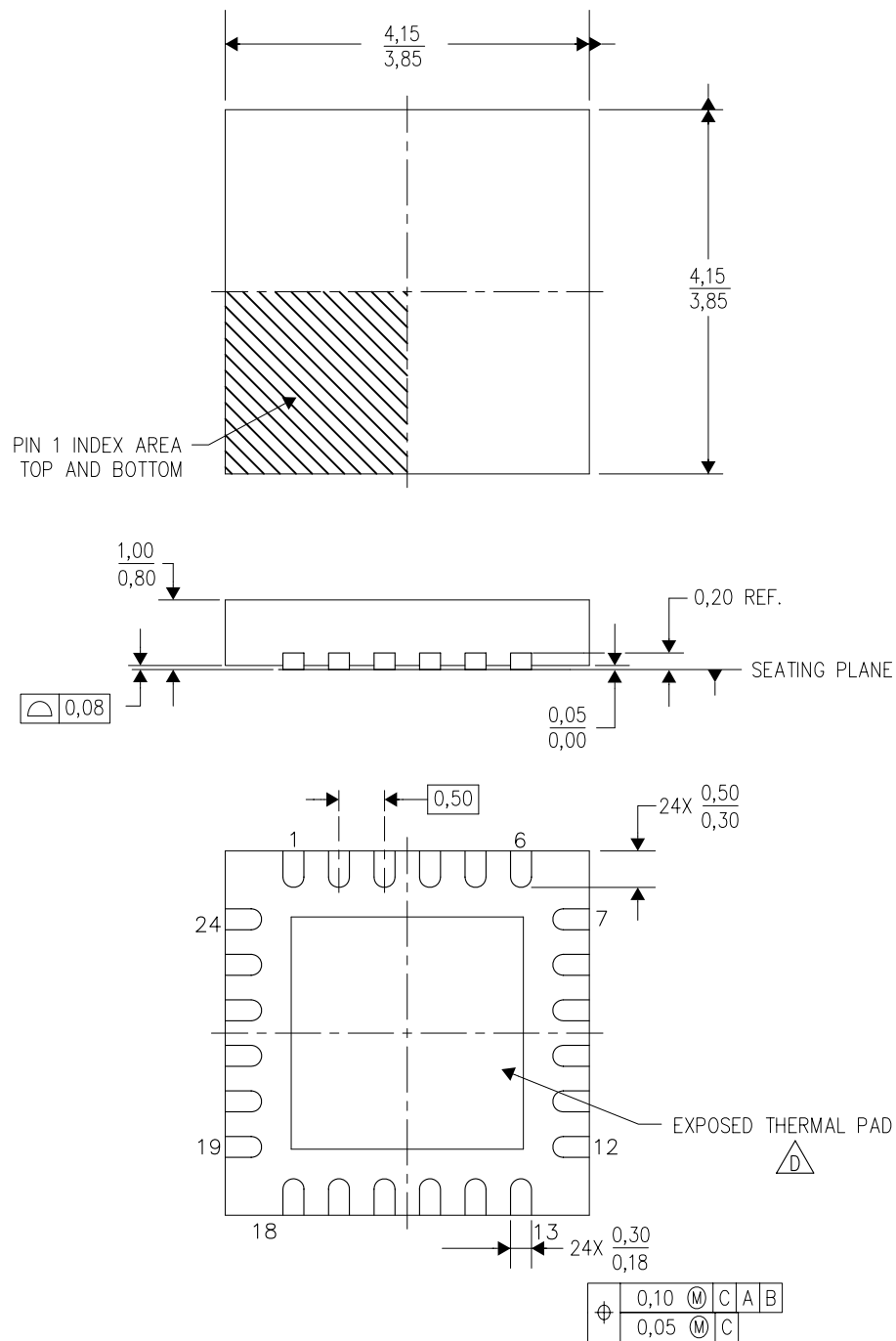


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS53129PWR | TSSOP | PW | 24 | 2000 | 346.0 | 346.0 | 33.0 |
| TPS53129RGER | VQFN | RGE | 24 | 3000 | 346.0 | 346.0 | 29.0 |
| TPS53129RGET | VQFN | RGE | 24 | 250 | 190.5 | 212.7 | 31.8 |

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



4204104/F 07/10

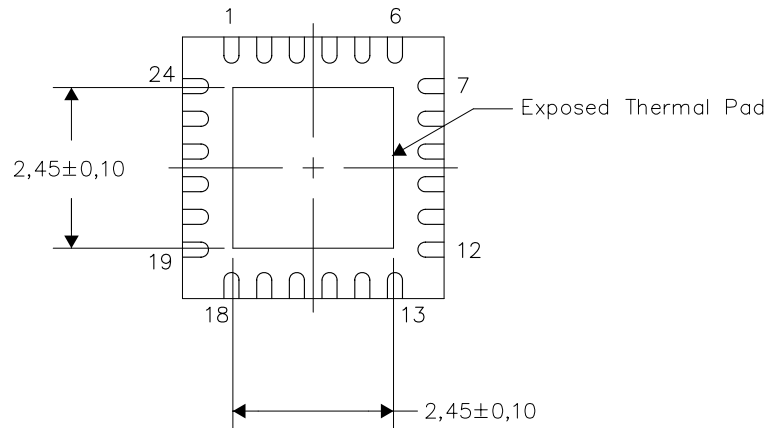
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-Leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

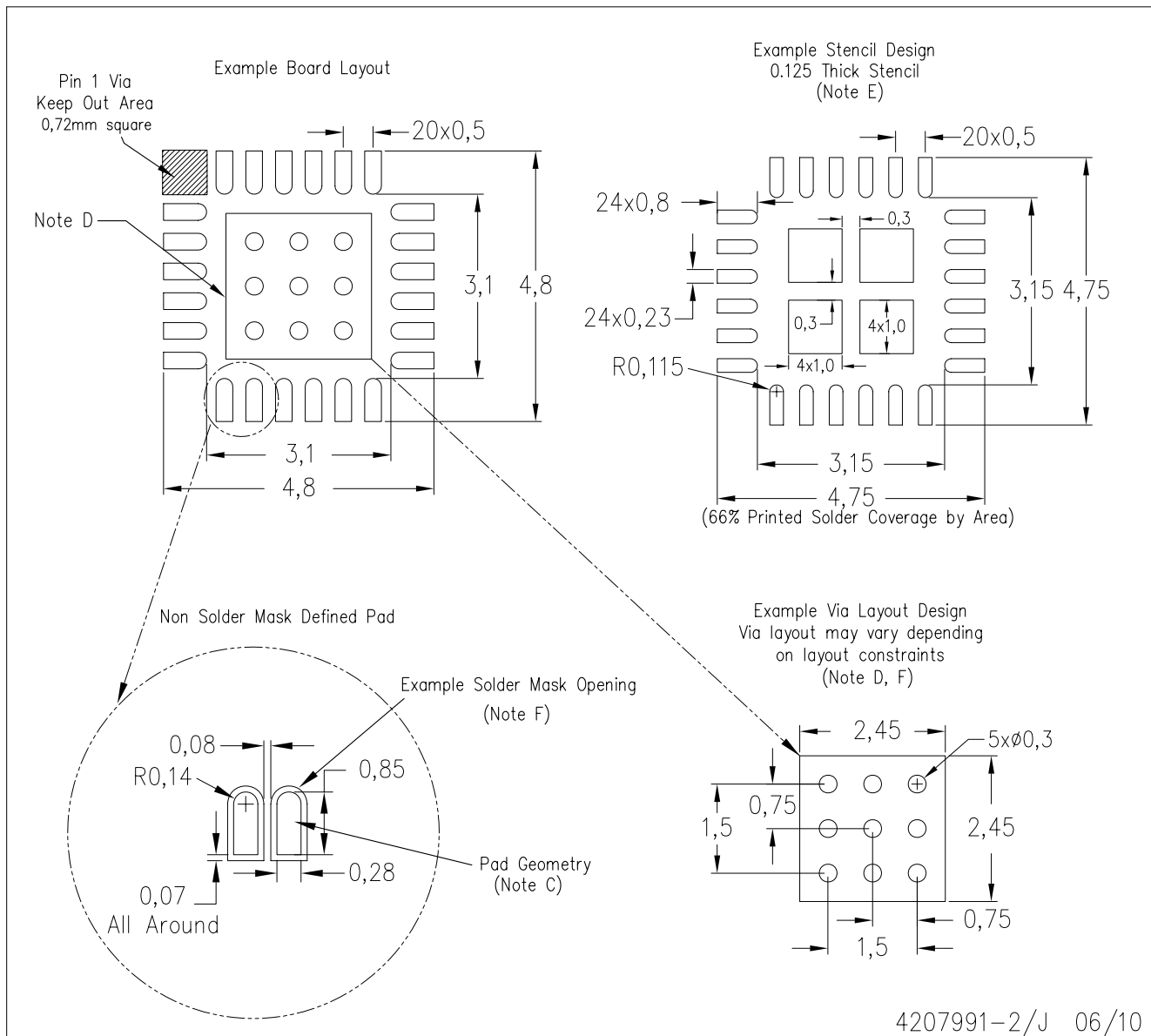
Exposed Thermal Pad Dimensions

4206344-3/U 09/10

NOTES: A. All linear dimensions are in millimeters

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD

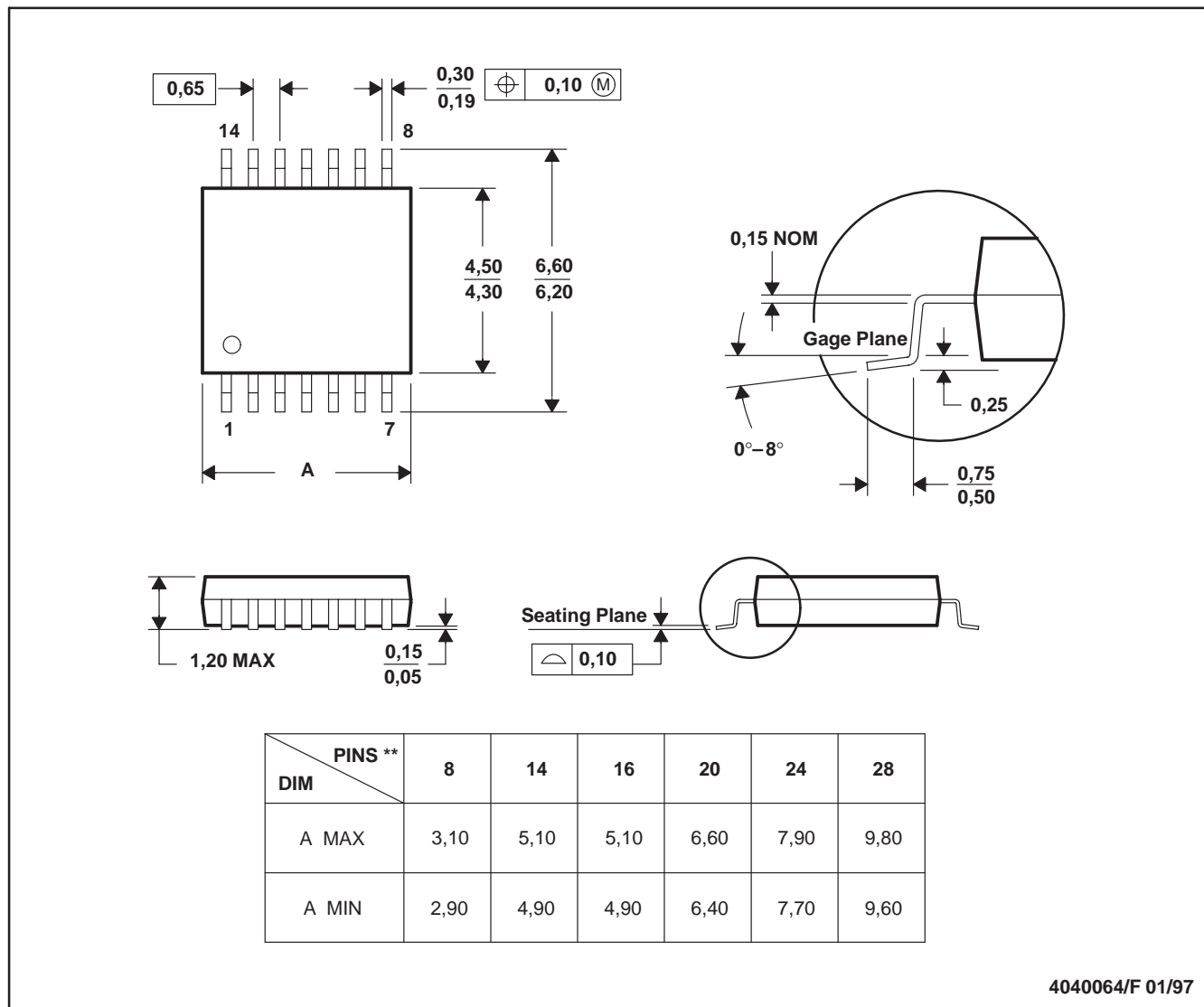


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| Products | | Applications | |
|-----------------------------|--|----------------------------|--|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DLP® Products | www.dlp.com | Communications and Telecom | www.ti.com/communications |
| DSP | dsp.ti.com | Computers and Peripherals | www.ti.com/computers |
| Clocks and Timers | www.ti.com/clocks | Consumer Electronics | www.ti.com/consumer-apps |
| Interface | interface.ti.com | Energy | www.ti.com/energy |
| Logic | logic.ti.com | Industrial | www.ti.com/industrial |
| Power Mgmt | power.ti.com | Medical | www.ti.com/medical |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| RFID | www.ti-rfid.com | Space, Avionics & Defense | www.ti.com/space-avionics-defense |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf | Video and Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless-apps |